

Additional Substrate Supplier for Virtex-6 and 7 Series FPGAs Flip Chip Packages

XCN14012 (v2.0) March 30, 2015

Product Change Notice

#### **Overview**

The purpose of this notification is to communicate that Xilinx is adding an additional qualified substrate supplier for all Virtex®-6 and selected 7 series FPGAs flip chip packages. In addition, Xilinx is aligning the substrate core material to an industry standard (E700FGR) for Virtex-6 FPGAs products.

## Description

The addition of this supplier is to ensure continuity of supply for Xilinx flip chip packages. 7 series FPGAs flip chip packages from the additional substrate supplier will have the identical material set, design and dimensions as the current 7 series FPGAs production substrates. For Virtex-6 FPGAs, Xilinx is aligning the substrate core to industry standard material E700FGR. E700FGR is already in production for 7 series FPGAs flip chip substrates. All other material, design, and dimensions for the Virtex-6 FPGAs with the added substrates are identical to the current production substrates. This added supplier is a qualified substrate supplier and is in production for Xilinx wire bond products. There is no change to the form, fit, or function.

# **Products Affected**

For Artix®-7, Zynq®-7000 All Programmable, Virtex®-7 and Kintex®-7 in the SB, FB, FF, SBG, FBG and FFG packages, this change affects all standard and specification control document (SCD) XC Commercial (C) grade, Extended (E) grade and Industrial (I) grade devices. Virtex-7 in the FL, FLG, FH and FHG packages, and Automotive "XA" devices for 7 series FPGAs are not affected by this PCN.

For Virtex-6 FPGAs, this change affects all standard and specification control document (SCD) "XC" Commercial (C) and Industrial (I) grade devices. Hi-Rel "XQ" devices in the FFG1156 package are not affected by this PCN.

Affected device package-pin are listed in the Table 1, Table 2, Table 3, Table 4 and Table 5 below:

Device	Package-Pin	Device	Package-Pin	Device	Package-Pin
VOOVOVADOT	FF(G)784 <sup>(1)</sup>		FF(G)1923 <sup>(1)</sup>	XC6VLX760	FF(G)1760 <sup>(1)</sup>
XC6VCX130T	FF(G)1156 <sup>(1)</sup>	XC6VHX565T	FF(G)1924 <sup>(1)</sup>	VOOVOVOAFT	FF(G)1156 <sup>(1)</sup>
XC6VCX195T	FF(G)784 <sup>(1)</sup>	XC6VLX130T	FF(G)784 <sup>(1)</sup>	XC6VSX315T	FF(G)1759 <sup>(1)</sup>
XC6VCX1951	FF(G)1156 <sup>(1)</sup>	ACOVEAT301	FF(G)1156 <sup>(1)</sup>	VOCUOVATET	FF(G)1156 <sup>(1)</sup>
XC6VCX240T	FF(G)784 <sup>(1)</sup>		FF(G)784 <sup>(1)</sup>	XC6VSX475T	FF(G)1759 <sup>(1)</sup>
AC6VCA2401	FF(G)1156 <sup>(1)</sup>	XC6VLX195T	FF(G)1156 <sup>(1)</sup>		
XC6VCX75T	FF(G)784 <sup>(1)</sup>	XC6VLX240T	FF(G)784 <sup>(1)</sup>		
XC6VHX250T	FF(G)1154 <sup>(1)</sup>		FF(G)1156 <sup>(1)</sup>		
	FF(G)1155 <sup>(1)</sup>		FF(G)1759 <sup>(1)</sup>		
XC6VHX255T	FF(G)1923 <sup>(1)</sup>		FF(G)1156 <sup>(1)</sup>		
	FF(G)1154 <sup>(1)</sup>	XC6VLX365T	FF(G)1759 <sup>(1)</sup>		
XC6VHX380T	FF(G)1155 <sup>(1)</sup>		FF(G)1759 <sup>(1)</sup>		
	FF(G)1923 <sup>(1)</sup>	XC6VLX550T	FF(G)1760 <sup>(1)</sup>		
	FF(G)1924 <sup>(1)</sup>	XC6VLX75T	FF(G)784 <sup>(1)</sup>		

Table 1: Virtex-6 FPGAs Devices Package Product Affected

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Device	Package-Pin	
	FF(G)1156 <sup>(2)</sup>	
XC7A200T	FB(G)484 <sup>(3)</sup>	
AG7A2001	FB(G)676 <sup>(3)</sup>	
	SB(G)484 (3)	

#### Table 3: Kintex-7 FPGAs Devices Package Product Affected

Device	Package-Pin	Device	Package-Pin
VOZKZOT	FB(G)484 <sup>(3)</sup>		FF(G)676 <sup>(1)</sup>
XC7K70T	FB(G)676 <sup>(3)</sup>	VOTKODET	FF(G)900 <sup>(1)</sup>
	FF(G)676 <sup>(2)</sup>	XC7K325T	FB(G)676 <sup>(3)</sup>
XC7K160T	FB(G)484 <sup>(3)</sup>		FB(G)900 <sup>(3)</sup>
	FB(G)676 <sup>(3)</sup>	XC7K355T	FF(G)901 <sup>(2)</sup>

Device	Package-Pin
	FF(G)676 <sup>(2)</sup>
XC7K410T	FF(G)900 <sup>(2)</sup>
	FB(G)676 <sup>(3)</sup>
	FB(G)900 <sup>(3)</sup>
XC7K420T	FF(G)901 <sup>(2)</sup>
	FF(G)1156 <sup>(2)</sup>
XC7K480T	FF(G)901 <sup>(2)</sup>
AC7K4001	FF(G)1156 <sup>(2)</sup>

#### Table 4: Virtex-7 FPGAs Devices Package Product Affected

Device	Package-Pin	
XC7V585T	FF(G)1157 <sup>(2)</sup>	
AC7 V 565 T	FF(G)1761 (2)	
XC7VX330T	FF(G)1157 <sup>(2)</sup>	Х
AC7VA3301	FF(G)1761 <sup>(2)</sup>	
	FF(G)1157 <sup>(2)</sup>	
XC7VX415T	FF(G)1158 <sup>(2)</sup>	x
	FF(G)1927 (2)	^

Device	Package-Pin
	FF(G)1157 <sup>(2)</sup>
	FF(G)1158 <sup>(2)</sup>
XC7VX485T	FF(G)1761 (2)
	FF(G)1927 (2)
	FF(G)1930 <sup>(2)</sup>
XC7VX550T	FF(G)1158 <sup>(2)</sup>
XC7VX5501	FF(G)1927 (2)

Device	Package-Pin
	FF(G)1157 <sup>(2)</sup>
	FF(G)1158 <sup>(2)</sup>
XC7VX690T	FF(G)1761 (2)
XC7 V X0901	FF(G)1926 <sup>(2)</sup>
	FF(G)1927 (2)
	FF(G)1930 <sup>(2)</sup>
	FF(G)1926 <sup>(2)</sup>
XC7VX980T	FF(G)1928 <sup>(2)</sup>
	FF(G)1930 <sup>(2)</sup>

#### Table 5: Zynq-7000 FPGAs Devices Package Product Affected

Device	Package-Pin
¥077000	FB(G)484 <sup>(3)</sup>
	FB(G)676 <sup>(3)</sup>
XC7Z030	FF(G)676 <sup>(3)</sup>
	SB(G)485 <sup>(3)</sup>
	FB(G)676 <sup>(3)</sup>
XC7Z035	FF(G)676 <sup>(3)</sup>
	FF(G)900 <sup>(3)</sup>

Device	Package-Pin	Device	Package-Pin
X077045	FB(G)676 <sup>(3)</sup> FF(G)676 <sup>(3)</sup>	V077400	FFG1156 <sup>(3)</sup>
XC7Z045	FF(G)900 <sup>(3)</sup>	XC7Z100	FFG900 <sup>(3)</sup>

#### Notes:

- (1) Please refer to <u>Table 6</u> Phase 1 cross-ship schedule
- (2) Please refer to <u>Table 7</u> Phase 2 cross-ship schedule
- (3) Please refer to <u>Table 8</u> Phase 3 cross-ship schedule

### **Key Dates and Ordering Information**

Xilinx may begin cross-ship product using new supplier substrate as early as Q1, CY2015; please reference <u>XTP385</u> for specific schedules.

Device	Qualification Report Available	Cross-Ship Date
XC6VCX130T	November 3 <sup>rd</sup> , 2014	Q1CY15
XC6VCX195T	November 3 <sup>rd</sup> , 2014	Q1CY15
XC6VCX240T	November 3 <sup>rd</sup> , 2014	Q1CY15
XC6VCX75T	November 3 <sup>rd</sup> , 2014	Q1CY15
XC6VHX250T	November 3 <sup>rd</sup> , 2014	Q1CY15
XC6VHX255T	November 3 <sup>rd</sup> , 2014	Q1CY15
XC6VHX380T	November 3 <sup>rd</sup> , 2014	Q1CY15
XC6VHX565T	November 3 <sup>rd</sup> , 2014	Q1CY15
XC6VLX130T	November 3 <sup>rd</sup> , 2014	Q1CY15
XC6VLX195T	November 3 <sup>rd</sup> , 2014	Q1CY15
XC6VLX240T	November 3 <sup>rd</sup> , 2014	Q1CY15
XC6VLX365T	November 3 <sup>rd</sup> , 2014	Q1CY15
XC6VLX550T	November 3 <sup>rd</sup> , 2014	Q1CY15
XC6VLX75T	November 3 <sup>rd</sup> , 2014	Q1CY15
XC6VLX760	November 3 <sup>rd</sup> , 2014	Q1CY15
XC6VSX315T	November 3 <sup>rd</sup> , 2014	Q1CY15
XC6VSX475T	November 3 <sup>rd</sup> , 2014	Q1CY15
XC7K325T	November 3 <sup>rd</sup> , 2014	Q1CY15

Table 6: Phase 1 - Virtex-6 and Kintex-7 Devices Qualification Completion and Cross-Ship Schedule

Table 7: Phase 2 - Artix-7, Kintex-7 and Virtex-7 Devices Qualification Completion and Cross-Ship Schedule

Device	Qualification Report Available	Cross-Ship Date
XC7A200T	November 3 <sup>rd</sup> , 2014	Q2CY15
XC7K160T	November 3 <sup>rd</sup> , 2014	Q2CY15
XC7K355T	November 3 <sup>rd</sup> , 2014	Q2CY15
XC7K410T	November 3 <sup>rd</sup> , 2014	Q2CY15
XC7K420T	November 3 <sup>rd</sup> , 2014	Q2CY15
XC7K480T	November 3 <sup>rd</sup> , 2014	Q2CY15
XC7V585T	November 3 <sup>rd</sup> , 2014	Q2CY15
XC7VX330T	November 3 <sup>rd</sup> , 2014	Q2CY15
XC7VX415T	November 3 <sup>rd</sup> , 2014	Q2CY15
XC7VX485T	November 3 <sup>rd</sup> , 2014	Q2CY15
XC7VX550T	November 3 <sup>rd</sup> , 2014	Q2CY15
XC7VX690T	November 3 <sup>rd</sup> , 2014	Q2CY15
XC7VX980T	November 3 <sup>rd</sup> , 2014	Q2CY15

Device	Qualification Report Available	Cross-Ship Date
XC7A200T-FBG484	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7A200T-FBG676	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7A200T-SBG484	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7K160T-FBG484	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7K160T-FBG676	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7K325T-FBG676	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7K325T-FBG900	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7K410T-FBG676	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7K410T-FBG900	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7K70T-FBG484	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7K70T-FBG676	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7Z030-FBG484	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7Z030-FBG676	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7Z030-FFG676	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7Z030-SBG485	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7Z035-FBG676	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7Z035-FFG676	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7Z035-FFG900	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7Z045-FBG676	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7Z045-FFG676	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7Z045-FFG900	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7Z100-FFG1156	November 3 <sup>rd</sup> , 2014	Q1CY16
XC7Z100-FFG900	November 3 <sup>rd</sup> , 2014	Q1CY16

Table 8:	Phase 3 - Art	ix-7, Zynq-7000	All Programmable and Kintex-7	Cross-Ship Schedule
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# **Qualification Data**

Xilinx has successfully passed and completed the qualification. Please refer to Xilinx <u>RPT204</u> for more details.

### Response

No response is required. For additional information or questions, please contact Xilinx Technical Support.

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### **Additional Documentation**

Qualification Report (RPT204):

https://secure.xilinx.com/webreg/clickthrough.do?cid=370836 FAQ (XTP385): Transition Schedule for Substrate Supplier for Virtex-6 and 7 Series FPGAs Flip Chip Packages https://secure.xilinx.com/webreg/clickthrough.do?cid=371043

## **Revision History**

The following table shows the revision history for this document:

Date	Version	Description of Revisions
11/03/2014	1.0	Initial released.
11/10/2014	1.1	Minor update on <u>Table 1</u> to remove $FF(G)1759$ package from XC6VCX240T device. Edit the statement under the Key Dates and Ordering Information.
03/30/2015	2.0	Added Zynq-7000 family, Artix-7 SB(G) and FB(G) package and Kintex-7 FB(G) package for Phase 3 release.

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