Wireless Components

ASK/FSK 915MHz Single Conversion Receiver

TDA 5212 Version 1.3

Specification December 2006

Revision History

Current Version: 1.3 as of 12.12.06		
Previous Version: 1.2		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
3-4, 5-12	3-4, 5-12	Correction of some typing mistakes
Product Info, 2-3	Product Info, 2-3	Change of package name to PG-TSSOP-28

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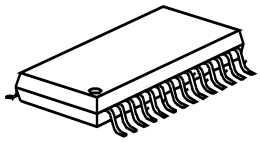
Product Info

General Description

The IC is a very low power consumption single chip FSK/ASK Superheterodyne Receiver (SHR) for the receive frequency range between 902 and 928 MHz that is pin compatible to the ASK Receiver TDA5202. The IC offers a high level of integration and needs only a few external components. The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesiser, a crystal oscillator, a limiter with RSSI generator, a PLL FSK demodulator, a data filter, a data comparator (slicer) and a peak detector. Additionally there is a power down feature to save battery life.

Package



Features

- Low supply current (I_S = 5.4 mA typ. in FSK mode, I_S = 4.8 mA typ. in ASK mode)
- Supply voltage range 5 V ±10%
- Power down mode with very low supply current (90 nA typ.)
- FSK and ASK demodulation capability
- Fully integrated VCO and PLL Synthesiser
- ASK sensitivity better than -109 dBm over specified temperature range (- 40 to +85°C)
- Receive frequency range 902 to 928 MHz
- Limiter with RSSI generation, operating at 10.7 MHz
- Selectable reference frequency
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold
- FSK sensitivity better than -102 dBm over specified temperature range (- 40 to +85°C)

Application

- Keyless Entry Systems
- Remote Control Systems
- Low Bitrate ISM-band Communication Systems

Ordering Information

Type	Ordering Code	Package
TDA 5212	SP000013430	PG-TSSOP-28
samples available		

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2 Product Description

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2.1 Overview

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2.2 Application

- Keyless Entry Systems
- Remote Control Systems
- Low Bitrate ISM-band Communication Systems

2.3 Features

- Low supply current (I_S = 5.4 mA typ.FSK mode, 4.8 mA typ. ASK mode)
- Supply voltage range 5V ±10%
- Power down mode with very low supply current (90nA typ.)
- FSK and ASK demodulation capability
- Fully integrated VCO and PLL Synthesiser
- RF input sensitivity ASK -112dBm typ. at 25°C, better than -109dBm over complete specified operating temperature range (-40 to +85°C)
- RF input sensitivity FSK -105dBm typ. at 25°C, better than -102dBm over complete specified operating temperature range (-40 to +85°C)
- Receive frequency range between 902 and 928 MHz
- Selectable reference frequency
- Limiter with RSSI generation, operating at 10.7MHz
- 2nd order low pass data filter with external capacitors
- Data slicer with self-adjusting threshold

2.4 Package Outlines

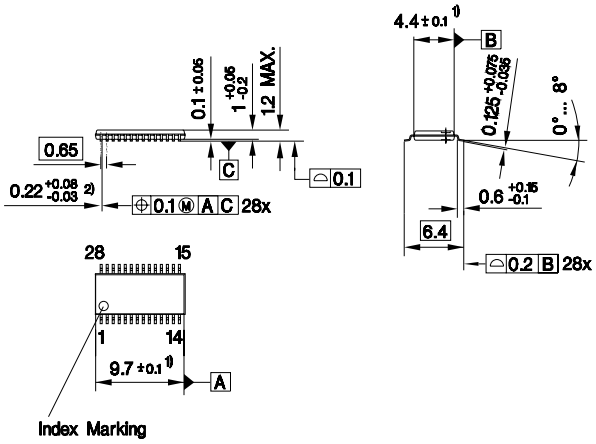

Figure 2-1 PG-TSSOP-28 package outlines

3 Functional Description

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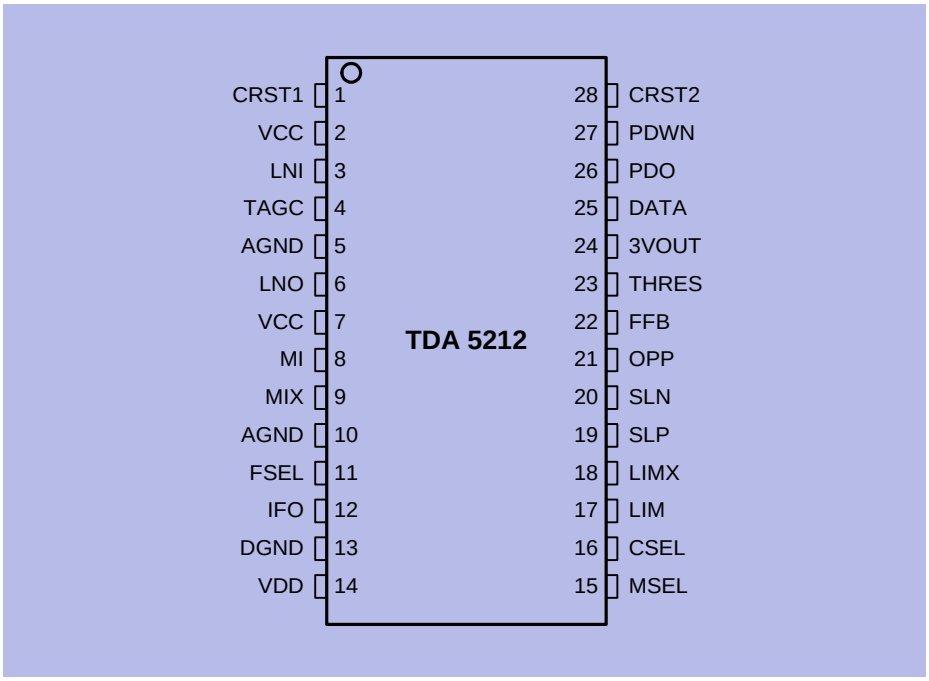
3.1 Pin Configuration

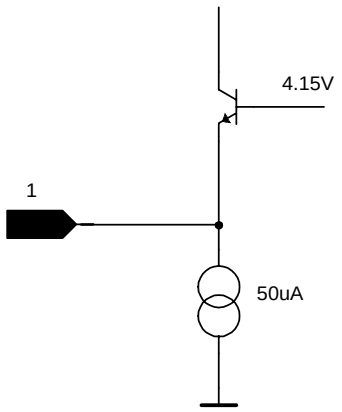
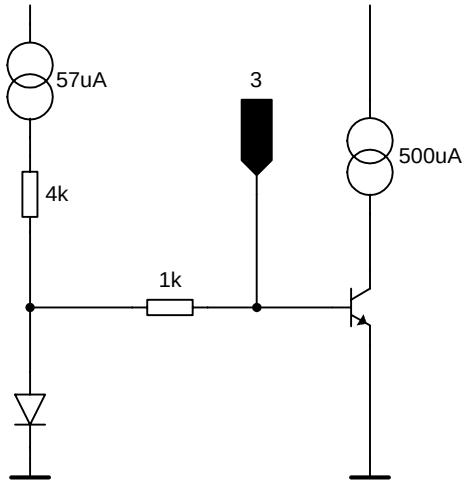


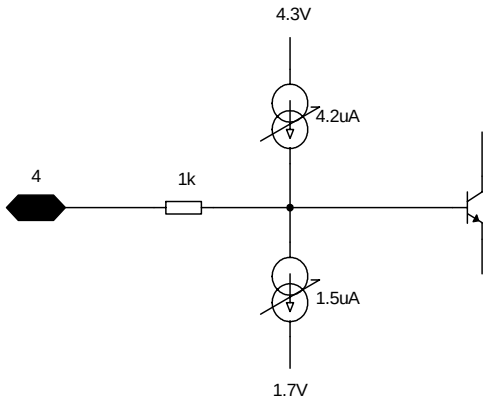
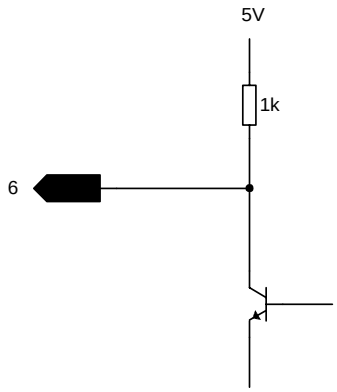
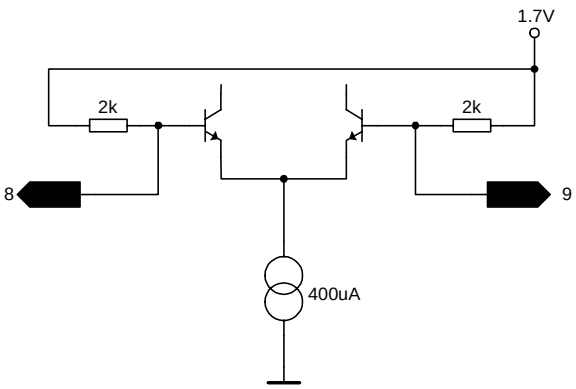
Pin_Configuration_5212_V1.0.wmf

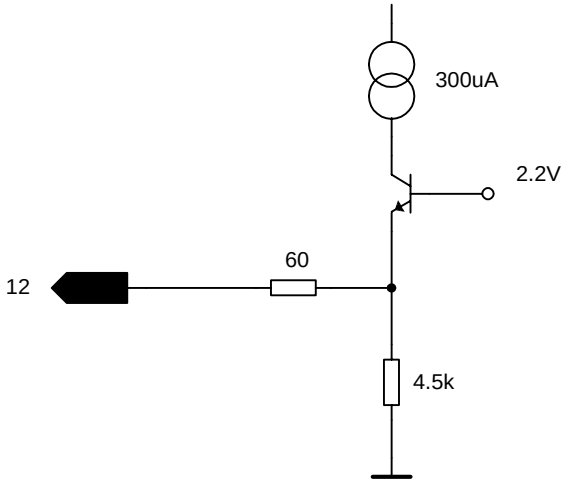
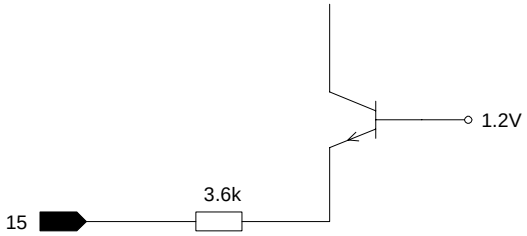
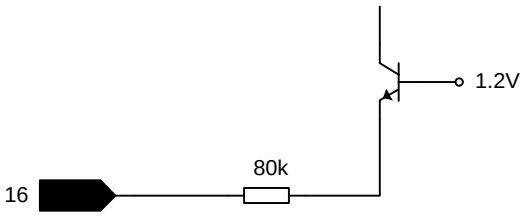
Figure 3-1 IC Pin Configuration

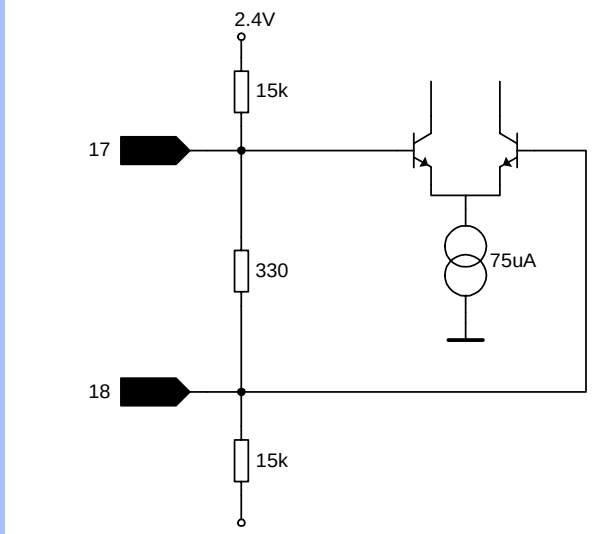
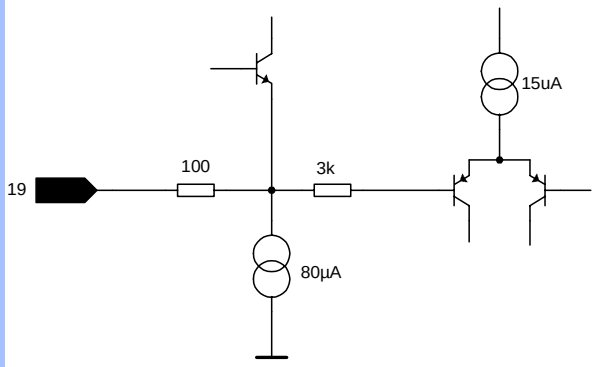
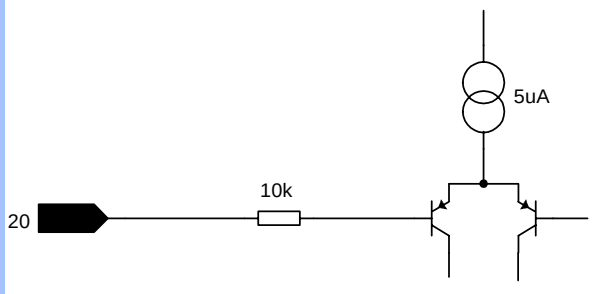
3.2 Pin Definition and Function

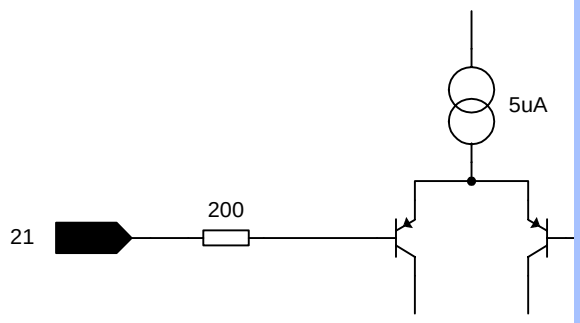
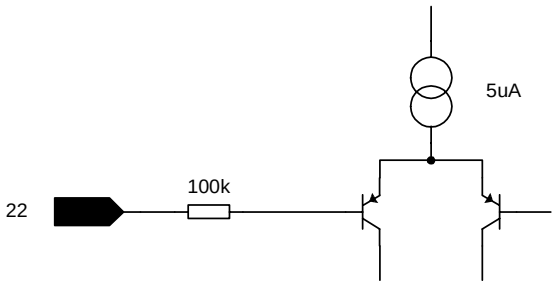
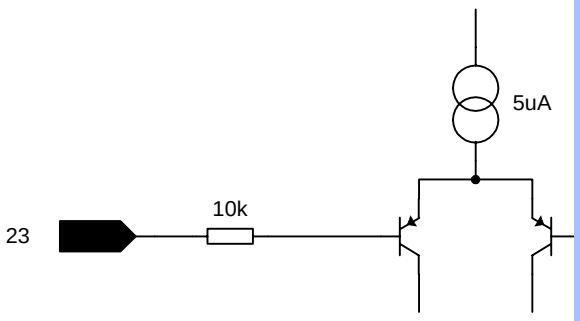
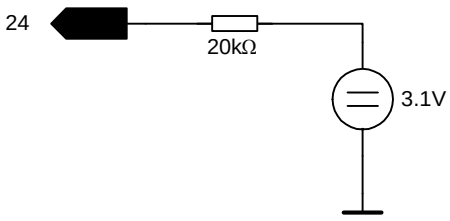
Table 3-1 Pin Definition and Function

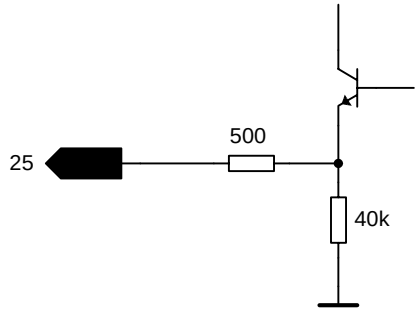
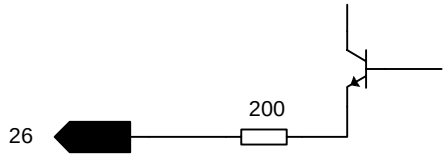
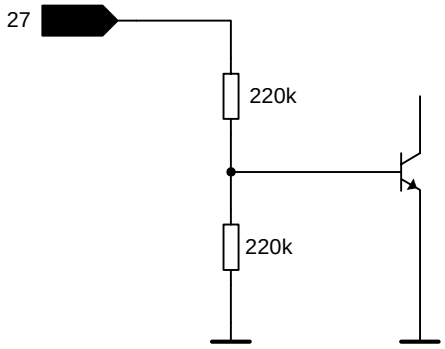
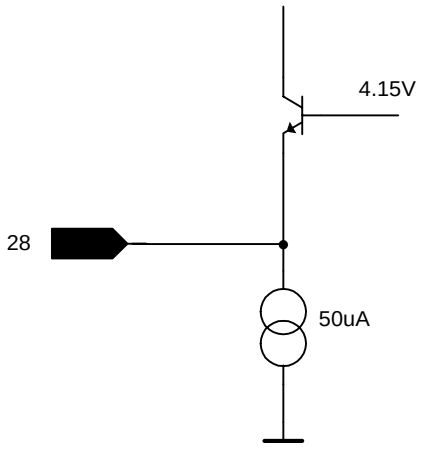
Pin No.	Symbol	Equivalent I/O-Schematic	Function
1	CRST1		External Crystal Connector 1
2	VCC		5V Supply
3	LNI		LNA Input

4	TAGC		AGC Time Constant Control
5	AGND		Analogue Ground Return
6	LNO		LNA Output
7	VCC		5V Supply
8	MI		Mixer Input
9	MIX		Complementary Mixer Input
10	AGND		Analogue Ground Return
11	BUF		Mixer Buffer Ground

12	IFO		10.7 MHz IF Mixer Output
13	DGND		Digital Ground Return
14	VDD		5V Supply (PLL Counter Circuitry)
15	MSEL		ASK/FSK Modulation Format Selector
16	CSEL		7.xx or 14.xx MHz Quartz Selector

17	LIM		Limiter Input
18	LIMX		Complementary Limiter Input
19	SLP		Data Slicer Positive Input
20	SLN		Data Slicer Negative Input

21	OPP		OpAmp Noninverting Input
22	FFB		Data Filter Feedback Pin
23	THRES		AGC Threshold Input
24	3VOUT		3V Reference Output

25	DATA		Data Output
26	PDO		Peak Detector Output
27	PDWN		Power Down Input
28	CRST2		External Crystal Connector 2

3.3 Functional Block Diagram

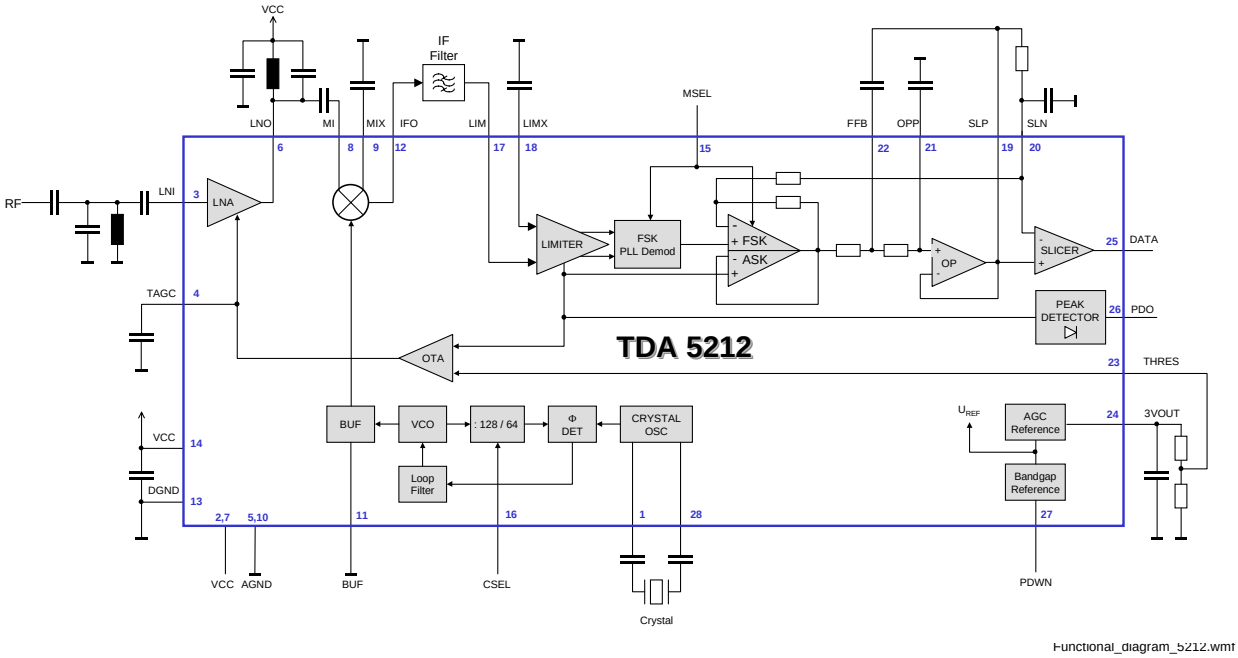


Figure 3-2 Main Block Diagram

3.4 Functional Blocks

3.4.1 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 to 20dB. The gain figure is determined by the external matching networks situated ahead of LNA and between the LNA output **LNO** (Pin 6) and the Mixer Inputs **MI** and **MIX** (Pins 8 and 9). The noise figure of the LNA is approximately 2dB, the current consumption is 500µA. The gain can be reduced by approximately 18dB. The switching point of this AGC action can be determined externally by applying a threshold voltage at the **THRES** pin (Pin 23). This voltage is compared internally with the received signal (RSSI) level generated by the limiter circuitry. In case that the RSSI level is higher than the threshold voltage the LNA gain is reduced and vice versa. The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin as described in Section 4.1. The time constant of the AGC action can be determined by connecting a capacitor to the **TAGC** pin (Pin 4) and should be chosen along with the appropriate threshold voltage according to the intended operating case and interference scenario to be expected during operation. The optimum choice of AGC time constant and the threshold voltage is described in Section 4.1.

3.4.2 Mixer

The Double Balanced Mixer downconverts the input frequency (RF) in the range of 902 to 928 MHz to the intermediate frequency (IF) at 10.7MHz with a voltage gain of approximately 18 dB. A low pass filter with a corner frequency of 20MHz is built on chip in order to suppress RF signals to appear at the IF output (**IFO** pin). The IF output is internally consisting of an emitter follower that has a source impedance of approximately 330Ω to facilitate interfacing the pin directly to a standard 10.7MHz ceramic filter without additional matching circuitry.

3.4.3 PLL Synthesizer

The Phase Locked Loop synthesiser consists of a VCO, an asynchronous divider chain, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCO is including spiral inductors and varactor diodes. The oscillator signal is fed both to the synthesiser divider chain and to the downconverting mixer via a buffer amplifier. The **BUF** pin (Pin 11) has to be tied to ground. No additional components are necessary. The loop filter is also realised fully on-chip.
Using high side injection of the local oscillator (L0) for receiving frequencies below 921MHz and low side injection for frequencies above 921MHz, the receiving frequency band of 902 to 928MHz can be covered due to the L0 fre-

quency band of 910 to 932MHz. But please note that using high side injetion of the L0 yields a sign inversion of the demodulated data signal in case of FSK. See also Section 4.4.

3.4.4 Crystal Oscillator

The on-chip crystal oscillator circuitry allows for utilisation of quartzes both in the 7 and 14MHz range as the overall division ratio of the PLL can be switched between 64 and 128 via the **CSEL** (Pin 16) pin according to the following table.

Table 3-2 CSEL Pin Operating States

CSEL	Crystal Frequency
Open	7.xx MHz
Shorted to ground	14.xx MHz

The calculation of the value of the necessary quartz load capacitance is shown in Section 4.3, the quartz frequency calculation is expained in Section 4.4.

3.4.5 Limiter

The Limiter is an AC coupled multistage amplifier with a cumulative gain of approximately 80dB that has a bandpass-characteristic centred around 10.7MHz. It has an input impedance of 330Ω to allow for easy interfacing to a 10.7MHz ceramic IF filter. The limiter circuit acts as a Receive Signal Strength Indicator (RSSI) generator which produces a DC voltage that is directly proportional to the input signal level as can be seen in Figure 4.2. This signal is used to demodulate the ASK receive signal in the subsequent baseband circuitry and to turn down the LNA gain by approximately 18dB in case the input signal strength is too strong as described in Section 3.4.1 and Section 4.1.

3.4.6 FSK Demodulator

To demodulate frequency shift keyed (FSK) signals a PLL circuit is used that is contained fully on chip. The Limiter output differential signal is fed to the linear phase detector as is the output of the 10.7MHz center frequency VCO. The demodulator gain is typically 200µV/kHz. The passive loop filter output that is comprised fully on chip is fed to both the VCO and the modulation format switch.This signal is representing the demodulated signal. This switch is actually a switchable amplifier with an AC gain of 11 that is controlled by the **MSEL**

pin (Pin 15) as shown in the following table. This gain was chosen to facilitate detection in the subsequent circuits.

Table 3-3 MSEL Pin Operating States

MSEL	Modulation Format
Open	ASK
Shorted to ground	FSK

The DC gain is 1 in order not to saturate the subsequent Data Filter wih the DC offset produced by the demodulator in case of large frequency offsets of the IF signal. The resulting frequency characteristic and details on the principle of operation of the switch are described in Section 4.6. The demodulator circuit is switched off in case of reception of ASK signals.

3.4.7 Data Filter

The data filter comprises an OP-Amp with a bandwidth of 100kHz used as a voltage follower and two 100kΩ on-chip resistors. Along with two external capacitors a 2nd order Sallen-Key low pass filter is formed. The selection of the capacitor values is described in Section 4.2.

3.4.8 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100 kHz. This allows for a maximum receive data rate of approximately 120kBaud. The maximum achievable data rate also depends on the IF Filter bandwidth and the local oscillator tolerance values. Both inputs are accessible. The output delivers a digital data signal (CMOS-like levels) for the detector. The self-adjusting threshold on pin 20 its generated by RC-term or peak detector depending on the baseband coding scheme. The data slicer threshold generation alternatives are described in more detail in Section 4.5.

3.4.9 Peak Detector

The peak detector generates a DC voltage which is proportional to the peak value of the receive data signal. An external RC network is necessary. The input is connected to the output of the RSSI-output of the Limiter, the output is connected to the **PDO** pin (Pin 26). This output can be used as an indicator for the received signal strength to use in wake-up circuits and as a reference for the data slicer in ASK mode. Note that the RSSI level is also output in case of FSK mode.

3.4.10 Bandgap Reference Circuitry

A Bandgap Reference Circuit provides a temperature stable reference voltage for the device. A power down mode is available to switch off all subcircuits which is controlled by the **PWDN** pin (Pin 27) as shown in the following table. The supply current drawn in this case is typically 90nA.

Table 3-4 PDWN Pin Operating States

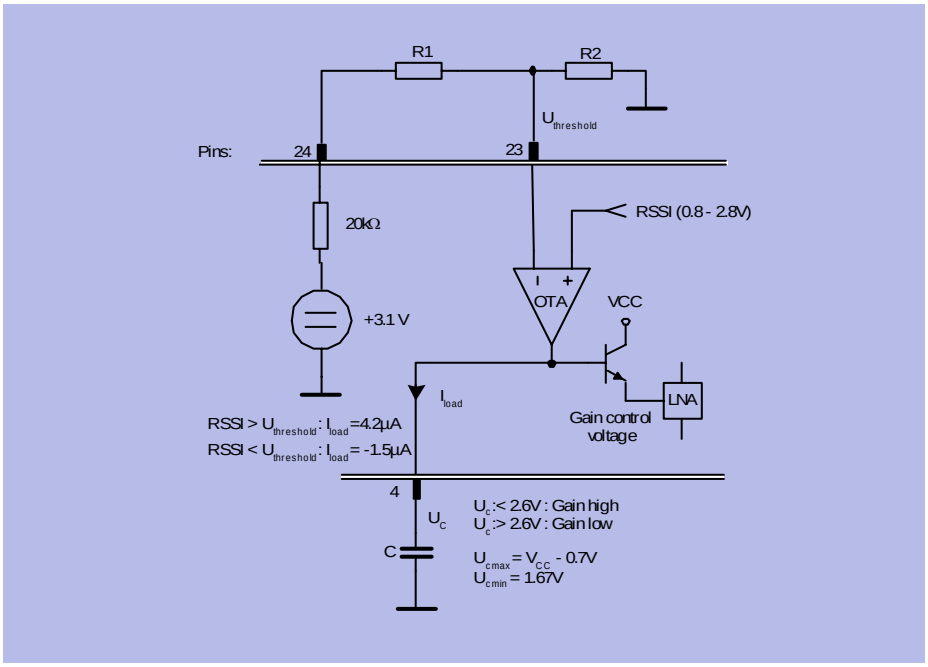
PDWN	Operating State
Open or tied to ground	Powerdown Mode
Tied to Vs	Receiver On

4 Applications

Contents of this Chapter

4.1 Choice of LNA Threshold Voltage and Time Constant

In the following figure the internal circuitry of the LNA automatic gain control is shown.



LNA_autom.wmf

Figure 4-1 LNA Automatic Gain Control Circuitry

The LNA automatic gain control circuitry consists of an operational transimpedance amplifier that is used to compare the received signal strength signal (RSSI) generated by the Limiter with an externally provided threshold voltage U_{thres}. As shown in the following figure the threshold voltage can have any value between approximately 0.8 and 2.8V to provide a switching point within the receive signal dynamic range.

This voltage U_{thres} is applied to the **THRES** pin (Pin 23) The threshold voltage can be generated by attaching a voltage divider between the **3VOUT** pin (i.e. Pin 24) which provides a temperature stable 3V output generated from the internal bandgap voltage and the **THRES** pin. If the RSSI level generated by the Limiter is higher than U_{thres}, the OTA generates a positive current I_{load}. This yields a voltage rise on the **TAGC** pin (Pin 4). Otherwise, the OTA generates a negative current. These currents do not have the same values in order to achieve a fast-attack and slow-release action of the AGC and are used to charge an external capacitor which finally generates the LNA gain control voltage.

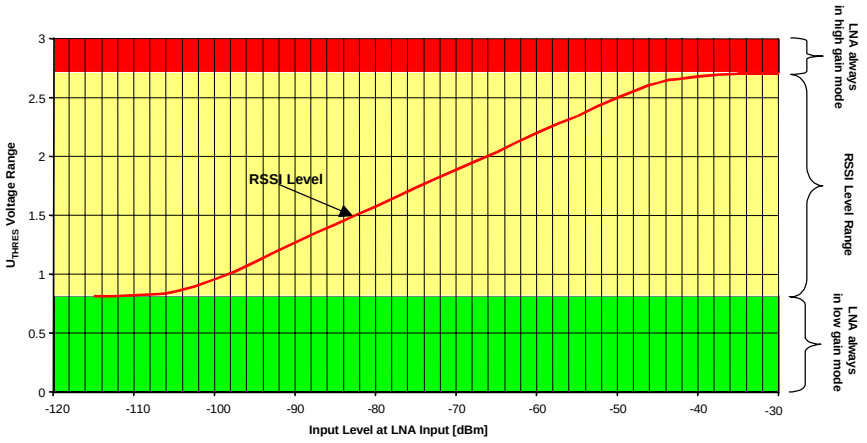


Figure 4-2 RSSI Level and Permissive AGC Threshold Levels

The switching point should be chosen according to the intended operating scenario. The determination of the optimum point is described in the accompanying Application Note, a threshold voltage level of 1.8V is apparently a viable choice. It should be noted that the output of the **3VOUT** pin is capable of driving up to 50µA, but that the **THRES** pin input current is only in the region of 40nA. As the current drawn out of the **3VOUT** pin is directly related to the receiver power consumption, the power divider resistors should have high impedance values. The sum of R1 and R2 has to be 600kΩ in order to yield 3V at the **3VOUT** pin. R1 can thus be chosen as 240kΩ, R2 as 360kΩ to yield an overall **3VOUT** output current of 5µA[1] and a threshold voltage of 1.8V

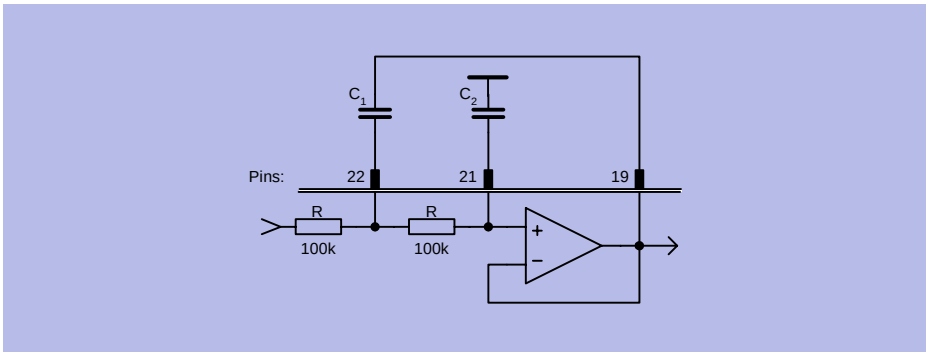
Note: If the LNA gain shall be kept in either high or low gain mode this has to be accomplished by tying the **THRES** pin to a fixed voltage. In order to achieve high gain mode operation, a voltage higher than 2.8V shall be applied to the **THRES** pin, such as a short to the **3VOLT** pin. In order to achieve low gain mode operation a voltage lower than 0.7V shall be applied to the **THRES**, such as a short to ground.

As stated above the capacitor connected to the **TAGC** pin is generating the gain control voltage of the LNA due to the charging and discharging currents of the OTA and thus is also responsible for the AGC time constant. As the charging and discharging currents are not equal two different time constants will result. The time constant corresponding to the charging process of the capacitor shall be chosen according to the data rate. According to measurements performed at Infineon the capacitor value should be greater than 47nF.

1. note the 20kΩ resistor in series with the 3.1V internal voltage source

4.2 Data Filter Design

Utilising the on-board voltage follower and the two 100kΩ on-chip resistors a 2nd order Sallen-Key low pass data filter can be constructed by adding 2 external capacitors between pins 19 (SLP) and 22 (FFB) and to pin 21 (OPP) as depicted in the following figure and described in the following formulas[1].



Filter_Design.wmf

Figure 4-3 Data Filter Design

$$C1 = \frac{2Q\sqrt{b}}{R2\Pi f_{3dB}} \qquad C2 = \frac{\sqrt{b}}{4QR\Pi f_{3dB}}$$

with

$$Q = \frac{\sqrt{b}}{a}$$

the quality factor of the poles

where

in case of a Bessel filter a = 1.3617, b = 0.618

and thus Q = 0.577

and in case of a Butterworth filter a = 1.141, b = 1

and thus Q = 0.71

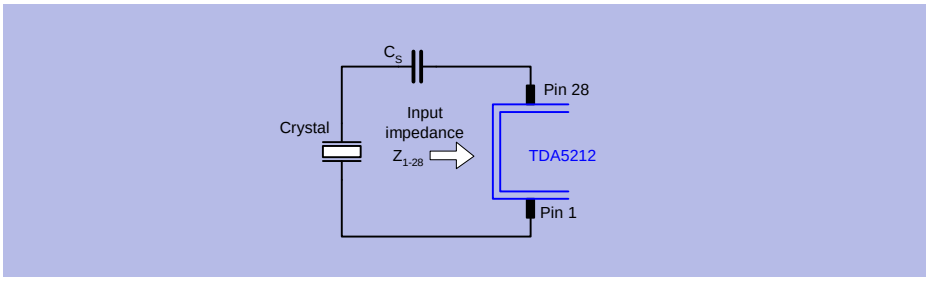
Example: Butterworth filter with f_{3dB} = 5kHz and R = 100kΩ:

C_1 = 450pF, C_2 = 225pF

1. taken from Tietze/Schenk: Halbleiterschaltungstechnik, Springer Berlin, 1999

4.3 Crystal Load Capacitance Calculation

The value of the capacitor necessary to achieve that the crystal oscillator is operating at the intended frequency is determined by the reactive part of the negative resistance of the oscillator circuit as shown in Section 5.1.3 and by the crystal specifications given by the crystal manufacturer.



Quartz_load_5212.wmf

Figure 4-4 Determination of Series Capacitance Value for the Crystal Oscillator

Crystal specified with load capacitance

$$C_S = \frac{1}{\frac{1}{C_L} + 2\pi f X_L}$$

with C_L the load capacitance (refer to the crystal specification).

Examples:

7.2 MHz:	C_L = 12 pF	X_L=500 Ω	C_S = 9.5 pF
14.5 MHz:	C_L = 12 pF	X_L=1050 Ω	C_S = 5.6 pF

These values may be obtained in high accuracy by putting two capacitors in series to the quartz, such as 18pF and 20pF in the 7.2MHz case and 18pF and 8.2pF in the 14.5MHz case. But please note that the calculated value for C_S includes also all parasitic capacitors.

4.4 Crystal Frequency Calculation

As mentioned in Section 3.4.3 the local oscillator (UHF PLL) signal has to be high-side injected for a RF below 921MHz and low-side injected for a RF above 921MHz into the downconverting mixer. Thus the crystal frequency is calculated by using the following formula:

$$f_{QU} = \frac{f_{RF} \pm 10.7}{r}$$

with f_{RF} .... receive frequency

f_{LO} .... local oscillator (PLL) frequency ($f_{RF} \pm 10.7$)

f_{QU} .... crystal oscillator frequency

r .... ratio of local oscillator (PLL) frequency and crystal frequency as shown in the subsequent table.

Table 4-1 PLL Division Ratio Dependence on States of CSEL

CSEL	Ratio r = (f_{LO}/f_{QU})
open	128
GND	64

This yields the following calculation for a RF of 915MHz for instance:

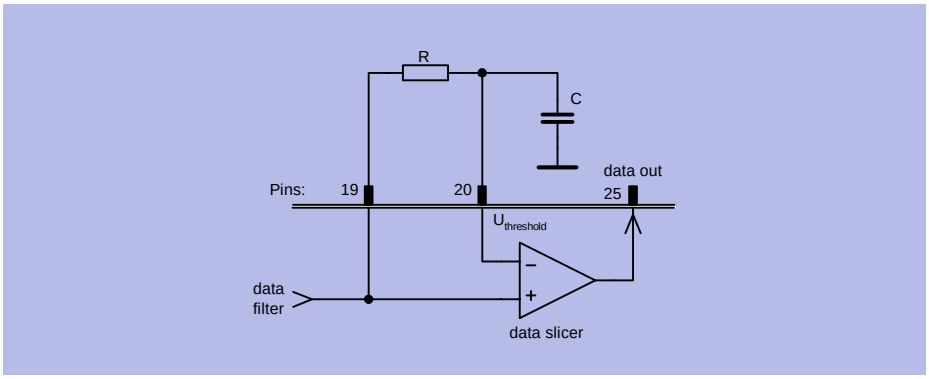
CSEL tied to GND[1]:

$$f_{QU} = \frac{915MHz + 10.7MHz}{64} = 14.4641MHz$$

1.In the Infineon Evalboard the L0 is used in low side injection mode and therefore crystal with 14.1296875MHz is used. But to guarantee the function over the whole temperature range the L0 has to be used in high side injection mode for a RF of 915MHz (see also VDO frequency range).

4.5 Data Slicer Threshold Generation

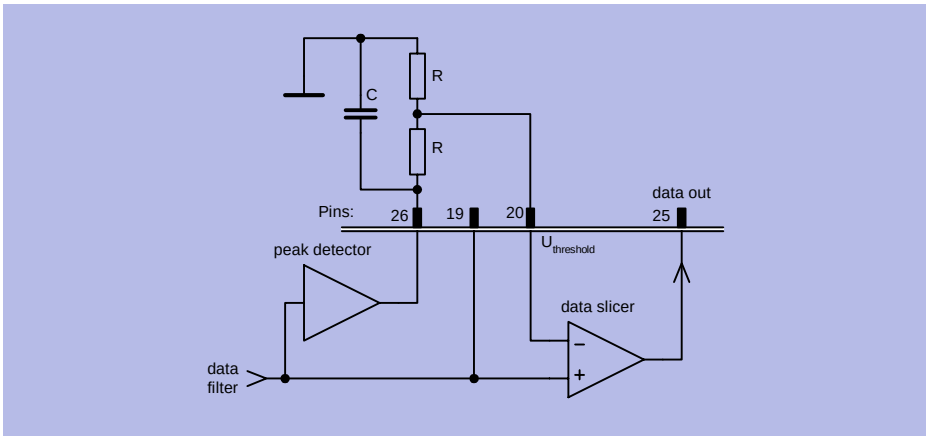
The threshold of the data slicer can be generated in two ways, depending on the signal coding scheme used. In case of a signal coding scheme without DC content such as Manchester coding the threshold can be generated using an external R-C integrator as shown in Figure 4-5. The time constant T_A of the R-C integrator has to be significantly larger than the longest period of no signal change T_L within the data sequence. For the calculation of the time constant T_A please see Application Note „TDA521X_ANV1.1.“ chapter „4.11. Data Slicer“. In order to keep distortion low, the minimum value for R is 20kΩ.



Data_slice1.wmf

Figure 4-5 Data Slicer Threshold Generation with External R-C Integrator

Another possibility for threshold generation is to use the peak detector in connection with two resistors and one capacitor as shown in the following figure. The component values are depending on the coding scheme and the protocol used.

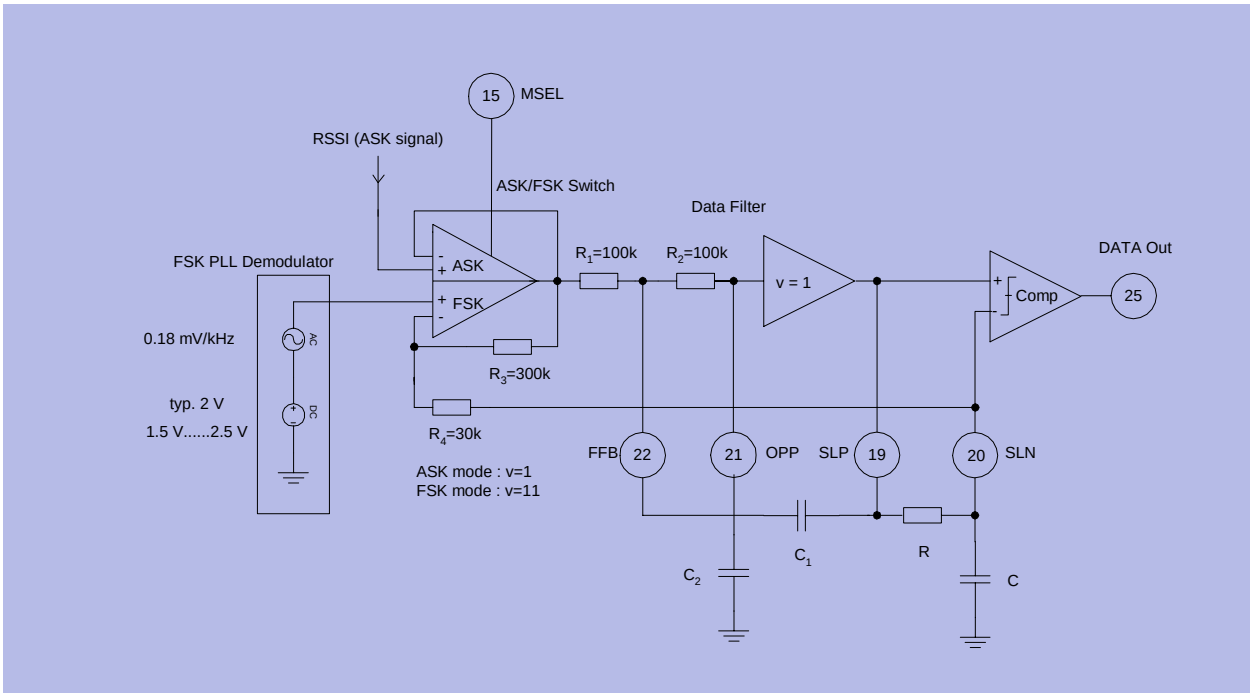


Data_slice2.wmf

Figure 4-6 Data Slicer Threshold Generation Utilising the Peak Detector

4.6 ASK/FSK Switch Functional Description

The TDA5211 is containing an ASK/FSK switch which can be controlled via Pin 15 (MSEL). This switch is actually consisting of 2 operational amplifiers that are having a gain of 1 in case of the ASK amplifier and a gain of 11 in case of the FSK amplifier in order to achieve an appropriate demodulation gain characteristic. In order to compensate for the DC-offset generated especially in case of the FSK PLL demodulator there is a feedback connection between the threshold voltage of the bit slicer comparator (Pin 20) to the negative input of the FSK switch amplifier. This is shown in the figure below:



ask_fsk_datapath.WMF

Figure 4-7 ASK/FSK mode datapath

4.6.1 FSK Mode

The FSK datapath has a bandpass characterisitc due to the feedback shown above (highpass) and the data filter (lowpass). The lower cutoff frequency f2 is determined by the external RC-combination. The upper cutoff frequency f3 is determined by the data filter bandwidth.

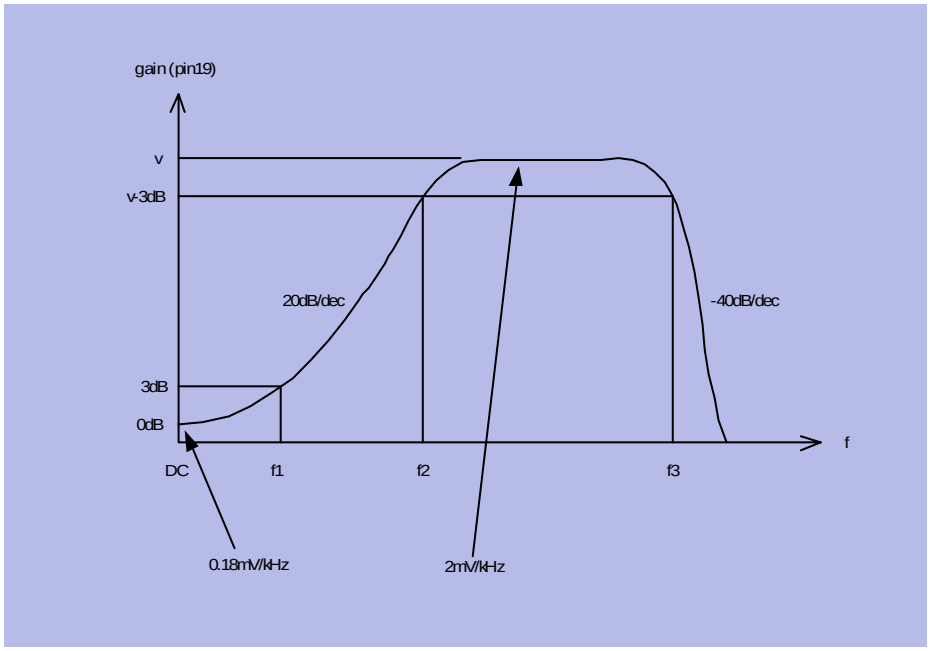
The demodulation gain of the FSK PLL demodulator is 200µV/kHz. This gain is increased by the gain v of the FSK switch, which is 11. Therefore the resulting dynamic gain of this circuit is 2.2mV/kHz round about within the bandpass. The

gain for the DC content of FSK signal remains at 200µV/kHz. The cutoff frequencies of the bandpass have to be chosen such that the spectrum of the data signal is influenced in an acceptable amount.

In case that the user data is containing long sequences of logical zeros the effect of the drift-off of the bit slicer threshold voltage can be lowered if the offset voltage inherent at the negative input of the slicer comparator (Pin20) is used. The comparator has no hysteresis built in.

This offset voltage is generated by the bias current of the negative input of the comparator (i.e. 20nA) running over the external resistor R. This voltage raises the voltage appearing at pin 20 (e.g. 1mV with R = 100kΩ). In order to obtain benefit of this asymmetrical offset for the demodulation of long zeros the lower of the two FSK frequencies should be chosen in the transmitter as the zero-symbol frequency.

In the following figure the shape of the above mentioned bandpass is shown.



frequenzgang.WMF

Figure 4-8 Frequency characterstic in case of FSK mode

The cutoff frequencies are calculated with the following formulas:

$$f_1 = \frac{1}{2\pi \frac{R \cdot 330k\Omega}{R + 330k\Omega} \times C}$$

$$f_2 = v \cdot f_1 = 11 \cdot f_1$$

$$f_3 = f_{3dB}$$

f_3 is the 3dB cutoff frequency of the data filter - see Section 4.2.

Example:

R = 100kΩ

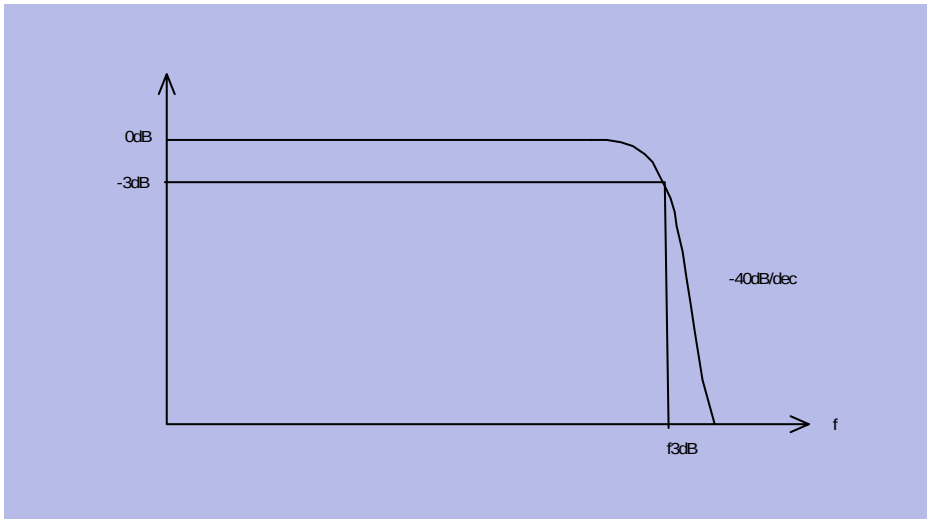
C = 47nF

This leads to f_1 = 44Hz

and f_2 = 485Hz

4.6.2 ASK Mode

In case the receiver is operated in ASK mode the datapath frequency charactersitic is dominated by the data filter alone, thus it is lowpass shaped.The cutoff frequency is determined by the external capacitors C12 and C14 and the internal 100k resistors as described in Section 4.2



freq_ask.WMF

Figure 4-9 Frequency charcteristic in case of ASK mode

4.7 Principle of the Precharge Circuit

In case the data slicer threshold shall be generated with an external RC network as described in Section 4.5 it is necessary to use large values for the capacitor C attached to the **SLN** pin (pin 20) in order to achieve long time constants. This results also from the fact that the choice of the value for R connected between the **SLP** and **SLN** pins (pins 19 and 20) is limited by the 330kΩ resistor appearing in parallel to R as can be seen in Figure 4-6. Apart from this a resistor value of 100kΩ leads to a voltage offset of 1mv at the comparator input as described in Section 4.6.1. The resulting startup time constant τ_1 can be calculated with:

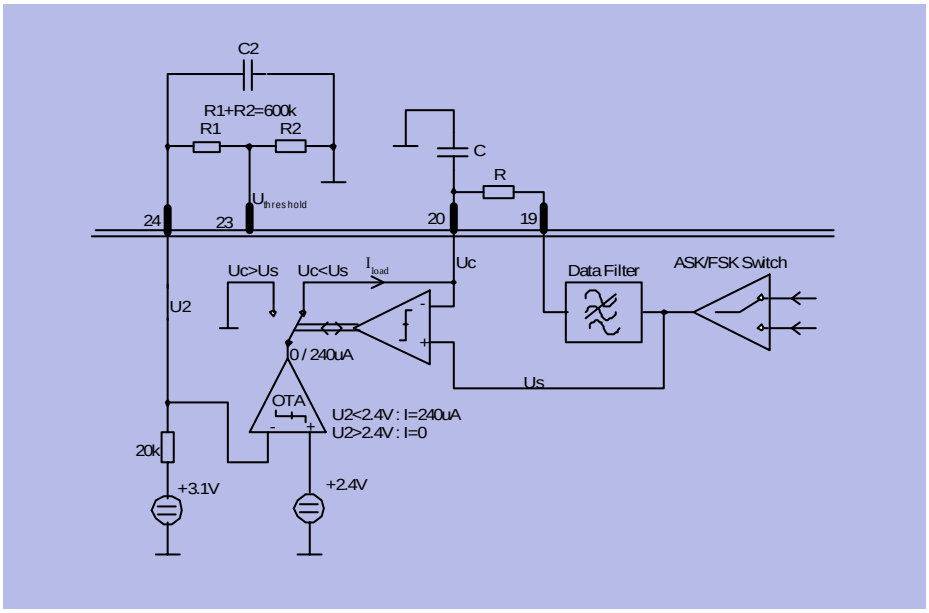
$$\tau_1 = \left(R \,||\, 330k\Omega\right) \times C$$

In case R is chosen to be 100kΩ and C is chosen as 47nF this leads to

$$\tau_1 = \left(100k\Omega \,||\, 330k\Omega\right) \times 47nF = 77k\Omega \times 47nF = 3.6ms$$

When the device is turned on this time constant dominates the time necessary for the device to be able to demodulate data properly. In the powerdown mode the capacitor is only discharged by leakage currents.

In order to reduce the turn-on time in the presence of large values of C a precharge circuit was included in the TDA5210 as shown in the following figure.



precharge.WMF

Figure 4-10 Principle of the precharge circuit

This circuit charges the capacitor C with an inrush current I_{load} of 240µA for a duration of T_2 until the voltage U_c appearing on the capacitor is equal to the voltage U_s at the input of the data filter. This voltage is limited to 2.5V. As soon as these voltages are equal or the duration T_2 is exceeded the precharge circuit is disabled.

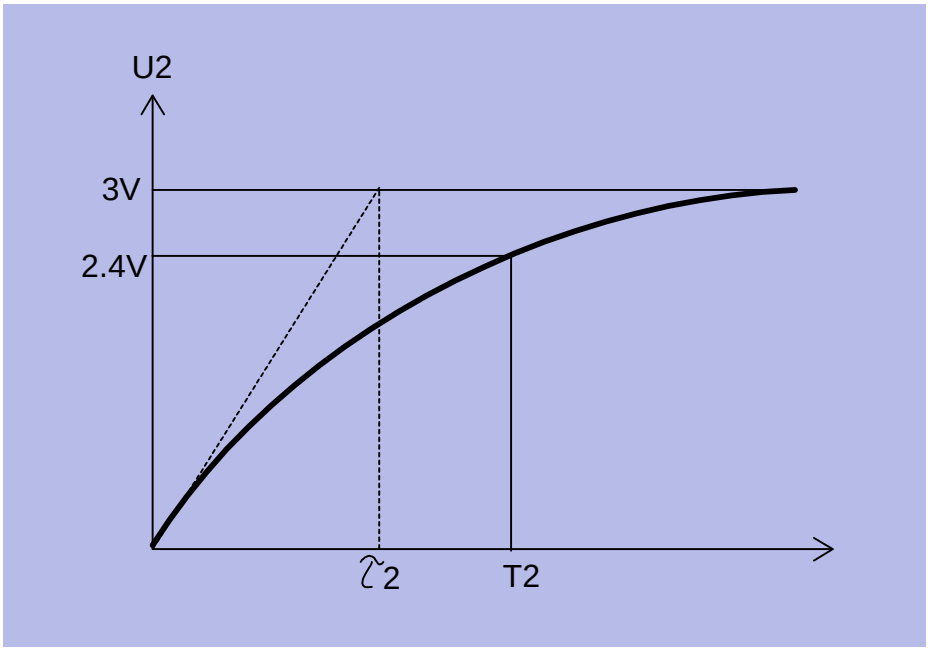
τ_2 is the time constant of the charging process of C which can be calculated as

$$\tau_2 \approx 20k\Omega \times C2$$

as the sum of R1 and R2 is sufficiently large and thus can be neglected. T2 can then be calculated according to the following formula:

$$T_2 = \tau_2 \ln\left(\frac{1}{1-\frac{2.4V}{3V}}\right) \approx \tau_2 \cdot 1.6$$

The voltage transient during the charging of C2 is shown in the following figure:



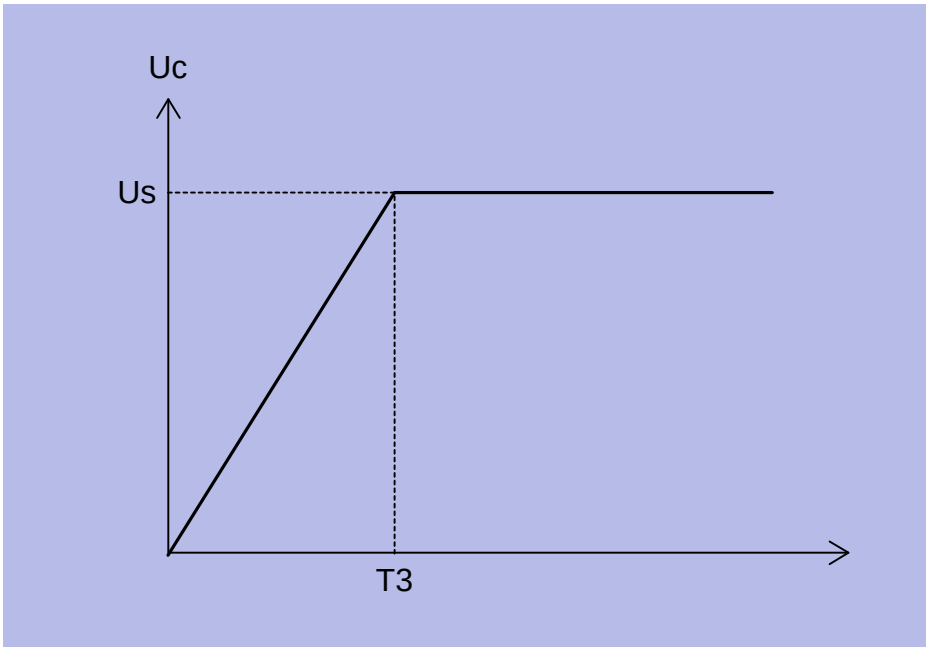
e-fkt1.WMF

Figure 4-11 Voltage appearing on C2 during precharging process

The voltage appearing on the capacitor C connected to pin 20 is shown in the following figure. It can be seen that due to the fact that it is charged by a constant current source it exhibits is a linear increase in voltage which is limited to

U_{Smax} = 2.5V which is also the approximate operating point of the data filter input. The time constant appearing in this case can be denoted as T3, which can be calculated with

$$T3 = \frac{U_{S\max} \times C}{240\mu A} = \frac{2.5V}{240\mu A} \times C$$



e-Fkt2.WMF

Figure 4-12 Voltage transient on capacitor C attached to pin 20

As an example the choice of C2 = 20nF and C = 47nF yields

τ_2 = 0.4ms

T_2 = 0.64ms

T_3 = 0.49ms

This means that in this case the inrush current could flow for a duration of 0.64ms but stops already after 0.49ms when the U_{Smax} limit has been reached. T3 should always be chosen to be shorter than T2.

It has to be noted finally that during the turn-on duration T2 the overall device power consumption is increased by the 240µA needed to charge C.

The precharge circuit may be disabled if C2 is not equipped. This yields a T2 close to zero. Note that the sum of R4 and R5 has to be 600kΩ in order to produce 3V at the THRES pin as this voltage is internally used also as the reference for the FSK demodulator.

5 Reference

Contents of this Chapter

5.1 Electrical Data

5.1.1 Absolute Maximum Ratings

WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC may result.

Table 5-1 Absolute Maximum Ratings, Ambient temperature T_{AMB}=-40°C ... + 85°C

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min	max		
1	Supply Voltage	V_s	-0.3	5.5	V	
2	Junction Temperature	T_j	-40	+125	°C	
3	Storage Temperature	T_s	-40	+150	°C	
4	Thermal Resistance	R_{thJA}		114	K/W	
5	ESD integrity, all pins	V_{ESD}	-1	+1	kV	HBM according to MIL STD 883D, method 3015.7

5.1.2 Operating Range

Within the operating range the IC operates as explained in the circuit description. The AC/DC characteristic limits are not guaranteed.

Supply voltage: VCC = 4.5V .. 5.5V

Table 5-2 Operating Range, Ambient temperature T_{AMB}= -40°C ... + 85°C

#	Parameter	Symbol	Limit Values		Unit	Test Conditions/Notes	L	Item
			min	max				
1	Supply Current	I_{SF} I_{SA}		6 5.4	mA mA	f_{RF} = 915MHz, FSK Mode f_{RF} = 915MHz, ASK Mode		
2	Receiver Input Level ASK FSK, frequ. dev. ± 50kHz	RF_{in}	 -109 -102	 -13 -13	 dBm dBm	@ source impedance 50Ω, BER 2E-3, average power level, Manchester encoded datarate 4kBit, 280kHz IF Bandwidth	■	
3	LNI Input Frequency	f_{RF}	902	928	MHz			
4	MI/X Input Frequency	f_{MI}	902	928	MHz			
6	UHF Local Oscillator Frequency Range	f_{LO}	910	932	MHz			
7	3dB IF Frequency Range	$f_{IF\ -3dB}$	5	23	MHz			
8	Powerdown Mode On	$PWDN_{ON}$	0	0.8	V			
9	Powerdown Mode Off	$PWDN_{OFF}$	2	V_S	V			
10	Gain Control Voltage, LNA high gain state	V_{THRES}	2.8	V_S	V			
11	Gain Control Voltage, LNA low gain state	V_{THRES}	0	0.7V	V			

■ Not part of the production test - either verified by design or measured in an Infineon Evalboard as described in Section 5.2.

5.1.3 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production. The device performance parameters marked with ■ are not part of the production test, but verified by design or measured in an Infineon Evalboard as described in Section 5.2.

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V

#	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L	Item
			min	typ	max				
Supply									
Supply Current									
1	Supply current, standby mode	$I_{S\ PDWN}$		90	120	nA	Pin 27 (PDWN) open or tied to 0 V		
2	Supply current, device operating in FSK mode	I_{SF}		5.4	5.7	mA	Pin 11 (FSEL) open, Pin 15 (MSEL) tied to GND		
3	Supply current, device operating in ASK mode	I_{SA}		4.8	5.1	mA	Pin 11 (FSEL) open, Pin 15 (MSEL) open		
LNA									
Signal Input LNI (PIN 3), V_{THRES} > 2.8V, high gain mode									
1	Average Power Level at BER = 2E-3 (Sensitivity) ASK	RF_{in}		-112		dBm	Manchester encoded datarate 4kBit, 280kHz IF Bandwidth	■	
2	Average Power Level at BER = 2E-3 (Sensitivity) FSK	RF_{in}		-105		dBm	Manchester enc. datarate 4kBit, 280kHz IF Bandw., ± 50kHz pk. dev.	■	
3	Input impedance, f_{RF} = 915 MHz	$S_{11\ LNA}$		0.717 / -78.4 deg				■	
4	Input level @ 1dB C.P. f_{RF}=915 MHz	$P1dB_{LNA}$		-15		dBm		■	
5	Input 3rd order intercept point f_{RF} = 915 MHz	$IIP3_{LNA}$		-14		dBm	f_{in} = 914 & 916MHz	■	
6	LO signal feedthrough at antenna port	LO_{LNI}			73	dBm		■	
Signal Output LNO (PIN 6), V_{THRES} > 2.8V, high gain mode									
1	Gain f_{RF} = 915 MHz	$S_{21\ LNA}$		1.401 / 98.4 deg				■	
2	Output impedance, f_{RF} = 915 MHz	$S_{22\ LNA}$		0.869 / -25.7 deg				■	

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V (continued)

#	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L	Item
			min	typ	max				
3	Voltage Gain Antenna to IFO f_{RF} = 915 MHz	G_{AntMI}		40		dB			
Signal Input LNI, V_{THRES} = GND, low gain mode									
1	Input impedance, f_{RF} = 915 MHz	$S_{11\ LNA}$		0.753 / -86.26 deg				■	
2	Input level @ 1dB C. P. f_{RF} = 915 MHz	$P1dB_{LNA}$		-6		dBm		■	
Signal Input LNI, V_{THRES} = GND, low gain mode									
3	Input 3rd order intercept point f_{RF} = 915 MHz	$IIP3_{LNA}$		-5		dBm	f_{in} = 914 & 916MHz	■	
Signal Output LNO, V_{THRES} = GND, low gain mode									
1	Gain f_{RF} = 915 MHz	$S_{21\ LNA}$		0.174 / 107.4 deg				■	
2	Output impedance, f_{RF} = 915 MHz	$S_{22\ LNA}$		0.868 / -28.1 deg				■	
3	Voltage Gain Antenna to IFO f_{RF} = 915 MHz	G_{AntMI}		19		dB			
Signal 3VOUT (PIN 24)									
1	Output voltage	V_{3VOUT}	2.9	3	3.1	V	I_{3Vout} = 5µA		
2	Current out	I_{3VOUT}			50	µA			
Signal THRES (PIN 23)									
1	Input Voltage range	V_{THRES}	0		V_S-1	V	see Section 4.1		
2	LNA low gain mode	V_{THRES}	0			V			
3	LNA high gain mode	V_{THRES}		3	V_S-1	V	or shorted to Pin 24		
4	Current in	I_{THRES_in}		5		nA		■	
Signal TAGC (PIN 4)									
1	Current out, LNA low gain state	I_{TAGC_out}	3.8	4.2	4.8	µA	RSSI > V_{THRES}		
2	Current in, LNA high gain state	I_{TAGC_in}	1	1.5	2	µA	RSSI < V_{THRES}		
MIXER									
Signal Input MI/MIX (PINS 8/9)									
1	Input impedance, f_{RF} = 915 MHz	$S_{11\ MIX}$		0.912 / -30.13 deg				■	
2	Input 3rd order intercept point	$IIP3_{MIX}$		-25		dBm		■	

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V (continued)

	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L	Item
			min	typ	max				
Signal Output IFO (PIN 12)									
1	Output impedance	Z_{IFO}		330		Ω		■	
2	Conversion Voltage Gain f_{RF}=915 MHz	G_{MIX}		18		dB			
LIMITER									
Signal Input LIM/X (PINS 17/18)									
1	Input Impedance	Z_{LIM}	264	330	396	Ω		■	
2	RSSI dynamic range	DR_{RSSI}	60		80	dB			
3	RSSI linearity	LIN_{RSSI}		±1		dB		■	
4	Operating frequency (3dB points)	f_{LIM}	5	10.7	23	MHz		■	
DATA FILTER									
1	Useable bandwidth	$BW_{BB\ FILT}$			100	kHz		■	
SLICER									
Signal Output DATA (PIN 25)									
1	Useable bandwith	$BW_{BB\ SLIC}$			100	kHz		■	
2	Capacitive loading of output	$C_{max\ SLIC}$			20	pF			
3	LOW output voltage	V_{SLIC_L}		0	0.1	V			
4	HIGH output voltage	V_{SLIC_H}	V_S-1.3	V_S-1	V_S-0.7	V	Output current= 200µA		
Slicer, SLN (PIN 20)									
1	Precharge Current Out	I_{PCH_SLN}	-100	-220	-300	µA	see Section 4.7		
PEAK DETECTOR									
Signal Output PDO (PIN 26)									
1	LOW output voltage	V_{SLIC_L}		0	0.1	V			
2	HIGH output voltage	V_{SLIC_H}	2.9	3	3.1	V			
3	Load current	I_{load}	-500			µA	Static output current must not exceed -500µA		
4	Leakage current	$I_{leakage}$	580	700	820	nA			

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V (continued)

	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L	Item
			min	typ	max				
CRYSTAL OSCILLATOR									
Signals CRSTL1, CRISTL 2, (PINS 1/28)									
1	Operating frequency	f_{CRSTL}	6		15	MHz	fundamental mode, series resonance		
2	Input Impedance @ ~7.2MHz	$Z_{1\text{-}28}$		- 860 + j500		Ω		■	
3	Input Impedance @ ~14.5MHz	$Z_{1\text{-}28}$		- 550 + j1050		Ω		■	
4	Serial Capacity @ ~7.2MHz	C_{S7}=C1		9.5		pF			
5	Serial Capacity @ ~14.5MHz	C_{S14}=C1		5.6		pF			
ASK/FSK Signal Switch									
Signal MSEL (PIN 15)									
1	ASK Mode	V_{MSEL}	1.4		4	V	or open		
2	FSK Mode	V_{MSEL}	0		0.2	V			
FSK DEMODULATOR									
1	Demodulation Gain	G_{FMDEM}		200		µV/ kHz			
2	Useable IF Bandwidth	BW_{IFPLL}	10.2	10.7	11.2	MHz			
POWER DOWN MODE									
Signal PDWN (PIN 27)									
1	Powerdown Mode On	$PWDN_{ON}$	0		0.8	V			
2	Powerdown Mode Off	$PWDN_{Off}$	2.8		V_S	V			
3	Input bias current PDWN	I_{PDWN}		19		µA			
4	Start-up Time until valid IF signal is detected	T_{SU}		<1		ms	**note:** startup - time is also depends on the used crystal		
PLL DIVIDER									
Signal CSEL (PIN 16)									
1	f_{CRSTL} range 7.xxMHz	V_{CSEL}	1.4		4	V	or open		

Table 5-3 AC/DC Characteristics with T_A 25 °C, V_{VCC} = 4.5 ... 5.5 V (continued)

	Parameter	Symbol	Limit Values			Unit	Test Conditions/ Notes	L	Item
			min	typ	max				
2	f_{CRSTL} range 14.xxMHz	V_{CSEL}	0		0.2	V			
3	Input bias current CSEL	I_{CSEL}		5		µA	CSEL tied to GND		

■ Not part of the production test - either verified by design or measured in an Infineon Evalboard as described in Section 5.2.

5.2 Test Circuit

The device performance parameters marked with ■ in Section 5.1.3 were either verified by design or measured on an Infineon evaluation board.

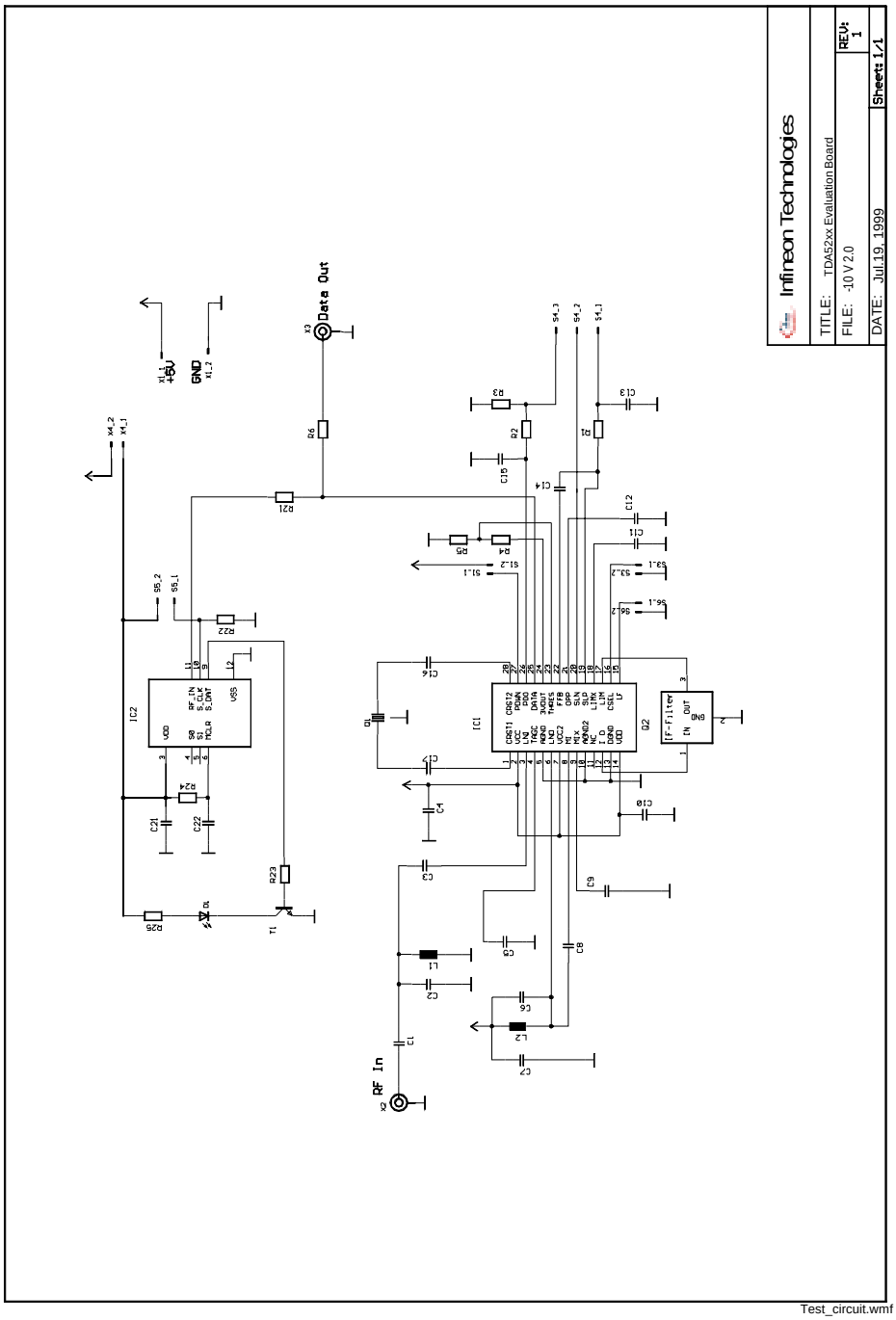


Figure 5-1 Schematic of the Evaluation Board

5.3 Test Board Layouts

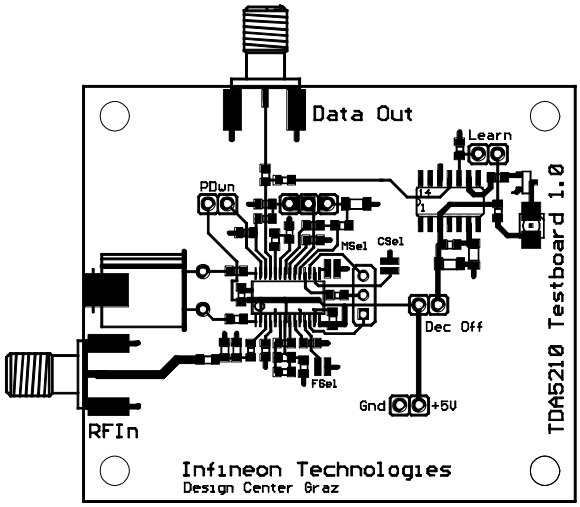


Figure 5-2 Top Side of the Evaluation Board

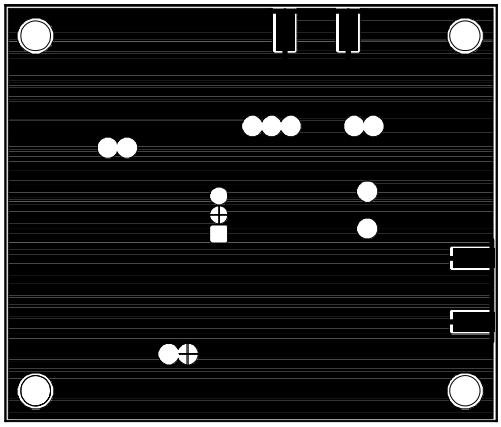


Figure 5-3 Bottom Side of the Evaluation Board

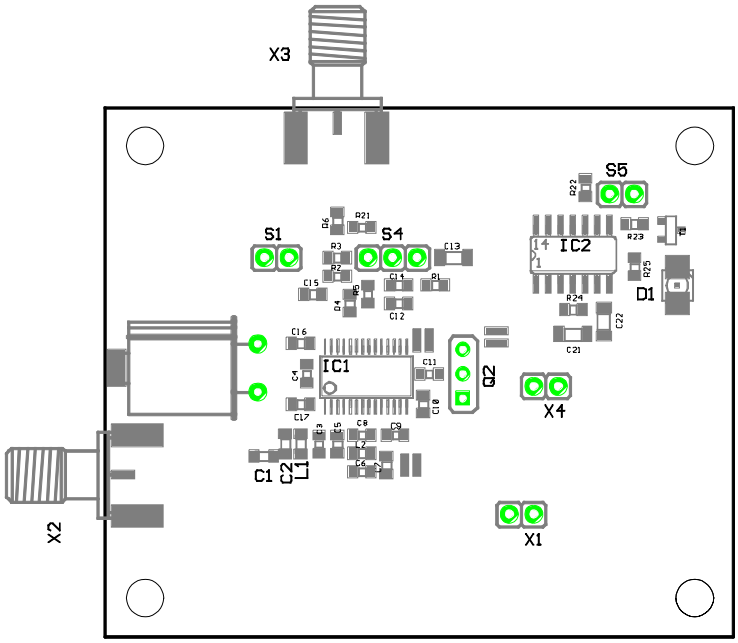


Figure 5-4 Component Placement on the Evaluation Board

5.4 Bill of Materials

The following components are necessary for evaluation of the TDA5212 at 915 MHz without use of a Microchip HCS515 decoder.

Table 5-4 Bill of Materials

Ref	Value	Specification
R1	100kΩ	0805, ± 5%
R2	100kΩ	0805, ± 5%
R3	820kΩ	0805, ± 5%
R4	240kΩ	0805, ± 5%
R5	360kΩ	0805, ± 5%
R6	10kΩ	0805, ± 5%
L1	3.3nH	Toko, PTL2012-F3N3C
L2	3.9nH	Toko, PTL2012-F3N9C
C1	1pF	0805, COG, ± 0.1pF
C2	3.3pF	0805, COG, ± 0.1pF
C3	4.7pF	0805, COG, ± 0.1pF
C4	100pF	0805, COG, ± 5%
C5	47nF	1206, X7R, ± 10%
C6	3.3pF	0805, COG, ± 0.1pF
C7	100pF	0805, COG, ± 5%
C8	22pF	0805, COG, ± 5%
C9	100pF	0805, COG, ± 5%
C10	10nF	0805, X7R, ± 10%
C11	10nF	0805, X7R, ± 10%
C12	220pF	0805, COG, ± 5%
C13	47nF	0805, X7R, ± 10%
C14	470pF	0805, COG, ± 5%
C15	47nF	0805, X7R, ± 10%
C16	8.2pF	0805, COG, ± 1%
C17	18pF	0805, COG, ± 0.25pF
Q1	14.129690MHz[1]	Jauch Q 14.129690-S1
Q2	SFE10.7MA5-A	Murata
X2, X3	142-0701-801	Johnson
X1, X4, S1, S5	STL_2POL	2-pole pin connector
S4	STL_3POL	3-pole pin connector, or not equipped
IC1	TDA 5212	Infineon

1. 14.129690MHz crystals are used in the Infineon Evalboard, which means that the L0 is in low side injection mode (L0-frequency=904.3MHz). But to guarantee the function of the IC over the whole temperature range the L0 has to be used in high side rejection mode (L0-frequency=925.7MHz), therefore 14.4640625MHz crystals have to be used for a RF of 915MHz (see also VCO-frequency range).

The following components are necessary in addition to the above mentioned ones for evaluation of the TDA5212 in conjunction with a Microchip HCS512 decoder.

Table 5-5 Bill of Materials Addendum

Ref	Value	Specification
R21	22kΩ	0805, ± 5%
R22	10kΩ	0805, ± 5%
R23	22kΩ	0805, ± 5%
R24	820kΩ	0805, ± 5%
R25	560kΩ	0805, ± 5%
C21	100nF	1206, X7R, ± 10%
C22	100nF	1206, X7R, ± 10%
IC2	HCS512	Microchip
T1	BC 847B	Infineon
D1	LS T670-JL	Infineon

6 List of Figures

7 List of Tables