19-2799; Rev 0; 4/03

MAXIM

Digitally Controlled, Variable-Gain, Differential ADC Driver/Amplifier

General Description

The MAX2055 high-performance, digitally controlled, variable-gain, differential analog-to-digital converter (ADC) driver/amplifier (DVGA) is designed for use from 30MHz to 300MHz in base station receivers.

The device integrates a digitally controlled attenuator and a high-linearity single-ended-to-differential output amplifier, which can either eliminate an external transformer, or can improve the even-order distortion performance of a transformer-coupled circuit, thus relaxing the requirements of the anti-alias filter preceding an ADC. Targeted for ADC driver applications to adjust gain either dynamically or as a one-time channel gain setting, the MAX2055 is ideal for applications requiring high performance. The attenuator provides 23dB of attenuation range with ±0.2dB accuracy.

The MAX2055 is available in a thermally enhanced 20-pin TSSOP-EP package and operates over the -40°C to +85°C temperature range.

Applications

Cellular Base Stations

PHS/PAS Infrastructure

Receiver Gain Control

Broadband Systems

Automatic Test Equipment

Terrestrial Links

High-Performance ADC Drivers

Features

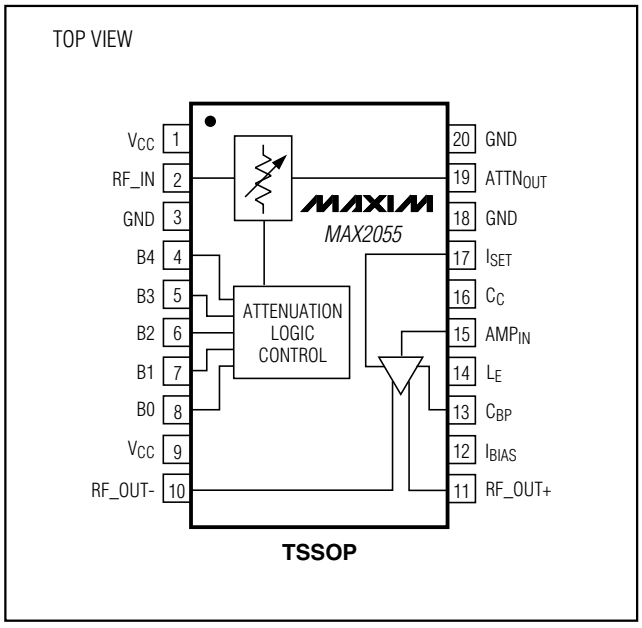
- **30MHz to 300MHz Frequency Range**
- **Single-Ended-to-Differential Conversion**
- **-3dB to +20dB Variable Gain**
- **40dBm Output IP3 (at All Gain States and 70MHz)**
- **2nd Harmonic -76dBc**
- **3rd Harmonic -69dBc**
- **Noise Figure: 5.8dB at Maximum Gain**
- **Digitally Controlled Gain with 1dB Resolution and ±0.2dB Accuracy**
- **Adjustable Bias Current**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2055EUP-T	-40°C to +85°C	20 TSSOP-EP*

**EP = Exposed paddle.*

Pin Configuration/ Functional Diagram



Digitally Controlled, Variable-Gain, Differential ADC Driver/Amplifier

ABSOLUTE MAXIMUM RATINGS

All Pins to GND. .....-0.3V to +(V_{CC} + 0.25V)
Input Signal (RF_IN).....20dBm
Output Power (RF_OUT).....24dBm
Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP (derate 21.7mW/°C above +70°C) 2.1W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1; V_{CC} = +4.75V to +5.25V, GND = 0V. No input signals applied, and input and output ports are terminated with 50Ω. R1 = 1.13kΩ, T_A = -40°C to +85°C. Typical values are at V_{CC} = +5V and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
Supply Voltage	V_{CC}		4.75	5.0	5.25	V
Supply Current	I_{CC}			240	290	mA
I_{SET} Current	I_{SET}			1.1		mA
CONTROL INPUTS						
Control Bits		Parallel		5		Bits
Input Logic High			2			V
Input Logic Low					0.6	V
Input Leakage Current			-1.2		+1.2	µA

AC ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1; V_{CC} = +4.75V to +5.25V, GND = 0V, max gain (B0 = B1 = B2 = B3 = B4 = 0), R_1 = 1.13kΩ, P_{OUT} = 5dBm, f_{IN} = 70MHz, 50Ω system impedance. Typical values are at V_{CC} = +5V and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range	f_R		30		300	MHz
Gain	G			19.9		dB
Amplitude Unbalance		(Note 3)		0.06		dB
Phase Unbalance		(Note 3)		0.7		Degrees
Minimum Reverse Isolation				29		dB
Noise Figure	NF			5.8		dB
Output 1dB Compression Point	P_{1dB}			25.7		dBm
2nd-Order Output Intercept Point	OIP2	$f_1 + f_2$, f_1 = 70MHz, f_2 = 71MHz, 5dBm/tone at RF_OUT		75		dBm
3rd-Order Output Intercept Point	OIP3	All gain conditions, 5dBm/tone at RF_OUT		40		dBm
2nd Harmonic	$2f_{IN}$			-76		dBc
3rd Harmonic	$3f_{IN}$			-69		dBc
RF Gain-Control Range				23		dB
Gain-Control Resolution				1		dB
Attenuation Absolute Accuracy		Compared to the ideal expected attenuation		±0.2		dB
Attenuation Relative Accuracy		Between adjacent states		+0.05/ -0.2		dB
Gain Drift Over Temperature		T_A = -40°C to +85°C		±0.3		dB

AC ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1; V_{CC} = +4.75V to +5.25V, GND = 0V, max gain (B0 = B1 = B2 = B3 = B4 = 0), R_1 = 1.13kΩ, P_{OUT} = 5dBm, f_{IN} = 70MHz, 50Ω system impedance. Typical values are at V_{CC} = +5V and T_A = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain Flatness Over 50MHz Bandwidth		Peak-to-peak for all settings		0.5		dB
Attenuator Switching Time		50% control to 90% RF		40		ns
Input Return Loss		f_R = 30MHz to 300MHz, all gain conditions		15		dB
Output Return Loss		f_R = 30MHz to 250MHz, all gain conditions		15		dB
		f_R = 250MHz to 300MHz, all gain conditions		12		

Note 1: Guaranteed by design and characterization.

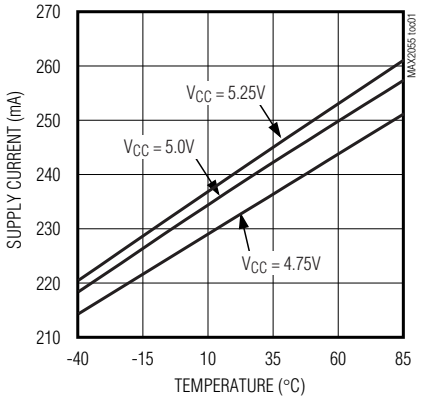
Note 2: All limits reflect losses of external components. Output measurements are taken at RF_OUT using the application circuit shown in Figure 1.

Note 3: The amplitude and phase unbalance are tested with 50Ω resistors connected from OUT+/OUT- to GND.

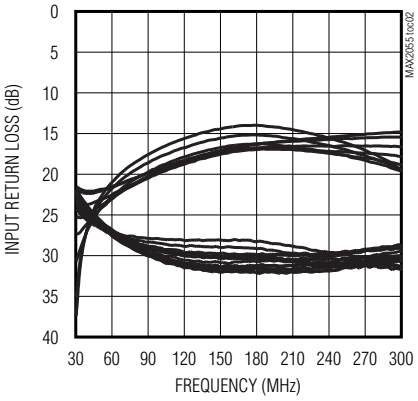
Typical Operating Characteristics

(**Circuit of Figure 1**, V_{CC} = 5.0V, **R_1 = 1.13kΩ**, max gain (B0 = B1 = B2 = B3 = B4 = 0), P_{OUT} = 5dBm, T_A = +25°C, unless otherwise noted.)

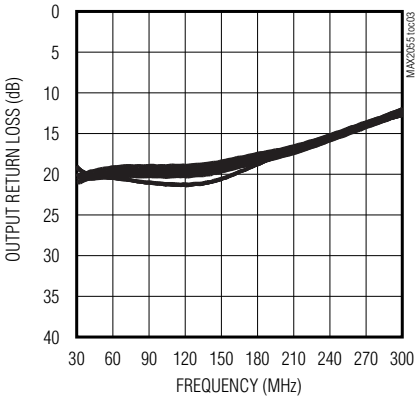
SUPPLY CURRENT vs. TEMPERATURE



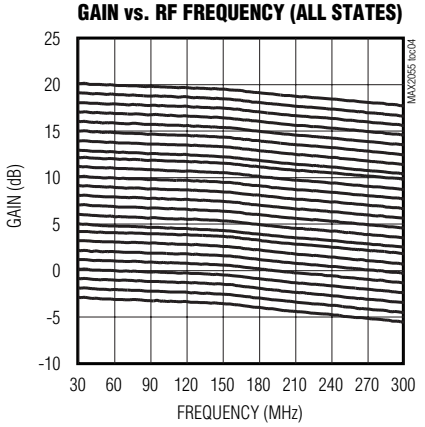
INPUT RETURN LOSS vs. RF FREQUENCY (ALL STATES)



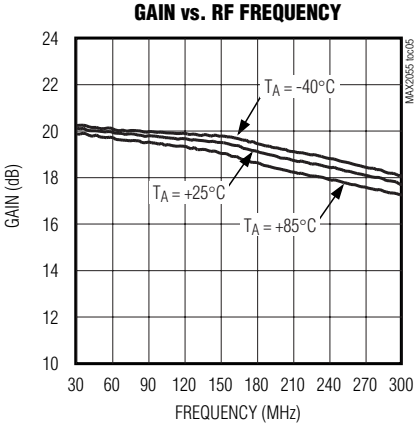
OUTPUT RETURN LOSS vs. RF FREQUENCY (ALL STATES)



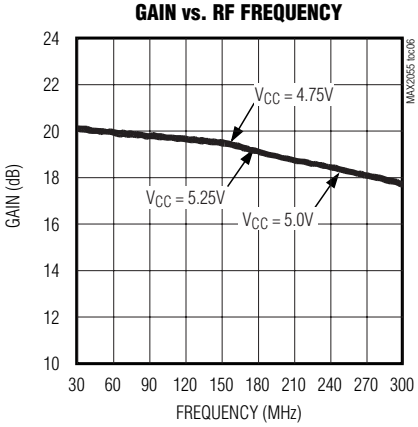
GAIN vs. RF FREQUENCY (ALL STATES)



GAIN vs. RF FREQUENCY



GAIN vs. RF FREQUENCY

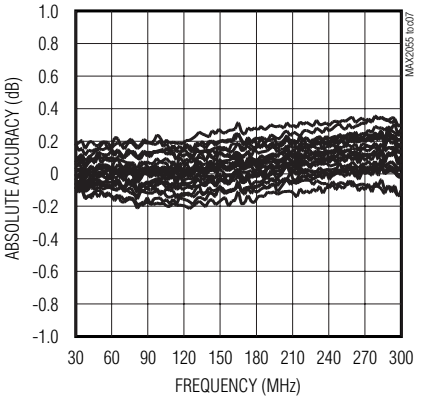


Digitally Controlled, Variable-Gain, Differential ADC Driver/Amplifier

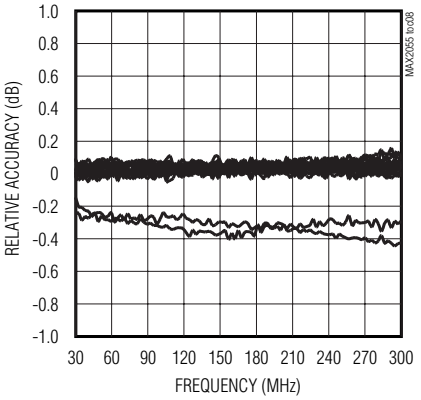
Typical Operating Characteristics (continued)

(**Circuit of Figure 1**, V_{CC} = 5.0V, **R_1 = 1.13kΩ**, max gain (B0 = B1 = B2 = B3 = B4 = 0), P_{OUT} = 5dBm, T_A = +25°C, unless otherwise noted.)

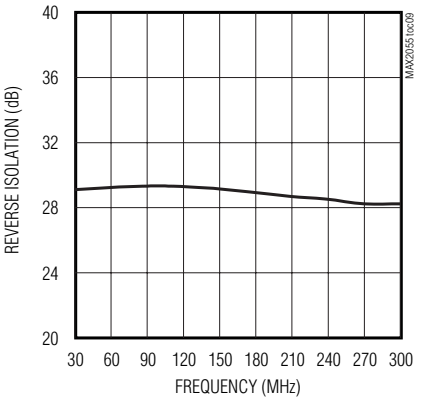
ATTENUATION ABSOLUTE ACCURACY (ALL STATES)



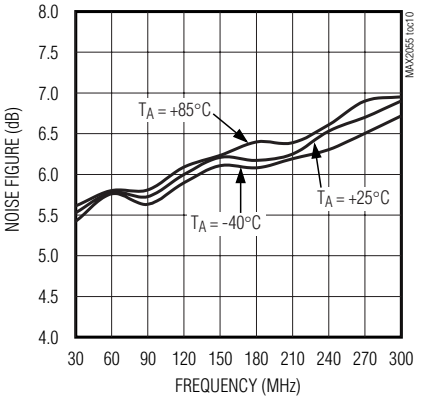
ATTENUATION RELATIVE ACCURACY (ALL STATES)



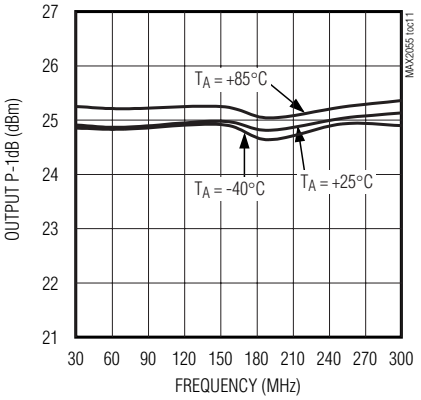
REVERSE ISOLATION vs. RF FREQUENCY



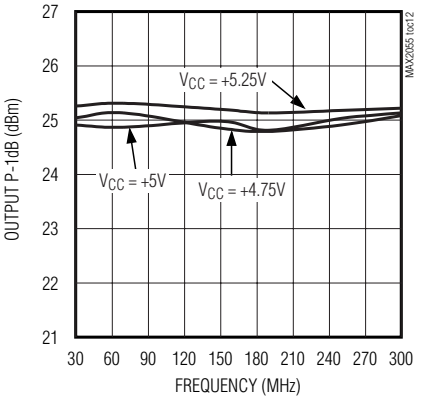
NOISE FIGURE vs. FREQUENCY



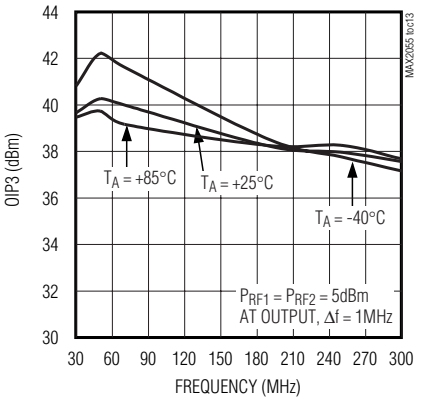
OUTPUT P-1dB vs. FREQUENCY



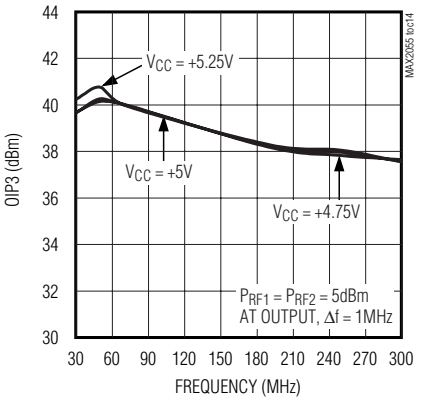
OUTPUT P-1dB vs. FREQUENCY



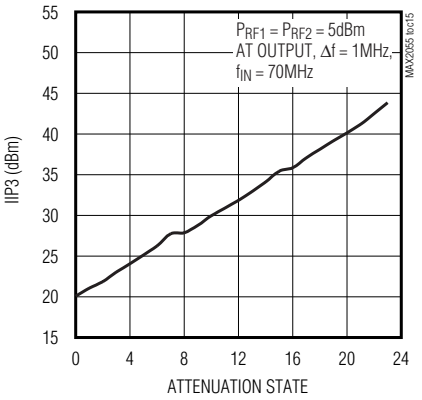
OUTPUT IP3 vs. FREQUENCY



OUTPUT IP3 vs. FREQUENCY



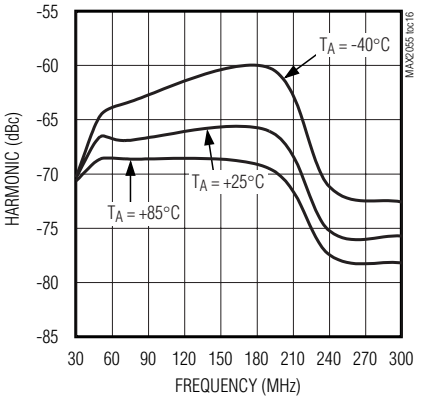
INPUT IP3 vs. ATTENUATION STATE



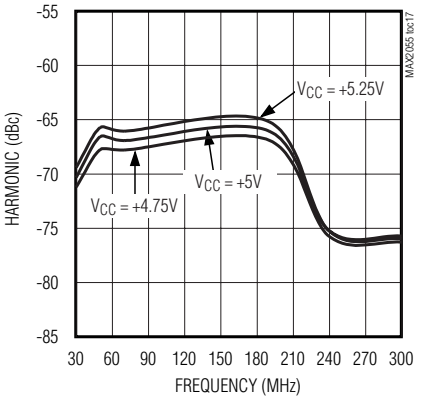
Typical Operating Characteristics (continued)

(**Circuit of Figure 1**, V_{CC} = 5.0V, **R_1 = 1.13kΩ**, max gain (B0 = B1 = B2 = B3 = B4 = 0), P_{OUT} = 5dBm, T_A = +25°C, unless otherwise noted.)

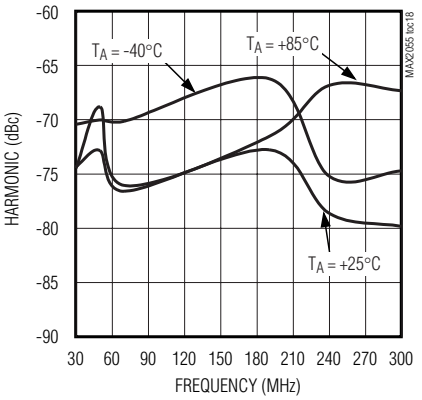
3RD HARMONIC vs. FREQUENCY



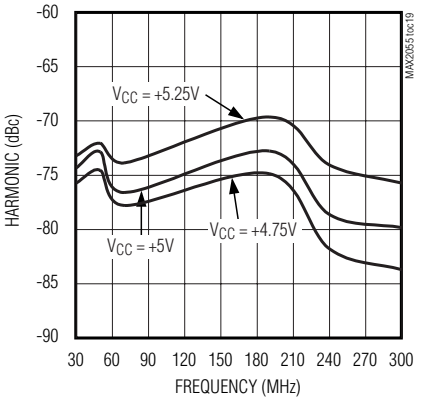
3RD HARMONIC vs. FREQUENCY



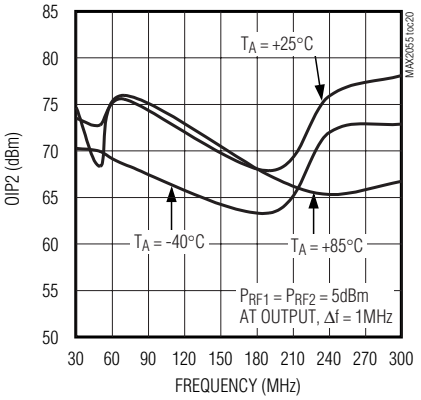
2ND HARMONIC vs. FREQUENCY



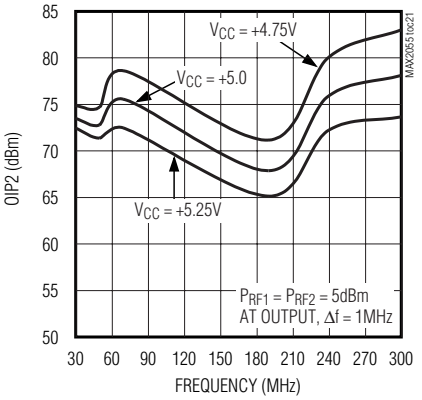
2ND HARMONIC vs. FREQUENCY



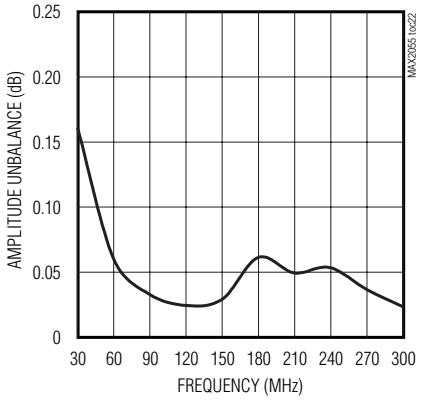
OUTPUT IP2 vs. FREQUENCY ($f_1 + f_2$)



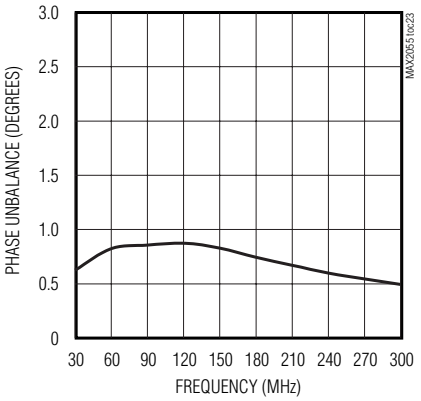
OUTPUT IP2 vs. FREQUENCY ($f_1 + f_2$)



OUTPUT-PORT AMPLITUDE UNBALANCE vs. FREQUENCY



OUTPUT-PORT PHASE UNBALANCE vs. FREQUENCY

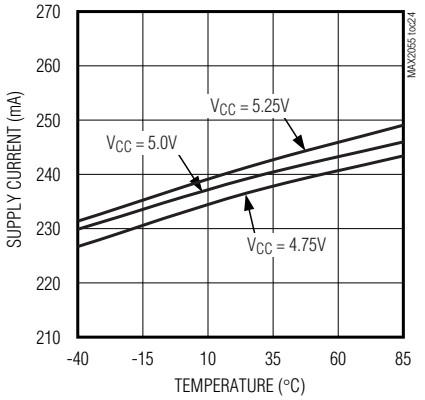


Digitally Controlled, Variable-Gain, Differential ADC Driver/Amplifier

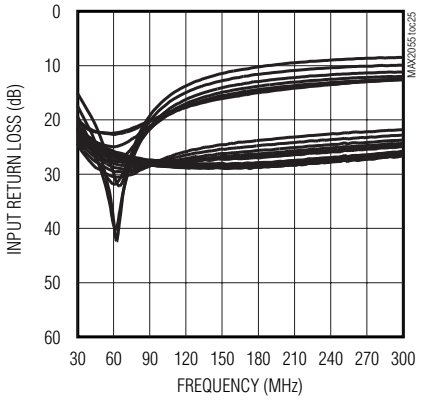
Typical Operating Characteristics

(**Circuit of Figure 2**, V_{CC} = 5.0V, **R_1 = 909Ω**, max gain, (B0 = B1 = B2 = B3 = B4 = 0), P_{OUT} = 5dBm, T_A = +25°C, unless otherwise noted.)

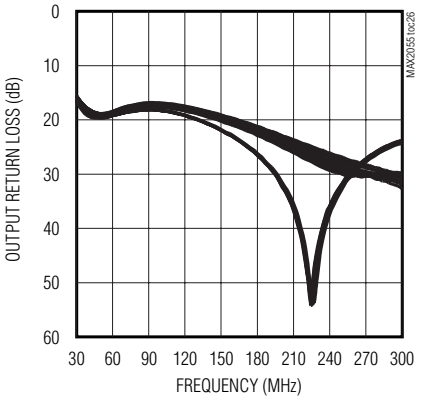
SUPPLY CURRENT vs. TEMPERATURE



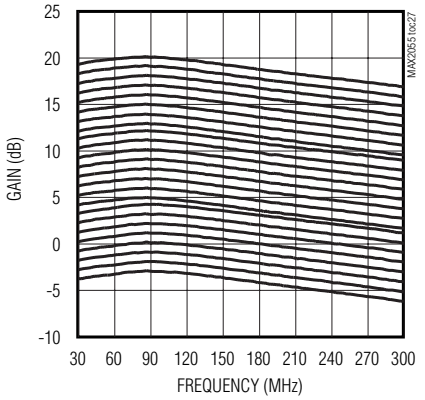
INPUT RETURN LOSS vs. RF FREQUENCY (ALL STATES)



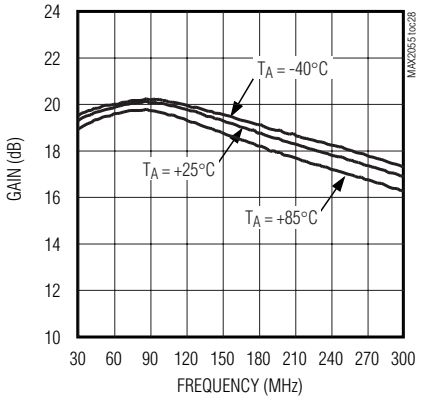
OUTPUT RETURN LOSS vs. FREQUENCY (ALL STATES)



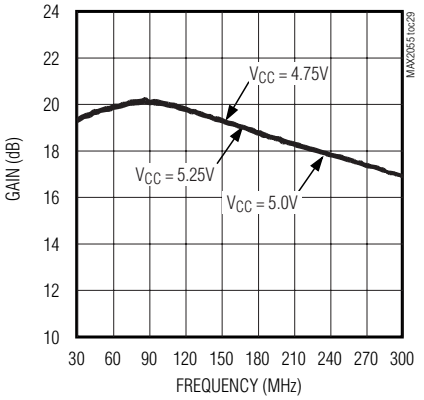
GAIN vs. RF FREQUENCY (ALL STATES)



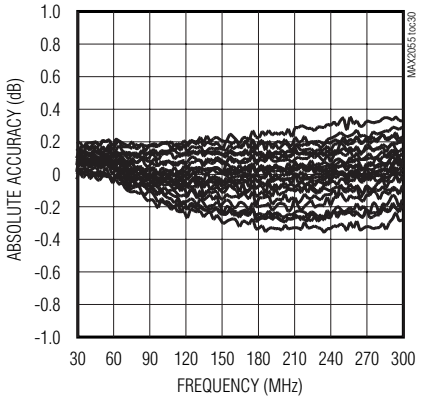
GAIN vs. RF FREQUENCY



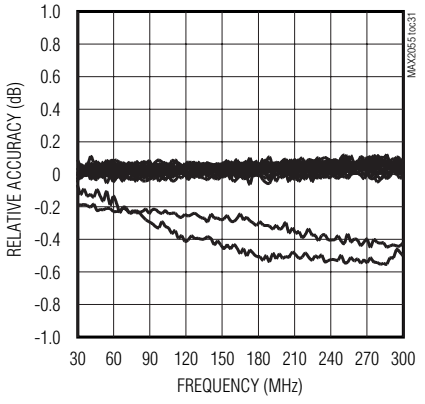
GAIN vs. RF FREQUENCY



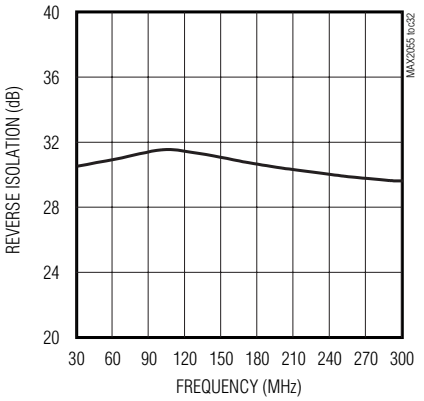
ATTENUATION ABSOLUTE ACCURACY (ALL STATES)



ATTENUATION RELATIVE ACCURACY (ALL STATES)



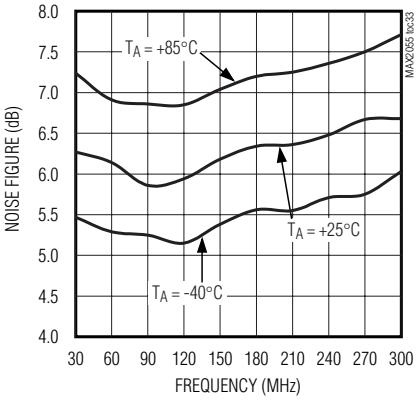
REVERSE ISOLATION vs. RF FREQUENCY



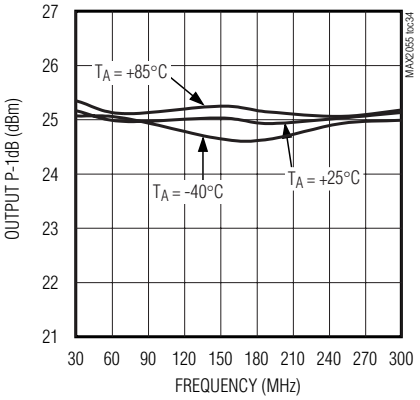
Typical Operating Characteristics (continued)

(**Circuit of Figure 2**, V_{CC} = 5.0V, **R_1 = 909Ω**, max gain, (B0 = B1 = B2 = B3 = B4 = 0), P_{OUT} = 5dBm, T_A = +25°C, unless otherwise noted.)

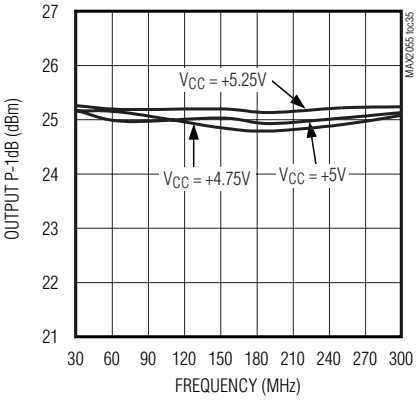
NOISE FIGURE vs. FREQUENCY



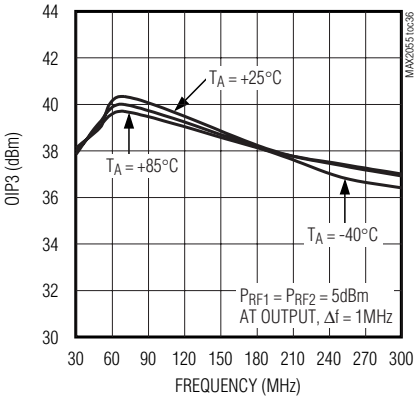
OUTPUT P-1dB vs. FREQUENCY



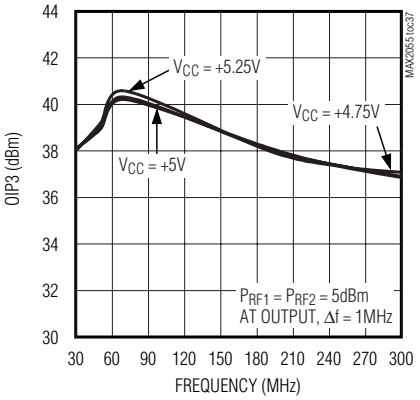
OUTPUT P-1dB vs. FREQUENCY



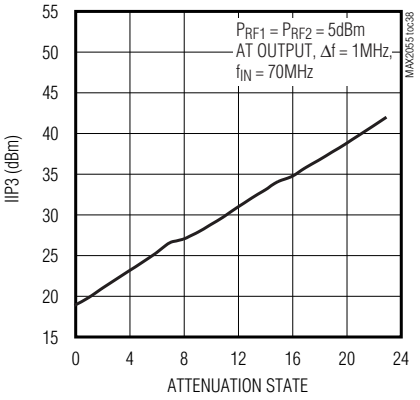
OUTPUT IP3 vs. FREQUENCY



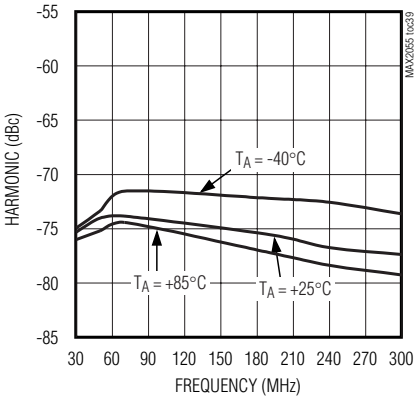
OUTPUT IP3 vs. FREQUENCY



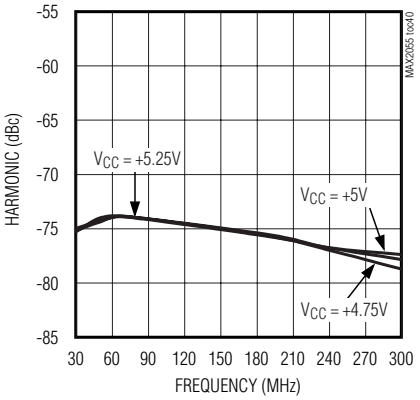
INPUT IP3 vs. ATTENUATION STATE



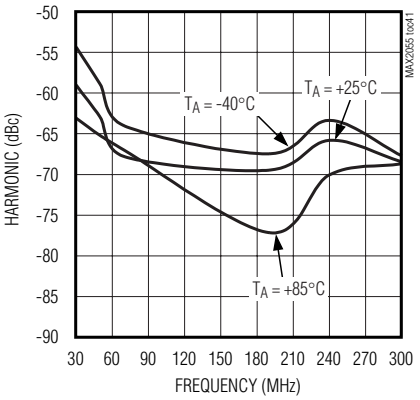
3RD HARMONIC vs. FREQUENCY



3RD HARMONIC vs. FREQUENCY



2ND HARMONIC vs. FREQUENCY

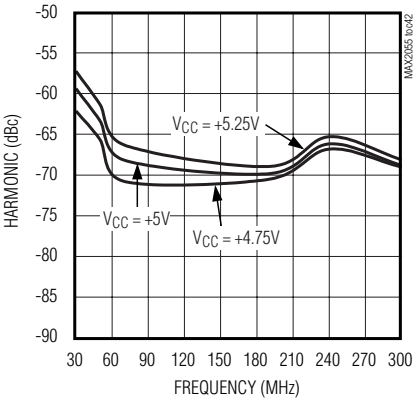


Digitally Controlled, Variable-Gain, Differential ADC Driver/Amplifier

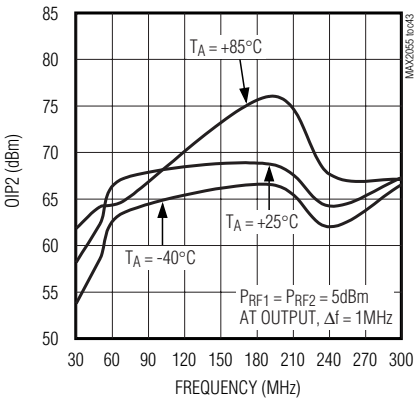
Typical Operating Characteristics (continued)

(**Circuit of Figure 2**, V_{CC} = 5.0V, **R_1 = 909Ω**, max gain, (B0 = B1 = B2 = B3 = B4 = 0), P_{OUT} = 5dBm, T_A = +25°C, unless otherwise noted.)

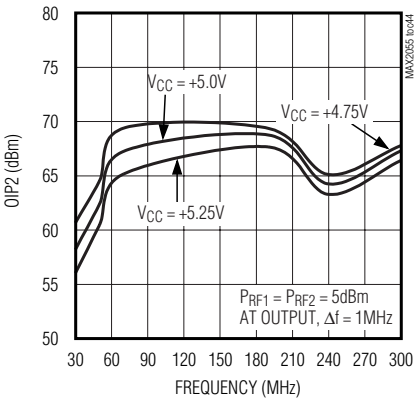
2ND HARMONIC vs. FREQUENCY



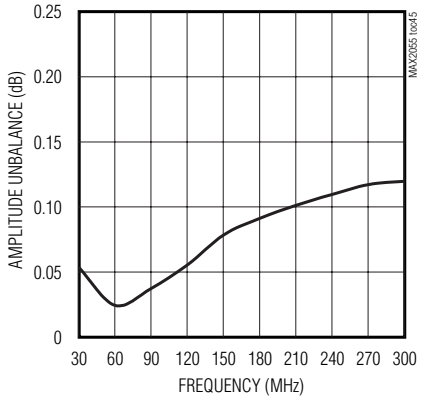
OUTPUT IP2 vs. FREQUENCY ($f_1 + f_2$)



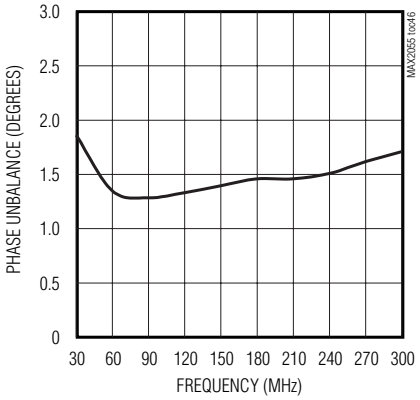
OUTPUT IP2 vs. FREQUENCY ($f_1 + f_2$)



OUTPUT-PORT AMPLITUDE UNBALANCE vs. FREQUENCY



OUTPUT-PORT PHASE UNBALANCE vs. FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1, 9	V_{CC}	Power Supply. Bypass to GND with capacitors as close to the pin as possible as shown in the typical application circuits (Figures 1 and 2).
2	RF_IN	Signal Input. Internally matched to 50Ω over the operating frequency. See the typical application circuit for recommended component values.
3, 18, 20, EP	GND	Ground. Use low-inductance layout techniques on the PC board. Solder the exposed paddle to the board ground plane.
4–8	B4–B0	Attenuation Control Bits. Digital input for attenuation control. See Table 3 for attenuation setting.
10	RF_OUT-	Inverted Differential Signal Output. Requires an external pullup choke inductor (120mA typical current) to V_{CC} along with a DC-blocking capacitor; see Figures 1 and 2.
11	RF_OUT+	Noninverted Differential Signal Output. Requires an external pullup choke inductor (120mA typical current) to V_{CC} along with a DC-blocking capacitor; see Figures 1 and 2.
12	I_{BIAS}	Amplifier Bias Input. See Figures 1 and 2 for detailed connection.
13	C_{BP}	Bypass Capacitor. See Figures 1 and 2 for detailed connection.
14	L_E	Amplifier DC Ground. Requires choke inductor that can handle supply current. DC resistance of inductor should be less than 0.2Ω.
15	AMP_{IN}	Amplifier Input. Requires DC-coupling to allow biasing.
16	C_C	Compensation Capacitor. Requires connection to AMP_{IN} (pin 15) for stability.
17	I_{SET}	Connect R1 from I_{SET} to GND (see Table 1 or Table 2 for values).
19	$ATTN_{OUT}$	Attenuator Output. Requires external DC-blocking capacitor.

Table 1. Suggested Components of Circuit of Figure 1

COMPONENT	VALUE	SIZE
C1, C3–C6, C8, C9, C10, C12	1nF	0603
C2, C11	100pF	0603
L1, L3	330nH	0603
L2	100nH	0603
L4, L5	680nH	1008
R1	1.13kΩ	0603
R7	10Ω	0603
T1, T2	1:1	—

Table 2. Suggested Components of Circuit of Figure 2

COMPONENT	VALUE	SIZE
C1, C3, C4, C5, C7–C10, C12	1nF	0603
C2, C11	100pF	0603
L1, L2, L3	330nH	0603
L4, L5	680nH	1008
R1	909Ω	0603
R7	10Ω	0603
T2	1:1	—

Digitally Controlled, Variable-Gain, Differential ADC Driver/Amplifier

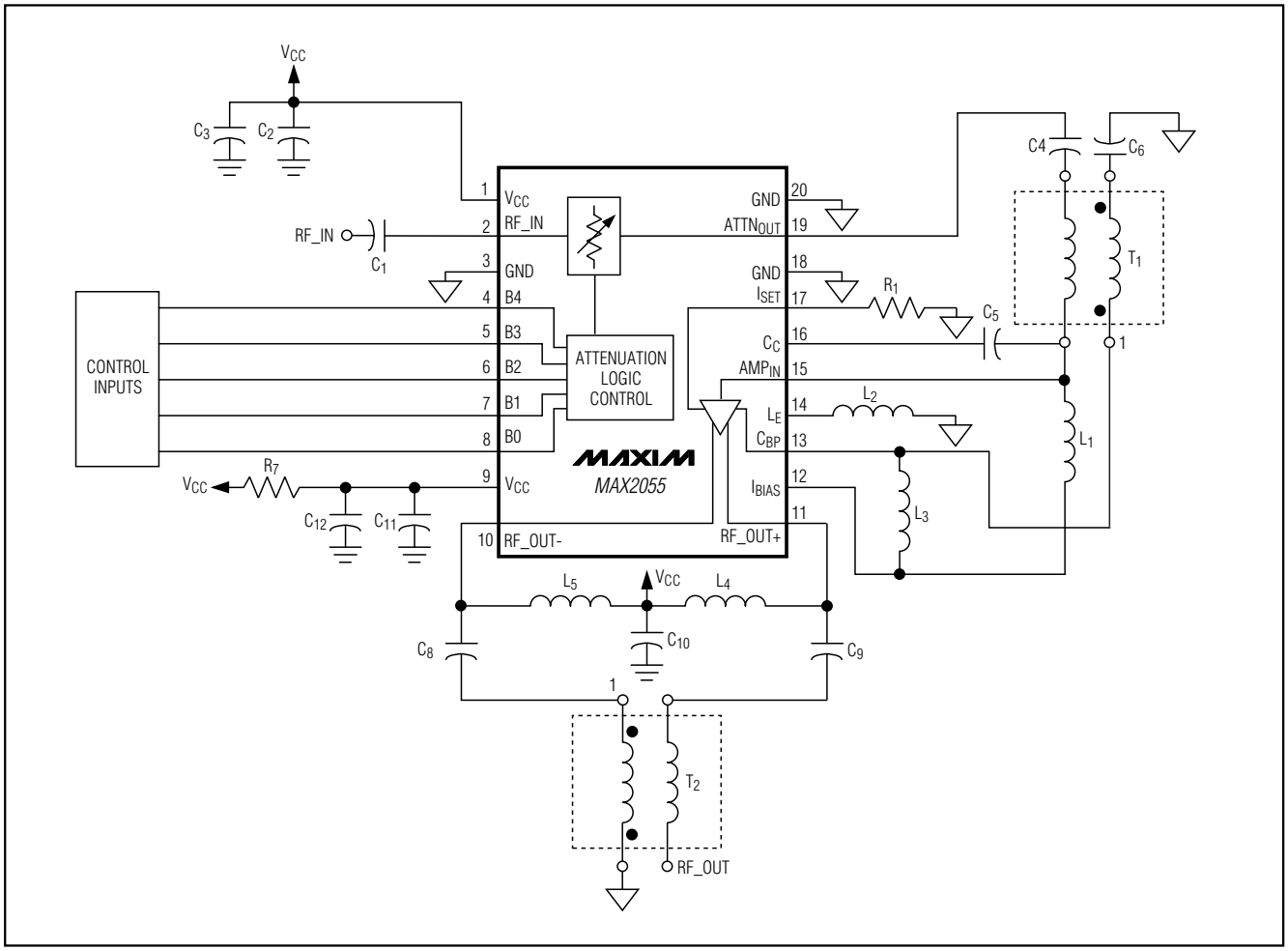


Figure 1. Typical Application Circuit

Detailed Description

The MAX2055 is a high-dynamic-range, digitally controlled, variable-gain differential ADC driver/amplifier (DVGA) for use in applications from 30MHz to 300MHz. The amplifier is designed for 50Ω single-ended input and 50Ω differential output systems.

The MAX2055 integrates a digital attenuator with a 23dB selectable attenuation range and a high-linearity, single-ended-to-differential output amplifier. The attenuator is digitally controlled through five logic lines: B0–B4. The on-chip attenuator provides up to 23dB of attenuation with ±0.2dB accuracy. The single-ended input to differential output amplifier utilizes negative feedback to achieve high gain and linearity over a wide bandwidth.

Applications Information

Digitally Controlled Attenuator

The digital attenuator is controlled through five logic lines: B0, B1, B2, B3, and B4. Table 3 lists the attenuation settings. The input and output of this attenuator require external DC blocking capacitors. The attenuator's insertion loss is approximately 2dB, when the control bits are set to 0dB (B0 = B1 = B2 = B3 = B4 = 0).

Single-Ended-to-Differential Amplifier

The MAX2055 integrates a single-ended-to-differential amplifier with a nominal gain of 22dB in a negative

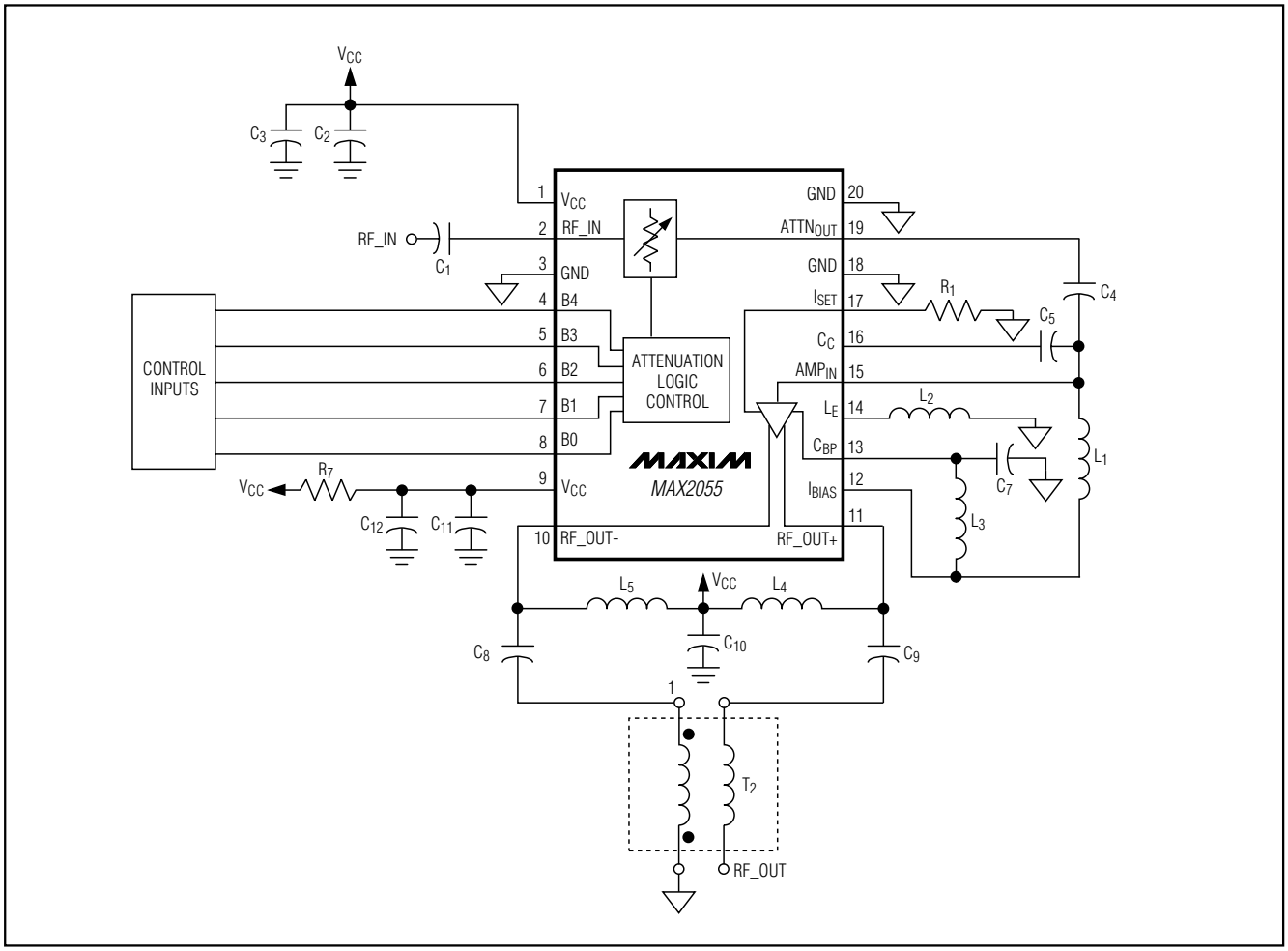


Figure 2. Low-Cost Application Circuit

feedback topology. This amplifier is optimized for a frequency range of operation from 30MHz to 300MHz with a high-output third-order intercept point (OIP3). The bias current is chosen to optimize the IP3 of the amplifier. When R_1 is 1.13kΩ (909Ω if using the circuit of Figure 2), the current consumption is 240mA while exhibiting a 40dBm typical output IP3 at 70MHz. The common-mode inductor, L_2, provides a high common-mode rejection with excellent amplitude and phase balance at the output. L_2 must handle the supply current and have DC resistance less than 0.2Ω.

Choke Inductor

The single-ended amplifier input and differential output ports require external choke inductors. At the input, connect a 330nH bias inductor from AMP_{IN} (pin 15) to I_{BIAS} (pin 12). Connect 680nH choke inductors from RF_OUT+ (pin 11) and RF_OUT- (pin 10) to V_{CC}. These connections provide bias current to the amplifier.

Layout Considerations

A properly designed PC board is an essential part of any RF/microwave circuit. Keep RF signal lines as short as possible to reduce losses, radiation, and inductance. For best performance, route the ground-pin traces directly to the exposed pad underneath the

Digitally Controlled, Variable-Gain, Differential ADC Driver/Amplifier

package. This pad should be connected to the ground plane of the board by using multiple vias under the device to provide the best RF/thermal conduction path. Solder the exposed pad on the bottom of the device package to a PC board exposed pad.

The MAX2055 Evaluation Kit can be used as a reference for board layout. Gerber files are available upon request at www.maxim-ic.com.

Power-Supply Bypassing

Proper voltage-supply bypassing is essential for high-frequency circuit stability. Bypass each V_{CC} pin with a 1000pF and 100pF capacitor. Connect the 100pF capacitor as close to the device as possible. Resistor R7 helps reduce switching transients. If switching transients are not a concern, R7 is not required. Therefore, connect pin 9 directly to V_{CC}.

Exposed Paddle RF Thermal Considerations

The EP of the MAX2055's 20-pin TSSOP-EP package provides a low thermal-resistance path to the die. It is important that the PC board on which the IC is mounted be designed to conduct heat from this contact. In addition, the EP provides a low-inductance RF ground path for the device.

It is recommended that the EP be soldered to a ground plane on the PC board, either directly or through an array of plated via holes.

Soldering the pad to ground is also critical for efficient heat transfer. Use a solid ground plane wherever possible.

Chip Information

TRANSISTOR COUNT: 325

PROCESS: BiCMOS

Table 3. Attenuation Setting vs. Gain-Control Bits

ATTENUATION	B4	B3*	B2	B1	B0
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
6	0	0	1	1	0
7	0	0	1	1	1
8	0	1	0	0	0
9	0	1	0	0	1
10	0	1	0	1	0
11	0	1	0	1	1
12	0	1	1	0	0
13	0	1	1	0	1
14	0	1	1	1	0
15	0	1	1	1	1
16	1	X	0	0	0
17	1	X	0	0	1
18	1	X	0	1	0
19	1	X	0	1	1
20	1	X	1	0	0
21	1	X	1	0	1
22	1	X	1	1	0
23	1	X	1	1	1

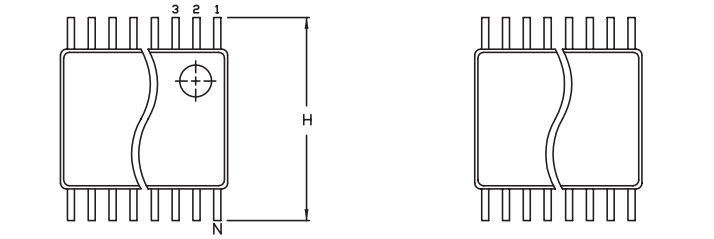
**Enabling B4 disables B3 and the minimum attenuation is 16dB.*

Digitally Controlled, Variable-Gain, Differential ADC Driver/Amplifier

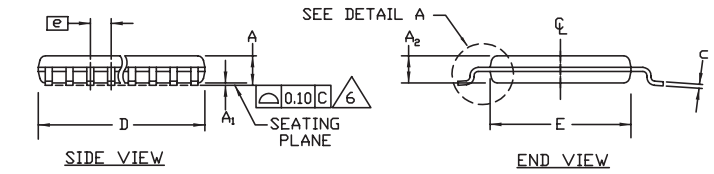
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°



JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-], THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	F	1/1