Keywords: line build-out, LBO, pulse amplitude

APPLICATION NOTE 402

Additional Pulse Amplitude Settings for DS2148, DS21348, DS21Q48, DS21Q348 and DS21448

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Abstract: This application note shows how to use undocumented settings to modify output amplitudes.

Introduction

This application note provides the register settings for the DS2148/DS21348/DS21Q48/DS213Q48 and DS21448 to configure the transmitter for pulse amplitudes that are different than the line build-out (LBO) modes documented in the respective data sheets. The following tables list the register settings and define the resulting pulse amplitudes for the 3.3V (DS21348, DS21Q348) and 5V (DS2148, DS21Q48) devices.

Table 1. DS21348, DS21Q348 Register Settings
Operating Voltage: 3.3V (VSM pin wired low)
Applicable Devices: DS21348, DS21Q348
Applicable Device Revisions: A2, B1, C1, and C2 (DS21Q348)
Operating Mode: E1

L2 (CCR4.7)	L1 (CCR4.6)	L0 (CCR4.5)	APPLICATION	TYPICAL CHANGE IN PULSE AMPLITUDE	RETURN LOSS (dB)	Rt (Ω)
0	1	0	75Ω normal	7% **enhancement** over LBO setting 0	N.M.	0
0	1	1	120Ω normal	8% **enhancement** over LBO setting 1	N.M.	0
1	1	0	120Ω normal with high return loss	8% **attenuation** over LBO setting 5	21	9.1
1	1	1	120Ω normal with high return loss	4% **attenuation** over LBO setting 5	21	10

N.M. = not meaningful

Table 2. DS2148, DS21Q48 Register Settings
Operating Voltage: 5V (VSM pin wired high)
Applicable Devices: DS2148, DS21Q48
Applicable Device Revisions: A2, B1, C1 and C2 (DS21Q48)
Operating Mode: E1

L2 (CCR4.7)	L1 (CCR4.6)	L0 (CCR4.5)	APPLICATION	TYPICAL CHANGE IN PULSE AMPLITUDE	RETURN LOSS (dB)	Rt (Ω)
0	1	0	75Ω normal	10% **enhancement** over LBO setting 0	N.M.	0
0	1	1	120Ω normal	10% **enhancement** over LBO setting 1	N.M.	0
1	1	0	120Ω normal with high return loss	10% **attenuation** over LBO setting 5	21	22
1	1	1	120Ω normal with high return loss	10% **enhancement** over LBO setting 5	21	33

In addition to the these settings, additional pulse amplitudes can be obtained in the following devices by setting test register 2 (Address 14h) as per Table 3.

Table 3. Additional Pulse Amplitude Settings

OPERATING MODE	APPLICABLE DEVICES	APPLICABLE DEVICE REVISIONS	TEST2 (ADDRESS 14h) REGISTER SETTINGS	TYPICAL CHANGE IN PULSE AMPLITUDE
E1	DS21348, DS21Q348	C1	D0	38% **enhancement** over LBO setting 0, 1, 2, and 3
	DS21348, DS21Q348, DS2148, DS21Q48	C1	E0	19% **enhancement** over LBO setting 0, 1, 2, and 3
T1/J1	DS21348, DS21Q348	C1	D0	38% **enhancement** over LBO setting 0, 5, 6, and 7
	DS21348, DS21Q348, DS2148, DS21Q48	C1	E0	19% **enhancement** over LBO setting 0, 5, 6, and 7
E1	DS21448	A1	D0	33% **enhancement** over LBO setting 0, 1, 2, and 3
T1/J1	DS21448	A1	D0	33% **enhancement** over LBO setting 0, 5, 6, and 7

In addition to the above settings, writing a HEX BO in address 14h (register TEST2) reduces any tendency of the waveform to ring.

To learn more about testing Dallas Semiconductor line interface units and transceivers for compliance to T1/J1 and E1 pulse mask specifications, refer to *Application Note 397: Pulse Template Measurement*

Related Parts		
DS21348	3.3V E1/T1/J1 Line Interface	Free Samples
DS21448	3.3V E1/T1/J1 Quad Line Interface	Free Samples
DS2148	5V E1/T1/J1 Line Interface	
DS21Q348	3.3V E1/T1/J1 Line Interface	
DS21Q48	5V E1/T1/J1 Line Interface	

More Information
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