Features

- High-density, High-performance, Electrically-erasable Complex Programmable Logic Device
  - 32 Macrocells
  - 5 Product Terms per Macrocell, Expandable up to 40 per Macrocell
  - 44 Pins
  - 7.5 ns Maximum Pin-to-pin Delay
  - Registered Operation up to 125 MHz
  - Enhanced Routing Resources
- In-System Programmability (ISP) via JTAG
- Flexible Logic Macrocell
  - D/T Latch Configurable Flip-flops
  - Global and Individual Register Control Signals
  - Global and Individual Output Enable
  - Programmable Output Slew Rate
  - Programmable Output Open Collector Option
  - Maximum Logic Utilization by Burying a Register with a COM Output
- Advanced Power Management Features
- Automatic 10 µA Standby for "L" Version
- Pin-controlled 1 mA Standby Mode
- Programmable Pin-keeper Inputs and I/Os
- Reduced-power Feature per Macrocell
- Available in Commercial and Industrial Temperature Ranges
- Available in 44-lead PLCC and TQFP
- Advanced EEPROM Technology
  - 100% Tested
  - Completely Reprogrammable
  - 10,000 Program/Erase Cycles
  - 20-year Data Retention
  - 2000V ESD Protection
  - 200 mA Latch-up Immunity
- JTAG Boundary-scan Testing to IEEE Std. 1149.1-1990 and 1149.1a-1993 Supported
- PCI-compliant
- Security Fuse Feature
- Green (Pb/Halide-fee/RoHS Compliant) Package Options

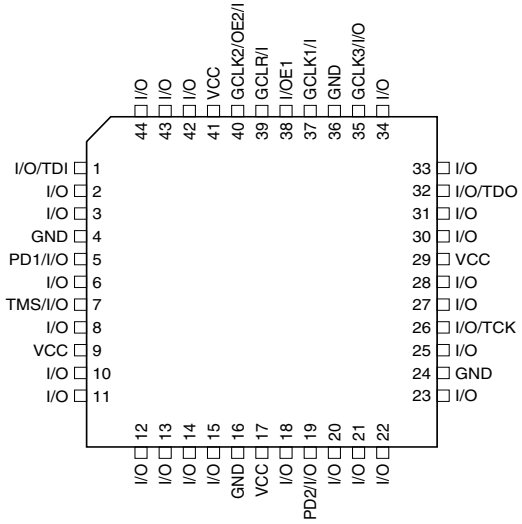
Enhanced Features

- Improved Connectivity (Additional Feedback Routing, Alternate Input Routing)
- Output Enable Product Terms
- D Latch Mode
- Combinatorial Output with Registered Feedback within Any Macrocell
- Three Global Clock Pins
- ITD (Input Transition Detection) Circuits on Global Clocks, Inputs and I/O ("L" Versions)
- Fast Registered Input from Product Term
- Programmable "Pin-keeper" Option
- V_{CC} Power-up Reset Option
- Pull-up Option on JTAG Pins TMS and TDI
- Advanced Power Management Features
  - Input Transition Detection
  - Power-down ("L" Versions)
  - Individual Macrocell Power Option
  - Disable ITD on Global Clocks, Inputs and I/O

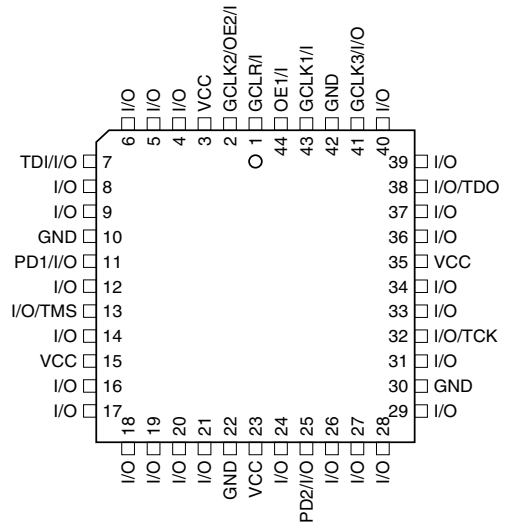
High-performance EEPROM CPLD

ATF1502AS
ATF1502ASL

44-lead TQFP
Top View



44-lead PLCC
Top View



Description

The ATF1502AS is a high-performance, high-density complex programmable logic device (CPLD) that utilizes Atmel's proven electrically-erasable technology. With 32 logic macrocells and up to 36 inputs, it easily integrates logic from several TTL, SSI, MSI, LSI and classic PLDs. The ATF1502AS's enhanced routing switch matrices increase usable gate count and the odds of successful pin-locked design modifications.

The ATF1502AS has up to 32 bi-directional I/O pins and four dedicated input pins, depending on the type of device package selected. Each dedicated pin can also serve as a global control signal, register clock, register reset or output enable. Each of these control signals can be selected for use individually within each macrocell.

PCI DC Characteristics (Preliminary)

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Supply Voltage		4.75	5.25	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
I_{IH}	Input High Leakage Current(1)	V_{IN} = 2.7V		70	µA
I_{IL}	Input Low Leakage Current(1)	V_{IN} = 0.5V		-70	µA
V_{OH}	Output High Voltage	I_{OUT} = -2 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OUT} = 3 mA, 6 mA		0.55	V
C_{IN}	Input Pin Capacitance			10	pF
C_{CLK}	CLK Pin Capacitance			12	pF
C_{IDSEL}	IDSEL Pin Capacitance			8	pF
L_{PIN}	Pin Inductance			20	nH

Note: 1. Leakage current is with pin-keeper off.

PCI AC Characteristics (Preliminary)

Symbol	Parameter	Conditions	Min	Max	Units
$I_{OH(AC)}$	Switching Current High (Test High)	$0 < V_{OUT} \leq 1.4$	-44		mA
		$1.4 < V_{OUT} < 2.4$	-44 + (V_{OUT} - 1.4) /0.024		mA
		$3.1 < V_{OUT} < V_{CC}$		Equation A	mA
		V_{OUT} = 3.1V		-142	µA
$I_{OL(AC)}$	Switching Current Low (Test Point)	$V_{OUT} > 2.2V$	95		mA
		$2.2 > V_{OUT} > 0$	V_{OUT}/0.023		mA
		$0.1 > V_{OUT} > 0$		Equation B	mA
		V_{OUT} = 0.71		206	mA
I_{CL}	Low Clamp Current	$-5 < V_{IN} \leq -1$	-25 + (V_{IN} + 1) /0.015		mA
$SLEW_R$	Output Rise Slew Rate	0.4V to 2.4V load	1	5	V/ns
$SLEW_F$	Output Fall Slew Rate	2.4V to 0.4V load	1	5	V/ns

Notes: 1. Equation A: I_{OH} = 11.9 (V_{OUT} - 5.25) * (V_{OUT} + 2.45) for $V_{CC} > V_{OUT} > 3.1V$.
2. Equation B: I_{OL} = 78.5 * V_{OUT} * (4.4 - V_{OUT}) for $0V < V_{OUT} < 0.71V$.

Power-down Mode

The ATF1502AS includes an optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin. When the PD pin is high, the device supply current is reduced to less than 5 mA. During power-down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in a high-Z state at the onset will remain at high-Z. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down pin feature is enabled in the logic design file. Designs using the power-down pin may not use the PD pin logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

Power-down AC Characteristics(1)(2)

		-7		-10		-15		-25		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
t_{IVDH}	Valid I, I/O before PD High	7		10		15		25		ns
t_{GVDH}	Valid OE(2) before PD High	7		10		15		25		ns
t_{CVDH}	Valid Clock(2) before PD High	7		10		15		25		ns
t_{DHIX}	I, I/O Don't Care after PD High		12		15		25		35	ns
t_{DHGX}	OE(2) Don't Care after PD High		12		15		25		35	ns
t_{DHCX}	Clock(2) Don't Care after PD High		12		15		25		35	ns
t_{DLIV}	PD Low to Valid I, I/O		1		1		1		1	µs
t_{DLGV}	PD Low to Valid OE (Pin or Term)		1		1		1		1	µs
t_{DLCV}	PD Low to Valid Clock (Pin or Term)		1		1		1		1	µs
t_{DLOV}	PD Low to Valid Output		1		1		1		1	µs

Notes: 1. For slow slew outputs, add t_{SSO}.
2. Pin or product term.

Absolute Maximum Ratings*

Temperature Under Bias ..... -40°C to +85°C

Storage Temperature ..... -65°C to +150°C

Voltage on Any Pin with
Respect to Ground .....-2.0V to +7.0V(1)

Voltage on Input Pins
with Respect to Ground
During Programming.....-2.0V to +14.0V(1)

Programming Voltage with
Respect to Ground .....-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
V_{CC} (5V) Power Supply	5V ± 5%	5V ± 10%

DC Characteristics

Symbol	Parameter	Condition			Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$V_{IN} = V_{CC}$				-2	-10	µA
I_{IH}	Input or I/O High Leakage Current					2	10	
I_{OZ}	Tri-state Output Off-state Current	$V_O = V_{CC}$ or GND			-40		40	µA
I_{CC1}	Power Supply Current, Standby	V_{CC} = Max V_{IN} = 0, V_{CC}	Std Mode	Com.		60		mA
				Ind.		75		mA
			"L" Mode	Com.		10		µA
				Ind.		10		µA
I_{CC2}	Power Supply Current, Power-down Mode	V_{CC} = Max V_{IN} = 0, V_{CC}	"PD" Mode			1	5	mA
I_{CC3}[2]	Reduced-power Mode Supply Current, Standby	V_{CC} = Max V_{IN} = 0, V_{CC}	Std Mode	Com.		35		mA
				Ind.		40		mA
V_{IL}	Input Low Voltage				-0.3		0.8	V
V_{IH}	Input High Voltage				2.0		V_{CCIO} + 0.3	V
V_{OL}	Output Low Voltage (TTL)	$V_{IN} = V_{IH}$ or V_{IL} V_{CC} = MIN, I_{OL} = 12 mA		Com.	3.0		0.45	V
				Ind.			0.45	
	Output Low Voltage (CMOS)	$V_{IN} = V_{IH}$ or V_{IL} V_{CC} = MIN, I_{OL} = 0.1 mA		Com.			0.2	V
				Ind.			0.2	V
V_{OH}	Output High Voltage (TTL)	$V_{IN} = V_{IH}$ or V_{IL} V_{CC} = MIN, I_{OH} = -4.0 mA				2.4		V

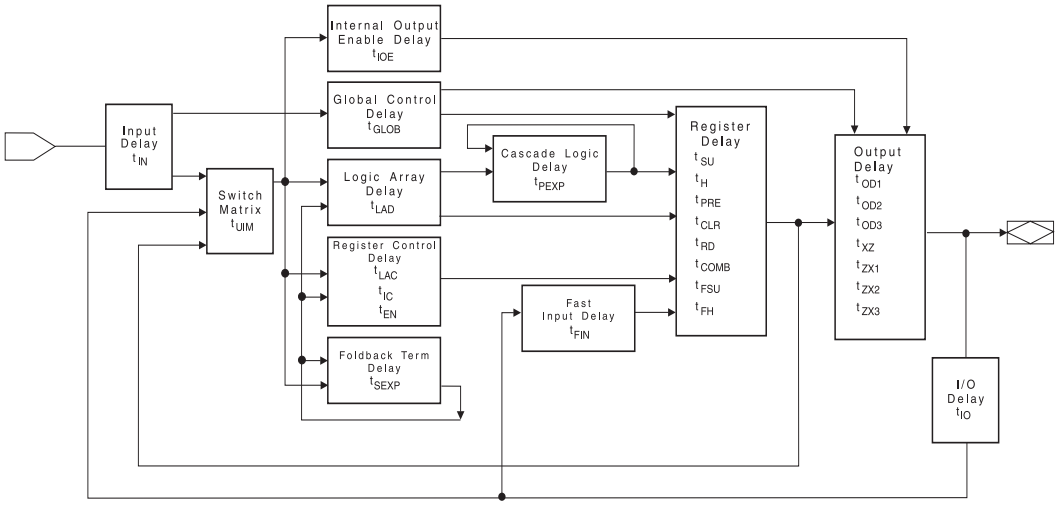
Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.
2. I_{CC3} refers to the current in the reduced-power mode when macrocell reduced-power is turned on.

Pin Capacitance[1]

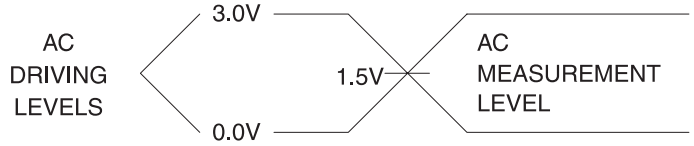
	Typ	Max	Units	Conditions
C_{IN}	8	10	pF	V_{IN} = 0V; f = 1.0 MHz
$C_{I/O}$	8	10	pF	V_{OUT} = 0V; f = 1.0 MHz

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.
The OGI pin (high-voltage pin during programming) has a maximum capacitance of 12 pF.

Timing Model

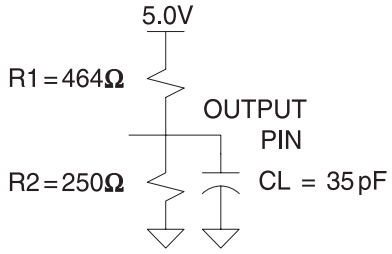


Input Test Waveforms and Measurement Levels



t_R, t_F = 1.5 ns typical

Output AC Test Loads



AC Characteristics (1)

Symbol	Parameter	-7		-10		-15		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Input or Feedback to Non-registered Output		7.5		10	3	15		25	ns
t_{PD2}	I/O Input or Feedback to Non-registered Feedback		7		9	3	12		25	ns
t_{SU}	Global Clock Setup Time	6		7		11		20		ns
t_{H}	Global Clock Hold Time	0		0		0		0		ns
t_{FSU}	Global Clock Setup Time of Fast Input	3		3		3		5		ns
t_{FH}	Global Clock Hold Time of Fast Input	0.5		0.5		1		2		MHz
t_{COP}	Global Clock to Output Delay		4.5		5		8		13	ns
t_{CH}	Global Clock High Time	3		4		5		7		ns
t_{CL}	Global Clock Low Time	3		4		5		7		ns
t_{ASU}	Array Clock Setup Time	3		3		4		5		ns
t_{AH}	Array Clock Hold Time	2		3		4		6		ns
t_{ACOP}	Array Clock Output Delay		7.5		10		15		25	ns
t_{ACH}	Array Clock High Time	3		4		6		10		ns
t_{ACL}	Array Clock Low Time	3		4		6		10		ns
t_{CNT}	Minimum Clock Global Period		8		10		13		22	ns
f_{CNT}	Maximum Internal Global Clock Frequency	125		100		76.9		50		MHz
t_{ACNT}	Minimum Array Clock Period		8		10		13		22	ns
f_{ACNT}	Maximum Internal Array Clock Frequency	125		100		76.9		50		MHz
f_{MAX}	Maximum Clock Frequency	166.7		125		100		60		MHz
t_{IN}	Input Pad and Buffer Delay		0.5		0.5		2		2	ns
t_{IO}	I/O Input Pad and Buffer Delay		0.5		0.5		2		2	ns
t_{FIN}	Fast Input Delay		1		1		2		2	ns
t_{SEXP}	Foldback Term Delay		4		5		8		12	ns
t_{PEXP}	Cascade Logic Delay		0.8		0.8		1		2	ns
t_{LAD}	Logic Array Delay		3		5		6		8	ns
t_{LAC}	Logic Control Delay		3		5		6		8	ns
t_{IOE}	Internal Output Enable Delay		2		2		3		4	ns
t_{OD1}	Output Buffer and Pad Delay (Slow slew rate = OFF; V_{CC} = 5V; C_L = 35 pF)		2		1.5		4		6	ns
t_{ZX1}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 5.0V; C_L = 35 pF)		4.0		5.0		7		10	ns
t_{ZX2}	Output Buffer Enable Delay (Slow slew rate = OFF; V_{CCIO} = 3.3V; C_L = 35 pF)		4.5		5.5		7		10	ns

AC Characteristics (Continued)[1]

Symbol	Parameter	-7		-10		-15		-25		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{ZX3}	Output Buffer Enable Delay (Slow slew rate = ON; V_{CCIO} = 5.0V/3.3V; C_L = 35 pF)		9		9		10		12	ns
t_{XZ}	Output Buffer Disable Delay (C_L = 5 pF)		4		5		6		8	ns
t_{SU}	Register Setup Time	3		3		4		6		ns
t_H	Register Hold Time	2		3		4		6		ns
t_{FSU}	Register Setup Time of Fast Input	3		3		2		3		ns
t_{FH}	Register Hold Time of Fast Input	0.5		0.5		2		5		ns
t_{RD}	Register Delay		1		2		1		2	ns
t_{COMB}	Combinatorial Delay		1		2		1		2	ns
t_{IC}	Array Clock Delay		3		5		6		8	ns
t_{EN}	Register Enable Time		3		5		6		8	ns
t_{GLOB}	Global Control Delay		1		1		1		1	ns
t_{PRE}	Register Preset Time		2		3		4		6	ns
t_{CLR}	Register Clear Time		2		3		4		6	ns
t_{UIM}	Switch Matrix Delay		1		1		2		2	ns
t_{RPA}	Reduced-power Adder[2]		10		11		13		15	ns

Notes: 1. See ordering information for valid part numbers.
2. The t_{RPA} parameter must be added to the t_{LAD}, t_{LAC},t_{TIC}, t_{ACL}, and t_{SEXP} parameters for macrocells running in the reduced-power mode.

ATF1502AS Dedicated Pinouts

Dedicated Pin	44-lead TQFP	44-lead J-lead
INPUT/OE2/GCLK2	40	2
INPUT/GCLR	39	1
INPUT/OE1	38	44
INPUT/GCLK1	37	43
I/O / GCLK3	35	41
I/O / PD (1,2)	5, 19	11, 25
I/O / TDI (JTAG)	1	7
I/O / TMS (JTAG)	7	13
I/O / TCK (JTAG)	26	32
I/O / TDO (JTAG)	32	38
GND	4, 16, 24, 36	10, 22, 30, 42
VCC	9, 17, 29, 41	3, 15, 23, 35
# of Signal Pins	36	36
# User I/O Pins	32	32

OE (1, 2)	Global OE pins
GCLR	Global Clear pin
GCLK (1, 2, 3)	Global Clock pins
PD (1, 2)	Power-down pins
TDI, TMS, TCK, TDO	JTAG pins used for boundary-scan testing or in-system programming
GND	Ground pins
VCC	VCC pins for the device (+5V)

ATF1502AS I/O Pinouts

MC	PLC	44-lead PLCC	44-lead TQFP
1	A	4	42
2	A	5	43
3	A/**PD1**	6	44
4/**TDI**	A	7	1
5	A	8	2
6	A	9	3
7	A	11	5
8	A	12	6
9/**TMS**	A	13	7
10	A	14	8
11	A	16	10
12	A	17	11
13	A	18	12
14	A	19	13
15	A	20	14
16	A	21	15
17	B	41	35
18	B	40	34
19	B	39	33
20/**TDO**	B	38	32
21	B	37	31
22	B	36	30
23	B	34	28
24	B	33	27
25/**TCK**	B	32	26
26	B	31	25
27	B	29	23
28	B	28	22
29	B	27	21
30	B	26	20
31	B	25	19
32	B	24	18

Ordering Information

Standard Package Options

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
7.5	4.5	166.7	ATF1502AS-7 AC44 ATF1502AS-7 JC44	44A 44J	Commercial (0°C to 70°C)
10	5	125	ATF1502AS-10 AC44 ATF1502AS-10 JC444	44A 44J	Commercial (0°C to 70°C)
			ATF1502AS-10 AI44 ATF1502AS-10 JI44	44A 44J	Industrial (-40°C to +85°C)
15	8	100	ATF1502AS-15 AC44 ATF1502AS-15 JC44	44A 44J	Commercial (0°C to 70°C)
			ATF1502AS-15 AI44 ATF1502AS-15 JI44	44A 44J	Industrial (-40°C to +85°C)
25	13	60	ATF1502ASL-25 AC44 ATF1502ASL-25 JC44	44A 44J	Commercial (0°C to 70°C)
			ATF1502ASL-25 AI44 ATF1502ASL-25 JI44	44A 44J	Industrial (-40°C to +85°C)

Notes: 1. The last time buy date is Sept. 30, 2005 for shaded parts.
2. In 2004, Atmel briefly offered the lead-free products ATF1502AS-7JL44 and ATF1502AS-10JJ44. They have since been discontinued effective Sept. 30,2005 and replaced with Green “U” packages.

Using “C” Product for Industrial

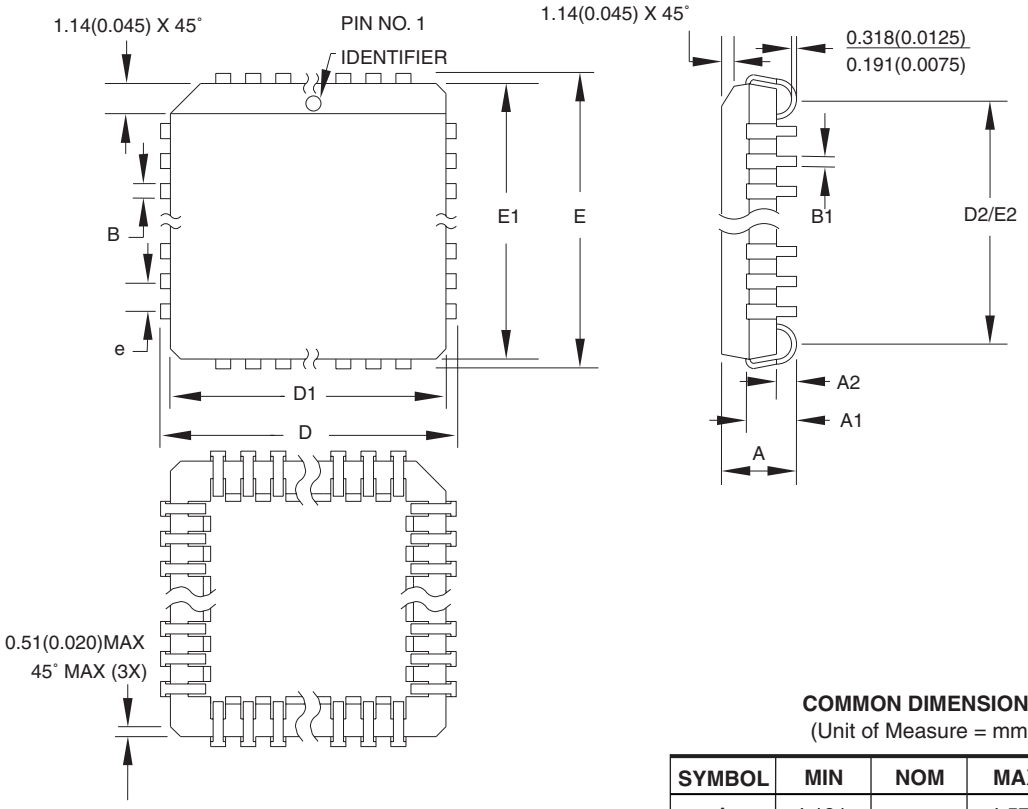
To use commercial product for industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

Green Package Options (Pb/Halide-free/RoHS Compliant)

t_{PD} (ns)	t_{CO1} (ns)	f_{MAX} (MHz)	Ordering Code	Package	Operation Range
7.5	4.5	166.7	ATF1502AS-7 AX44 ATF1502AS-7 JX44	44A 44J	Commercial (0°C to 70°C)
10	5	125	ATF1502AS-10 AU44 ATF1502AS-10 JU44	44A 44J	Industrial (-40°C to +85°C)
25	13	60	ATF1502ASL-25 AU44 ATF1502ASL-25 JU44	44A 44J	Industrial (-40°C to +85°C)

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier OTP (PLCC)

44J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	17.399	–	17.653	
D1	16.510	–	16.662	Note 2
E	17.399	–	17.653	
E1	16.510	–	16.662	Note 2
D2/E2	14.986	–	16.002	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

TITLE	DRAWING NO.
44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)	44J