Features

- **Industry-standard Architecture**
  - **Emulates Many 20-pin PALs**
  - **Low-cost Easy-to-use Software Tools**
- **High-speed Electrically-erasable Programmable Logic Devices**
  - **12 ns Maximum Pin-to-pin Delay**
- **Low-power - 5 µA (Typ) Standby Current**
- **CMOS and TTL Compatible Inputs and Outputs**
  - **Input and I/O Pin Keeper Circuits**
- **Advanced Flash Technology**
  - **Reprogrammable**
  - **100% Tested**
- **High-reliability CMOS Process**
  - **20 Year Data Retention**
  - **100 Erase/Write Cycles**
  - **2,000V ESD Protection**
  - **200 mA Latchup Immunity**
- **Commercial and Industrial Temperature Ranges**
- **Dual-in-line and Surface Mount Packages in Standard Pinouts**
- **PCI-compliant**
- **Green (Pb/Halide-free/RoHS Compliant) Package Options Available**

High-performance EE PLD

ATF16V8CZ

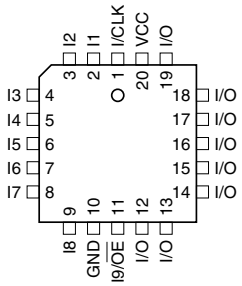
1. Description

The ATF16V8CZ is a high-performance EECMOS programmable logic device that utilizes Atmel's proven electrically-erasable Flash memory technology. Speeds down to 12 ns and a 5 µA (Typ) edge-sensing power-down mode are offered. All speed ranges are specified over the full 5V ±10% range for industrial temperature ranges; 5V ±5% for commercial range 5-volt devices.

The ATF16V8CZ incorporates a superset of the generic architectures, which allows direct replacement of the 16R8 family and most 20-pin combinatorial PLDs. Eight outputs are each allocated eight product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

The ATF16V8CZ can significantly reduce total system power, thereby enhancing system reliability and reducing power supply costs. When all the inputs and internal nodes are not switching, supply current drops to less than 5 µA typically. This automatic power-down feature (or sleep mode) allows for power savings in slow clock systems and asynchronous applications. Also, the pin-keeper circuits eliminate the need for internal pull-up resistors along with their attendant power consumption.

Figure 2-3. PLCC



3. Absolute Maximum Ratings*

Temperature Under Bias	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-2.0V to +7.0V(1)
Voltage on Input Pins with Respect to Ground During Programming	-2.0V to +14.0V(1)
Programming Voltage with Respect to Ground	-2.0V to +14.0V(1)

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is V_{CC} + 0.75V DC, which may overshoot to 7.0V for pulses of less than 20 ns.

4. DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
V_{CC} Power Supply	5V ±5%	5V ±10%

4.1 DC Characteristics

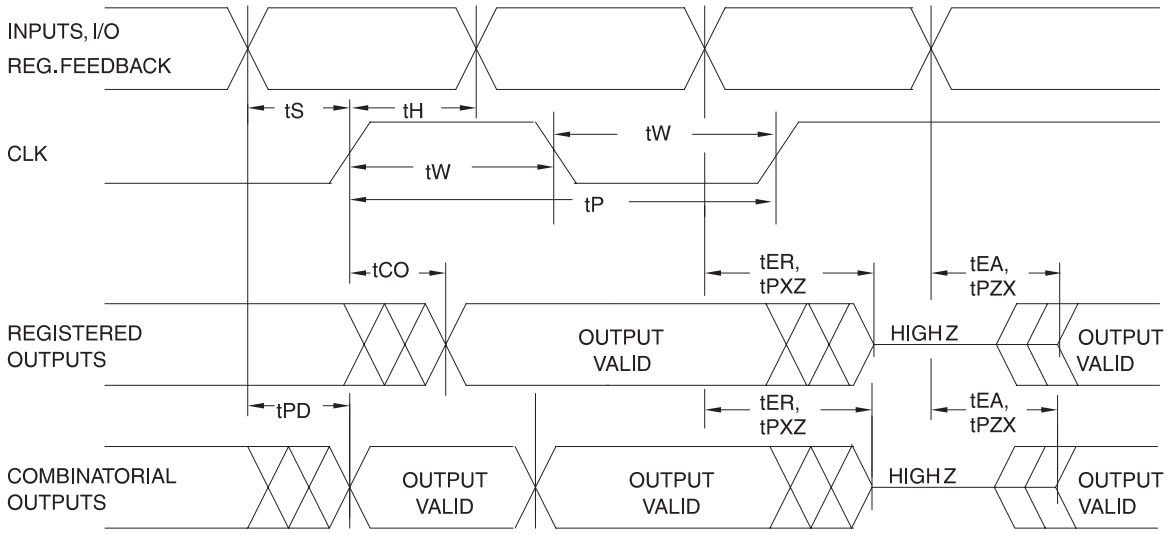
Symbol	Parameter	Condition		Min	Typ	Max	Units
I_{IL}	Input or I/O Low Leakage Current	$0 \le V_{IN} \le V_{IL}$(Max)				-10	µA
I_{IH}	Input or I/O High Leakage Current	$3.5 \le V_{IN} \le V_{CC}$				10	µA
I_{CC1}	Power Supply Current	15 MHz, V_{CC} = Max, V_{IN} = 0, V_{CC}, Outputs Open	Com			95	mA
			Ind.			105	mA
I_{CC}(1)	Power Supply Current, Standby Mode	0 MHz, V_{CC} = Max, V_{IN} = 0, V_{CC}, Outputs Open	Com.		5		µA
			Ind		5		µA
I_{OS}	Output Short Circuit Current	V_{OUT} = 0.5V; V_{CC}= 5V; TA = 25°C				-150	mA
V_{IL}	Input Low Voltage	Min < V_{CC} < Max		-0.5		0.8	V
V_{IH}	Input High Voltage			2.0		V_{CC}+1	V
V_{OL}	Output Low Voltage	V_{CC} = Min, All Outputs I_{OL} = -16 mA	Com, Ind.			0.5	V

4.1 DC Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Units
V_{OH}	Output High Voltage	V_{CC} = Min I_{OL} = -3.2 mA		2.4			V
I_{OL}	Output Low Current	V_{CC} = Min	Com.	24			mA
			Ind.	12			
I_{OH}	Output High Current	V_{CC} = Min	Com., Ind.	4			mA

Note: 1. All I_{CC} parameters measured with outputs open. Data is based on Atmel test patterns. Reading may vary with pattern.

4.2 AC Waveforms[1]



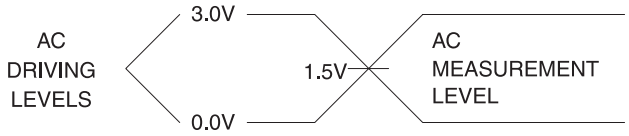
Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

4.3 AC Characteristics

Symbol	Parameter	-12		-15		Units
		Min	Max	Min	Max	
t_{PD}	Input or Feedback to Non-registered Output	3	12	3	15	ns
t_{CF}	Clock to Feedback		6		8	ns
t_{CO}	Clock to Output	2	8	2	10	ns
t_S	Input or Feedback Setup Time	10		12		ns
t_H	Input Hold Time	0		0		ns
t_P	Clock Period	12		16		ns
t_W	Clock Width	6		8		ns
f_{MAX}	External Feedback $1/(t_S + t_{CO})$		55		45	MHz
	Internal Feedback $1/(t_S + t_{CF})$		62		50	MHz
	No Feedback $1/(t_P)$		83		62	MHz
t_{EA}	Input to Output Enable – Product Term	3	12	3	15	ns
t_{ER}	Input to Output Disable – Product Term	2	15	2	15	ns
t_{PZX}	$\overline{OE}$ pin to Output Enable	2	12	2	15	ns
t_{PXZ}	$\overline{OE}$ pin to Output Disable	1.5	12	1.5	15	ns

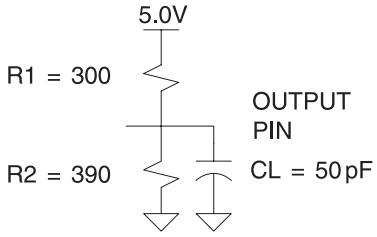
4.4 Input Test Waveforms

4.4.1 Input Test Waveforms and Measurement Levels



t_R, t_F < 1.5 ns (10% to 90%)

4.4.2 Output Test Loads



Note: Similar devices are tested with slightly different loads. These load differences may affect output signals' delay and slew rate. Atmel devices are tested with sufficient margins to meet compatible devices.

4.4.3 Pin Capacitance

Table 4-1. Pin Capacitance (f = 1 MHz, T = 25°C[1])

	Typ	Max	Units	Conditions
C_{IN}	5	8	pF	V_{IN} = 0V
C_{OUT}	6	8	pF	V_{OUT} = 0V

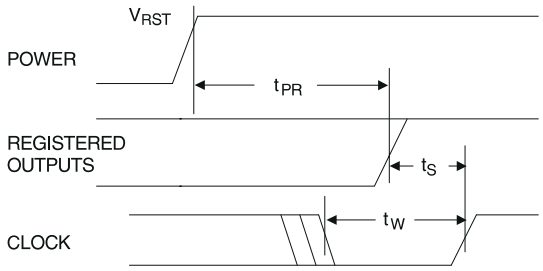
Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

4.5 Power-up Reset

The ATF16V8CZ's registers are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST}, all registers will be reset to the low state. As a result, the registered output state will always be high on power-up.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic, from below 0.7V,
2. After reset occurs, all input and feedback setup times must be met before driving the clock term high, and
3. The signals from which the clock is derived must remain stable during t_{PR}.



Parameter	Description	Typ	Max	Units
t_{PR}	Power-up Reset Time	600	1,000	ns
V_{RST}	Power-up Reset Voltage	3.8	4.5	V

4.6 Preload of Registered Outputs

The ATF16V8CZ's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by approved programmers.

5. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF16V8CZ fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

10. Ordering Information

10.1 Standard Package Options

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
12	10	8	ATF16V8CZ-12JC ATF16V8CZ-12PC ATF16V8CZ-12SC ATF16V8CZ-12XC	20J 20P3 20S 20X	Commercial (0°C to 70°C)
15	12	10	ATF16V8CZ-15JC ATF16V8CZ-15PC ATF16V8CZ-15SC ATF16V8CZ-15XC	20J 20P3 20S 20X	Commercial (0°C to 70°C)
	12	10	ATF16V8CZ-15JI ATF16V8CZ-15PI ATF16V8CZ-15SI ATF16V8CZ-15XI	20J 20P3 20S 20X	Industrial (-40°C to 85°C)

Note: Shaded parts are being obsoleted in Q3-05 and being replaced by Green parts.

10.2 Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

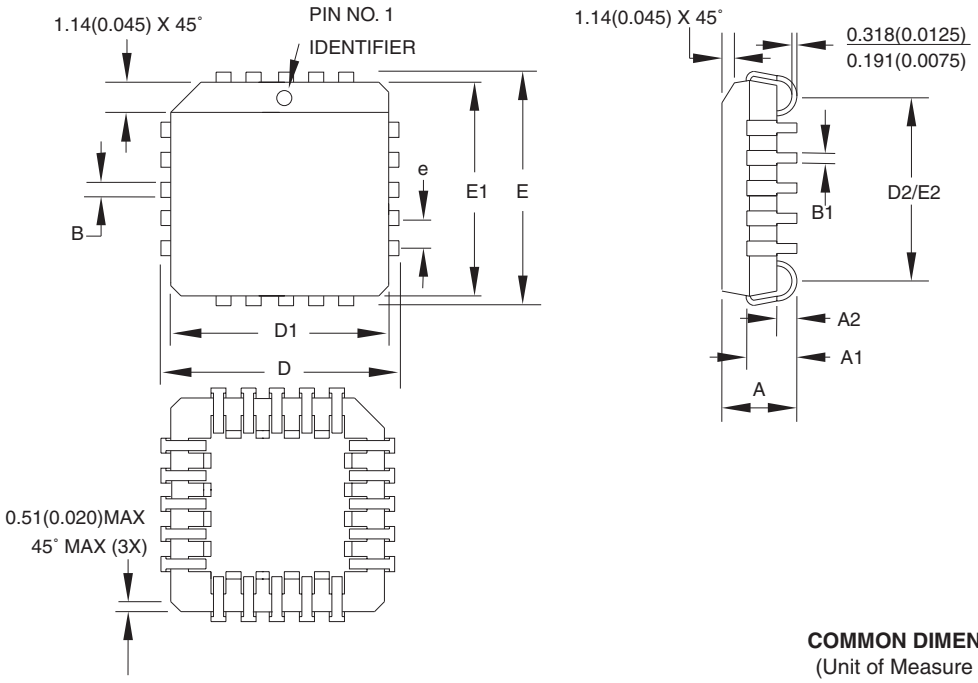
10.3 Green Package Options (Pb/Halide-free/RoHS Compliant)

t_{PD} (ns)	t_S (ns)	t_{CO} (ns)	Ordering Code	Package	Operation Range
15	12	10	ATF16V8CZ-15JU ATF16V8CZ-15PU ATF16V8CZ-15SU ATF16V8CZ-15XU	20J 20P3 20S 20X	Industrial (-40°C to 85°C)

Package Type	
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)
20P3	20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20S	20-lead, 0.300" Wide, Plastic Gull-wing Small Outline (SOIC)
20X	20-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)

11. Package Information

11.1 20J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	9.779	–	10.033	
D1	8.890	–	9.042	Note 2
E	9.779	–	10.033	
E1	8.890	–	9.042	Note 2
D2/E2	7.366	–	8.382	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

TITLE	DRAWING NO.
20J, 20-lead, Plastic J-leaded Chip Carrier (PLCC)	20J