## MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR, LOW-POWER SCHOTTKY TTL,
CASCADABLE LATCHES, MONOLITHIC SILICON
Inactive for new design after 18 April 1997.
This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE
1.1 Scope. This specification covers the detail requirements for monolithic silicon, low-power Schottky TTL, latches. Two product assurance classes and a choice of case outlines and lead finishes are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.3).
1.2 Part number. The part number should be in accordance with MIL-PRF-38535, and as specified herein.
1.2.1 Device types. The device types should be as follows:

Device type
01
02

03
04
05

## Circuit

4 - bit cascadable bistable latch
Quad cascadable $\bar{S}-\bar{R}$ latch
8 - bit cascadable addressable latch
4 - bit cascadable bistable latch
8 - bit cascadable addressable latch
1.2.2 Device class. The device class should be the product assurance level as defined in MIL-PRF-38535.
1.2.3 Case outlines. The case outlines should be as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
| :---: | :---: | :---: | :---: |
| E | GDIP1-T16 or CDIP2-T16 | 16 | Dual-in-line |
| F | GDFP2-F16 or CDFP3-F16 | 16 | Flat pack |
| X | CQCC2-N20 | 20 | Square leadless chip carrier |
| 2 | CQCC1-N20 | 20 | Square leadless chip carrier |

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43216-5000, by using the self addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

### 1.3 Absolute maximum ratings.

| Supply voltage range | -1.5 V at -18 mA to 5.5 V |
| :---: | :---: |
| Input voltage range |  |
| Storage temperature range | $-65^{\circ}$ to $+150^{\circ} \mathrm{C}$ |
| Maximum power dissipation ( $\mathrm{P}_{\mathrm{D}}$ ) 1/ |  |
| Device types 01 and 04 | 66 mW |
| Device type 02 | 38.5 mW |
| Device type 03 | 198 mW |
| Lead temperature (soldering, 10 seconds) | $300^{\circ} \mathrm{C}$ |
| Thermal resistance, junction to case ( $\theta_{\mathrm{Jc}}$ ): |  |
| Cases E, F, X, and 2 .... | (See MIL-STD-1835) |
| Junction temperature ( $\mathrm{T}_{\mathrm{J}}$ ) $\underline{2} /$. | $+175^{\circ} \mathrm{C}$ |

1.4 Recommended operating conditions.

| Supply voltage ( $\mathrm{V}_{\mathrm{CC}}$ ) | 4.5 V minimum to 5.5 V maximum |
| :---: | :---: |
| Minimum high level input voltage ( $\mathrm{V}_{\mathrm{HH}}$ ) | 2.0 V |
| Maximum low level input voltage ( $\mathrm{V}_{\mathrm{IL}}$ ) | 0.7 V |
| Normalized fanout (each output) ... | 10 maximum |
| Case operating temperature range ( $\mathrm{T}_{\mathrm{C}}$ ) | $-55^{\circ} \mathrm{C}$ to $+125^{\circ} \mathrm{C}$ |
| Setup time, $\mathrm{t}_{\text {(SETUP) }}$ : |  |
| Data to enable: |  |
| Device types 01 and 04 | 20 ns minimum |
| Data to enable $\uparrow$ : |  |
| Device type 03 | 17 ns minimum |
| Device type 05 | 24 ns minumum |
| Address to enable $\downarrow$ |  |
| Device type 03 | 15 ns minimum |
| Device type 05 | 0 ns minimum |
| Input hold time, $\mathrm{t}_{\text {(HOLD) }}$ : |  |
| Data to enable: |  |
| Device type 01 and 04 | o ns minimum |
| Data to enable $\uparrow$ : |  |
| Device type 03 | 5 ns minimum |
| Device type 05 | 0 ns minimum |
| Address to enable $\downarrow$ : |  |
| Device type 03 | 15 ns minimum |
| Device type 05 | 0 ns minimum |

NOTE: Refers to rising $\uparrow$ or falling $\downarrow$ edge of the enable pulse.

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## 2. APPLICABLE DOCUMENTS

### 2.1 Government documents.

2.1.1 Specifications and Standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Departments of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

## SPECIFICATION

DEPARTMENT OF DEFENSE
MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

## STANDARDS

DEPARTMENT OF DEFENSE

| MIL-STD-883 | - | Test Method Standard for Microelectronics. |
| :--- | :--- | :--- |
| MIL-STD-1835 | Interface Standard Electronic Component Case Outlines |  |

(Unless otherwise indicated, copies of the above specifications and standards are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)
2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.4).
3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.
3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.
3.3.1 Terminal connections. The terminal connections shall be as specified on figure 1.
3.3.2 Truth table. The truth table shall be as specified on figure 2.
3.3.3 Schematic circuits. The schematic circuits shall be_maintained by the manufacturer and made available to the qualifying activity and the preparing activity upon request.
3.3.4 Case outlines. The case outlines shall be as specified in 1.2.3.
3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).
3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.
3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.
3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.
3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 10 (see MIL-PRF-38535, appendix A).
4. VERIFICATION
4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.
4.2 Screening. Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:
a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
c. Additional screening for space level product shall be as specified in MIL-PRF-38535, appendix B.
4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.
4.4 Technology Conformance Inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).
4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:
a. Tests shall be as specified in table II herein.
b. Subgroups 4,5 , and 6 shall be omitted.

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TABLE I. Electrical performance characteristics.

| Test | Symbol | Conditions$-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{C}} \leq+125^{\circ} \mathrm{C}$ | Device type | Limits |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max |  |
| High level output voltage | $\mathrm{V}_{\mathrm{OH}}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=2.0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IL}}=0.7 \mathrm{~V}, \mathrm{I}_{\mathrm{OH}}=-400 \mu \mathrm{~A} \end{aligned}$ | All | 2.5 |  | V |
| Low level output voltage | VoL | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IH}}=2.0 \mathrm{~V} \\ & \mathrm{~V}_{\mathrm{IL}}=0.7 \mathrm{~V}, \mathrm{l}_{\mathrm{LL}}=4 \mathrm{~mA} \end{aligned}$ | All |  | 0.4 | V |
| Input clamp voltage | VIC | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=4.5 \mathrm{~V}, \mathrm{I}_{\mathrm{IN}}=-18 \mathrm{~mA}, \\ & \mathrm{~T}_{\mathrm{C}}=+25^{\circ} \mathrm{C} \end{aligned}$ | All |  | -1.5 | V |
| Low level input current:$\qquad$ At data | $\mathrm{I}_{\text {L1 }}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=0.4 \mathrm{~V}$ | 01 | -. 03 | -0.42 | mA |
|  |  |  | 04 | -. 0005 | -0.4 |  |
|  |  |  | 02 | 0 | -0.4 |  |
| At all inputs |  |  | 03, 05 | -. 005 | -0.72 |  |
| Low level input current enable | IIL2 | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=0.4 \mathrm{~V}$ | 01 | -. 06 | -1.6 | mA |
|  |  |  | 04 | 0 | -1.6 |  |
| High level input current: <br> At data | $\mathrm{I}_{\mathrm{H} 1}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=2.7 \mathrm{~V}$ | 01, 04 |  | 20 | $\mu \mathrm{A}$ |
| At $\bar{S}, \bar{R}$ |  |  | 02 |  | 20 |  |
| At all inputs |  |  | 03, 05 |  | 20 |  |
| High level input current enable | $\mathrm{I}_{1+2}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=2.7 \mathrm{~V}$ | 01, 04 |  | 80 | $\mu \mathrm{A}$ |
| High level input current: <br> At data | $1_{1+3}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=5.5 \mathrm{~V}$ | 01, 04 |  | 100 | $\mu \mathrm{A}$ |
| At $\bar{S}, \bar{R}$ |  |  | 02 |  | 100 |  |
| At all inputs |  |  | 03, 05 |  | 100 |  |
| High level input current enable | $\mathrm{I}_{1+4}$ | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{IN}}=5.5 \mathrm{~V}$ | 01, 04 |  | 400 | $\mu \mathrm{A}$ |
| Short circuit output current | los | $\mathrm{V}_{\mathrm{CC}}=5.5 \mathrm{~V} \quad 1 /$ | All | -15 | -100 | mA |
| Supply current | Icc | $\mathrm{V}_{C C}=5.5 \mathrm{~V}$ | 01, 04 |  | 12 | mA |
|  |  |  | 02 |  | 7 |  |
|  |  |  | 03, 05 |  | 36 |  |
| Low to high level, from D input to Q output | tplh1 | $\begin{aligned} & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \pm 10 \%, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \pm 5 \% \\ & \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V} \end{aligned}$ | 01, 04 | 3 | 42 | ns |
| High to low level, from D input to Q output | $\mathrm{t}_{\text {PHL1 }}$ |  | 01, 04 | 3 | 29 | ns |
| Low to high level, from D input to $\bar{Q}$ output | tpLH2 |  | 01, 04 | 3 | 32 | ns |
| High to low level, from D input to $\bar{Q}$ output | $\mathrm{t}_{\text {PHL2 }}$ |  | 01, 04 | 3 | 26 | ns |
| Low to high level, from enable input to Q output | tpLH3 |  | 01, 04 | 3 | 42 | ns |
| High to low level, from enable input to Q output | tpHL3 |  | 01, 04 | 3 | 39 | ns |

1/ Not more than one output should be shorted at one time.

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TABLE I. Electrical performance characteristics - Continued.

| Test | Symbol | Conditions$-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{C}} \leq+125^{\circ} \mathrm{C}$ | Device type | Limits |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max |  |
| Low to high level, from enable input to Q output | tpLH4 | $\begin{aligned} & \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \pm 10 \%, \mathrm{R}_{\mathrm{L}}=2 \mathrm{k} \Omega \pm 5 \% \\ & \mathrm{~V}_{\mathrm{CC}}=5.0 \mathrm{~V} \end{aligned}$ | 01, 04 | 3 | 46 | ns |
| High to low level, from enable input to Q output | tpHL4 |  | 01, 04 | 3 | 26 | ns |
| Low to high level, from $\overline{\mathrm{S}}$ input to Q output | $\mathrm{t}_{\text {PLH1 }}$ |  | 02 | 3 | 35 | ns |
| High to low level, from $\bar{S}$ input to $Q$ output | $\mathrm{t}_{\text {PL } 1}$ |  | 02 | 3 | 26 | ns |
| High to low level, from $\bar{R}$ input to $Q$ output | tpHL2 |  | 02 | 3 | 42 | ns |
| High to low level, from clear input to Q output | tPHL1 |  | 03 | 3 | 42 | ns |
|  |  |  | 05 | 3 | 30 |  |
| Low to high level, from data input to Q output | tpLH2 |  | 03 | 3 | 48 | ns |
|  |  |  | 05 | 3 | 46 |  |
| High to low level, from data input to Q output | tpHL2 |  | 03 | 3 | 34 | ns |
|  |  |  | 05 | 3 | 33 |  |
| Low to high level, from address input to Q output | $\mathrm{t}_{\text {PLH3 }}$ |  | 03 | 3 | 56 | ns |
|  |  |  | 05 | 3 | 42 |  |
| High to low level, from address input to Q output | $\mathrm{t}_{\text {PHL3 }}$ |  | 03 | 3 | 44 | ns |
|  |  |  | 05 | 3 | 42 |  |
| Low to high level, from enable input to Q output | tpLH4 |  | 03 | 3 | 52 | ns |
|  |  |  | 05 | 3 | 38 |  |
| High to low level, from enable input to Q output | $\mathrm{t}_{\text {PHL4 }}$ |  | 03, 05 | 3 | 38 | ns |

TABLE II. Electrical test requirements.

| MIL-PRF-38535 <br> test requirements | Subgroups (see table III) |  |
| :--- | :--- | :--- |
|  | Class S <br> devices | Class B <br> devices |
| Interim electrical parameters | 1 | 1 |
| Final electrical test parameters | $1^{*}, 2,3,7,9$, | $1^{*}, 2,3,7,9$ |
|  | 10,11 |  |
| Group A test requirements | $1,2,3,7,8$, | $1,2,3,7,8$, |
|  | $9,10,11$ | $9,10,11$ |
| Group B electrical test parameters | $1,2,3,9$, | $\mathrm{N} / \mathrm{A}$ |
| when using method 5005 QCI option | 10,11 |  |
| Group C end-point electrical parameters | $1,2,3,9$, | $1,2,3$ |
|  | 10,11 |  |
| Group D end-point electrical parameters | $1,2,3$ | $1,2,3$ |

*PDA applies to subgroup 1.
4.4.2 Group B inspection. Group B inspection shall be in accordance with table II MIL-PRF-38535.
4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:
a. End-point electrical parameters shall be as specified in table II herein.
b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.
4.5 Methods of inspection. Methods of inspection shall be specified and as follows:
4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

| Pin number | Pin symbol Device type 01 |  | Pin symbol Device type 02 |  | Pin symbol Device type 03 |  | Pin symbol Device type 04 |  | Pin symbol Device type 05 |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | $\begin{gathered} \text { Case } \\ 2, X \end{gathered}$ | $\begin{gathered} \text { Case } \\ E, F \end{gathered}$ | $\begin{gathered} \text { Case } \\ 2, \mathrm{X} \\ \hline \end{gathered}$ | $\begin{aligned} & \text { Case } \\ & \text { E, F } \end{aligned}$ | $\begin{aligned} & \text { Case } \\ & 2, X \\ & \hline \end{aligned}$ | $\begin{gathered} \text { Case } \\ \mathrm{E}, \mathrm{~F} \end{gathered}$ | $\begin{aligned} & \text { Case } \\ & 2, \mathrm{X} \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { Case } \\ & \text { E, F } \end{aligned}$ | $\begin{aligned} & \text { Case } \\ & 2, X \\ & \hline \end{aligned}$ | $\begin{aligned} & \text { Case } \\ & \text { E, F } \end{aligned}$ |
| 1 | NC | $1 \overline{\mathrm{Q}}$ | NC | 1 $\bar{R}$ | NC | A | NC | 1D | NC | A |
| 2 | $1 \overline{\mathrm{Q}}$ | 1D | $1 \overline{\mathrm{R}}$ | $1 \overline{\mathrm{~S}} 1$ | A | B | 1D | $1 \bar{Q}$ | A | B |
| 3 | 1D | 2D | $1 \overline{\mathrm{~S}} 1$ | $1 \bar{S}^{2}$ | B | C | $1 \overline{\mathrm{Q}}$ | 1Q | B | C |
| 4 | 2D | ENBL 3-4 | $1 \bar{S} 2$ | 1Q | C | Q0 | 1Q | ENBL 1-2 | C | Q0 |
| 5 | ENBL 3-4 | $\mathrm{V}_{\mathrm{cc}}$ | 1 Q | $2 \overline{\mathrm{R}}$ | Q0 | Q1 | ENBL 1-2 | 2Q | Q0 | Q1 |
| 6 | NC | 3D | NC | $2 \bar{S}$ | NC | Q2 | NC | $2 \bar{Q}$ | NC | Q2 |
| 7 | $\mathrm{V}_{\mathrm{cc}}$ | 4D | $2 \bar{R}$ | 2Q | Q1 | Q3 | 2Q | 2D | Q1 | Q3 |
| 8 | 3D | $4 \overline{\mathrm{Q}}$ | $2 \bar{S}$ | GND | Q2 | GND | $2 \bar{Q}$ | GND | Q2 | GND |
| 9 | 4D | 4Q | 2Q | 3Q | Q3 | Q4 | 2D | 3D | Q3 | Q4 |
| 10 | $4 \overline{\mathrm{Q}}$ | 3Q | GND | $3 \overline{\mathrm{R}}$ | GND | Q5 | GND | $3 \overline{\mathrm{Q}}$ | GND | Q5 |
| 11 | NC | $3 \bar{Q}$ | NC | $3 \bar{S} 1$ | NC | Q6 | NC | 3Q | NC | Q6 |
| 12 | 4Q | GND | 3Q | $3 \bar{S} 2$ | Q4 | Q7 | 3D | ENBL 3-4 | Q4 | Q7 |
| 13 | 3Q | ENBL 1-2 | $3 \overline{\mathrm{R}}$ | 4Q | Q5 | DATA IN | $3 \bar{Q}$ | 4Q | Q5 | DATA IN |
| 14 | $3 \bar{Q}$ | $2 \bar{Q}$ | $3 \bar{S} 1$ | $4 \overline{\mathrm{R}}$ | Q6 | ENBL | 3Q | $4 \overline{\mathrm{Q}}$ | Q6 | ENBL |
| 15 | GND | 2Q | $3 \bar{S} 2$ | $4 \bar{S}$ | Q7 | $\overline{\text { CLR }}$ | ENBL 3-4 | 4D | Q7 | $\overline{\text { CLR }}$ |
| 16 | NC | 1Q | NC | $\mathrm{V}_{\mathrm{cc}}$ | NC | $\mathrm{V}_{\mathrm{CC}}$ | NC | $\mathrm{V}_{\text {c }}$ | NC | $\mathrm{V}_{\text {c }}$ |
| 17 | ENBL 1-2 |  | 4Q |  | DATA IN |  | 4Q |  | DATA IN |  |
| 18 | $2 \bar{Q}$ |  | $4 \overline{\mathrm{R}}$ |  | ENBL |  | $4 \overline{\mathrm{Q}}$ |  | ENBL |  |
| 19 | 2Q |  | $4 \bar{S}$ |  | $\overline{\mathrm{CLR}}$ |  | 4D |  | $\overline{\mathrm{CLR}}$ |  |
| 20 | 1Q |  | $\mathrm{V}_{\mathrm{cc}}$ |  | $\mathrm{V}_{\text {c }}$ |  | $\mathrm{V}_{\text {cc }}$ |  | $\mathrm{V}_{c \mathrm{c}}$ |  |

FIGURE 1. Terminal connections.

Device type 01 and 04

| Inputs |  | Outputs |  |
| :---: | :---: | :---: | :---: |
| D | Enable | Q | $\overline{\mathrm{Q}}$ |
| L | H | L | H |
| H | H | H | L |
| X | L | Q 0 | $\overline{\mathrm{Q}} 0$ |

$H=$ high level, $L=$ low level, $X=$ irrelevant
$Q 0=$ the level of $Q$ before the high-to-low transition of enable

## Device type 02

| Inputs |  | Outputs |
| :---: | :---: | :---: |
| $\overline{\mathrm{S}} \dagger$ | $\overline{\mathrm{R}}$ | Q |
| H | H | Q 0 |
| L | H | H |
| H | L | L |
| L | L | $\mathrm{H}^{*}$ |

$H=$ high level, $L=$ low level, $Q 0=$ the level of $Q$ before the indicated input conditions were established.

* This output level is pseudo stable; that is, it may not persist when the $\overline{\mathrm{S}}$ and $\overline{\mathrm{R}}$ inputs return to their inactive (high) level.
$\dagger$ For latches with double $\bar{S}$ inputs:
$\mathrm{H}=$ both $\overline{\mathrm{S}}$ inputs high
$\mathrm{L}=$ one or both $\overline{\mathrm{S}}$ inputs low

FIGURE 2. Truth tables.

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Device type 03 and 05

| Inputs |  | Output of <br> addressed <br> latch | Each <br> other <br> output | Function |
| :---: | :---: | :---: | :---: | :--- |
| Clear | Enable | D | Qio | Addressable latch |
| H | L | D | Qio | Memory |
| H | H | Qio | L | 8-line demultiplexer |
| L | L | D | L | L |
| L | H | L | Clear |  |

Latch Selection Table

| Select inputs |  |  | Latch |
| :---: | :---: | :---: | :---: |
| C | B | A |  |
| L | L | L | 0 |
| L | L | H | 1 |
| L | H | L | 2 |
| L | H | H | 3 |
| H | L | L | 4 |
| $H$ | L | H | 5 |
| H | H | L | 6 |
| $H$ | $H$ | $H$ | 7 |

$H=$ high level, $L=$ low level
$Q=$ the level at the data input
Qio = the level of $\mathrm{Qi}(\mathrm{i}=0,1, \ldots, 7$, as appropriate) before the indicated steady-state input conditions were established.

FIGURE 2. Truth tables - Continued.


FIGURE 3. Switching test circuit and waveforms for device types 01 and 04.


## NOTES:

1. The $D$ input pulse generator has the following characteristics: $\mathrm{V}_{\mathrm{GEN}}=3 \mathrm{~V}, \mathrm{t}_{0} \leq 15 \mathrm{~ns}, \mathrm{t}_{1} \leq 6 \mathrm{~ns}, \mathrm{t}_{\mathrm{P}}=30 \mathrm{~ns}$, and $Z_{\text {Out }}=50 \Omega$ except when measuring $V_{\text {SETUP }}$.
2. The enable pulse generator is identical to the $D$ input pulse generator.
3. $C_{L}=50 \mathrm{pF} \pm 10 \%$ and includes probe and jig capacitance.
4. $R_{L}=2 \mathrm{k} \Omega \pm 5$ percent.
5. All diodes are 1N3064 or equivalent.
6. $\mathrm{V}_{\text {SETUP }}$ is to be measured 500 ns minimum after input transitions to assure that the device has latched with minimum setup and maximum hold conditions applied to inputs.

FIGURE 3. Switching test circuit and waveforms for device types 01 and 04 - Continued.

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NOTES:

1. $\bar{R}$ and $\bar{S}$ pulse generator has the following characteristics: $t_{P}=40 \pm 10 \mathrm{~ns}, \mathrm{t}_{0} \leq 15 \mathrm{~ns}, \mathrm{t}_{1} \leq 6 \mathrm{~ns}$, and $P R R \leq 1.0 \mathrm{MHz}$.
2. $\mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \pm 10 \%$ and includes probe and jig capacitance.
3. $R_{L}=2 \mathrm{k} \Omega \pm 5$ percent.
4. All diodes are 1 N3064 or equivalent.

FIGURE 4. Switching test circuit and waveforms for device type 02.


NOTE: For Q0 output waveform is inverted and tpLH3 and $t_{P H L 3}$ are interchanged.
FIGURE 5. Switching test circuit and waveforms for device types 03 and 05


## NOTES:

1. $R_{L}=2 \mathrm{k} \Omega \pm 5$ percent.
2. $C_{L}=50 \mathrm{pF} \pm 10 \%$ and includes probe and jig capacitance.
3. All loads are the same as the $Q_{0}$ load.
4. All diodes are 1N3064 or equivalent.
5. The clear, enable, data, and address pulse generator have the following characteristics: $\mathrm{V}_{\mathrm{GEN}}=3 \mathrm{~V}, \mathrm{t}_{0} \leq 15 \mathrm{~ns}$, $\mathrm{t}_{1} \leq 6 \mathrm{~ns}, \mathrm{t}_{\mathrm{P}}=30 \mathrm{~ns}$, and PRR $\leq 1 \mathrm{MHz}$ except when measuring test nos. 152 thru $193, \mathrm{t}_{\text {P(ENABLE })}=17 \mathrm{~ns}$, $t_{P(D A T A)}=22 \mathrm{~ns}, \mathrm{t}_{\text {P(ADDRESS })}=47 \mathrm{~ns}$, and $\mathrm{t}_{\text {setup }}$ and $\mathrm{t}_{\text {hold }}$ are as specified on the waveforms above.
6. Immediately prior to test 152 , all outputs shall be cleared low; then beginning with test 152, test 152 thru 193 are to be performed in sequence with a wait of 500 ns minimum between each test. These tests are to assure latchup of the outputs under worst case setup and hold input conditions.

FIGURE 6. Switching test circuit and waveforms for device type 03-Continued.


## NOTES:

1. $R_{L}=2 \mathrm{k} \Omega \pm 5$ percent.
2. $C_{L}=50 \mathrm{pF} \pm 10 \%$ and includes probe and jig capacitance.
3. All loads are the same as the $Q_{0}$ load.
4. All diodes are 1N3064 or equivalent.
5. The clear, enable, data, and address pulse generator have the following characteristics: $\mathrm{V}_{\mathrm{GEN}}=3 \mathrm{~V}, \mathrm{t}_{0} \leq 15 \mathrm{~ns}$, $\mathrm{t}_{1} \leq 6 \mathrm{~ns}, \mathrm{t}_{\mathrm{p}}=30 \mathrm{~ns}$, and PRR $\leq 1 \mathrm{MHz}$ except when measuring test nos. 152 thru $193, \mathrm{t}_{\text {(ENABLE })}=24 \mathrm{~ns}$, $t_{P(D A T A)}=24 \mathrm{~ns}, \mathrm{t}_{\text {P(ADDRESS }}=24 \mathrm{~ns}$, and $\mathrm{t}_{\text {setup }}$ and $\mathrm{t}_{\text {hold }}$ are as specified on the waveforms above.
6. Immediately prior to test 152, all outputs shall be cleared low; then beginning with test 152, test 152 thru 193 are to be performed in sequence with a wait of 500 ns minimum between each test. These tests are to assure latchup of the outputs under worst case setup and hold input conditions.

FIGURE 5. Switching test circuit and waveforms for device type 05 - Continued.
See footnotes at end of device type 01 and 04
TABLE III. Group A inspection for device type 01 and 04 - Continued.

See footnotes at end of device types 01 and 04 .
TABLE III. Group A inspection for device type 01 and 04 - Continued.


| Test | Min/max limits (mA) |  |  |  |  |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  | Circuit A, B | Circuit C | Circuit D |  |  |
|  |  |  | Device 01 | Device 04 |  |
| $\mathrm{I}_{\text {IL1 }}$ | $-.16 /-.40$ | $-.0005 /-.40$ | $-.03 /-.40$ | $-.16 /-.40$ | $-.19 /-.42$ |
| $\mathrm{I}_{\text {IL2 }}$ | $-.64 /-1.60$ | $0 /-1.20$ | $-.12 /-1.20$ | $-.64 /-1.60$ | $-.75 /-1.60$ |

TABLE III. Group A inspection for device type 02.

TABLE III. Group A inspection for device type 02.


TABLE III. Group A inspection for device type 03.

TABLE III. Group A inspection for device type 03.

TABLE III. Group A inspection for device type 03.

See footnotes at end of device type 05
TABLE III. Group A inspection for device type 03.

TABLE III. Group A inspection for device type 03.

See footnotes at end of device type 05.
TABLE III. Group A inspection for device type 05.

TABLE III. Group A inspection for device type 05 .

See footnotes at end of device type 05.
TABLE III. Group A inspection for device type 05.

TABLE III. Group A inspection for device type 05 .

TABLE III. Group A inspection for device type 05.

| Terminal conditions (pins not designated may be high $\geq 2.0 \mathrm{~V}$; low $\leq 0.7 \mathrm{~V}$; or open). |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Subgroup | Symbol | $\begin{aligned} & \text { MIL-STD- } \\ & 883 \\ & \text { method } \end{aligned}$ | Cases E, F | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |  |  |  |  |
|  |  |  | $\begin{gathered} \text { Cases } \\ 2, X \end{gathered}$ | 2 | 3 | 4 | 5 | 7 | 8 | 9 | 10 | 12 | 13 | 14 | 15 | 17 | 18 | 19 | 20 | Measured terminal |  |  | Unit |
|  |  |  | Test no. | A | B | C | Q0 | Q1 | Q2 | Q3 | GND | Q4 | Q5 | Q6 | Q7 | $\begin{aligned} & \text { DATA } \\ & \text { IN } \end{aligned}$ | ENBL | $\overline{C L R}$ | $\mathrm{V}_{\mathrm{cc}}$ |  | Min | Max |  |
| $\begin{array}{c\|} \hline 9 \\ T_{\mathrm{C}}=25^{\circ} \mathrm{C} \end{array}$ | $\mathrm{t}_{\text {PHL4 }}$ | $\begin{aligned} & 3003 \\ & \text { Fig } 5 \end{aligned}$ | 179 | GND | IN | GND |  |  | OUT |  | GND |  |  |  |  | GND | IN | 4.5 V | 5.0 V | $\overline{\text { ENBL }}$ to Q2 | 3 | 29 | ns |
|  |  |  | 180 | " | " | " |  |  | " |  | " |  |  |  |  | 4.5 V | " | " | " | $\overline{\text { ENBL }}$ to Q2 | " | " | " |
|  | PHL4 |  | 181 | " | " | " |  |  | " |  | " |  |  |  |  | GND | " | " | " | ENBL to Q2 | " | " | " |
|  | PHL4 PLH4 |  | 182 | " | GND | IN |  |  |  |  | " | OUT |  |  |  | GND | " | " | " | ENBL to Q4 | " | " | " |
|  |  |  | 183 | " | " | " |  |  |  |  | " | " |  |  |  | 4.5 V | " | " | " | ENBL to Q4 | " | " | " |
|  | PHL4 |  | 184 | " | " | " |  |  |  |  | " | " |  |  |  | GND | " | " | " | ENBL to Q4 | " | " | " |
|  | PHL4 |  | 185 | IN | " | GND | OUT |  |  |  | " |  |  |  |  | GND | " | " | " | ENBL to Q0 | " | " | " |
|  | PLH4 PHL4 |  | 186 | " | " | ${ }^{\prime}$ | " |  |  |  | " |  |  |  |  | 4.5 V | " | " | " | ENBL to Q0 | " | " | " |
|  |  |  | 187 | " | " | " | " |  |  |  | " |  |  |  |  | GND | " | " | " | ENBL to Q0 | " | " | " |
|  | PHL4 |  | 188 | 4.5 V | IN | 4.5 V |  |  |  |  | " |  | OUT |  |  | GND | " | " | " | ENBL to Q5 | " | " | " |
|  | PLH4 |  | 189 | " | " | " |  |  |  |  | " |  | " |  |  | 4.5 V | " | " | " | ENBL to Q5 | " | " | " |
|  | PHL4 |  | 190 | " | " | " |  |  |  |  | " |  | " |  |  | GND | " | " | " | ENBL to Q5 | " | " | " |
|  | PHL4 |  | 191 | " | 4.5 V | IN |  |  |  | OUT | " |  |  |  |  | GND | " | " | " | ENBL to Q3 | " | " | " |
|  | PLH4PHL4 |  | 192 | " | " | " |  |  |  | " | " |  |  |  |  | 4.5 V | " | " | " | $\overline{\text { ENBL }}$ to Q3 | " | " | " |
|  |  |  | 193 | " | " | " |  |  |  | " | " |  |  |  |  | GND | " | " | " | ENBL to Q3 | " | " | " |
| $\begin{array}{c\|} \hline 10 \\ T_{\mathrm{C}}=125^{\circ} \mathrm{C} \\ \hline \end{array}$ | $\mathrm{t}_{\text {PHL1 }}$ | Same tests and terminal conditions as for subgroup 9, except $\mathrm{T}_{\mathrm{C}}=+125^{\circ} \mathrm{C}$ and test limits as shown |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | " | 30 | " |
|  | tpLH2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | " | 46 | " |
|  | PHL2 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | " | 33 | " |
|  | PLH3 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | " | 42 | " |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | " | 42 | " |
|  | ${ }_{P}^{\text {PLH4 }}$ |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | " | 38 | " |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | " | 38 | " |
| 11 | Same tests, terminal conditions and limits as for subgroup 10, except $\mathrm{T}_{\mathrm{C}}=-55^{\circ} \mathrm{C}$. |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

1/ Apply a $3 \mathrm{~V} / 0 \mathrm{~V} / 3 \mathrm{~V}$ momentary pulse 500 ns minimum prior to measurements.
2/ $\mathrm{A}=2.4 \mathrm{~V}, \mathrm{~B}=0.4 \mathrm{~V}$.
4/ IIL limits are as follows:

| Symbol | Min/max limits (mA) |  |  |  |
| :---: | :---: | :---: | :---: | :---: |
|  | $\begin{array}{c}\text { Circuit B, C } \\ \text { Device 03 }\end{array}$ | $\begin{array}{c}\text { Circuit A } \\ \text { Device 05 }\end{array}$ |  |  |
|  | $-.12 /-.36$ |  | $-.16 /-.40$ |  |

5/ See note 6 of figure 5 .
6/ Apply $\quad 4.5 \mathrm{~V} \square \quad 4.5 \mathrm{v}$ momentary pulse prior to each test.

## 5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department of Defense Agency, or within the Military Department's System Command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.
6. NOTES
(This section contains information of a general or explanatory nature which may be helpful, but is not mandatory.)
6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.
6.2 Acquisition requirements. Acquisition documents should specify the following:
a. Title, number, and date of the specification.
b. Complete part number (see 1.2).
c. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
d. Requirements for certificate of compliance, if applicable.
e. Requirements for notification of change of product or process to contracting activity in addition to notification to the qualifying activity, if applicable.
f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
g. Requirements for product assurance options.
h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements should not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
j. Requirements for "JAN" marking.
6.3 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.
6.4 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

## MIL-M-38510/316E

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and as follows:

| GND | Ground zero voltage pote |
| :---: | :---: |
|  | Current flowing into an input terminal. |
| $\mathrm{V}_{\text {IN }}$ | Voltage level at an input terminal. |
| $V_{\text {SUH }}$ | Setup high |
| $V_{\text {SUL }}$ | Setup low |

6.6 Logistic support. Lead materials and finishes (see 3.4) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.
6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

| Military device <br> type | Generic-industry <br> type |
| :---: | :---: |
| 01 | 54 LS 75 |
| 02 | 54 LS 279 |
| 03 | 54 LS 259 |
| 04 | 54 LS 375 |
| 05 | 54 LS 259 B |

6.8 Manufacturers' designation. Manufacturers' circuits, which form a part of this specification, are designated with an "X" as shown in table IV herein.

TABLE IV. Manufacturer's designator.

|  | CIRCUITS |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | A | B | C | D | E |
| Device <br> type | Texas <br> Instruments | Motorola <br> Inc. | Fairchild Co. | Signetics <br> Corp. | National <br> Semconductor |
| 01 | X | X |  | X | X |
| 02 | X | X | X | X | X |
| 03 | X | X | X |  | X |
| 04 | X | X | X | X |  |
| 05 | X |  |  |  |  |

6.9 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

| Custodians: | Preparing activity: |
| :--- | :---: |
| Army - CR | DLA - CC |
| Navy - EC |  |
| Air Force - 11 | (Project 5962-1965) |
| DLA - CC |  |

Review activities:
Army - MI, SM
Navy - AS, CG, MC, SH, TD
Air Force-03, 19, 99

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MICROCIRCUITS, DIGITAL, BIPOLAR, LOW-POWER SCHOTTKY TTL, CASCADABLE LATCHES, MONOLITHIC SILICON
4. NATURE OF CHANGE (Identify paragraph number and include proposed rewrite, if possible. Attach extra sheets as needed.)
5. REASON FOR RECOMMENDATION

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| c. ADDRESS (Include Zip Code) DSCC-VA <br> P. O. Box 3990 <br> Columbus, Ohio 43216-5000 | IF YOU DO NOT RECEIVE A REPLY WITHIN 45 DAYS, CONTACT: <br> Defense Standardization Program Office (DLSC-LM) <br> 8725 John J. Kingman Road, Suite 2533 <br> Fort Belvoir, Virginia 22060-6221 <br> Telephone (703)767-6888 DSN 427-6888 |


[^0]:    1/ Must withstand the added $P_{D}$ due to short-circuit test (e.g., los).
    2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with MIL-PRF-38535.

