DC-15 GHz Programmable Integer-N Prescaler

Features

- Wide Operating Range:
  - DC-20 GHz for Div-by-2/4/8
  - DC-15 GHz for Div-by-4/5/6/7/8/9
- Low SSB Phase Noise: -153 dBc @ 10 kHz
- Large Output Swings: >1 Vppk/side
- Single-Ended and/or Differential Operation
- Low power consumption: 0.6 W
- 4x4 QFN package
- Parallel Control Lines

Description

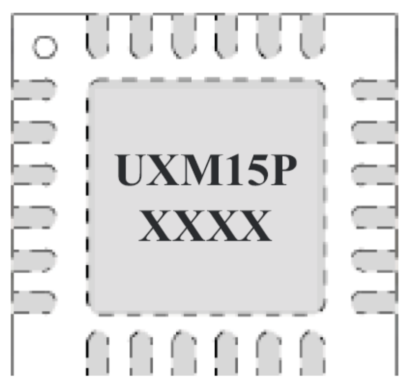
The UXM15P is a low noise programmable divider featuring a binary divide-by-2/4/8 mode and multi-modulus divide-by-4/5/6/7/8/9 mode. The device features differential inputs and outputs, adjustable output swing and high input sensitivity. The control inputs are CMOS and LVTTL compatible. The UXM15P is packaged in a 24 pin, 4x4 mm leadless surface mount package.

Application

The UXM15P can be used as a general purpose, fixed modulus prescaler in high frequency PLLs. The multi-modulus mode of the device allows it to be used in phase locked loops such as integer-N and fractional-N architectures. The low phase noise of the divider makes it ideal for generating low jitter, synchronous clocks in telecom applications.

Pad Metallization

The QFN package pad metallization consists of a Ni/Pd/Au plating over a Cu(c194) leadframe.



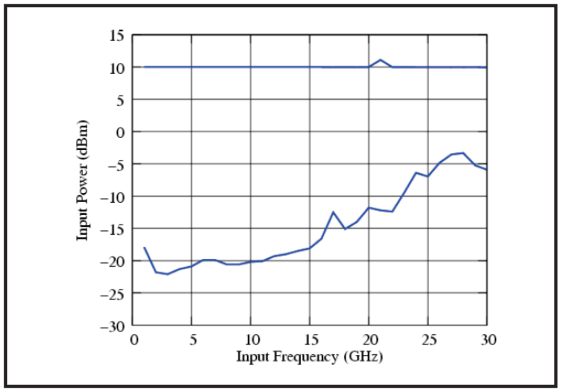
Key Specifications (T = 25˚C):
Vee = -3.3 V, Iee = 185 mA, Zo=50 Ω

Parameter	Description	Min	Typ	Max
F1in (GHz)	Input Frequency (Div-by-2/4/8)	DC*	-	20
F2in (GHz)	Input Frequency (Div-by-4/5/6/7/8/9)	DC*	-	15
Pin (dBm)	Nominal Input Power	-10	0	10
Pout (dBm)	Nominal Output Power	-5	3	-
£ (dBc/Hz)	SSB Phase Noise @10 kHz Offset	-	-153	-
PDC (mW)	DC Power Dissipation	-	610	-
θjc (ºC/W)	Junction-Case Thermal Resistance	-	20	-

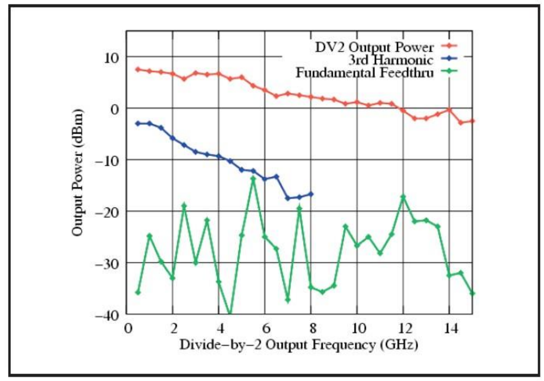
** Low frequency limit dependent on input edge speed*

Frequency Divider Application

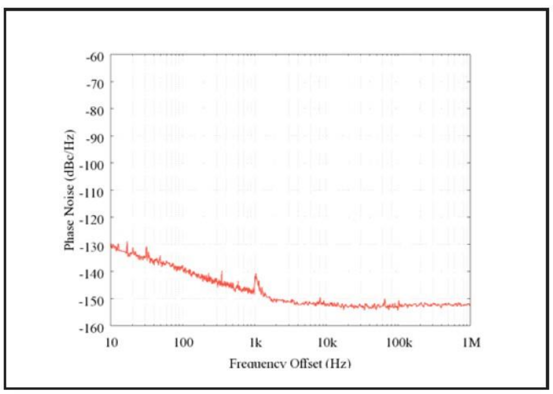
Min/Max Single-Ended Power Input Sensitivity Window



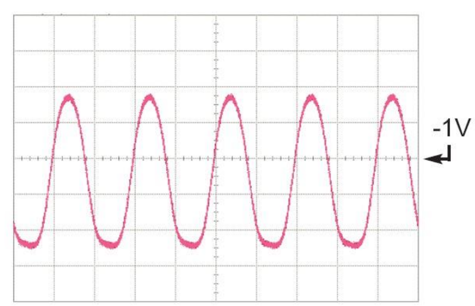
Divide-by-2 Output Power, 3rd Harmonic & Input Feedthru



SSB Phase Noise for Binary Divide-by-8 Configuration Input Freq = 7.8 GHz

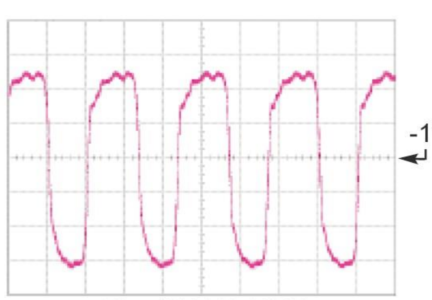


Binary Divide-by-2 Configuration Input Freq = 20 GHz



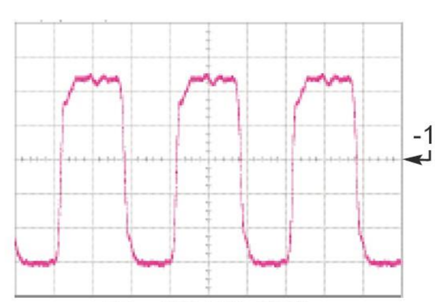
50 ps/DIV, 150mV/DIV

Integer Divide-by-7 Configuration Input Freq = 15 GHz



200 ps/DIV, 200mV/DIV

Integer Divide-by-9 Configuration Input Freq = 15 GHz



200 ps/DIV, 200mV/DIV

Functional Block Diagram

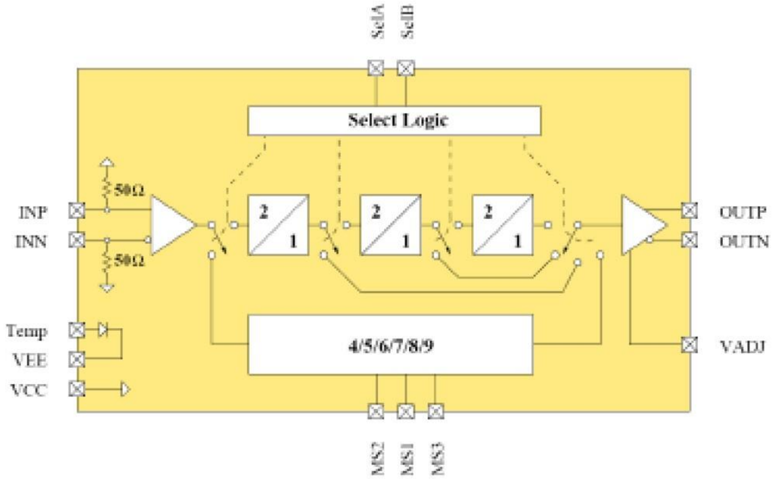


Table 1: Pin Description

Port Name	Description	Notes
INP	Prescaler Input, Positive Terminal	CML signal levels
INN	Prescaler Input, Negative Terminal	CML signal levels
OUTP	Prescaler Output, Positive Terminal	Requires DC return path to VCC
OUTN	Prescaler Output, Negative Terminal	Requires DC return path to VCC
VADJ	Output Amplitude Control	Tie to VCC via resistor, refer to text for value
SelA	Divider Select Control Line	Divider Select, See Table 1, defaults to logic 0
SelB	Divider Select Control Line	Divider Select, See Table 1, defaults to logic 0
MS1	Modulus Select Control Line	Modulus Select, See Table 2, defaults to logic 0
MS2	Modulus Select Control Line	Modulus Select, See Table 2, defaults to logic 0
MS3	Modulus Select Control Line	Modulus Select, See Table 2, defaults to logic 0
Temp	Temperature Diode	Optional Temperature diode, refer to text
VCC	RF & DC Ground	-
VEE	-3.3 V @ 185 mA	Negative Supply Voltage

Table 2: Divider Mode Select Logic

SelA	SelB	Mode	DC Current
0	0	Multi-Modulus	185 mA
1	0	Divide-by-8	165 mA
0	1	Divide-by-4	160 mA
1	1	Divide-by-2	150 mA

Table 3: Multi-Modulus Control Logic

MS1	MS2	MS3	Modulus
0	1	1	Divide-by-4
1	1	1	Divide-by-5
0	0	1	Divide-by-6
1	0	1	Divide-by-7
0	0	0	Divide-by-8
1	0	0	Divide-by-9
X	1	0	Invalid

Simplified Control Logic Schematic

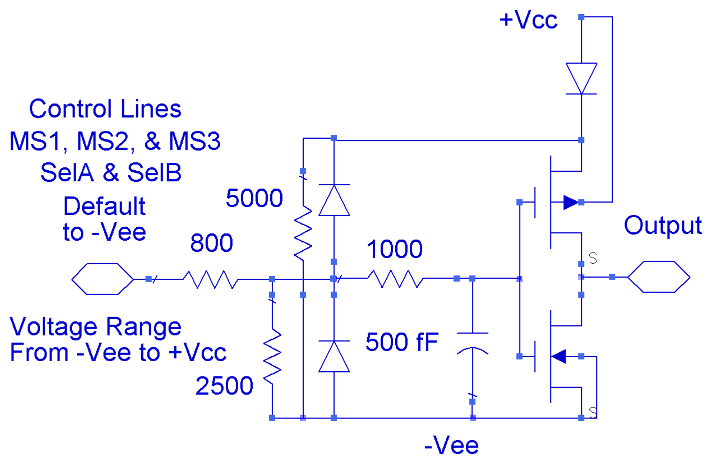


Table 4: Control Voltages

State	Bias Condition	Comment
Low (logic 0)	VEE @ 0 mA	Default condition (internally pulled low)
High (logic 1)	VCC @ 1 mA	

Application Notes

Divider Mode:

The UXM15P has two main modes of operation, a binary division mode (2/4/8) optimized for high speed operation and an integer-N mode where N can take on any value from 4 to 9. The prescaler can be configured for one of the four states using two select lines which are compatible with CMOS/LVTTL signaling levels. Table 1 lists the four states for the given logic levels on the SelA and SelB select lines. For any given mode, circuitry which is not used is automatically powered down to reduce power consumption.

Modules Control:

When placed into integer-N mode, three modulus control lines determine the divide value. Table 2 lists the modulus logic levels required for a given divide ratio. Users requiring a fixed divide-by-4 or divide-by-8 mode are urged to use the binary division mode due to the higher toggle rate and lower power consumption. The modulus control lines are compatible with CMOS/LVTTL signaling levels and are internally pulled low by default.

There are two invalid multi-modulus mode states shown in Table 2. The invalid states must be avoided. Divide sequences that include transition through an invalid state can result in an incorrect divide ratio. For example, transitions from 011 or 111 to 000 should be avoided, because if MS3 changes before MS2, the divider passes through an invalid state.

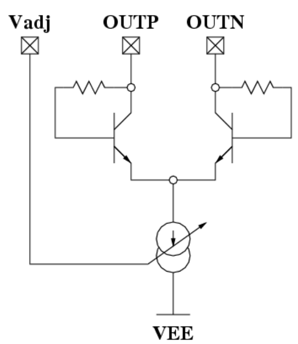
Application Notes (continued)

Divider Outputs:

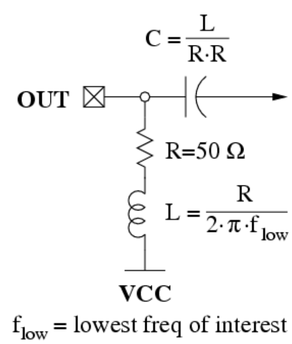
The equivalent circuit of the divider outputs is shown on the below. The outputs require a DC return path capable of handling ~35 mA per side. If DC coupling is employed, the DC resistance of the receiving circuits should be ~50 Ω (or less) to VCC to prevent excessive common mode voltage from saturating the prescaler outputs. If AC coupling is used, the perfect embodiment is shown in figure 2. The discrete R/L/C elements should be resonance free up to the maximum frequency of operation for broadband applications.

The output amplitude can be adjusted over a 1.5:1 range by one of the two methods The Vadj pin voltage can be set to VCC for maximum amplituded or VCC-1.3 V for an amplitude ~2/3 the max swing. Voltages between these two values will produce a linear change in output swing. Alternatively, users can use a 1k potentiometer or fixed resistor tied between Vadj and VCC. Resistor values approaching 0 ohms will lead to the maximum swing, while values approaching 1k will lead to the minimum output swing. Users who only need/want the maximum swing should simply tie Vadj to VCC.

Equivalent Circuit of Output Buffer



Recommended Circuit for AC Coupled Outputs



Low Frequency Operation:

Low frequency operation is limited by external bypass capacitors and the slew rate of the input clock. The next paragraph shows the calculations for the bypass capacitors. If DC coupled, the device operates down to DC for square-wave inputs. Sine-wave inputs are limited to ~50 MHz due to the 10 dBm max input power limitation.

The values of the coupling capacitors for the high-speed inputs and outputs (I/O’s) are determined by the lowest frequency the IC will be operated at.

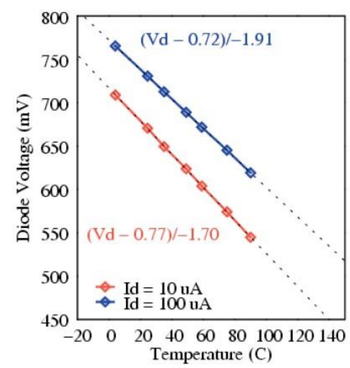
$$C \gg \frac{1}{2 \cdot \pi \cdot 50\Omega \cdot f_{lowest}}$$

For example to use the device below 30 kHz, coupling capacitors should be larger than 0.1uF.

Temperature Diode:

An optional on chip temperature diode is provided for users interested in evaluating the IC's temperature. A single resistor to VCC establishes a nominal current thru the diode. The voltage developed across the temperature pin (pin 8) referenced to VEE (pin 9) can then be used to indicate the surface temperature of the IC. The plot below was obtained by forcing a fixed current thru the diode for an unbiased device at multiple temperatures and fitting a line to the data to allow extrapolation over a range of temperatures.

Diode Voltage vs Temp for 2 Bias Currents



Package Heatsink:

The package backside provides the primary heat conduction path and should be attached to a good heatsink on the PC board to maximize performance. User PC boards should maximize the contact area to the package paddle and contain an array of vias to aid thermal conduction to either a backside heatsink or internal copper planes.

IC Assembly:

The device is designed to operate with either single-ended or differential inputs. Figures 4, 5 & 6 show the IC assembly diagrams for positive and negative supply voltages. In either case the supply should be capacitively bypassed to the ground to provide a good AC ground over the frequency range of interest. The backside of the chip should be connected to a good thermal heat sink.

All RF I/O's are connected to VCC through on-chip termination resistors. This implies that when VCC is not DC grounded (as in the case of positive supply), the RF I/O's should be AC coupled through series capacitors unless the connecting circuit can generate the correct levels through level shifting.

CML Logic Levels for DC Coupling (T = 25˚C):

Assuming 50 Ω Terminations at Inputs and Outputs

Parameter			Minimum	Typical	Maximum
Input	Differential	Logic $Input_{high}$	Vcc	Vcc	Vcc
		Logic $Input_{low}$	Vcc - 0.05 V	Vcc - 0.3 V	Vcc - 1 V
	Single	Logic $Input_{high}$	Vcc + 0.05 V	Vcc + 0.3 V	Vcc + 1 V
		Logic $Input_{low}$	Vcc - 0.05 V	Vcc - 0.3 V	Vcc - 1 V
Output	Differential & Single	Logic $Input_{high}$	Vcc - 0.9 V	Vcc – 0.6 V	Vcc – 0.5 V
		Logic $Input_{low}$	Vcc – 1.1 V	Vcc – 1.6 V	Vcc – 1.7 V

Differential vs. Single-Ended:

The UXM15P is fully differential to maximize signal-to-noise ratios for high-speed operation. High speed inputs are terminated to VCC with on-chip resistors (refer to functional block diagram for specific resistor values). The maximum DC voltage on any terminal must be limited to V max to prevent damaging the termination resistors with excessive current. Regardless of bias conditions, the following equation should be satisfied when driving the inputs differentially:

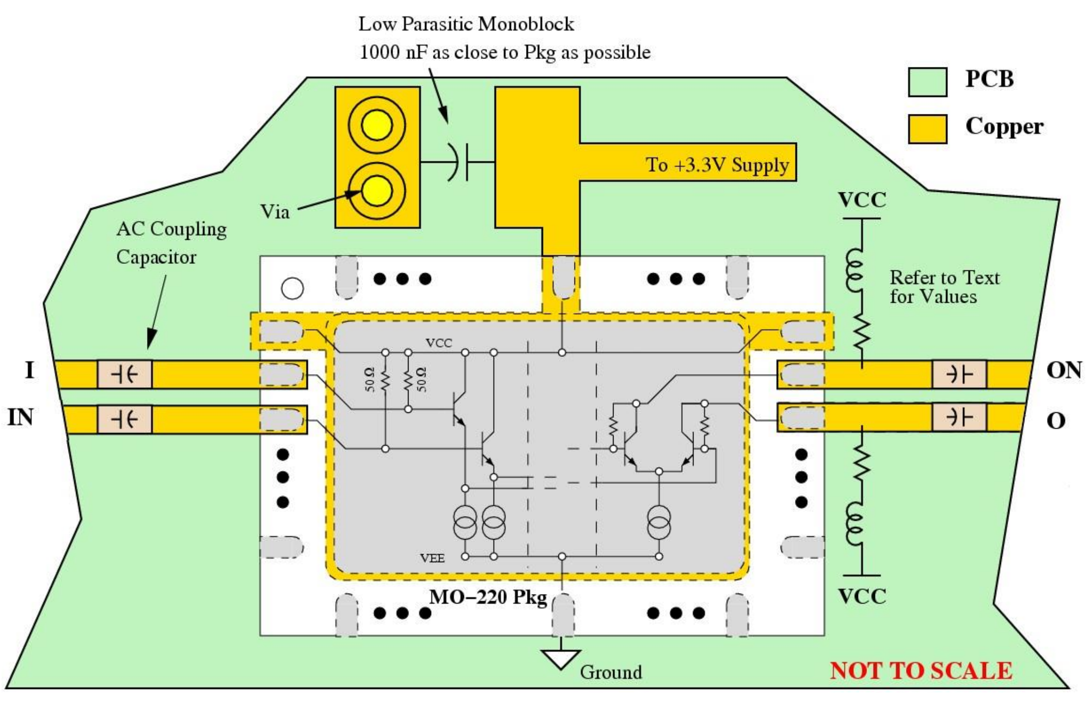
$$| Vdm/2 + Vcm | < Vcc \geq Vmax$$

where Vdm is the differential input signal and Vcm is the common-mode voltage.

In addition to the maximum input signal levels, single-ended operation imposes additional restrictions: the average DC value of the waveform at IC should be equal to VCC for single-ended operation. In practice, this is easily achieved with a single capacitor on the input acting as a DC block. The value of the capacitor should be large enough to pass the lowest frequencies of interest. Use the positive terminals for single-ended operation while terminating the negative terminal to VCC.

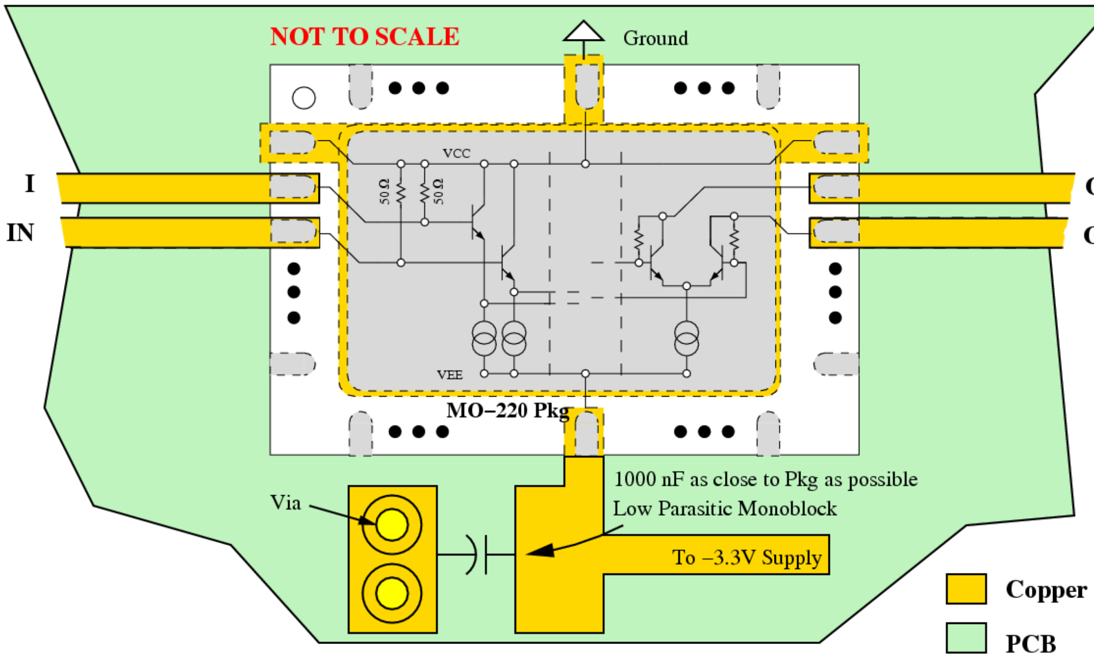
Note that a potential oscillation mechanism exists if both inputs are static and have identical DC voltages; a small DC offset on either input is sufficient to prevent possible oscillations. Tying unused inputs directly to VCC shorts out the internal 50 Ω bias resistor, imposing a DC offset sufficient to prevent oscillations. Driving the differential inputs with DC blocks, or driving the single-ended inputs without terminating unused inputs, is not recommended without taking additional steps to eliminate the potential oscillation issues.

Positive Supply (AC Coupling)



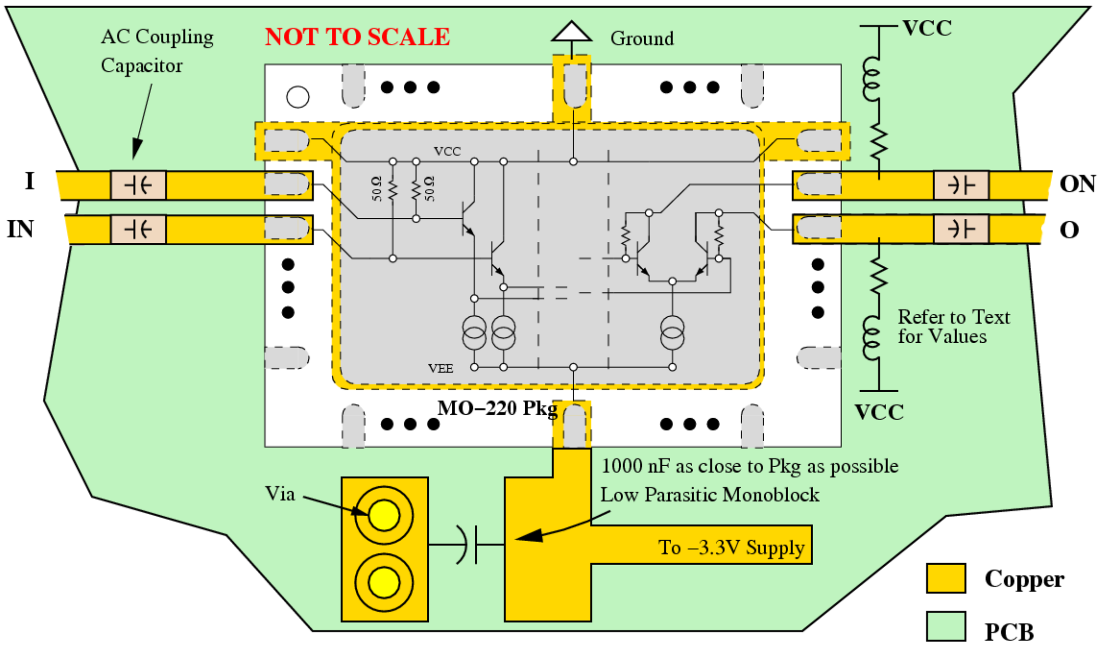
Biasing recommendations for positive supply with AC coupling applications

Negative Supply (DC Coupling)



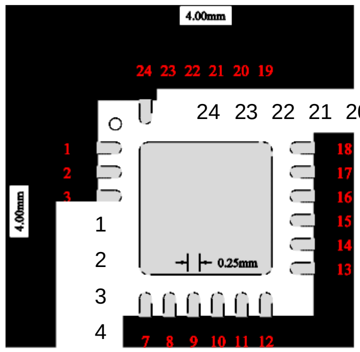
Biasing recommendations for negative supply with DC coupling applications

Negative Supply (AC Coupling)



Biasing recommendations for negative supply with AC coupling applications

UXM15P Physical Characteristics



Pkg size:	4.00 x 4.00 mm
Pkg size tolerance:	+/- 0.25 mm
Pkg thickness:	0.9 +/- 0.1 mm
Pad dimensions:	0.25 x 0.4 mm
Center paddle:	2.2 x 2.2 mm
JEDEC designator:	MO-220

Top View

Table 5: UXM15P Pin Definition

	Function	Notes
1,3,5,6,7,13,15,17,19,20 (Vcc)	RF and DC Ground	0 V (+3.3 V when using positive supply)
9,23,24 (Vee)	Negative Supply Voltage	Nominally -3.3 V (0 V when using positive supply)
2 (INP)	Divider Input	Positive Terminal of differential output
4 (INN)	Divider Input	Negative Terminal of differential output
8 (Temp)	Temperature Diode	IC Surface temperature, Refer to text
10 (MS2)	Integer-N Modulus Control	Modulus Select, Refer to Table 2
11 (MS1)	Integer-N Modulus Control	Modulus Select, Refer to Table 2
12 (MS3)	Integer-N Modulus Control	Modulus Select, Refer to Table 2
14 (VADJ)	Output Amplitude Control	Tie to VCC for max swing. Refer to text
16 (OUTP)	Divider Output	Positive Terminal of differential output
18 (OUTN)	Divider Output	Negative Terminal of differential output
21 (SelB)	Divider Mode	Divider Select Line, Refer to Table 1
22 (SelA)	Divider Mode	Divider Select Line, Refer to Table 1
Paddle	Package Paddle	Tie to heatsink, Refer to text

Table 6: Absolute Maximum Ratings

Parameter	Value	Unit
Supply Voltage (VCC-VEE)	4	V
RF Input Power (INP, INN)	10	dBm
Operating Temperature	-40 to 85	ºC
Storage Temperature	-85 to 125	ºC
Junction Temperature	125	ºC

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