TJA1101B

100BASE-T1 PHY for automotive Ethernet

Rev. 1 — 1 March 2021 Product data sheet

1 General description

The TJA1101B is a 100BASE-T1-compliant Ethernet PHY optimized for automotive use cases such as gateways, IP camera links, radar modules, driver assistance systems and back-bone networks. The device provides 100 Mbit/s transmit and receive capability over a single unshielded twisted-pair cable, supporting a cable length of up to at least 15 m. The TJA1101B has been designed for automotive robustness and ISO 26262, ASIL-A compliance, while minimizing power consumption and system costs.

Being ASIL-A compliant, adequate safety features have been implemented to ensure that ASIL requirements are met at system level. Additional documentation, including a safety manual, is available on request.

The TJA1101B supports OPEN Alliance TC-10-compliant sleep and wake-up request forwarding, with an always-on power domain connected directly to the battery supply without the need for a dedicated voltage regulator.

2 Features and benefits

2.1 General

- 100BASE-T1 PHY
- MII- and RMII-compliant interfaces
- Compact 36-pin HVQFN package (6 × 6 mm) for PCB space-constrained applications
- ISO 26262, ASIL-A compliant

2.2 Optimized for automotive use cases

- Transmitter optimized for capacitive coupling to unshielded twisted-pair cable
- Adaptive receive equalizer optimized for automotive cable length of up to at least 15 m
- Enhanced integrated PAM-3 pulse shaping for low RF emissions
- EMC-optimized output driver strength for MII and RMII
- MDI pins meet class IV conducted emission limit as per OPEN Alliance EMC Specification 2.0
- MDI pins protected against ESD to ±6 kV HBM and ±8 kV IEC61000-4-2
- MDI pins protected against transients in automotive environment
- MDI pins do not need external filtering or ESD protection
- Automotive-grade temperature range from -40 °C to +125 °C
- Automotive product qualification in accordance with AEC-Q100
- Host-configurable MDI polarity
- Automated polarity detection and correction

2.3 Low-power mode

- OPEN Alliance TC-10-compliant sleep and wake-up forwarding
  – Robust remote wake-up detection via bus lines
  – Wake-up forwarding at PHY level (supporting global system wake-up)
- Inhibit output for voltage regulator control
- Dedicated PHY enable/disable input pin to minimize power consumption
- Local wake-up pin
- Wake-up via SMI-access

2.4 Diagnosis

- Signal Quality Indicator for real-time monitoring of link stability and transmitted data quality
- Diagnosis of cable errors (shorts and opens)
- Gap-free supply undervoltage detection with fail-silent behavior
- Internal, external and remote loopback modes

2.5 Miscellaneous

- Reverse MII mode for back-to-back connection of two PHYs
- On-chip regulators to provide 3.3 V single-supply operation
- Supports optional 1.8 V external supply for digital core
- On-chip termination resistors for the differential cable pair
- Jumbo frame support up to 16 kB

3 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TJA1101BHN	HVQFN36	plastic thermal enhanced very thin quad flat package; no leads; 36 terminals; body 6 × 6 × 0.85 mm	SOT1092-2

4 Block diagram

A block diagram of the TJA1101B is shown in Figure 1. The 100BASE-T1 section contains the functional blocks specified in the 100BASE-T1 standard that make up the Physical Coding Sublayer (PCS) and the Physical Medium Attachment (PMA) layer for both the transmit and receive signal paths. The MII/RMII interface (including the Serial Management Interface (SMI)) conforms to IEEE 802.3 clause 22.

Additional blocks are defined for mode control, register configuration, interrupt control, system configuration, reset control, local wake-up, remote wake-up, undervoltage detection and configuration control. A number of power-supply-related functional blocks are defined: an internal 1.8 V regulator for the digital core, a Very Low Power (VLP) supply for Sleep mode, the reset circuit, supply monitoring and inhibit control.

The clock signals needed for the operation of the PHY are generated in the PLL block, derived from an external crystal or an oscillator input signal.

Pin strapping allows a number of default PHY settings (e.g. Master or Slave configuration) to be hardware-configured at power-up.

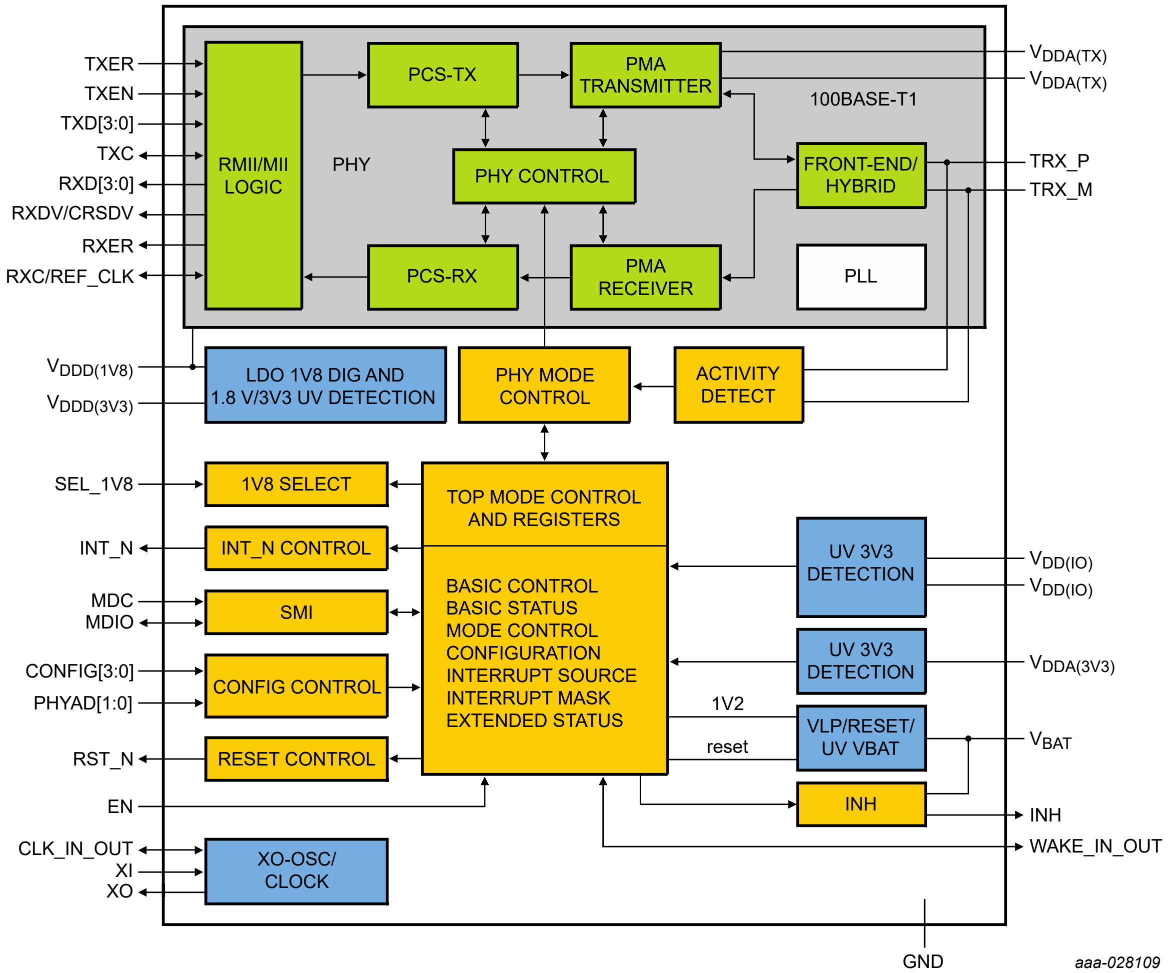


Figure 1. Block diagram

5 Pinning information

5.1 Pinning

The pin configuration of the TJA1101B is shown in Figure 2. Since 100BASE-T1 allows for full-duplex bidirectional communication, the standard MII signals COL and CRS are not needed.

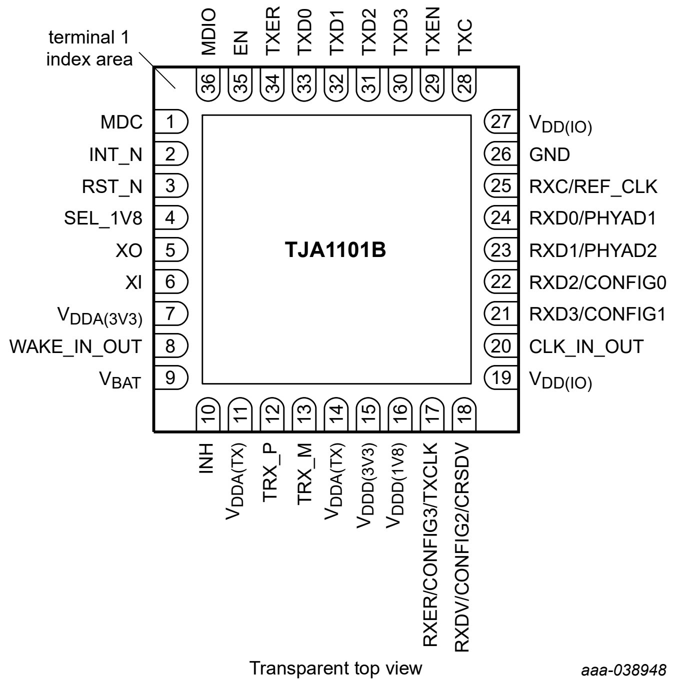


Figure 2. Pin configuration diagram

Table 2. Pin description

Symbol	Pin	Type[1]	Description
MDC	1	I	SMI clock input (weak pull-down)
INT_N	2	O	interrupt output (active-LOW, open-drain output, level-based)
RST_N	3	I	reset input (active-LOW, weak pull-up)
SEL_1V8	4	I	1.8 V LDO mode selection (external or internal; weak pull-down)
XO	5	AO	crystal feedback - used in all MII/RMII and Reverse MII modes when a 25 MHz crystal is used
XI	6	AI	crystal input - used in all MII/RMII and Reverse MII modes when a 25 MHz crystal is used
$V_{DDA(3V3)}$	7	P	3.3 V analog supply voltage
WAKE_IN_OUT	8	AIO	local/forwarding wake-up input/output (configurable)
V_{BAT}	9	P	battery supply voltage
INH	10	AO	inhibit output for voltage regulator control (V_{BAT}-related, active-HIGH)

Table 2. Pin description...*continued*

Symbol	Pin	Type[1]	Description
$V_{DDA(TX)}$[2]	11	P	3.3 V analog supply voltage for the transmitter
TRX_P	12	AIO	+ terminal for transmit/receive signal
TRX_M	13	AIO	- terminal for transmit/receive signal
$V_{DDA(TX)}$[2]	14	P	3.3 V analog supply voltage for the transmitter
$V_{DDD(3V3)}$	15	P	3.3 V digital supply voltage
$V_{DDD(1V8)}$	16	P	1.8 V digital supply voltage (internally or externally generated; needs to be filtered if generated internally)
RXER	17	O	MII/RMII receive error output
CONFIG3	17	I	pin strapping configuration input 3
TXCLK	17	O	transmit clock output in test mode and during slave jitter test
RXDV	18	O	MII receive data valid output
CONFIG2	18	I	pin strapping configuration input 2
CRSDV	18	O	RMII mode: carrier sense/receive data valid output
$V_{DD(IO)}$[3]	19	P	3.3 V I/O supply voltage
CLK_IN_OUT	20	IO	25 MHz reference clock input/output (configurable)
RXD3	21	O	MII mode: receive data output, bit 3 of RXD[3:0] nibble
CONFIG1	21	I	pin strapping configuration input 1
RXD2	22	O	MII mode: receive data output, bit 2 of RXD[3:0] nibble
CONFIG0	22	I	pin strapping configuration input 0
RXD1	23	O	MII mode: receive data output, bit 1 of RXD[3:0] nibble RMII mode: receive data output, bit 1 of RXD[1:0] nibble
PHYAD2	23	I	pin strapping configuration input for bit 2 of the PHY address used for the SMI address/Cipher scrambler
RXD0	24	O	MII mode: receive data output, bit 0 of RXD[3:0] nibble RMII mode: receive data output, bit 0 of RXD[1:0] nibble
PHYAD1	24	I	pin strapping configuration input for bit 1 of the PHY address used for the SMI address/Cipher scrambler
RXC	25	O	MII mode: external 25 MHz receive clock output
		I	MII reverse mode: 25 MHz receive clock input
REF_CLK	25	I	RMII mode: interface reference clock input (50 MHz external oscillator)
		O	RMII mode: interface reference clock output (25 MHz crystal at PHY or 25 MHz clock at input of pin CLK_IN_OUT)
GND[4]	26	G	ground reference
$V_{DD(IO)}$[3]	27	P	3.3 V I/O supply voltage
TXC	28	O	MII mode: 25 MHz transmit clock output
		I	MII reverse mode: external 25 MHz transmit clock input
TXEN	29	I	MII/RMII mode: transmit enable input (active-HIGH; weak pull-down)
TXD3	30	I	MII mode: transmit data input, bit 3 of TXD[3:0] nibble (weak pull-down)

Table 2. Pin description...*continued*

Symbol	Pin	Type[1]	Description
TXD2	31	I	MII mode: transmit data input, bit 2 of TXD[3:0] nibble (weak pull-down)
TXD1	32	I	MII mode: transmit data input, bit 1 of TXD[3:0] nibble (weak pull-down) RMII mode: transmit data input, bit 1 of TXD[1:0] nibble (weak pull-down)
TXD0	33	I	MII mode: transmit data input, bit 0 of TXD[3:0] nibble (weak pull-down) RMII mode: transmit data input, bit 0 of TXD[1:0] nibble (weak pull-down)
TXER	34	I	MII/RMII: transmit error input (weak pull-down)
EN	35	I	PHY enable input (active-HIGH; weak pull-down)
MDIO	36	IO	SMI data I/O (weak pull-up)

[1] AIO: analog input/output; AO: analog output; AI: analog input; I: digital input ($V_{DD(IO)}$ related); O: digital output ($V_{DD(IO)}$ related); IO: digital input/output ($V_{DD(IO)}$ related); P: power supply; G: ground.

[2] $V_{DDA(TX)}$ pins are connected internally and should be connected together on the PCB (pins 11 and 14).

[3] $V_{DD(IO)}$ pins are connected internally and should be connected together on the PCB (pins 19 and 27).

[4] HVQFN36 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is also recommended to connect the exposed center pad to board ground..

6 Functional description

6.1 System configuration

The TJA1101B contains a 100BASE-T1 compliant Ethernet PHY, with 100 Mbit/s transmit and receive capability over a single unshielded twisted-pair cable. The TJA1101B supports a cable length of up to at least 15 m, with a bit error rate of 1E-10 or less. It is optimized for capacitive signal coupling to the twisted-pair lines. A common-mode choke is typically inserted into the signal path to comply with automotive EMC requirements.

The TJA1101B is designed to provide a cost-optimized system solution for automotive Ethernet links. It communicates with the Media Access Control (MAC) unit via the MII or RMII interface.

The TJA1101B can operate with a crystal or an external clock. The clock can be forwarded to other PHYs (see Figure 3). The clocking and power supply schemes are independent of each other.

The TJA1101B can be powered via a single 3.3 V supply. An internal LDO generates the required 1.8 V supply, requiring only the addition of a decoupling capacitor.

When the TJA1101B is used in a switch application with several PHY ports, it may be more efficient to use an external SMPS to provide the 1.8 V supply. In this configuration, the internal LDO is switched off to allow an external supply to be used.

The state of SEL_1V8 is captured and copied to bit LDO_MODE (see Table 11) when the device is powered up. A bit value of 0 enables the internal 1.8 V LDO. If LDO_MODE = 1, the internal LDO is disabled and $V_{DDD(1V8)}$ must be supplied externally. The value of LDO_MODE can be changed after power-up via register access.

Control and status information is exchanged with the host controller via the SMI interface. The INH output can be used to switch off the external regulator when all ports are in Sleep mode.

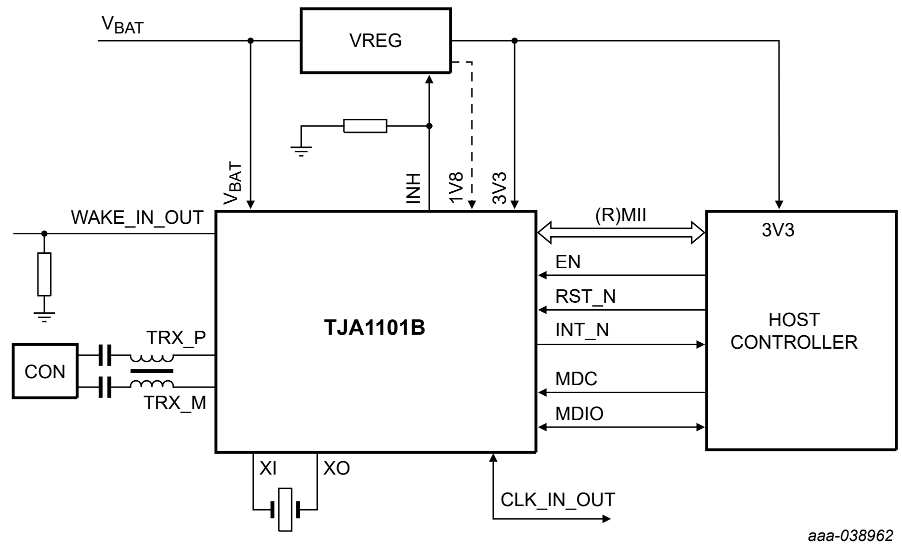


Figure 3. Typical TJA1101B switch application circuit

6.2 MII and RMII

The TJA1101B supports a number of MII modes that can be selected via pin strapping or the SMI. The following modes are supported:

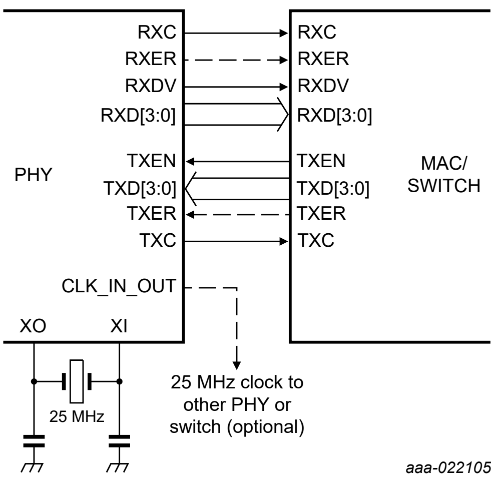
- MII
- RMII (25 MHz XTAL or external 50 MHz via REF_CLK)
- Reverse MII (connected externally)

Refer to the SMI register description (Section 6.11) for further configuration options. The strength of the (R)MII output driver signals can be limited in all modes (via bit MII_DRIVER; see Table 21) to optimize EMC behavior.

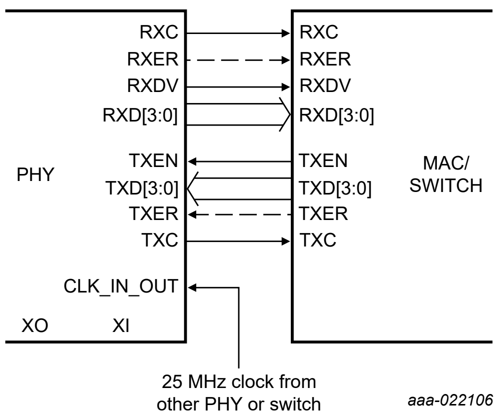
6.2.1 MII

The connections between the PHY and the MAC are shown in more detail in Figure 4. Data is exchanged via 4-bit wide data nibbles on TXD[3:0] and RXD[3:0]. Transmit and receive data is synchronized with the transmit (TXC) and receive (RXC) clocks. Both clock signals are provided by the PHY and are typically derived from an external clock or crystal running at a nominal frequency of 25 MHz (±100 ppm). Normal data transmission is initiated with a HIGH level on TXEN, while a HIGH level on RXDV indicates normal data reception.

MII encoding is described in Table 3 and Table 4.



a. Using external XTAL showing optional 25 MHz clock output



b. Using external reference clock

Figure 4. MII signaling

Table 3. MII encoding of TXD[3:0], TXEN and TXER

TXEN	TXER	TXD[3:0]	Indication
0	0	0000 through 1111	normal interframe
0	1	0000 through 1111	reserved
1	0	0000 through 1111	normal data transmission
1	1	0000 through 1111	transmit error propagation

Table 4. MII encoding of RXD[3:0], RXDV and RXER

RXDV	RXER	RXD[3:0]	Indication
0	0	0000 through 1111	normal interframe
0	1	0000	normal interframe
0	1	0001 through 1101	reserved
0	1	1110	false carrier indication
0	1	1111	reserved
1	0	0000 through 1111	normal data transmission
1	1	0000 through 1111	data reception with errors

6.2.2 RMII

6.2.2.1 Signaling and encoding

RMII data is exchanged via 2-bit wide data nibbles on TXD[1:0] and RXD[1:0], as illustrated in Figure 5. To achieve the same data rate as MII, the interface is clocked at a nominal frequency of 50 MHz. A single clock signal, REF_CLK, is provided for both transmitted and received data. This clock signal is provided by the PHY and is typically derived from an external 25 MHz (±100 ppm) crystal (see Figure 5 (a)). Alternatively, a 50 MHz clock signal (±50 ppm) generated by an external oscillator can be connected to pin REF_CLK (see Figure 5 (b)). A third option is to connect a 25 MHz (±100 ppm) clock signal generated by another PHY or switch to pin CLK_IN_OUT (see Figure 5 (c)).

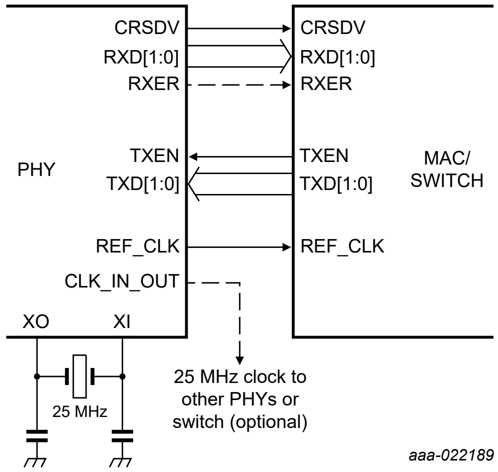
RMII encoding is described in Table 5 and Table 6.

Table 5. RMII encoding of TXD[1:0], TXEN

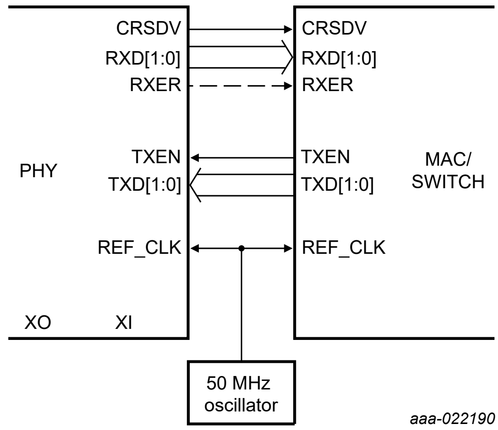
TXEN	TXD[1:0]	Indication
0	00 through 11	normal interframe
1	00 through 11	normal data transmission

Table 6. RMII encoding of RXD[1:0], CRSDV and RXER

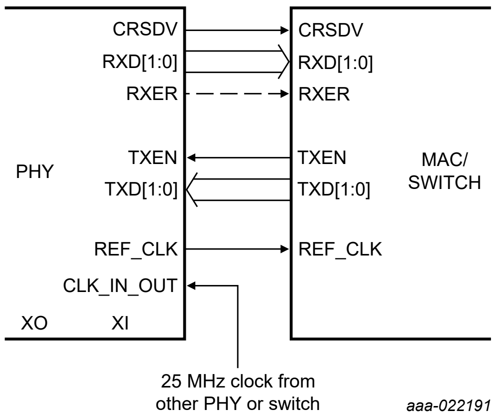
CRSDV	RXER	RXD[1:0]	Indication
0	0	00 through 11	normal interframe
0	1	00	normal interframe
0	1	01 through 11	reserved
1	0	00 through 11	normal data transmission
1	1	00 through 11	data reception with errors



a. Using external XTAL showing optional 25 MHz clock output



b. Using external reference clock



c. Using externally generated 25 MHz reference clock

Figure 5. RMII signaling

6.2.3 Reverse MII

In Reverse MII mode, two PHYs are connected back-to-back via the MII interface to realize a repeater function on the physical layer (see Figure 6). The MII signals are cross-connected: RX output signals from one PHY are connected to the TX inputs on the other PHY. The TXC and RXC clock signals become inputs on the PHY connected in Reverse MII mode. Reverse MII mode is selected by setting bits MII_MODE = 11

Since the MII interface is a standard solution, two PHYs could be used to implement two different physical layers to realize, for example, a conversion from Fast Ethernet to 100BASE-T1 and vice versa. Another use case for such a repeater could be to double the link length to 30 m.

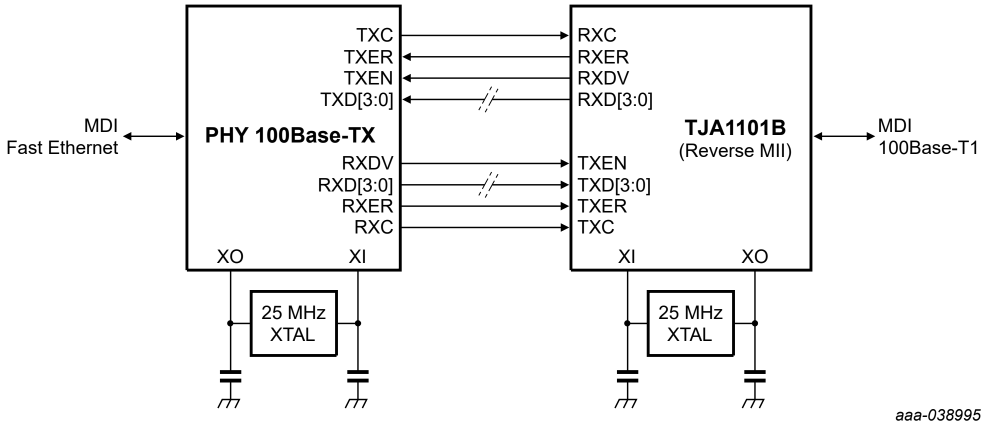


Figure 6. Fast Ethernet to 100BASE-T1 media converter with TJA1101B in Reverse MII

6.3 System controller

6.3.1 Operating modes

6.3.1.1 Power-off mode

The TJA1101B remains in Power-off mode as long as the voltage on pin V_{BAT} is below the power-on reset threshold. The analog blocks are disabled and the digital blocks are in a passive reset state in this mode.

6.3.1.2 Standby mode

At power-on, when the voltage on pin V_{BAT} rises above the under-voltage recovery threshold ($V_{uvr(VBAT)}$), the TJA1101B enters Standby mode and switches on the INH control output (pin INH HIGH). This control signal may be used to activate the supply to the microcontroller in the ECU. Once the 3.3 V supply voltage is available, the internal 1.8 V regulator is activated (if selected) and the PHY is configured according to the pin strapping implemented on the CONFIGn and PHYADn pins. No SMI access takes place during the power-on settling time ($t_{s(pon)}$).

From an operating point of view, Standby mode corresponds to the IEEE 802.3 Power-down mode, where the transmit and receive functions (in the PHY) are disabled. Standby mode also acts as a fail-silent mode. The TJA1101B switches to Standby mode when an undervoltage condition is detected on $V_{DDA(3V3)}$, $V_{DDD(3V3)}$, $V_{DDD(1V8)}$ or $V_{DD(IO)}$.

6.3.1.3 Normal mode

To establish a communication link, the TJA1101B must be switched to Normal mode, either autonomously (AUTO_OP = 1; see Table 30) or via an SMI command from the host (AUTO_OP = 0).

When the TJA1101B is configured for autonomous operation, the PHY enters Normal mode automatically and activates the link on power-on. When the TJA1101B is host-controlled, the PHY must be enabled via the SMI.

When the PHY is enabled and enters Normal mode, the internal PLL starts running and the transmit and receive functions (both PCS and PMA) are enabled. After a period of stabilization, $t_{init(PHY)}$, the PHY is ready to set up a link.

If link control is enabled (LINK_CONTROL = 1; see Table 20), a PHY configured as Master initiates the training sequence by transmitting an idle pattern. The receiver of a PHY configured as Slave will attempt to synchronize with the idle pattern. Once the descrambler is synchronized (SCR_LOCKED = 1), the slave PHY itself starts sending an idle pattern using the recovered clock signal.

The link is established (LINK_STATUS = 1) when the TJA1101B PHY and the remote PHY indicate that their local receiver status is OK.

6.3.1.4 Disable mode

When the Ethernet interface is not in use or must be disabled for fail-safe reasons, the PHY can be switched off by pulling pin EN LOW. The PHY is switched off completely in Disable mode, minimizing power consumption. The configuration register settings are maintained. EN must be forced HIGH to exit Disable mode and activate the PHY.

6.3.1.5 Sleep mode

If the network manager decides to withdraw a node from the network because it is no longer needed, the PHY can be switched to Sleep mode (powering down the entire ECU).

In Sleep mode, the transmit and receive functions are switched off and no signal is driven onto the twisted-pair lines. Transmit requests from the MII interface are ignored and the MII output pins are in a high-ohmic state. The only valid SMI operations in Sleep mode are reading the POWER_MODE status bits in the Extended control register and issuing a Standby mode command (POWER_MODE = 1100; see Table 20).

Releasing the INH output (INH LOW) allows the ECU to switch off its main power supply unit. Typically, the entire ECU is powered-down. The TJA1101B is kept partly alive by the permanent battery supply and can still react to activity on the Ethernet lines. Once valid Ethernet idle pulses longer than $t_{det(PHY)}$ are detected on the lines (with REMWUPHY = 1), the TJA1101B wakes up in Standby mode and switches on the main power unit via the INH control signal. The TJA1101B PHY enters Normal mode via autonomous operation once the supply voltages are stable within their operating ranges, or can be switched to Normal mode via an SMI command if host-controlled. The communication link to the partner can then be re-established.

Sleep mode can be entered from Normal mode via the intermediate Sleep Request mode as well as from Standby mode, as shown in Figure 7. Note that the configuration register settings are maintained in Sleep mode.

If CLK_IN_OUT is used to provide the clock for other devices (e.g. other PHYs), the clock signal can be configured to remain active (CLK_HOLD = 1) along with INH even when the PHY is in Sleep mode or disabled. When CLK_HOLD = 1, the device enters Sleep mode automatically but remains active until a FORCE_SLEEP SMI command is received. Note that this command forces the PHY to Sleep mode immediately (if it was not already in Sleep mode).

6.3.1.6 Sleep Request mode

Sleep Request mode is an intermediate state used to initiate a transition to Sleep mode. In Sleep Request mode, the PHY transmits scrambler code with an encoded LPS command to inform the link partner about the request to enter Sleep mode.

The PHY sleep request timer ($t_{to(req)sleep}$; see Table 37) starts when the TJA1101B enters Sleep Request mode. This timer determines the maximum length of time the PHY remains in Sleep Request mode. The PHY switches to Sleep mode (via an intermediate step through Silent mode) on receiving LPS confirmation of the sleep request from the Link partner. If the timer expires before confirmation is received from the link partner, the PHY returns to Normal mode. This process is valid when LPS_ACTIVE = 1 and SLEEP_CONFIRM = 1.

If bit SLEEP_ACK is not set when the PHY enters Sleep Request mode, it switches back to Normal mode if data is detected on MII or MDI (see Table 21). The DATA_DET_WU flag in the General status register is set and a WAKEUP interrupt is generated (if REMWUPHY = 1).

If SLEEP_ACK is set when the PHY enters Sleep Request mode, the PHY sleep acknowledge timer ($t_{to(ack)sleep}$; see Table 37) is started. While the timer is running, the PHY switches back to Normal mode in response to a host command or wake-up request. When the timer expires, LPS transmission begins to initiate a transition to Sleep mode. Data detected at MII or MDI is ignored.

INH is released when the PHY is in Sleep mode.

6.3.1.7 Silent mode

Silent mode is an intermediate state between Sleep Request mode and Sleep mode. It is provided to allow time to switch off the transmitter after a sleep request has been accepted before entering Sleep mode. The TJA1101B switches to Sleep mode once the channel goes silent.

If the channel remains active for longer than $t_{to(req)sleep}$, the PHY returns to Normal mode and a SLEEP_ABORT interrupt is generated.

6.3.1.8 Reset mode

The TJA1101B switches to Reset mode from any mode except Power-off when pin RST_N is held LOW for at least $t_{det(rst)(max)}$, provided the voltage on $V_{DD(IO)}$ is above the undervoltage threshold.

When RST_N goes HIGH again, or an undervoltage is detected on $V_{DD(IO)}$, the TJA1101B switches to Standby mode. All register bits are reset to their default values in Reset mode and the state of the pin strapping pins is captured.

6.3.2 Status of functional blocks in TJA1101B operating modes

Table 7 presents an overview of the status of TJA1101B functional blocks in each operating mode.

Table 7. Status of functional blocks in TJA1101B operating modes

Functional block	Normal	Standby	Sleep Request	Sleep	Disable
MII	on	high-ohmic[1]	on	high-ohmic	high-ohmic
PMA/PCS-TX	on	off	on	off	off
PMA/PCS-RX	on	off	on	off	off
SMI	on	on	on	on[2]	off
Activity detection	off	on	off	on	off
Crystal oscillator	on/off[3]	off	on/off[3]	off[4]	off
LDO_1V8	on/off[5]	on/off[5]	on/off[5]	off	off

Table 7. Status of functional blocks in TJA1101B operating modes *...continued*

Functional block	Normal	Standby	Sleep Request	Sleep	Disable
RST_N input	on	on	on	off	on
EN input	on	on	on	off	on
WAKE_IN_OUT	on/off[6]	on/off[6]	on/off[6]	on/off[6]	off
INT_N output	on	on	on	high-ohmic	high-ohmic
INH output	on	on	on	off	on/off[7]
Temp detection	on	on	on	off	off

[1] Outputs RXD[3:0], RXER and RXDV are LOW in Standby mode; the other MII pins are configured as inputs via internal 100 kΩ pull-down resistors.
[2] Limited access to SMI registers in Sleep mode to allow mode control/wake-up via SMI. $V_{DD(IO)}$ must be available.
[3] Configurable; depends on bits CLK_MODE in the Common configuration register.
[4] The crystal will be off in Sleep mode unless bit CLK_HOLD = 1 and bits CLK_MODE = 00 or 01.
[5] Configurable; $V_{DDD(1V8)}$ can be supplied internally (bit LDO_MODE in the Common configuration register LOW) or externally (bit LDO_MODE HIGH).
[6] Configurable.
[7] The behavior of the INH output in Disable mode is configurable and depends on bit CONFIG_INH in the Common configuration register.

6.4 Mode transitions

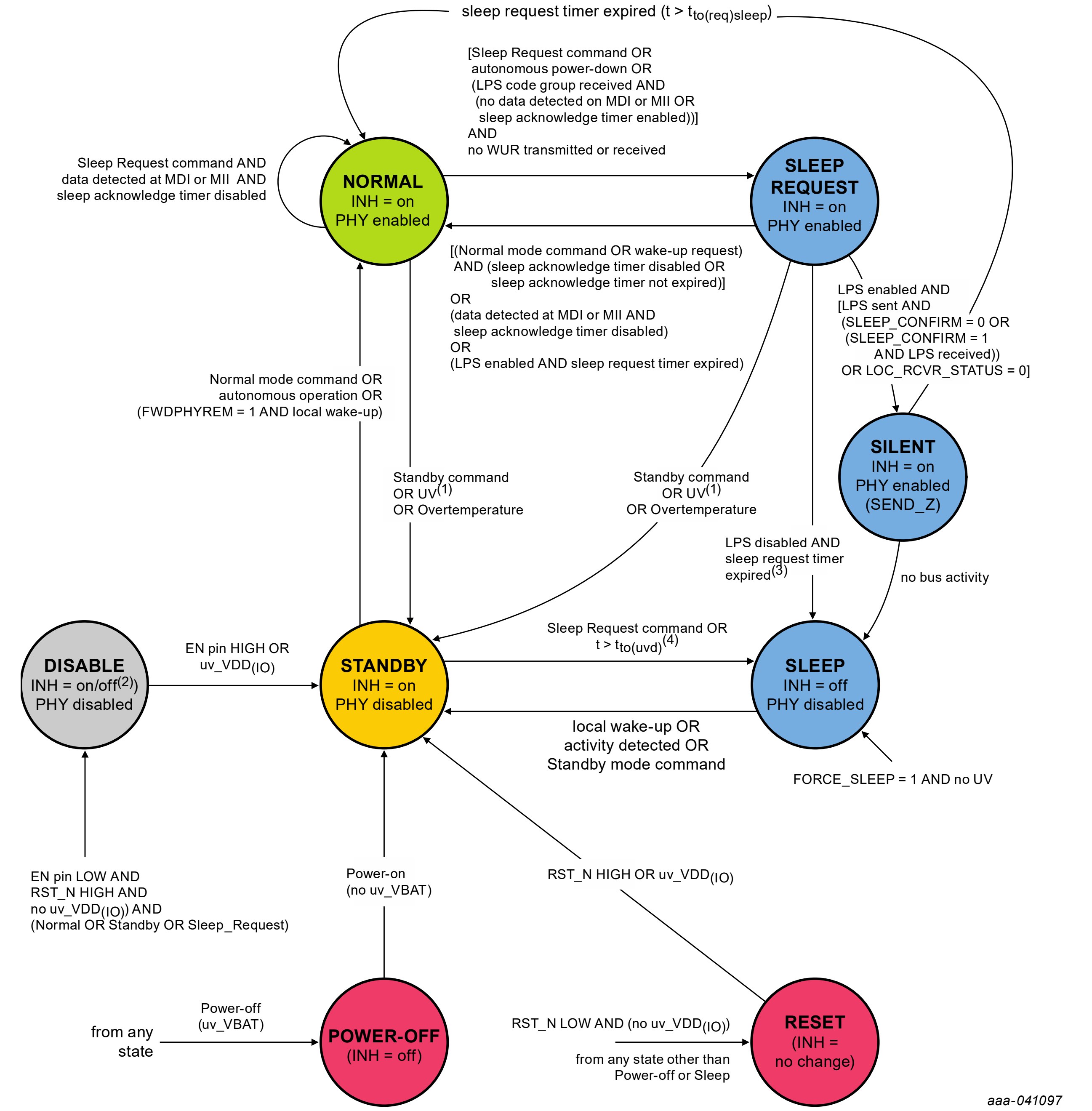
A mode transition diagram for the TJA1101B is shown in Figure 7. Abbreviations used in the mode transition diagram are defined in Table 8.

The following events, listed in order of priority, trigger mode transitions:

- Power on/off
- Undervoltage on $V_{DD(IO)}$
- RST_N input
- EN input
- Overtemperature or Undervoltage on $V_{DDA(3V3)}$, $V_{DDD(3V3)}$, $V_{DDD(1V8)}$
- SMI command and wake-up (local, remote or forwarding)

Table 8. State diagram legend

Transition	Abbreviation	Description
Silent to Normal	sleep request timer expired	$t > t_{to(req)sleep}$
Normal to Sleep Request	Sleep Request command	POWER_MODE = 1011
	autonomous power-down	no frame transmission or reception for longer than $t_{to(pd)autn}$ AND AUTO_PWD = 1
	LPS code group received	LPS_WUR_DIS = 0 (LPS/WUR enabled) AND LPS_RECEIVED = 1 AND $t > t_{to(req)sleep}$ AND LPS_ACTIVE = 1
	no data detected on MDI or MII	pcs_rx_dv = FALSE AND TXEN = LOW
	sleep acknowledge timer enabled	SLEEP_ACK = 1
Sleep Request to Normal	Normal mode command	POWER_MODE = 0011
	wake-up request	(FWDPHYREM = 1 and WAKEUP = 1) OR WUR symbols received at the bus pins
	sleep acknowledge timer disabled	SLEEP_ACK = 0
	sleep acknowledge time-out time not expired	$t < t_{to(ack)sleep}$
	data detected on MDI or MII	pcs_rx_dv = TRUE OR TXEN = HIGH
	LPS enabled	LPS_WUR_DIS = 0
	sleep request timer expired	$t > t_{to(req)sleep}$
Normal to Normal	data detected on MDI or MII	pcs_rx_dv = TRUE OR TXEN = HIGH
	sleep acknowledge timer disabled	SLEEP_ACK = 0
Sleep Request to Sleep	LPS disabled	LPS_WUR_DIS = 1
	sleep request timer expired	$t > t_{to(req)sleep}$
Sleep Request to Silent	LPS enabled	LPS_WUR_DIS = 0
Standby to Normal	autonomous operation	see Section 6.6



1. UV means undervoltage on one of the power supply pins $V_{DD(IO)}$, $V_{DDA(3V3)}$, $V_{DDD(1V8)}$, $V_{DDD(3V3)}$.
2. INH can be configured to be on or off.
3. The PHY will not be in Sleep mode, and cannot be woken up, until the timeout associated with the transition has expired (after $t_{to(req)sleep}$).
4. At power-on, after a transition from Power-off to Standby mode, undervoltage detection timeout is enabled once all supply voltages are available. When an undervoltage is detected, the TJA1101B switches to Sleep mode after $t_{to(uvd)}$.

Figure 7. Mode transition diagram

6.5 Sleep and wake-up forwarding concept

The sleep and wake-up forwarding concept of the TJA1101B is compliant with the OPEN Alliance Sleep/Wake-up specification. The TJA1101B features a wake-up request forwarding function that enables fast wake-up forwarding without the need for a switch, MAC or μC action. The wake-up forwarding principle is illustrated in Figure 8. The wake-up request can be forwarded via non-active (gray PHYs in the figure) or active links (white PHY). In the case of a non-active link, a wake-up pulse (WUP; duration $t_{w(wake)}$) is transmitted, to be detected as activity at the link partner. For an active link, wake up request (WUR) scrambler code groups are sent.

The wake-up behavior of the PHY can be configured. This arrangement allows WAKE_IN_OUT to be used as a local wake-up or to have a mixed system with only some ports forwarding wake-up requests. The following configuration options are available and are selected via the SMI Configuration register 1 (Table 21):

REMWUPHY determines whether the PHY reacts to a remote wake-up request.

FWDPHYREM determines whether the PHY forwards a wake-up request (via WAKE_IN_OUT) to its MDI. A WUP or WUR is sent, depending on the link status.

LOCWUPHY determines whether the PHY should be woken up in response to a local wake-up event (forwarded via WAKE_IN_OUT)

FWDPHYLOC determines whether a wake-up event should be forwarded to other ports (i.e. should the WAKE_IN_OUT signal be activated).

The WAKE_IN_OUT signal features a programmable timeout to enable it to support a number of wake-up concepts (e.g. wake-up line). It reacts on a rising edge.

The wake-up detection time, $t_{det(wake)}$ (see Table 37) on pin WAKE_IN_OUT is determined by register bit settings LOC_WU_TIM (see Table 30). The wake-up pulse duration (t_p; see Table 37) is also determined by LOC_WU_TIM.

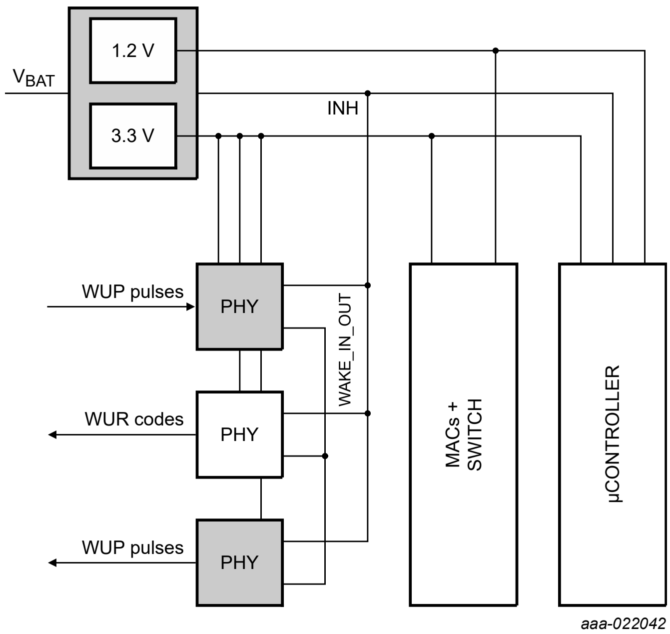


Figure 8. Wake-up request forwarding

6.6 Autonomous operation

When the TJA1101B is configured for autonomous operation (either via pin strapping, see Section 6.10, or via bit AUTO_OP in the Common configuration register, Table 30), it can operate and establish a link without further interaction with a host controller. On power-on or wake-up from Sleep mode, the TJA1101B goes directly to Normal mode once all supply voltages are available and the link-up process starts automatically. Host configuration (e.g. for link or mode control) will not be possible until the device is switched from autonomous to managed operation by resetting bit AUTO_OP.

6.7 Autonomous power-down

If autonomous power-down is enabled for the PHY (AUTO_PWD = 1), it goes to Sleep Request mode automatically if no Ethernet frames have been received at the MDI and (R)MII within the timeout time, $t_{to(pd)autn}$.

6.8 Test modes

Five test modes are supported. Only test modes 1, 2, 4 and 5 are included in the 100BASE-T1 specification [1]. The test modes can be selected individually via an SMI command in Normal mode while link control is disabled. Pin RXER is used as a reference clock output for test modes 1 to 4 (the nominal RXER function is disabled when test modes are active). No load should be connected when the reference clock is being measured.

6.8.1 Test mode 1

Test mode 1 is used to test transmitter droop. In Test mode 1, the PHY transmits '+1' symbols for 600 ns followed by '-1' symbols for a further 600 ns. This sequence is repeated continuously.

6.8.2 Test mode 2

Test mode 2 is used to test transmitter timing jitter in Master mode. In Test mode 2, the PHY transmits the data symbol sequence {+1, -1} repeatedly. The transmission of the symbols is synchronized with the local external oscillator.

6.8.3 Test mode 3

Test mode 3 is used to test transmitter timing jitter in Slave mode. In Test mode 3, the PHY transmits the data symbol sequence {+1, -1} repeatedly. The transmission of the symbols is synchronized with the local external oscillator.

6.8.4 Test mode 4

Test mode 4 is used to test transmitter distortion. In Test mode 4, the PHY transmits the sequence of symbols generated by the scrambler polynomial gs1 = 1 + x9 + x11.

The bit sequence x0n, x1n is derived from the scrambler according to the following equations:

$$x0n = Scrn[0]$$

$$x1n = Scrn[1] \text{ XOR } Scrn[1]$$

This stream of 3-bit nibbles is mapped to a stream of ternary symbols according to Table 9.

Table 9. Symbol mapping in test mode 4

x1n	x0n	PAM-3 transmit symbol
0	0	0
0	1	+1
1	0	0
1	1	-1

6.8.5 Test mode 5

Test mode 5 is used to test the transmit PSD mask. In Test mode 5, the PHY transmits a random sequence of PAM-3 symbols.

6.8.6 Slave jitter test

To enable the Slave jitter test in Normal mode, bit SLAVE_JITTER_TEST must be set to 1 before link control is enabled (LINK_CONTROL = 1; see Table 20). During this test, the transmitter reference clock is fed to pin TXCLK.

6.9 Error diagnosis

6.9.1 Undervoltage detection

The TJA1101B continuously monitors the status of the supply voltages. Once a supply voltage drops below the specified minimum operating threshold, the TJA1101B enters the fail-silent Standby mode and communication is halted. If an undervoltage is detected on V_{BAT}, the TJA1101B switches to Power-off mode.

At power-on, after a transition from Power-off to Standby mode, undervoltage detection timeout is enabled once all supply voltages are available. The timeout timer is started when an undervoltage is detected. If the undervoltage is still active when the timer expires (after $t_{to(uvd)}$), the TJA1101B switches from Standby mode to Sleep mode.

The microcontroller can determine the source of the interruption by reading the contents of the External status register (Table 28). The under-voltage detection/recovery range is positioned immediately next to the operating range, without a gap. Since parameters are specified down to the minimum value of the under-voltage detection threshold, it is guaranteed that the behavior of the TJA1101B is fully specified and defined for all possible voltage condition on the supply pins.

6.9.2 Cabling errors

The TJA1101B can detect open and short circuits between the twisted-pair bus lines when neither of the link partners is transmitting (link control disabled). It may make sense to run the diagnostic before establishing the Ethernet link. When bit CABLE_TEST in the Extended Control register (Table 20) is set to 1, test pulses are transmitted onto the transmission medium with a repetition rate of 666.6 kHz. The TJA1101B evaluates the reflected signals and uses impedance mismatch data along the channel to determine the quality of the link. The results of the cable test are available in the External status register

(Table 28) within $t_{to(cbl\_tst)}$. The tests performed and associated results are summarized in Table 10.

Table 10. Cable tests and results

The cable bus lines are designated BI_DA+ and BI_DA-, in alignment with 100BASE-T1 [1].

BI_DA+	BI_DA-	Result
open	open	open detected
+ shorted to -	- shorted to +	short detected
shorted to V_{DD}	open	open detected
open	shorted to V_{DD}	open detected
shorted to V_{DD}	shorted to V_{DD}	short detected
shorted to GND	open	open detected
open	shorted to GND	open detected
shorted to GND	shorted to GND	short detected
connected to active link partner (master)	connected to active link partner (master)	short and open detected

6.9.3 Link stability

The Signal Quality Indicator (SQI) is the parameter used to estimate link stability. The PMA receive function monitors the SQI. Once the value falls below a configurable threshold (SQI_FAILLIMIT), the link status is set to FAIL and communication is interrupted. The TJA1101B allows for adjusting the sensitivity of the PMA receive function by configuring this threshold. The microcontroller can always check the current value of the SQI via the SMI, allowing it to track a possible degradation in link stability.

6.9.4 Link-fail counter

High losses and/or a noisy channel may cause the link to shut down when reception is no longer reliable. In such cases, the PHY generates a LINK_STATUS_FAIL interrupt. Retraining of the link begins automatically provided link control is enabled (LINK_CONTROL = 1).

Bits LOC_RCVR_COUNTER and REM_RCVR_COUNTER in the Link-fail counter register (Table 29) are incremented after every link fail event. Both counters are reset when this register is read.

6.9.5 Jabber detection

The Jabber detection function prevents the PHY being locked in the DATA state of the PCS Receive state diagram when the End-of-Stream Delimiters, ESD1 and ESD2, are not detected.

The maximum time the PHY can reside in the DATA state is limited to $t_{to(PCS-RX)}$ (rcv_max_timer in the IEEE specification [1]). After this time, the PCS-RX state machine is reset, triggering a transition to PHY Idle state.

6.9.6 Polarity detection

A polarity error occurs when the two signal wires in the twisted pair cable are swapped. According to the IEEE specification [1], the polarity is always observed to be correct by the Master PHY; only the Slave is allowed to correct the polarity. When the TJA1101B is in Slave configuration, it can detect if the ternary symbols sent from the Master PHY are received with the wrong polarity and will correct this error internally and set the POLARITY_DETECT bit in the External status register (Table 28). Irrespective of the Master or Slave mode, the host can overwrite and swap the default MDI polarity by setting MDI_POL in Configuration Register 3 (Table 31).

6.9.7 Interleave detection

A 100BASE-T1 PHY can send two different interleave sequences of ternary symbols (TAn, TBn) or (TBn, TAn). The receivers in the TJA1101B are able to de-interleave both sequences. The order of the ternary symbols detected by the receiver is indicated by the INTERLEAVE_DETECT bit in the External status register (Table 28).

6.9.8 Loopback modes

The TJA1101B supports three loopback modes:

- Internal loopback (PCS loopback in accordance with IEEE 802.3bw)
- External loopback
- Remote loopback

To run the PHY in loopback mode, the LOOPBACK control bit in the Basic control register should be set before enabling link control.

6.9.8.1 Internal loopback

In Internal loopback mode, the PCS receive function gets the ternary symbols A_n and B_n directly from the PCS transmit function as shown in Figure 9. This action allows the MAC to compare packets sent through the MII transmit function with packets received from the MII receive function and, therefore, to validate the functionality of the 100BASE-T1 PCS function.

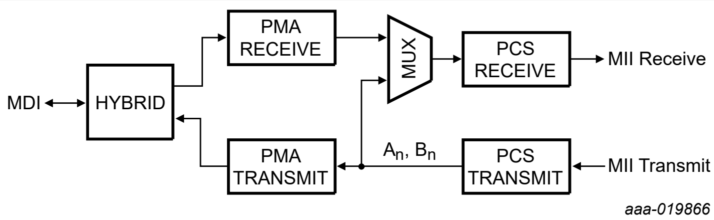


Figure 9. Internal loopback

6.9.8.2 External loopback

In External loopback mode, the PMA receive function receives signals directly from the PMA transmit function as shown in Figure 10. This external loopback test allows the MAC to compare packets sent through the MII transmit function with packets received from the MII receive function and, therefore, to validate the functionality of the 100BASE-T1 PCS and PMA functions.

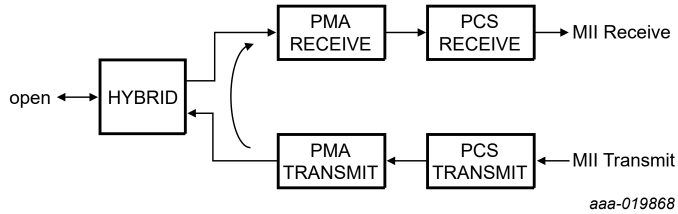


Figure 10. External loopback

6.9.8.3 Remote loopback

In Remote loopback mode, the packet received by the link partner at the MDI is passed through the PMA receive and PCS receive functions and forwarded to the PCS transmit function, which in turn sends it back to the link partner from where it came. The PCS receive data is made available at the MII. Remote loopback allows the MAC to compare the packets sent to the MDI with the packets received back from the MDI and, therefore, to validate the functionality of the physical channel, including both 100BASE-T1 PHYs.

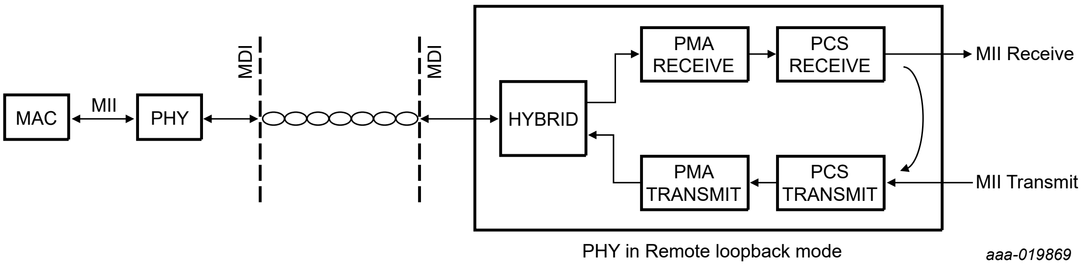


Figure 11. Remote loopback

6.10 Hardware configuration

A number of pins are provided to allow default values for a number of features to be hardware-configured, without microcontroller interaction. The pull-up/down behavior of these pins is sensed at power-up and after a reset. A pull-up behavior is coded as logic 1, while a pull-down behavior is coded as logic 0. The results are stored in the corresponding SMI registers. All pre-configuration settings (except for the PHY addresses) can be overwritten via SMI commands.

Pin strapping at pins 23 (PHYAD2) and 24 (PHYAD1) determines bits 2 and 1, respectively, of the PHY address used for the SMI address/Cipher scrambler. The PHY address cannot be changed once the PHY has been configured. Besides the address configured via pin strapping, the TJA1101B can always be accessed via address 0.

Table 11 gives an overview of the functions to be configured via hardware pins.

Table 11. Pin strapping configuration

Symbol	Pin	Value	Description
MASTER_SLAVE	22 (CONFIG0)	0	PHY configured as Slave
		1	PHY configured as Master
AUTO_OP	21 (CONFIG1)	0	managed operation
		1	autonomous operation
MII_MODE	17 (CONFIG3) 18 (CONFIG2)	00	Normal MII mode
		01	RMII mode (50 MHz input on REF_CLK)
		10	RMII mode (50 MHz output on REF_CLK)
		11	Reverse MII mode
PHYAD[2:1]	23 (PHYAD2)	-	bit 2 of PHY address used for the SMI
	24 (PHYAD1)	-	bit 1 of PHY address used for the SMI
LDO_MODE	4 (SEL_1V8)	0	internal 1.8 V LDO enabled
		1	external 1.8 V supply

6.11 SMI registers

6.11.1 Register mapping overview

Table 12. SMI register mapping

Register index (dec)	Register name	Group
0	Basic control register	Basic
1	Basic status register	Basic
2	PHY identification register 1	Extended
3	PHY identification register 2	Extended
15	Extended status register	Extended
16	PHY identification register 3	NXP specific
17	Extended control register	NXP specific
18	Configuration register 1	NXP specific
19	Configuration register 2	NXP specific
20	Symbol error counter register	NXP specific
21	Interrupt source register	NXP specific
22	Interrupt enable register	NXP specific
23	Communication status register	NXP specific
24	General status register	NXP specific
25	External status register	NXP specific
26	Link-fail counter register	NXP specific
27	Common configuration register	NXP specific
28	Configuration register 3	NXP specific

Table 13. Register notation

Notation	Description
R/W	Read/write
R	Read only
LH	Latched HIGH; must be read out to reset
LL	Latched LOW; must be read out to reset
SC	Self-clearing
PS	Pin strapping

6.11.2 TJA1101B registers

Table 14. Basic control register (register 0)

Bit	Symbol	Access	Value	Description
15	RESET	R/W SC		software reset control:
			0[1]	normal operation
			1	PHY reset
14	LOOPBACK[2]	R/W		loopback control:
			0[1]	normal operation
			1	loopback mode
13	SPEED_SELECT (LSB)	R/W	[3]	speed select (LSB):
			0	10 Mbit/s if SPEED_SELECT (MSB) = 0 1000 Mbit/s if SPEED_SELECT (MSB) = 1
			1[1]	100 Mbit/s if SPEED_SELECT (MSB) = 0 reserved if SPEED_SELECT (MSB) = 1
12	AUTONEG_EN	R/W SC	0[1]	Auto negotiation not supported; always 0; a write access is ignored.
11	POWER_DOWN	R/W		Standby power down enable:
			0[1]	normal operation (clearing this bit automatically triggers a transition to Normal mode, provided control bits POWER_MODE are set to 0011 Normal mode, see Table 20)
			1	power down and switch to Standby mode (provided ISOLATE = 0; ignored if ISOLATE = 1 and CONTROL_ERR interrupt generated)
10	ISOLATE	R/W		PHY isolation:
			0[1]	normal operation
			1	isolate PHY from MII/RMII (provided POWER_DOWN = 0; ignored if POWER_DOWN = 1 and CONTROL_ERR interrupt generated)
9	RE_AUTONEG	R/W SC	0[1]	Auto negotiation not supported; always 0; a write access is ignored.
8	DUPLEX_MODE	R/W	1[1]	only full duplex supported; always 1; a write access is ignored.
7	COLLISION_TEST	R/W	0[1]	COL signal test not supported; always 0; a write access is ignored.
6	SPEED_SELECT (MSB)	R/W	[3]	speed select (MSB):
			0[1]	10 Mbit/s if SPEED_SELECT (LSB) = 0 100 Mbit/s if SPEED_SELECT (LSB) = 1
			1	1000 Mbit/s if SPEED_SELECT (LSB) = 0 reserved if SPEED_SELECT (LSB) = 1
5	UNIDIRECT_EN	R/W		unidirectional enable when bit 12 (AUTONEG_EN) = 0 and bit 8 (DUPLEX_MODE) = 1:

Table 14. Basic control register (register 0)*...continued*

Bit	Symbol	Access	Value	Description
			0[1]	enable transmit from MII only when the PHY has determined that a valid link has been established
			1	enable transmit from MII regardless of whether the PHY has determined that a valid link has been established
4:0	reserved	R/W	00000[1]	always write 00000; ignore on read

[1] Default value.
[2] The loopback mode is selected via bits LOOPBACK_MODE in the Extended control register (Table 20).
[3] Speed Select: 00: 10 Mbit/s; 01: 100 Mbit/s; 10: 1000 Mbit/s; 11: reserved; a write access value other than 01 is ignored.

Table 15. Basic status register (register 1)

Bit	Symbol	Access	Value	Description
15	100BASE-T4	R	0[1]	PHY not able to perform 100BASE-T4
			1	PHY able to perform 100BASE-T4
14	100BASE-X_FD	R	0[1]	PHY not able to perform 100BASE-X full-duplex
			1	PHY able to perform 100BASE-X full-duplex
13	100BASE-X_HD	R	0[1]	PHY not able to perform 100BASE-X half-duplex
			1	PHY able to perform 100BASE-X half-duplex
12	10Mbps_FD	R	0[1]	PHY not able to perform 10 Mbit/s full-duplex
			1	PHY able to perform 10 Mbit/s full-duplex
11	10Mbps_HD	R	0[1]	PHY not able to perform 10 Mbit/s half-duplex
			1	PHY able to perform 10 Mbit/s half-duplex
10	100BASE-T2_FD	R	0[1]	PHY not able to perform 100BASE-T2 full-duplex
			1	PHY able to perform 100BASE-T2 full-duplex
9	100BASE-T2_HD	R	0[1]	PHY not able to perform 100BASE-T2 half-duplex
			1	PHY able to perform 100BASE-T2 half-duplex
8	EXTENDED_STATUS	R	0	no extended status information in register 15h
			1[1]	extended status information in register 15h
7	UNIDIRECT_ ABILITY	R	0	PHY able to transmit from MII only when the PHY has determined that a valid link has been established
			1[1]	PHY able to transmit from MII regardless of whether the PHY has determined that a valid link has been established
6	MF_PREAMBLE_SUPPRESSION	R	0	PHY will not accept management frames with preamble suppressed
			1[1]	PHY will accept management frames with preamble suppressed
5	AUTONEG_COMPLETE	R	0	Autonegotiation process not completed
			1[1]	Autonegotiation process completed
4	REMOTE_FAULT	R LH	0[1][2]	no remote fault condition detected
			1	remote fault condition detected

Table 15. Basic status register (register 1)*...continued*

Bit	Symbol	Access	Value	Description
3	AUTONEG_ABILITY	R	0[1]	PHY not able to perform Autonegotiation
			1	PHY able to perform Autonegotiation
2	LINK_STATUS	R LL	0[1][2][3]	link is down
			1	link is up
1	JABBER_DETECT	R LH	0[1][2]	no jabber condition detected
			1	jabber condition detected
0	EXTENDED_CAPABILITY	R	0	basic register set capabilities only
			1[1]	extended register capabilities

[1] Default value.
[2] Reset to default value when link control is disabled (LINK_CONTROL = 0).
[3] According to IEEE 802.3; LINK_STATUS = 1 when LOC_RCVR_STATUS = 1.

Table 16. PHY identification register 1 (register 2)

Bit	Symbol	Access	Value	Description
15:0	PHY_ID	R	0180h[1]	bits 3 to 18 of the Organizationally Unique Identifier (OUI)[2]

[1] Default value.
[2] OUI = 00.60.37h.

Table 17. PHY identification register 2 (register 3)

Bit	Symbol	Access	Value	Description
15:10	PHY_ID	R	110111[1]	bits 19 to 24 of the OUI[2]
9:4	TYPE_NO	R	010000	six-bit manufacturer’s type number
3:0	REVISION_NO	R	0010[1]	four-bit manufacturer’s revision number

[1] Default value.
[2] OUI = 00.60.37h.

Table 18. PHY identification register 3 (Register 16)

Bit	Symbol	Access	Value	Description
15:8	reserved	R	-	
7:0	VERSION_NO	R	xxh[1]	8-bit manufacturer's firmware revision number

[1] Default value.

Table 19. Extended status register (register 15)

Bit	Symbol	Access	Value	Description
15	1000BASE-X_FD	R	0[1]	PHY not able to perform 1000BASE-X full-duplex
			1	PHY able to perform 1000BASE-X full-duplex

Table 19. Extended status register (register 15)*...continued*

Bit	Symbol	Access	Value	Description
14	1000BASE-X_HD	R	0[1]	PHY not able to perform 1000BASE-X half-duplex
			1	PHY able to perform 1000BASE-X half-duplex
13	1000BASE-T_FD	R	0[1]	PHY not able to perform 1000BASE-T full-duplex
			1	PHY able to perform 1000BASE-T full-duplex
12	1000BASE-T_HD	R	0[1]	PHY not able to perform 1000BASE-T half-duplex
			1	PHY able to perform 1000BASE-T half-duplex
11:8	reserved	R	0000[1]	always 0000; ignore on read
7	100BASE-T1	R	0	PHY not able to 1-pair 100BASE-T1 100 Mbit/s
			1[1]	PHY able to 1-pair 100BASE-T1 100 Mbit/s
6	1000BASE-RTPGE	R	0[1]	PHY not able to support RTPGE
			1	PHY supports RTPGE
5:0	reserved	R	-	ignore on read

[1] Default value.

Table 20. Extended control register (register 17)

Bit	Symbol	Access	Value	Description
15	LINK_CONTROL	R/W	[1]	link control enable:
			0	link control disabled
			1	link control enabled
14:11	POWER_MODE	R/W	[2]	operating mode select:
			0000[3]	no change
			0011	Normal mode (command)
			1001	Silent mode (read only)
			1010	Sleep mode (read only)
			1011	Sleep Request mode (command)
			1100	Standby mode (command)
10	SLAVE_JITTER_TEST[4]	R/W		enable/disable Slave jitter test
			0[3]	disable Slave jitter test
			1	enable Slave jitter test
9	TRAINING_RESTART	R/W SC		Autonegotiation process restart:
			0[3]	halts the training phase
			1	forces a restart of the training phase
8:6	TEST_MODE[4]	R/W		test mode selection:
			000[3]	no test mode
			001	100BASE-T1 test mode 1
			010	100BASE-T1 test mode 2

Table 20. Extended control register (register 17)*...continued*

Bit	Symbol	Access	Value	Description
			011	test mode 3
			100	100BASE-T1 test mode 4
			101	100BASE-T1 test mode 5
			110	scrambler and descrambler bypassed
			111	reserved; ignore on read
5	CABLE_TEST	R/W SC		TDR-based cable test:
			0[3]	stops TDR-based cable test
			1	forces TDR-based cable test
4:3	LOOPBACK_MODE[4][5]	R/W		loopback mode select:
			00[3]	internal loopback
			01	external loopback
			10	external loopback
			11	remote loopback
2	CONFIG_EN	R/W	[3]	configuration register access:
			0[3]	configuration register access disabled
			1	configuration register access enabled
1	reserved	R/W	-	ignore on read
0	WAKE_REQUEST	SC		wake-up request configuration:
			0[3]	no wake-up signal to be transmitted
			1	LINK_CONTROL = 0: transmit idle symbols as bus wake-up request LINK_CONTROL = 1: transmit WUR symbols

[1] Default value is 0 when AUTO_OP = 0; default value is 1 when AUTO_OP = 1.
[2] Any other value generates a CONTROL_ERR interrupt.
[3] Default value.
[4] Link control must be disabled (LINK_CONTROL = 0) before entering this mode.
[5] The selected loopback mode is enabled when bit LOOPBACK in the Basic control register (Table 14) is set to 1.

Table 21. Configuration register 1 (register 18)

Bit	Symbol	Access	Value	Description
15	MASTER_SLAVE	R/W	[1]	PHY Master/Slave configuration:
			0	PHY configured as Slave
			1	PHY configured as Master
14	FWDPHYLOC	R/W	[2]	local wake-up forwarding:
			0	wake-up event not forwarded locally
			1[3]	wake-up event forwarded locally
13:12	reserved	R/W	-	ignore on read
11	REMWUPHY	R/W	[2]	remote wake-up:

Table 21. Configuration register 1 (register 18)...*continued*

Bit	Symbol	Access	Value	Description
			0	PHY does not react to a remote wake-up
			1[3]	PHY reacts to a remote wake-up
10	LOCWUPHY	R/W	[2] [4]	local wake-up:
			0	PHY does not react to a local wake-up
			1[3]	PHY reacts to a local wake-up
9:8	MII_MODE	R/W	[1]	MII mode:
			00	MII mode enabled
			01	RMII mode enabled (50 MHz input on REF_CLK)
			10	RMII mode enabled (50 MHz output on REF_CLK)
			11	Reverse MII mode
7	MII_DRIVER	R/W		MII output driver strength:
			0[3]	standard
			1	reduced
6	SLEEP_CONFIRM	R/W		sleep confirmation setting:
			0[3]	no confirmation needed from another PHY before going to sleep
			1	confirmation needed from another PHY before going to sleep
5	LPS_WUR_DIS	R/W		LPS/WUR setting:
			0[3]	LPS/WUR enabled
			1	LPS/WUR disabled
4	SLEEP_ACK	R/W		sleep acknowledge:
			0[3]	sleep acknowledge timer disabled; auto-transition back from Sleep Request mode to Normal mode enabled during data transmission on MII or MDI
			1	sleep acknowledge timer enabled; auto-transition back from Sleep Request mode to Normal mode disabled during data transmission on MII or MDI
3	reserved	R/W	-	ignore on read
2	FWDPHYREM	R/W	[2]	remote wake-up forwarding:
			0	remote wake-up event not forwarded
			1[3]	remote wake-up event forwarded
1	AUTO_PWD	R/W		autonomous power down:
			0[3]	autonomous power-down disabled
			1	autonomous power-down enabled
0	LPS_ACTIVE	R/W		LPS code group reception:
			0	automatic transition from Normal to Sleep Request when LPS code group received disabled

Table 21. Configuration register 1 (register 18)*...continued*

Bit	Symbol	Access	Value	Description
			1[3]	automatic transition from Normal to Sleep Request when LPS code group received enabled

[1] Default value determined by pin strapping (see Section 6.10).
[2] Clear bits FWDPHYLOC, REMWUPHY, LOCWUPHY and FWDPHYREM if the corresponding wake-up/forwarding feature is not being used.
[3] Default value.
[4] Setting LOCWUPHY has an activation time of $t_{det(wake)}$. If a wake-up occurs within the activation time, it may not be detected.

Table 22. Configuration register 2 (register 19)

Bit	Symbol	Access	Value	Description
15:11	PHYAD[4:0]	R	[1]	PHY address used for the SMI address and for initializing the Cipher scrambler key: PHYAD[4:3] is set to 00 PHYAD[2:1] is predetermined by the hardware configuration straps on pins 23 and 24 respectively PHYAD[0] set to 0
10:9	SQI_AVERAGING	R/W	[2]	Signal Quality Indicator (SQI) averaging:
			00	SQI averaged 32 symbols
			01[3]	SQI averaged 64 symbols
			10	SQI averaged 128 symbols
			11	SQI averaged 256 symbols
8:6	SQI_WLIMIT	R/W		SQI warning limit:
			000	no warning limit
			001[3]	class A SQI warning limit
			010	class B SQI warning limit
			011	class C SQI warning limit
			100	class D SQI warning limit
			101	class E SQI warning limit
			110	class F SQI warning limit
			111	class G SQI warning limit
5:3	SQI_FAILLIMIT	R/W		SQI fail limit:
			000[3]	no fail limit
			001	class A SQI fail limit
			010	class B SQI fail limit
			011	class C SQI fail limit
			100	class D SQI fail limit
			101	class E SQI fail limit
			110	class F SQI fail limit
			111	class G SQI fail limit
2	JUMBO_ENABLE	R/W		Jumbo packet support:

Table 22. Configuration register 2 (register 19)...continued

Bit	Symbol	Access	Value	Description
			0	packets up to 4 kB supported
			1[3]	packets up to 16 kB supported
1:0	SLEEP_REQUEST_TO	R/W	[4]	sleep request/acknowledge timeout:
			00	0.4 ms/0.2 ms
			01[3]	1 ms/0.5 ms
			10	4 ms/2 ms
			11	16 ms/8 ms

[1] Default value determined by pin strapping (see Section 6.10.
[2] The SQI is derived from the actual internal slicer margin and includes filtering. Averaging the SQI value itself does not, therefore, have any added value.
[3] Default value.
[4] The specified values are nominal settings; see parameters $t_{to(req)sleep}$ and $t_{to(ack)sleep}$, respectively, for the limits.

Table 23. Symbol error counter register (register 20)

Bit	Symbol	Access	Value	Description
15:0	SYM_ERR_CNT	R	0000h[1]	The symbol error counter is incremented when an invalid code symbol is received (including idle symbols). The counter is incremented only once per packet, even when the received packet contains more than one symbol error. This counter increments up to 2^{16}. When the counter overflows, the value FFFFh is retained. The counter is reset when the register is read.

[1] Default value. Bits NOT reset to default value when link control is disabled (LINK_CONTROL = 0).

Table 24. Interrupt source register (register 21)

Bit	Symbol	Access	Value	Description
15	PWON	R LH	0[1]	power-on not detected
			1	power-on detected
14	WAKEUP	R LH	0[1][2]	no local or remote wake-up detected
			1	local or remote wake-up detected
13	WUR_RECEIVED	R LH	0[1]	no dedicated wake-up request detected
			1	dedicated wake-up request detected
12	LPS_RECEIVED	R LH	0[1]	no LPS code groups received
			1	LPS code groups received
11	PHY_INIT_FAIL	R LH	0[1]	no PHY initialization error detected
			1	PHY initialization error detected
10	LINK_STATUS_FAIL	R LH	0[1][3]	link status not changed
			1	link status bit LINK_UP changed from 'link OK' to 'link fail'
9	LINK_STATUS_UP	R LH	0[1][3]	link status not changed
			1	link status bit LINK_UP changed from 'link fail' to 'link OK'

Table 24. Interrupt source register (register 21)*...continued*

Bit	Symbol	Access	Value	Description
8	SYM_ERR	R LH	0[1][3]	no symbol error detected
			1	symbol error detected
7	TRAINING_FAILED	R LH	0[1]	no training phase failure detected
			1	training phase failure detected
6	SQI_WARNING	R LH	0[1][3]	SQI value above warning limit
			1	SQI value below warning limit and bit LINK_UP set
5	CONTROL_ERR	R LH	0[1]	no SMI control error detected
			1	SMI control error detected
4	reserved	R	-	ignore on read
3	UV_ERR	R LH	0[1]	no undervoltage detected
			1	undervoltage detected on $V_{DD(IO)}$, $V_{DDD(3V3)}$, $V_{DDD(1V8)}$ or $V_{DDA(3V3)}$
2	UV_RECOVERY	R LH	0[1]	no undervoltage recovery detected
			1	undervoltage recovery detected
1	TEMP_ERR	R LH	0[1]	no overtemperature error detected
			1	overtemperature error detected
0	SLEEP_ABORT	R LH	0[1]	no transition from Sleep Request back to Normal as a result of the Sleep Request timer expiring
			1	transition from Sleep Request back to Normal as a result of the Sleep Request timer expiring

[1] Default value.

[2] Bit WAKEUP may be set when an undervoltage is detected on $V_{DD(IO)}$ in Sleep_Request mode. Ignore this bit when bit UV_VDDIO is set. Bit WAKEUP is reset by a read operation; however wake-up detection will not be enabled again until a state transition has been completed.

[3] Interrupts LINK_STATUS_FAIL, LINK_STATUS_UP, SYM_ERR and SQI_WARNING are cleared on entering Sleep Request mode, on entering Standby mode due to an undervoltage and when an undervoltage is detected in Standby mode.

Table 25. Interrupt enable register (register 22)

Disabling an interrupt source disables signaling at pin INT_N for that interrupt. However, the corresponding bit in the Interrupt source register (Table 24) remains active.

Bit	Symbol	Access	Value	Description
15	PWON_EN	R/W	0	PWON interrupt disabled
			1[1]	PWON interrupt enabled
14	WAKEUP_EN	R/W	0[1]	WAKEUP interrupt disabled
			1	WAKEUP interrupt enabled
13	WUR_RECEIVED_EN	R/W	0[1]	WUR_RECEIVED interrupt disabled
			1	WUR_RECEIVED interrupt enabled
12	LPS_RECEIVED_EN	R/W	0[1]	LPS_RECEIVED interrupt disabled
			1	LPS_RECEIVED interrupt enabled
11	PHY_INIT_FAIL_EN	R/W	0[1]	PHY_INIT_FAIL interrupt disabled

Table 25. Interrupt enable register (register 22)*...continued*

Disabling an interrupt source disables signaling at pin INT_N for that interrupt. However, the corresponding bit in the Interrupt source register (Table 24) remains active.

Bit	Symbol	Access	Value	Description
			1	PHY_INIT_FAIL interrupt enabled
10	LINK_STATUS_FAIL_EN	R/W	0[1]	LINK_STATUS_FAIL interrupt disabled
			1	LINK_STATUS_FAIL interrupt enabled
9	LINK_STATUS_UP_EN	R/W	0[1]	LINK_STATUS_UP interrupt disabled
			1	LINK_STATUS_UP interrupt enabled
8	SYM_ERR_EN	R/W	0[1]	SYM_ERR interrupt disabled
			1	SYM_ERR interrupt enabled
7	TRAINING_FAILED_EN	R/W	0[1]	TRAINING_FAILED interrupt disabled
			1	TRAINING_FAILED interrupt enabled
6	SQI_WARNING_EN	R/W	0[1]	SQI_WARNING interrupt disabled
			1	SQI_WARNING interrupt enabled
5	CONTROL_ERR_EN	R/W	0[1]	CONTROL_ERR interrupt disabled
			1	CONTROL_ERR interrupt enabled
4	reserved	R/W	0[1]	always write 0; ignore on read
3	UV_ERR_EN	R/W	0[1]	UV_ERR interrupt disabled
			1	UV_ERR interrupt enabled
2	UV_RECOVERY_EN	R/W	0[1]	UV_RECOVERY interrupt disabled
			1	UV_RECOVERY interrupt enabled
1	TEMP_ERR_EN	R/W	0[1]	TEMP_ERR interrupt disabled
			1	TEMP_ERR interrupt enabled
0	SLEEP_ABORT_EN	R/W	0[1]	SLEEP_ABORT interrupt disabled
			1	SLEEP_ABORT interrupt enabled

[1] Default value.

Table 26. Communication status register (register 23)

Bit	Symbol	Access	Value	Description
15	LINK_UP	R	0[1][2]	link failure
			1	link OK
14:13	TX_MODE	R	00[1][2]	transmitter disabled
			01	transmitter in SEND_N mode
			10	transmitter in SEND_I mode
			11	transmitter in SEND_Z mode
12	LOC_RCVR_STATUS	R LL	0[1][2]	local receiver not OK
			1	local receiver OK

Table 26. Communication status register (register 23)*...continued*

Bit	Symbol	Access	Value	Description
11	REM_RCVR_STATUS	R LL	0[1][2]	remote receiver not OK
			1	remote receiver OK
10	SCR_LOCKED	R	0[1][2]	descrambler unlocked
			1	descrambler locked
9	SSD_ERR	R LH	0[1][2]	no SSD error detected
			1	SSD error detected
8	ESD_ERR	R LH	0[1][2]	no ESD error detected
			1	ESD error detected
7:5	SQI	R	000[1][2]	worse than class A SQI (unstable link)
			001	class A SQI (unstable link)
			010	class B SQI (unstable link)
			011	class C SQI (good link)
			100	class D SQI (good link; bit error rate < 1e-10)
			101	class E SQI (good link)
			110	class F SQI (very good link)
			111	class G SQI (very good link)
4	RECEIVE_ERR	R LH	0[1][2]	no receive error detected
			1	receive error detected since register last read
3	TRANSMIT_ERR	R LH	0[1][2]	no transmit error detected
			1	transmit error detected since register last read
2:0	PHY_STATE	R	000[1]	PHY Idle
			001	PHY Initializing
			010	PHY Configured
			011	PHY Offline
			100	PHY Active
			101	PHY Isolate
			110	PHY Cable test
			111	PHY Test mode

[1] Default value.
[2] Reset to default value when link control is disabled (LINK_CONTROL = 0).

Table 27. General status register (register 24)

Bit	Symbol	Access	Value	Description
15	INT_STATUS	R	0[1]	all interrupts cleared
			1	unmasked interrupt pending

Table 27. General status register (register 24)...*continued*

Bit	Symbol	Access	Value	Description
14	PLL_LOCKED	R LL	0[1]	PLL unstable and not locked
			1	PLL stable and locked
13	LOCAL_WU	R LH	0[1][2]	no local wake-up detected
			1	local wake-up detected
12	REMOTE_WU	R LH	0[1][2]	no remote wake-up detected
			1	remote wake-up detected
11	DATA_DET_WU	R LH	0[1][3]	no 100BASE-T1 data detected at MDI or MII in Sleep Request mode
			1	100BASE-T1 data detected at MDI (pcs_rx_dv = TRUE; see [1]) or MII (TXEN = 1) in Sleep Request mode
10	EN_STATUS	R LH	0[1]	EN HIGH
			1	EN switched LOW since register last read
9	RESET_STATUS	R LH	0[1]	no hardware reset detected
			1	hardware reset detected since register last read
8	reserved	R	-	ignore on read
7:3	LINKFAIL_CNT	R	00000[1][4]	number of link fails since register last read
2:0	reserved	R	-	ignore on read

[1] Default value.
[2] Status bit is cleared by a read operation; however wake-up detection will not be enabled again until a state transition has been completed.
[3] Bit DATA_DET_WU may be set when an undervoltage is detected on $V_{DD(IO)}$ in Sleep_Request mode. Ignore this bit when bit UV_VDDIO is set.
[4] Bits NOT reset to default value when link control is disabled (LINK_CONTROL = 0).

Table 28. External status register (register 25)

Bit	Symbol	Access	Value	Description
15	UV_VDDD_3V3	R LH	0[1]	no undervoltage detected on pin $V_{DDD(3V3)}$
			1	undervoltage detected on pin $V_{DDD(3V3)}$
14	UV_VDDA_3V3	R LH	0[1]	no undervoltage detected on pin $V_{DDA(3V3)}$
			1	undervoltage detected on pin $V_{DDA(3V3)}$
13	UV_VDDD_1V8	R LH	0[1]	no undervoltage detected on pin $V_{DDD(1V8)}$
			1	undervoltage detected on pin $V_{DDD(1V8)}$
12	reserved	R	-	ignore on read
11	UV_VDDIO	R LH	0[1]	no undervoltage detected on pin $V_{DD(IO)}$
			1	undervoltage detected on pin $V_{DD(IO)}$
10	TEMP_HIGH	R LH	0[1]	temperature below high level
			1	temperature above high level
9	TEMP_WARN	R LH	0[1]	temperature below warning level
			1	temperature above warning level

Table 28. External status register (register 25)*...continued*

Bit	Symbol	Access	Value	Description
8	SHORT_DETECT	R LH	0[2]	no short circuit detected
			1	short circuit detected since register last read
7	OPEN_DETECT	R LH	0[2]	no open circuit detected
			1	open circuit detected since register last read
6	POLARITY_DETECT	R	0[2]	no polarity inversion detected at MDI
			1	polarity inversion detected at MDI
5	INTERLEAVE_DETECT	R	0[2]	interleave order of detected ternary symbols: TAn, TBn
			1	interleave order of detected ternary symbols: TBn, TAn
4:0	reserved	R	-	ignore on read

[1] Default value.
[2] Default value; bit NOT reset to default value when link control is disabled (LINK_CONTROL = 0).

Table 29. Link fail counter register (register 26)

Bit	Symbol	Access	Value	Description
15:8	LOC_RCVR_CNT	R	00h[1][2]	The counter is incremented when local receiver is NOT_OK; when the counter overflows, the value FFh is retained. The counter is reset when the register is read.
7:0	REM_RCVR_CNT	R	00h[1][2]	The counter is incremented when remote receiver is NOT_OK; when the counter overflows, the value FFh is retained. The counter is reset when the register is read.

[1] Default value.
[2] Bits NOT reset to default value when link control is disabled (LINK_CONTROL = 0).

Table 30. Common configuration register (register 27)

Bit	Symbol	Access	Value	Description
15	AUTO_OP	R/W	[1]	managed/autonomous operation:
			0	managed operation
			1	autonomous operation
14	reserved	R/W	-	ignore on read
13:12	CLK_MODE	R/W		clock mode:
			00[2]	25 MHz XTAL; no clock at CLK_IN_OUT
			01	25 MHz XTAL; 25 MHz output at CLK_IN_OUT
			10	25 MHz external clock at CLK_IN_OUT
			11	50 MHz input at REF_CLK; RMII mode only; no XTAL; no clock at CLK_IN_OUT
11	LDO_MODE	R/W	[1]	LDO mode:
			0	internal 1.8 V LDO enabled
			1	external 1.8 V supply

Table 30. Common configuration register (register 27)...continued

Bit	Symbol	Access	Value	Description
10	CLK_DRIVER	R/W		output driver strength on CLK_IN_OUT:
			0[2]	standard output driver strength at output of CLK_IN_OUT
			1	reduced output driver strength at output of CLK_IN_OUT
9	CLK_HOLD	R/W		local wake-up:
			0[2]	XTAL and CLK_IN_OUT output switched off in Sleep mode
			1	XTAL and CLK_IN_OUT output remain active until device switched to Sleep mode via SMI
8:7	LOC_WU_TIM	R/W		local wake-up timer:
			00[2]	longest (10 ms to 20 ms)
			01	long (250 μs to 500 μs)
			10	short (100 μs to 200 μs)
			11	shortest (10 μs to 40 μs)
6	CONFIG_WAKE	R/W		local wake configuration:
			0	absolute input threshold
			1[2]	ratiometric input threshold ($V_{DD(IO)}$)
5	CONFIG_INH	R/W		INH configuration:
			0	INH switched off in Disable mode
			1[2]	INH switched on in Disable mode
4:0	reserved	R/W	-	ignore on read

[1] Default value determined by pin strapping (see Section 6.10).
[2] Default value.

Table 31. Configuration register 3 (register 28)

Bit	Symbol	Access	Value	Description
15:3	reserved	R/W	-	ignore on read
2	MDI_POL	R/W		MDI polarity:
			0[1]	regular polarity: pin 12 = TRX_P; pin 13 = TRX_M
			1	swapped polarity: pin 12 = TRX_M; pin 13 = TRX_P
1	FORCE_SLEEP	R/W SC		forced sleep operation:
			0[1]	forced sleep inactive
			1	force PHY to Sleep mode
0	reserved	R/W	1[1]	always write 1; ignore on read

[1] Default value.

7 Limiting values

Table 32. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

Symbol	Parameter	Conditions		Min	Max	Unit
V_x	voltage on pin x[1]	on pin V_{BAT}		-0.3	+40	V
		on pin INH		-0.3	V_{BAT} + 0.3	V
		on pin WAKE_IN_OUT		-36	+42	V
		on pins $V_{DDA(3V3)}$, $V_{DDA(TX)}$, $V_{DDD(3V3)}$, $V_{DD(IO)}$, TRX_P, TRX_M		-0.3	+4.6	V
		on pins $V_{DDD(1V8)}$, XI, XO		-0.3	+2.5	V
		on input pins MDC, MDIO, RST_N, INT_N, EN, CLK_IN_OUT, SEL_1V8 and MII digital input pins		-0.3	min($V_{DD(IO)}$ + 0.3, +4.6)	V
		on digital output pins		-0.3	$V_{DD(IO)}$ + 0.3	V
$I_{O(INH)}$	output current on pin INH			-2	-	mA
V_{trt}	transient voltage	on pins WAKE_IN_OUT, V_{BAT}, TRX_P, TRX_M	[2]			
		pulse 1		-100	-	V
		pulse 2a		-	75	V
		pulse 3a		-150	-	V
		pulse 3b		-	100	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; 150 pF, 330 Ω	[3]			
		on pins TRX_P, TRX_M	[4]	-8.0	+8.0	kV
		on pin WAKE_IN_OUT	[5]	-8.0	+8.0	kV
		on pin V_{BAT} to GND	[6]	-8.0	+8.0	kV
		Human Body Model (HBM)				
		on any pin	[7]	-2.0	+2.0	kV
		on pins TRX_P, TRX_M		-6.0	+6.0	kV
		on pin WAKE_IN_OUT	[8]	-6.0	+6.0	kV
		on pin V_{BAT}	[9]	-6.0	+6.0	kV
		Charged Device Model (CDM)				
		on any pin	[10]	-500	+500	V
T_{amb}	ambient temperature			-40	+125	°C
T_{stg}	storage temperature			-55	+150	°C

[1] The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.
[2] Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO7637.
[3] Verified by an external test house according to IEC TS 62228, Section 4.3.
[4] Tested with a common mode choke and 100 nF coupling capacitors.
[5] Tested with 10 nF capacitor to GND and 10 kΩ in series between the capacitor and the WAKE_IN_OUT pin.
[6] Tested with 100 nF capacitor from V_{BAT} to GND.
[7] According to AEC-Q100-002.
[8] With 10 nF capacitor to GND and 10 kΩ in series between the capacitor and the WAKE_IN_OUT pin.
[9] With 100 nF from V_{BAT} to GND.
[10] According to AEC-Q100-011.

8 Thermal characteristics

Table 33. Thermal characteristics

Symbol	Parameter		Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	HVQFN36 package; in free air		
			LDO disabled (LDO_MODE = 1)	30	K/W
			LDO enabled (LDO_MODE = 0)	34	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	[2]	HVQFN36 package; in free air		
			LDO disabled (LDO_MODE = 1)	5	K/W
			LDO enabled (LDO_MODE = 0)	10	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package	[1]	HVQFN36 package; in free air		
			LDO disabled (LDO_MODE = 1)	2	K/W
			LDO enabled (LDO_MODE = 0)	7	K/W

[1] According to JEDEC JESD51-2, JESD51-5 and JESD51-7 at natural convection on 2s2p board. Board with two inner copper layers (thickness: 35 μm) and thermal via array under the exposed pad connected to the first inner copper layer.

[2] Determined using an isothermal cold plate.

9 Static characteristics

Table 34. Supply characteristics

T_{vj} = -40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)} = V_{DDA(TX)} = V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Battery supply: pin V_{BAT}						
V_{BAT}	battery supply voltage	operating range	3.1	-	36	V
V_{uvd}	undervoltage detection voltage		2.8	-	-	V
V_{uvr}	undervoltage recovery voltage		-	-	3.1	V
V_{uvhys}	undervoltage hysteresis voltage		15	100	-	mV
I_{BAT}	battery supply current	all modes except Sleep; V_{BAT} < 36 V; I_{INH} = 0 μA	-	-	2.0	mA
		Sleep mode; T_{vj} ≤ 85 °C; V_{BAT} < 7.4 V	-	130	300	μA
		Sleep mode; T_{vj} ≤ 85 °C; 7.4 V < V_{BAT} < 30 V	-	45	100	μA
		V_{BAT} < 40 V; I_{INH} = 0 μA	-	-	6	mA
3.3 V analog supply: pin $V_{DDA(3V3)}$						
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	operating range	3.1	3.3	3.5	V
V_{uvd}	undervoltage detection voltage		2.9	-	-	V
V_{uvr}	undervoltage recovery voltage		-	-	3.1	V
V_{uvhys}	undervoltage hysteresis voltage		50	80	-	mV
$I_{DDA(3V3)}$	analog supply current (3.3 V)	Normal/Sleep Request modes	-	21	27	mA

Table 34. Supply characteristics*...continued*

T_{vj} = -40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Standby mode	-	75	150	µA
		Disable/Reset modes	-	4	50	µA
3.3 V digital supply: pin $V_{DDD(3V3)}$						
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)	operating range	3.1	3.3	3.5	V
V_{uvd}	undervoltage detection voltage		2.9	-	-	V
V_{uvr}	undervoltage recovery voltage		-	-	3.1	V
V_{uvhys}	undervoltage hysteresis voltage		50	80	-	mV
$I_{DDD(3V3)}$	digital supply current (3.3 V)	Normal/Sleep Request modes; LDO_MODE = 0	-	50	60	mA
		Normal/Sleep Request modes; LDO_MODE = 1	-	2.5	4	mA
		Standby mode; LDO_MODE = 0	-	0.2	5	mA
		Disable/Reset modes	-	1	50	µA
1.8 V digital supply: pin $V_{DDD(1V8)}$						
$V_{DDD(1V8)}$	digital supply voltage (1.8 V)	operating range; LDO_MODE = 1	1.745	1.84	1.95	V
V_{uvd}	undervoltage detection voltage	LDO_MODE = 1	1.65	-	-	V
V_{uvr}	undervoltage recovery voltage	LDO_MODE = 1	-	-	1.745	V
V_{uvhys}	undervoltage hysteresis voltage	LDO_MODE = 1	20	35	-	mV
$I_{DDD(1V8)}$	digital supply current (1.8 V)	Normal/Sleep Request modes; LDO_MODE = 1 [1]	-	46	55	mA
Transmitter analog supply: pins $V_{DDA(TX)}$						
$V_{DDA(TX)}$	transmitter analog supply voltage	operating range	3.1	3.3	3.5	V
$I_{DDA(TX)}$	transmitter analog supply current	Normal/Sleep Request modes	-	27	33	mA
		Standby/Disable/Reset modes	-	0	50	µA
Input/output supply: pin $V_{DD(IO)}$						
$V_{DD(IO)}$	input/output supply voltage	operating range	3.1	3.3	3.5	V
V_{uvd}	undervoltage detection voltage		2.9	-	-	V
V_{uvr}	undervoltage recovery voltage		-	-	3.1	V
V_{uvhys}	undervoltage hysteresis voltage		50	80	-	mV
$I_{DD(IO)}$	input/output supply current	Normal/Sleep Request modes; C_{load} on MII pins = 15 pF [1]	-	5	7.5	mA
		Standby/Disable modes; no currents in pull-up resistors on digital inputs	-	3	25	µA
		Reset mode; no currents in pull-up resistors on digital inputs	-	35	80	µA

Table 34. Supply characteristics*...continued*

T_{vj} = -40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power consumption						
P	power dissipation	Normal/Sleep Request modes; LDO_MODE = 0	-	360	480	mW
		Normal/Sleep Request modes; LDO_MODE = 1	-	290	400	mW

[1] Not measured in production; guaranteed by design.

Table 35. xMI interfaces characteristics

T_{vj} = -40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SMI interface: pins MDC and MDIO						
V_{IH}	HIGH-level input voltage		2	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
C_i	input capacitance	pin MDC [1]	-	-	8	pF
		pin MDIO [1]	-	-	10	pF
V_{OH}	HIGH-level output voltage	pin MDIO; I_{OH} = -4 mA	$V_{DD(IO)}$ - 0.4	-	-	V
V_{OL}	LOW-level output voltage	pin MDIO; I_{OL} = 4 mA	-	-	0.4	V
I_{IH}	HIGH-level input current	V_{IH} = $V_{DD(IO)}$	-	-	20	µA
I_{IL}	LOW-level input current	pin MDC; V_{IL} = 0 V	-20	-	-	µA
		pin MDIO; V_i = 0 V	-100	-	-20	µA
R_{pd}	pull-down resistance	on pin MDC	262.5	500	-	kΩ
R_{pu}	pull-up resistance	on pin MDIO	70	100	130	kΩ
(R)MII interface: pins TXER, TXEN, TXDx, TXC, RXDx, RXDV, RXER, RXC						
V_{IH}	HIGH-level input voltage		2	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
C_i	input capacitance	[1]	-	-	8	pF
V_{OH}	HIGH-level output voltage	I_{OH} = -4 mA	$V_{DD(IO)}$ - 0.4	-	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 4 mA	-	-	0.4	V
I_{IH}	HIGH-level input current	V_{IH} = $V_{DD(IO)}$	-	-	200	µA
I_{IL}	LOW-level input current	V_{IL} = 0 V	-20	-	-	µA
R_{pd}	pull-down resistance	on pins TXER, TXEN, TXDx, TXDx	70	100	130	kΩ
		on pin TXC; Reverse MII mode	70	100	130	kΩ

[1] Not measured in production; guaranteed by design.

Table 36. General electrical characteristics

T_{vj} = -40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
pins RST_N, EN						
V_{IH}	HIGH-level input voltage		2	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
$V_{hys(i)}$	input hysteresis voltage		0.36	0.5	-	V
C_i	input capacitance	[1]	-	-	8	pF
I_{IH}	HIGH-level input current	at pin RST_N; V_{IH} = $V_{DD(IO)}$	-	-	20	μA
I_{IL}	LOW-level input current	at pin EN; V_{IL} = 0 V	-20	-	-	μA
R_{pd}	pull-down resistance	on pin EN	70	100	130	kΩ
R_{pu}	pull-up resistance	on pin RST_N	70	100	130	kΩ
pin INT_N						
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	-	-	0.4	V
pin SEL_1V8						
V_{IH}	HIGH-level input voltage		0.7 × $V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3 × $V_{DD(IO)}$	V
$V_{hys(i)}$	input hysteresis voltage		0.1 × $V_{DD(IO)}$	-	-	V
I_{IL}	LOW-level input current	V_{IL} = 0 V	-5	-	+5	μA
R_{pd}	pull-down resistance	on pin SEL_1V8	70	100	130	kΩ
pin CLK_IN_OUT						
V_{IH}	HIGH-level input voltage		0.7 × $V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.3 × $V_{DD(IO)}$	V
$V_{hys(i)}$	input hysteresis voltage		0.1 × $V_{DD(IO)}$	-	-	V
V_{OH}	HIGH-level output voltage	CLK_MODE = 01; I_{OH} = -4 mA	$V_{DD(IO)}$ - 0.4	-	-	V
V_{OL}	LOW-level output voltage	CLK_MODE = 01; I_{OL} = 4 mA	-	-	0.4	V
I_{IL}	LOW-level input current	CLK_MODE = 00 or 11; V_{IL} = 0 V	-5	-	+5	μA
R_{pd}	pull-down resistance	CLK_MODE = 00 or 11	70	100	130	kΩ
pins RXD[3:0], RXER, RXDV, during pin strapping						
V_{IH}	HIGH-level input voltage		2	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V

Table 36. General electrical characteristics*...continued*

T_{vj} = -40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
pin WAKE_IN_OUT						
V_{IH}	HIGH-level input voltage	CONFIG_WAKE = 0 (see Table 30)	2.8	-	4.1	V
		CONFIG_WAKE = 1	0.44 × $V_{DD(IO)}$	-	0.64 × $V_{DD(IO)}$	V
V_{IL}	LOW-level input voltage	CONFIG_WAKE = 0	2.4	-	3.75	V
		CONFIG_WAKE = 1	0.38 × $V_{DD(IO)}$	-	0.55 × $V_{DD(IO)}$	V
$V_{hys(i)}$	input hysteresis voltage	CONFIG_WAKE = 0	0.25	-	0.8	V
		CONFIG_WAKE = 1	0.025 × $V_{DD(IO)}$	-	0.2 × $V_{DD(IO)}$	V
I_i	input current		-5	-	+5	µA
V_{OH}	HIGH-level output voltage	all modes except Sleep and Power-off; $I_{WAKE\_IN\_OUT}$ = 0 mA	V_{BAT} - 0.8	-	V_{BAT}	V
I_{OL}	LOW-level output current	all modes except Sleep, Power-off; $V_{WAKE\_IN\_OUT}$ = 0 V	-30	-	-	mA
pin INH						
V_{OH}	HIGH-level output voltage	all modes except Sleep, Power-off; I_{INH} = -1 mA	V_{BAT} - 1	-	V_{BAT}	V
I_{OL}	LOW-level output current	all modes except Sleep, Power-off; V_{INH} = 0 V	-15	-7	-2	mA
I_L	leakage current	Sleep, Power-off modes	-5	-	+5	µA
pins XI, XO						
C_i	input capacitance	pin XI	-	3.5	-	pF
		pin XO [1]	-	2	-	pF
$g_{m(DC)}$	DC transconductance	Normal, Sleep Request modes; MII_MODE = 00, 01 or 11	13.3	25	47	mA/V
Transmitter test results: pins TRX_M, TRX_P[2]						
V_{droop}/V_M	droop voltage to peak voltage ratio	100BASE-T1 test mode 1; with respect to initial peak value [1]	-45	-	+45	%
$V_{dist(M)}$	peak distortion voltage	100BASE-T1 test mode 4 [1]	-	-	15	mV
PSDM	power spectral density mask	100BASE-T1 test mode 5 [1]				
		f = 1 MHz	-70.9	-	-63.3	dBm/Hz
		f = 20 MHz	-75.8	-	-64.8	dBm/Hz
		f = 40 MHz	-89.2	-	-68.5	dBm/Hz

Table 36. General electrical characteristics...*continued*

T_{vj} = -40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		f = 57 MHz to 200 MHz	-	-	-76.5	dBm/Hz
Transmitter output amplitude: pins TRX_M, RX_P[2]						
$V_{oM(TX)}$	transmitter peak output voltage		-	1	-	V
R_{term}	termination resistance	on each pin; Normal, Sleep Request modes; LINK_CONTROL = 1 [3]	47.5	50	52.5	Ω
Temperature protection						
$T_{j(sd)}$	shutdown junction temperature		180	-	200	°C
$T_{j(sd)rel}$	release shutdown junction temperature		147	-	167	°C
$T_{j(warn)}$	warning junction temperature		155	-	175	°C
$T_{j(warn)rel}$	release warning junction temperature		147	-	167	°C
$T_{j(warn)hys}$	warning junction temperature hysteresis		2	8	-	°C

[1] Not measured in production; guaranteed by design.
[2] Test carried out with external common mode choke and coupling capacitors connected.
[3] Including the resistance of an external common mode choke (average 3.5 Ω) with a 1 kΩ parallel resistor.

10 Dynamic characteristics

Table 37. Dynamic characteristics

T_{vj} = -40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
MII transmit timing (see Figure 12); MII_DRIVER = 0 (standard output driver strength)[1]						
T_{clk}	clock period	pin TXC	-	40	-	ns
δ	duty cycle	pin TXC	35	-	65	%
t_{WH}	pulse width HIGH	pin TXC	14	20	-	ns
t_{WL}	pulse width LOW	pin TXC	14	20	-	ns
t_{su}	set-up time	TXC to TXD[3:0], TXER, TXEN				
		MII	10	-	-	ns
		Reverse MII	10	-	-	ns
t_h	hold time	TXC to TXD[3:0], TXEN, TXER				
		MII	0	-	-	ns
		Reverse MII	10	-	-	ns
MII receive timing (see Figure 13); MII_DRIVER = 0 (standard output driver strength)[1]						
T_{clk}	clock period	pin RXC	-	40	-	ns

Table 37. Dynamic characteristics...*continued*

T_{vj} = -40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
δ	duty cycle	pin RXC	35	-	65	%
t_{WH}	pulse width HIGH	pin RXC	14	20	-	ns
t_{WL}	pulse width LOW	pin RXC	14	20	-	ns
t_d	delay time	RXC to RXD[3:0], RXDV, RXER				
		MII	15	-	25	ns
		Reverse MII	0	-	25	ns
RMII transmit and receive timing (see Figure 14 and Figure 15); MII_DRIVER = 0 (standard output driver strength)[1]						
T_{clk}	clock period	pin REF_CLK	-	20	-	ns
δ	duty cycle	pin REF_CLK	35	-	65	%
t_{WH}	pulse width HIGH	pin REF_CLK	7	10	-	ns
t_{WL}	pulse width LOW	pin REF_CLK	7	10	-	ns
t_{su}	set-up time	REF_CLK to TXD[1:0], TXEN, TXER	4	-	-	ns
t_h	hold time	REF_CLK to TXD[1:0], TXEN, TXER	2	-	-	ns
t_d	delay time	REF_CLK to RXD[1:0], RXER, CRSDV	4	-	13	ns
(R)MII interface timing[1]						
t_f	fall time[2]	MII: RXD[3:0], RXDV, RXER				
		MII_DRIVER = 0; C_L = 15 pF	1.3	-	5	ns
		MII_DRIVER = 1; C_L = 7.5 pF	2	-	7.7	ns
		MII: TXC, RXC; C_L = 15 pF	1.3	-	5	ns
		RMII: RXD[1:0], CRSDV, RXER				
		MII_DRIVER = 0; C_L = 15 pF	0.7	-	2.5	ns
		MII_DRIVER = 1; C_L = 7.5 pF	0.9	-	3.4	ns
		RMII: REF_CLK; C_L = 15 pF	0.7	-	2.5	ns
t_r	rise time[3]	MII: RXD[3:0], RXDV, RXER				
		MII_DRIVER = 0; C_L = 15 pF	1.3	-	5	ns
		MII_DRIVER = 1; C_L = 7.5 pF	2	-	7.7	ns
		MII: TXC, RXC; C_L = 15 pF	1.3	-	5	ns
		RMII: RXD[1:0], CRSDV, RXER				
		MII_DRIVER = 0; C_L = 15 pF	0.7	-	2.5	ns
		MII_DRIVER = 1; C_L = 7.5 pF	0.9	-	3.4	ns
		RMII: REF_CLK; C_L = 15 pF	0.7	-	2.5	ns
SMI timing (see Figure 16)[1]						
$T_{clk(MDC)}$	MDC clock period		400	-	-	ns
$t_{WH(MDC)}$	MDC pulse width HIGH		160	-	-	ns
$t_{WL(MDC)}$	MDC pulse width LOW		160	-	-	ns

Table 37. Dynamic characteristics*...continued*

T_{vj} = -40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)} = V_{DDA(TX)} = V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(MDIO)}$	MDIO set-up time	to rising edge on MDC	10	-	-	ns
$t_{h(MDIO)}$	MDIO hold time	from rising edge on MDC	10	-	-	ns
$t_{d(MDC-MDIO)}$	delay time from MDC to MDIO	from rising edge on MDC; read from PHY	0	-	300	ns
WAKE timing; pin WAKE_IN_OUT[1]						
$t_{det(wake)}$	wake-up detection time	LOC_WU_TIM = 00	10	-	20	ms
		LOC_WU_TIM = 01	250	-	500	μs
		LOC_WU_TIM = 10	100	-	200	μs
		LOC_WU_TIM = 11	20	-	40	μs
t_p	pulse duration	LOC_WU_TIM = 00	20	-	40	ms
		LOC_WU_TIM = 01	500	-	1000	μs
		LOC_WU_TIM = 10	200	-	400	μs
		LOC_WU_TIM = 11	40	-	80	μs
t_{on}	turn-on time	R_L = 100 kΩ; C_L = 50 pF; $V_{WAKE\_IN\_OUT}$ = 2 V	0	2	50	μs
t_{off}	turn-off time	R_L = 100 kΩ; C_L = 50 pF; $V_{WAKE\_IN\_OUT}$ = 2 V	5	50	65	μs
INH timing; pin INH[1]						
t_{on}	turn-on time	R_L = 100 kΩ; C_L = 50 pF; $V_{th(INH)}$ = 2 V	0	2	50	μs
t_{off}	turn-off time	R_L = 100 kΩ; C_L = 50 pF; $V_{th(INH)}$ = 2 V	5	50	65	μs
interrupt timing; pin INT_N[1]						
t_{on}	turn-on time	R_{pu} = 10 kΩ; C_L = 15 pF	8	-	20	μs
t_{off}	turn-off time	R_{pu} = 10 kΩ; C_L = 15 pF	8	-	20	μs
PCS-RX timeout timing						
$t_{to(PCS-RX)}$[4]	PCS-RX time-out time	Normal and Sleep Request modes				
		JUMBO_ENABLE = 0	-	1.1	-	ms
		JUMBO_ENABLE = 1	-	2.2	-	ms
Cable test timing						
$t_{to(cbl\_tst)}$	cable test time-out time	Normal mode; CABLE_TEST = 1	-	100	-	μs
pins RST_N, EN[1]						
$t_{det(rst)}$	reset detection time	on pin RSTN; $V_{uvd(VDDIO)} < V_{DD(IO)} \leq$ 3.5 V	5	-	20	μs
$t_{det(EN)}$	detection time on pin EN	$V_{uvd(VDDIO)} < V_{DD(IO)} \leq$ 3.5 V	5	-	20	μs
Transmitter test results						
$t_{jit(RMS)}$	RMS jitter time	Master mode	-	-	50	ps

Table 37. Dynamic characteristics*...continued*

T_{vj} = -40 °C to +150 °C; $V_{DD(IO)}$ = 2.9 V to 3.5 V; V_{BAT} = 2.8 V to 40 V; $V_{DDA(3V3)}$ = $V_{DDA(TX)}$ = $V_{DDD(3V3)}$ = 2.9 V to 3.5 V; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		Slave mode (with link); SLAVE_ JITTER_TEST = 1 [1] [5]	-	-	150	ps
Undervoltage detection[1]						
$t_{det(uv)}$	undervoltage detection time	on pin V_{BAT}; V_{BAT} = 2.7 V	0	-	30	µs
		on pin $V_{DDA(3V3)}$; $V_{DDA(3V3)}$ = 2.8 V	2	-	30	µs
		on pin $V_{DDD(3V3)}$; $V_{DDD(3V3)}$ = 2.8 V	2	-	30	µs
		on pin $V_{DDD(1V8)}$	2	-	30	µs
		$V_{DD(IO)}$ = 2.8 V	2	-	30	µs
$t_{rec(uv)}$	undervoltage recovery time	on pin $V_{DDA(3V3)}$; $V_{DDA(3V3)}$ = 3.2 V	2	-	30	µs
		on pin $V_{DDD(3V3)}$; $V_{DDD(3V3)}$ = 3.2 V	2	-	30	µs
		on pin $V_{DDD(1V8)}$	2	-	30	µs
		on pin $V_{DD(IO)}$; $V_{DD(IO)}$ = 3.2 V	2	-	30	µs
$t_{to(uvd)}$	undervoltage detection time-out time	for transition from Standby to Sleep mode (see Section 6.9.1)	300	-	670	ms
General timing parameters[1]						
$t_{s(pon)}$	power-on settling time	from power-on to Standby mode	-	-	2	ms
$t_{init(PHY)}$	PHY initialization time	from Standby mode to Normal mode	-	-	2	ms
$t_{to(req)sleep}$	sleep request time-out time	SLEEP_REQUEST_TO = 00	360	-	500	µs
		SLEEP_REQUEST_TO = 01	900	-	1150	µs
		SLEEP_REQUEST_TO = 10	3.6	-	4.4	ms
		SLEEP_REQUEST_TO = 11	14.4	-	17.6	ms
$t_{to(ack)sleep}$	sleep acknowledge time-out time	SLEEP_REQUEST_TO = 00	180	-	250	µs
		SLEEP_REQUEST_TO = 01	450	-	575	µs
		SLEEP_REQUEST_TO = 10	1.8	-	2.2	ms
		SLEEP_REQUEST_TO = 11	7.2	-	8.8	ms
$t_{det(PHY)}$	PHY detection time	on bus pins TRX_P, TRX_M	-	-	0.7	ms
$t_{to(pd)autn}$	autonomous power-down time-out time	Normal mode; AUTO_PWD = 1	1	-	2	s
t_{PD}	propagation delay	from MII to MDI; Normal mode	140	-	300	ns
		from MDI to MII; Normal mode	760	-	920	ns
		from RMII to MDI; Normal mode	190	-	540	ns
		from MDI to RMII; Normal mode	700	-	1070	ns
$t_{w(wake)}$	wake-up pulse width	Normal mode; no active link; wake-up forwarding	0.7	1.0	1.3	ms

[1] Not measured in production; guaranteed by design.
[2] From 2 V to 0.8 V.
[3] From 0.8 V to 2 V.

[4] rcv_max_timer in the IEEE specification [1].

[5] Measured at the RXER pin, representing the transmit clock (TX_CLK).

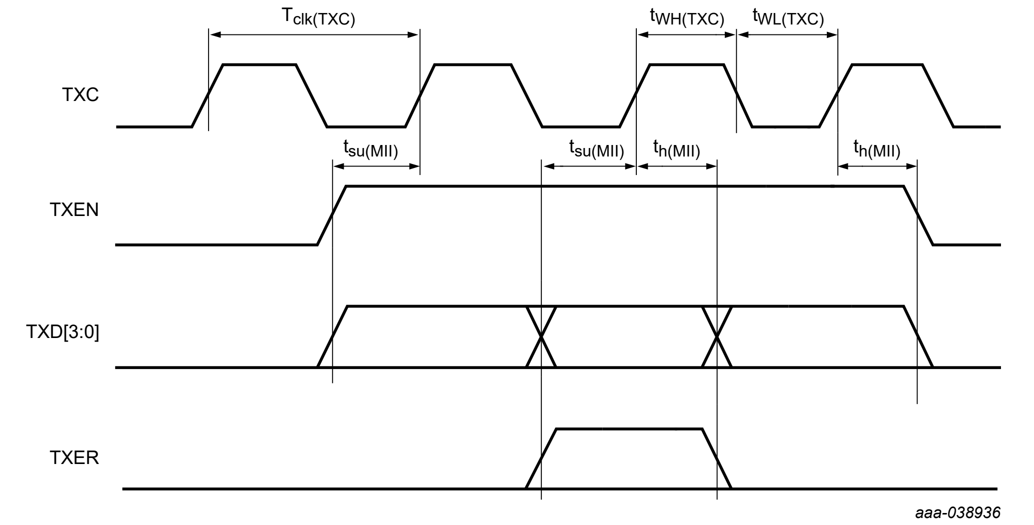


Figure 12. MII transmit timing diagram

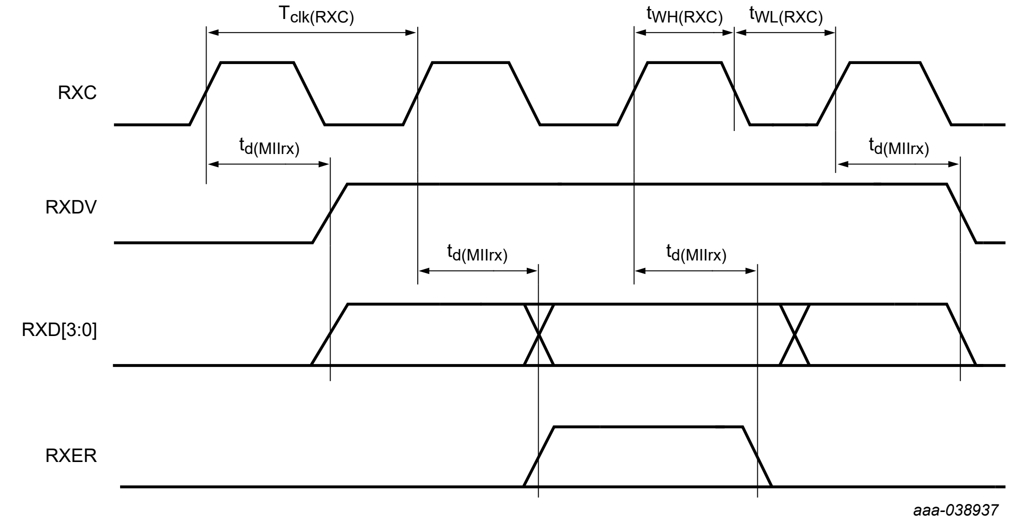


Figure 13. MII receive timing diagram

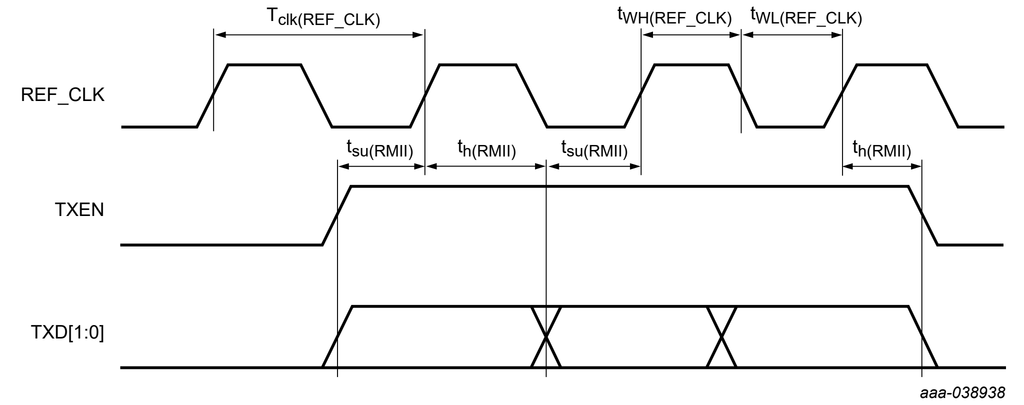


Figure 14. RMII transmit timing diagram

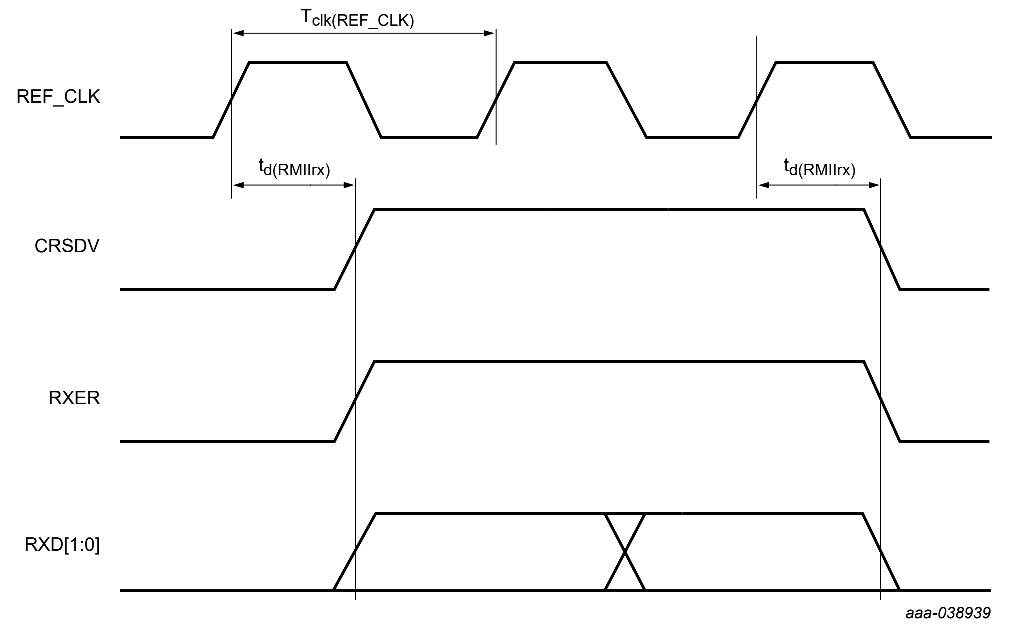


Figure 15. RMII receive timing diagram

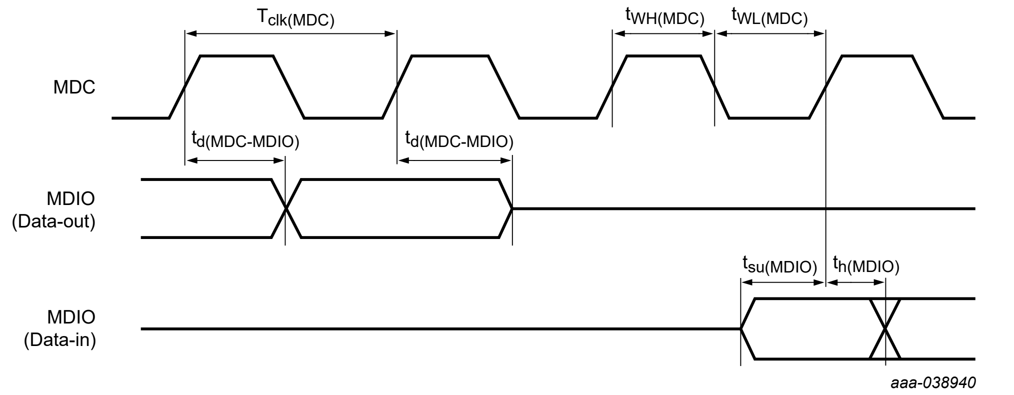


Figure 16. SMI timing diagram

11 Application information

The MDI circuit for the TJA1101B is shown in Figure 17. The common mode termination depends on OEM requirements and might vary, depending on the application.

The common mode choke is expected to be compliant with the OPEN Alliance CMC specification. The 100 nF coupling capacitors should have a voltage range ≥ 50 V with 10 % (max) tolerance.

The TJA1101B provides an ESD robustness of ±6 kV according to IEC 61000-4-2 and HBM at the IC pins. With CMC and coupling capacitors, it is able to withstand ≥ ±8 kV for IEC 61000-4-2 on the connector pins.

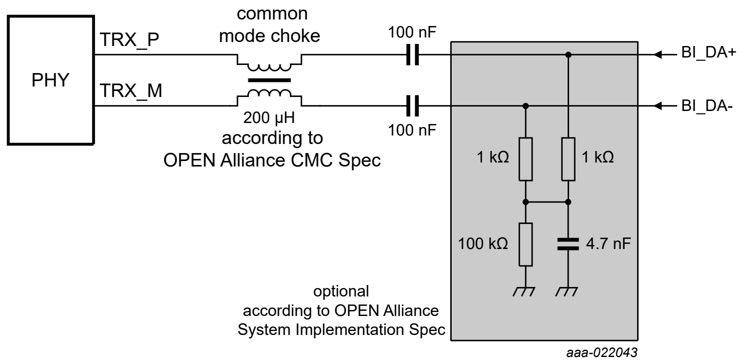


Figure 17. MDI circuit diagram

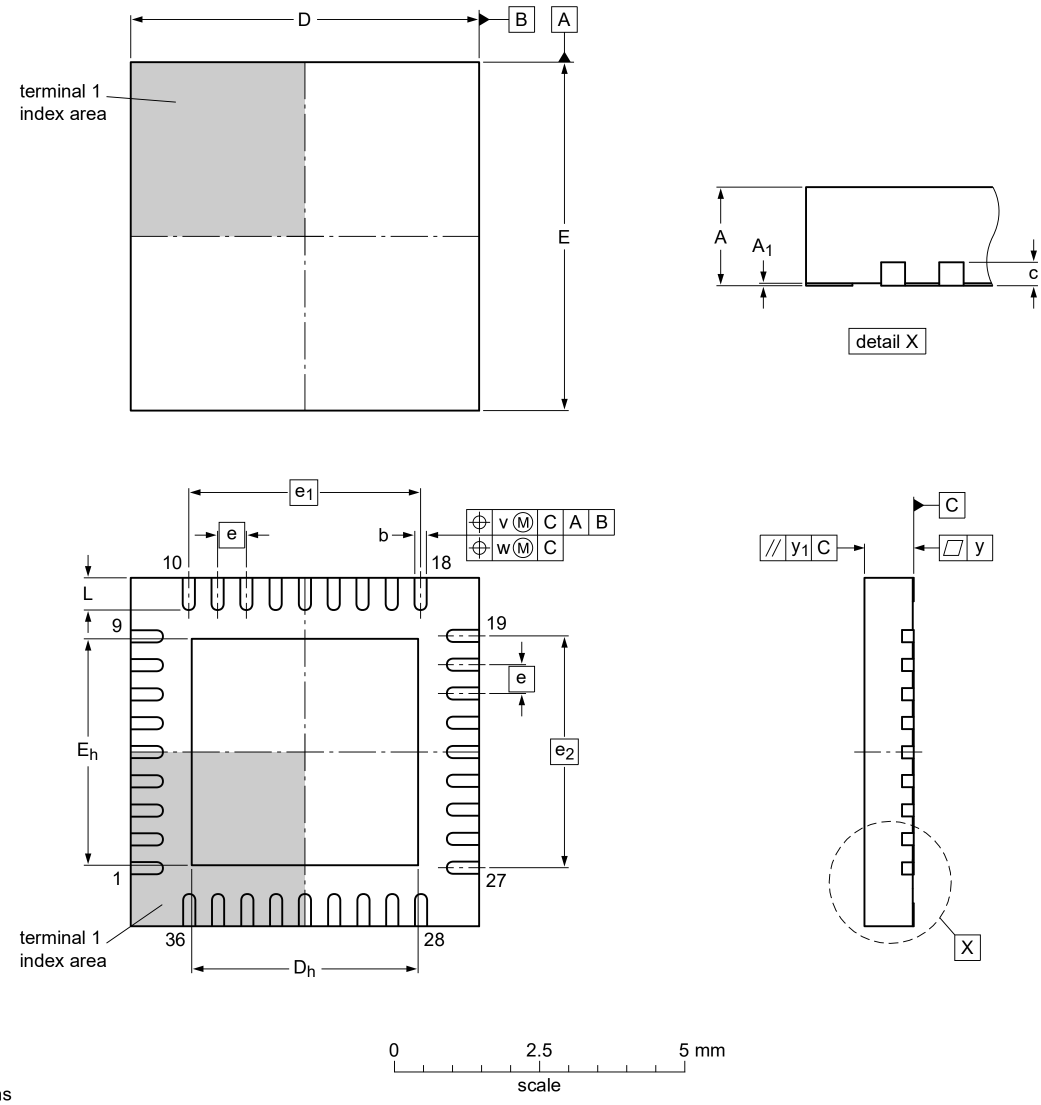
Further information can be found in the TJA1101B application hints [2].

12 Package information

The TJA1101B comes in a 36-pin HVQFN package as shown in Figure 18. Measuring just 36 mm^2 with a pitch of 0.5 mm, the HVQFN36 package is particularly suited to PCB space-constrained applications, such as an integrated IP camera module. The package features wettable sides/flanks to allow for optical inspection of the soldering process. The exposed die pad must be connected to ground.

13 Package outline

HVQFN36: plastic thermal enhanced very thin quad flat package; no leads; 36 terminals; body 6 x 6 x 0.85 mm **SOT1092-2**



Dimensions

Unit		A(1)	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	max	1.00	0.05	0.30		6.1	4.05	6.1	4.05				0.65				
	nom	0.85	0.02	0.21	0.2	6.0	3.90	6.0	3.90	0.5	4	4	0.55	0.1	0.05	0.05	0.1
	min	0.80	0.00	0.18		5.9	3.75	5.9	3.75				0.45				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1092-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1092-2		- - -	- - -			~~09-02-23~~ 09-02-24

Figure 18. Package outline SOT1092-2 (HVQFN36)

14 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 19) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 38 and Table 39

Table 38. SnPb eutectic process (from J-STD-020D)

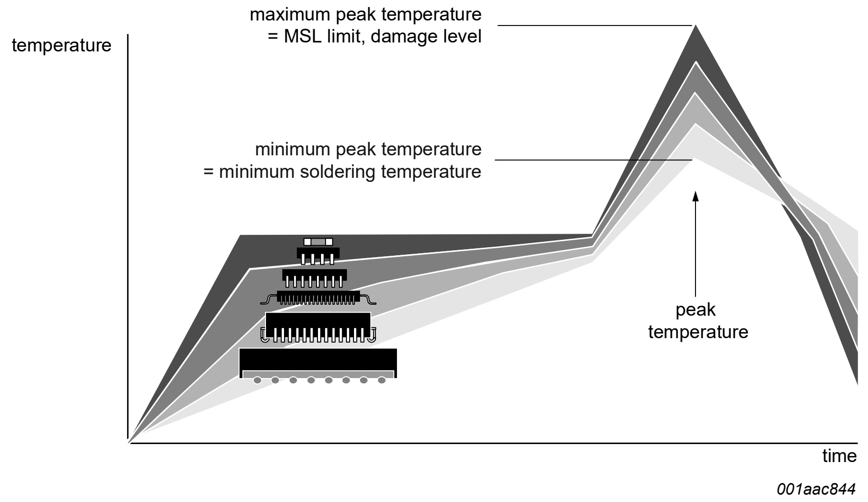
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 39. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 19.



MSL: Moisture Sensitivity Level

Figure 19. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

15 References

[1] **IEEE 802.3bw-2015** — IEEE Standard for Ethernet Amendment 1: Physical Layer Specifications and Management Parameters for 100 Mb/s Operation over a Single Balanced Twisted Pair Cable (100BASE-T1)

[2] **AN13147** — Application note for TJA1101B 100BASE-T1 PHY for automotive Ethernet, NXP Semiconductors

16 Revision history

Table 40. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TJA1101B v.1	20210301	Product data sheet	-	-

17 Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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