

## 5V/3.3V ECL $\div 2$ Divider

### Features

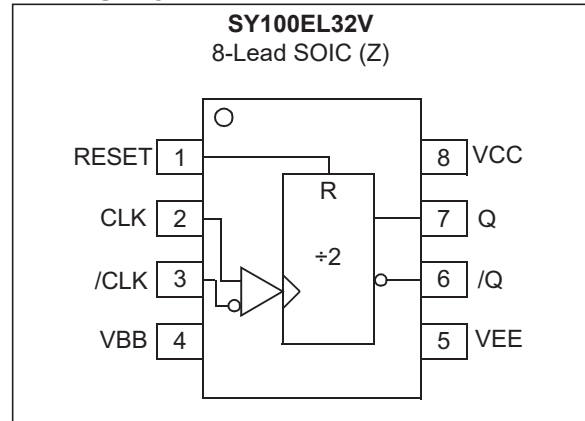
- 3.3V and 5V Power Supply Options
- 510 ps Propagation Delay (Typical)
- 3.0 GHz Toggle Frequency (Typical)
- High Bandwidth Output Transitions
- Internal 75 k $\Omega$  Input Pull-Down Resistors
- Available in 8-Lead SOIC Package

### General Description

The SY100EL32V is an integrated  $\div 2$  divider. The differential clock inputs and the VBB allow a differential, single-ended or AC-coupled interface to the device. If used, the VBB output should be bypassed to ground with a 0.01  $\mu\text{F}$  capacitor. Also note that the VBB is designed to be used as an input bias on the EL32V only; the VBB output has limited current sink and source capability.

The RESET pin is asynchronous and is asserted on the rising edge. Upon power-on, the internal flip-flop will attain a random state. The RESET allows for the synchronization of multiple EL32Vs in a system.

### Package Type



# SY100EL32V

## 1.0 ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

PECL Power Supply Voltage ( $V_{CC}$ ) (Note 1)	+8V
NECL Power Supply Voltage ( $V_{EE}$ ) (Note 2)	-8V
PECL Mode Input Voltage ( $V_{IN}$ ) (Note 3)	+6V
NECL Mode Input Voltage ( $V_{IN}$ ) (Note 4)	-6V
Continuous Output Current ( $I_{OUT}$ )	50 mA
Surge Output Current ( $I_{OUT}$ )	100 mA

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Note 1:**  $V_{EE} = 0V$ .

**2:**  $V_{CC} = 0V$ .

**3:**  $V_{EE} = 0V, V_{IN} \leq V_{CC}$ .

**4:**  $V_{CC} = 0V, V_{IN} \geq V_{EE}$ .

### PECL DC ELECTRICAL CHARACTERISTICS

**Electrical Characteristics PECL:**  $V_{CC} = 3.0V$  to  $5.5V$ ;  $V_{EE} = 0V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Current	$I_{EE}$	—	25	30	mA	$T_A = -40^\circ C$ to $+25^\circ C$
		—	29	35		$T_A = +85^\circ C$
Output High Voltage (Note 2)	$V_{OH}$	$V_{CC} - 1.085$	$V_{CC} - 1.005$	$V_{CC} - 0.88$	V	$T_A = -40^\circ C$
		$V_{CC} - 1.025$	$V_{CC} - 0.955$	$V_{CC} - 0.88$		$T_A = 0^\circ C$ to $+85^\circ C$
Output Low Voltage (Note 2)	$V_{OL}$	$V_{CC} - 1.830$	$V_{CC} - 1.695$	$V_{CC} - 1.555$	V	$T_A = -40^\circ C$
		$V_{CC} - 1.810$	$V_{CC} - 1.705$	$V_{CC} - 1.620$		$T_A = 0^\circ C$ to $+85^\circ C$
Output Reference Voltage	$V_{BB}$	$V_{CC} - 1.38$	—	$V_{CC} - 1.26$	V	—
Input High Voltage (Single-Ended)	$V_{IH}$	$V_{CC} - 1.165$	—	$V_{CC} - 0.880$	V	—
Input Low Voltage (Single-Ended)	$V_{IL}$	$V_{CC} - 1.810$	—	$V_{CC} - 1.475$	V	—
Common Mode Range (Note 3)	$V_{IHCMR}$	2.0	—	$V_{CC} - 0.4$	V	$T_A = -40^\circ C$
		1.9	—	$V_{CC} - 0.4$		$T_A = 0^\circ C$ to $+85^\circ C$
Input High Current	$I_{IH}$	—	—	150	$\mu A$	—
Input Low Current	$I_{IL}$	0.5	—	—	$\mu A$	$V_{IN} = V_{IL(MIN)}$

**Note 1:** Devices are designed to meet the DC specifications shown in the above table after thermal equilibration has been established. The circuit is in a test socket or mounted on a printed circuit board, and transverse airflow greater than 500 lfm is maintained.

**2:** Outputs are terminated through a  $50\Omega$  resistor to  $V_{CC} - 2.0V$ .

**3:** The CMR range is referenced to the most positive side of the differential input voltage. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between 150 mV and 1V.

## NECL DC ELECTRICAL CHARACTERISTICS

**Electrical Characteristics NECL:**  $V_{EE} = -5.5V$  to  $-3.0V$ ;  $V_{CC} = 0V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise stated.  
**(Note 1)**

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Current	$I_{EE}$	—	25	30	mA	$T_A = -40^{\circ}C$ to $+25^{\circ}C$
		—	29	35		$T_A = +85^{\circ}C$
Output High Voltage <b>(Note 2)</b>	$V_{OH}$	-1.085	-1.005	-0.88	V	$T_A = -40^{\circ}C$
		-1.025	-0.955	-0.88		$T_A = 0^{\circ}C$ to $+85^{\circ}C$
Output Low Voltage <b>(Note 2)</b>	$V_{OL}$	-1.830	-1.695	-1.555	V	$T_A = -40^{\circ}C$
		-1.810	-1.705	-1.620		$T_A = 0^{\circ}C$ to $+85^{\circ}C$
Output Reference Voltage	$V_{BB}$	-1.380	—	-1.260	V	—
Input High Voltage (Single-Ended)	$V_{IH}$	-1.165	—	-0.880	V	—
Input Low Voltage (Single-Ended)	$V_{IL}$	-1.810	—	-1.475	V	—
Common Mode Range <b>(Note 3)</b>	$V_{IHCMR}$	$V_{EE} + 2.0$	—	-0.4	V	$T_A = -40^{\circ}C$
		$V_{EE} + 1.9$	—	-0.4		$T_A = 0^{\circ}C$ to $+85^{\circ}C$
Input High Current	$I_{IH}$	—	—	150	$\mu A$	—
Input Low Current	$I_{IL}$	0.5	—	—	$\mu A$	$V_{IN} = V_{IL(MIN)}$

- Note 1:** Devices are designed to meet the DC specifications shown in the above table after thermal equilibration has been established. The circuit is in a test socket or mounted on a printed circuit board, and transverse airflow greater than 500 lfm is maintained.
- 2:** Outputs are terminated through a  $50\Omega$  resistor to  $V_{CC} - 2.0V$ .
- 3:** The CMR range is referenced to the most positive side of the differential input voltage. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between 150 mV and 1V.

# SY100EL32V

## AC ELECTRICAL CHARACTERISTICS

**Electrical Characteristics:**  $V_{CC} = 3.0V$  to  $5.5V$ ;  $V_{EE} = 0V$  or  $V_{EE} = -5.5V$  to  $-3.0V$ ;  $V_{CC} = 0V$ ;  $R_L = 50\Omega$  to  $V_{CC} - 2V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Toggle Frequency	$f_{MAX}$	2.2	3.0	—	GHz	$T_A = -40^\circ C$
		2.6	3.0	—		$T_A = 0^\circ C$ to $+85^\circ C$
Propagation Delay CLK to Q	$t_{PD}$	360	500	640	ps	$T_A = -40^\circ C$
		410	500	590		$T_A = 0^\circ C$
		420	510	600		$T_A = +25^\circ C$
		450	540	630		$T_A = +85^\circ C$
Propagation Delay RESET to Q	$t_{PD}$	390	540	690	ps	$T_A = -40^\circ C$
		440	540	640		$T_A = 0^\circ C$ to $+25^\circ C$
		450	550	650		$T_A = +85^\circ C$
Random Clock Jitter (RMS)	$t_{JITTER}$	—	2.0	—	ps	—
Input Swing (Note 1)	$V_{PP}$	150	—	1000	mV	—
Output Rise/Fall Time Q (20% to 80%)	$t_r/t_f$	100	225	350	ps	—

**Note 1:** Input swing for which AC parameters are ensured.

## TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Operating Temperature Range	$T_A$	-40	—	+85	$^\circ C$	—
Storage Temperature Range	$T_S$	-65	—	+150	$^\circ C$	—
Lead Temperature	$T_{LEAD}$	—	—	+260	$^\circ C$	Soldering, 20s

## 2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

**TABLE 2-1: PIN FUNCTION TABLE**

Pin Number	Pin Name	Description
1	RESET	Asynchronous Reset.
2, 3	CLK, /CLK	Clock Inputs.
4	VBB	Reference Voltage Output.
5	VEE	Negative Power Supply.
6, 7	/Q, Q	Data Output.
8	VCC	Positive Power Supply.

# SY100EL32V

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## 3.0 PACKAGING INFORMATION

### 3.1 Package Marking Information

8-Lead SOIC\*



Example



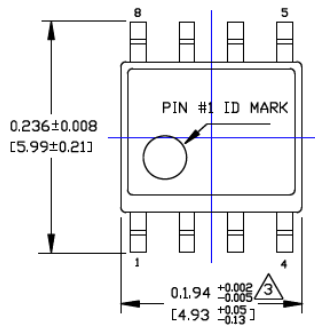
<b>Legend:</b>	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
<b>Note:</b>	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (̄) and/or Overbar (¯) symbol may not be to scale.	

## 8-Lead SOIC Package Outline and Recommended Land Pattern

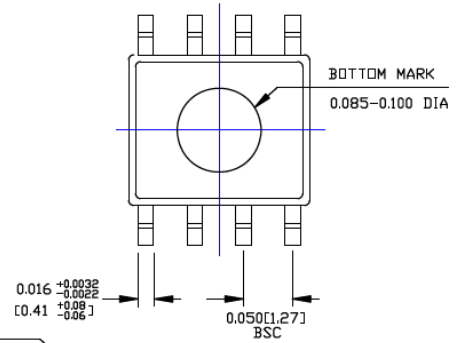
**TITLE**

8 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

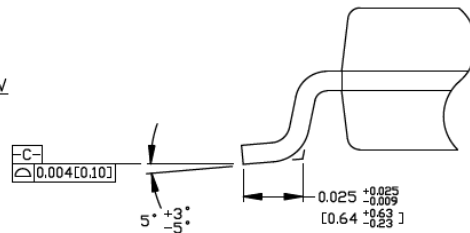
DRAWING #	SOICN-8LD-PL-1	UNIT	INCH [MM]
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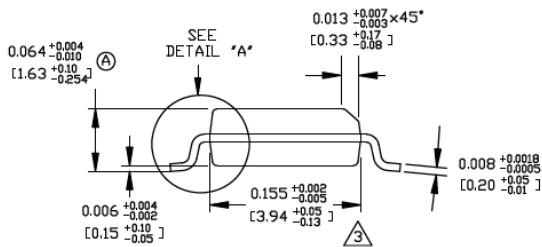
TOP VIEW



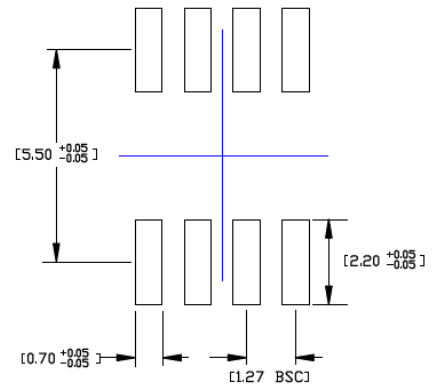
BOTTOM VIEW



DETAIL 'A'



END VIEW



RECOMMENDED LAND PATTERN

**NOTES:**

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

# SY100EL32V

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NOTES:



## APPENDIX A: REVISION HISTORY

### Revision A (October 2018)

- Converted Micrel document SY100EL32V to Microchip data sheet DS20006083A.
- Minor text changes throughout.
- Removed all reference to the EOL SY10EL32V version.

### Revision B (August 2019)

- Updated minimum values for Common Mode Range voltage in [PECL DC Electrical Characteristics](#) table and [NECL DC Electrical Characteristics](#) table.
- Minor stylistic updates to align data sheet with current style.
- Correct the description of the part in all relevant places to reflect  $\pm 2$ .

# SY100EL32V

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NOTES:

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>-XX</u>
Device	Supply Voltage	Package	Temperature Range	Special Processing
<b>Device:</b>	SY100EL32: 5V/3.3V ECL +2 Divider			
<b>Supply Voltage Range:</b>	V	=	3.3V/5V	
<b>Package:</b>	Z	=	8-Lead SOIC (Pb-free NiPdAu)	
<b>Temperature Range:</b>	G	=	-40°C to +85°C	
<b>Special Processing:</b>	<blank>	=	95/Tube	
	TR	=	1,000/Reel	

<b>Examples:</b>	
a) SY100EL32VZG:	SY100EL32V, 8-Lead SOIC (Pb-free NiPdAu), -40°C to +85°C, 95/Tube
b) SY100EL32VZG-TR:	SY100EL32V, 8-Lead SOIC (Pb-free NiPdAu), -40°C to +85°C, 1,000/Reel

**Note 1:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

# SY100EL32V

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NOTES:

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