RMLV0414E Series

4Mb Advanced LPSRAM (256-kword × 16-bit)

R10DS0216EJ0300
Rev.3.00
2021.8.18

Description

The RMLV0414E Series is a family of 4-Mbit static RAMs organized 262,144-word × 16-bit, fabricated by Renesas's high-performance Advanced LPSRAM technologies. The RMLV0414E Series has realized higher density, higher performance and low power consumption. The RMLV0414E Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 44-pin TSOP (II).

Features

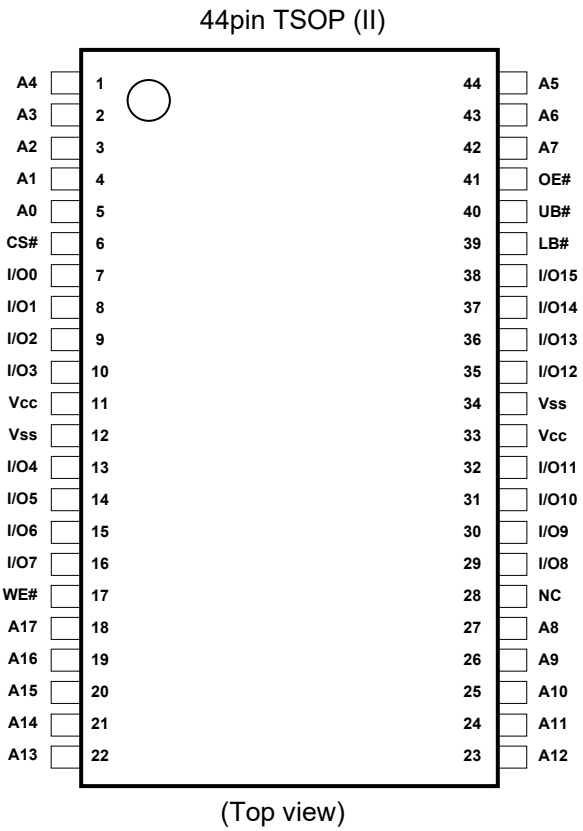
- Single 3V supply: 2.7V to 3.6V
- Access time: 45ns (max.)
- Current consumption:
  — Standby: 0.3µA (typ.)
- Equal access and cycle times
- Common data input and output
  — Three state output
- Directly TTL compatible
  — All inputs and outputs
- Battery backup operation

Orderable part number information

Part name	Access time	Temperature range	Package	Shipping container
RMLV0414EGSB-4S2#AA*	45 ns	-40 ~ +85°C	400-mil 44pin plastic TSOP (II)	Tray
RMLV0414EGSB-4S2#HA*				Embossed tape

Note 1. * = Revision code for Assembly site change, etc. (* = 0, 1, etc.)

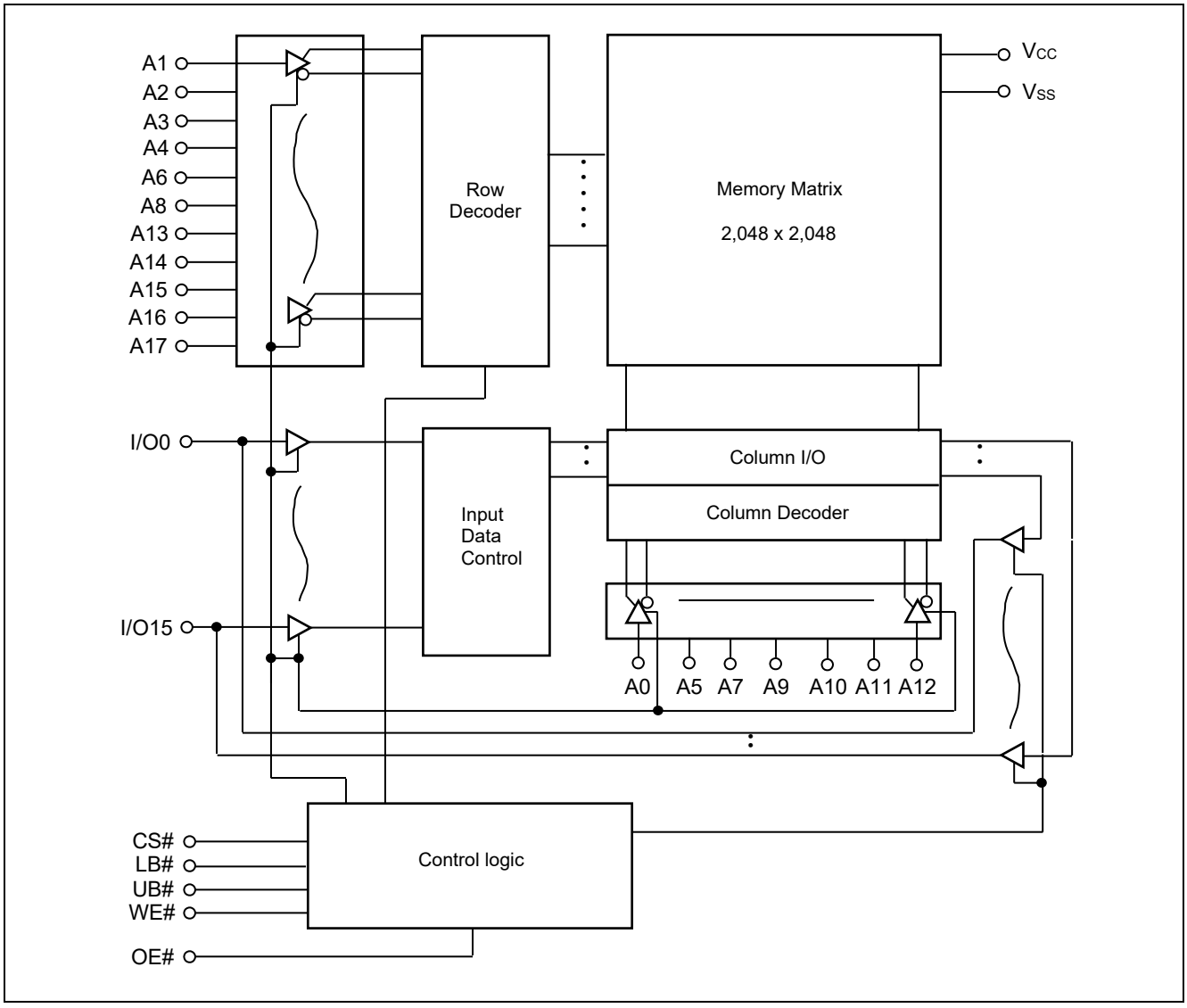
Pin Arrangement



Pin Description

Pin name	Function
V_{CC}	Power supply
V_{SS}	Ground
A0 to A17	Address input
I/O0 to I/O15	Data input/output
CS#	Chip select
OE#	Output enable
WE#	Write enable
LB#	Lower byte select
UB#	Upper byte select
NC	No connection

Block Diagram



Operation Table

CS#	WE#	OE#	UB#	LB#	I/O0 to I/O7	I/O8 to I/O15	Operation
H	X	X	X	X	High-Z	High-Z	Standby
X	X	X	H	H	High-Z	High-Z	Standby
L	H	L	L	L	Dout	Dout	Read
L	H	L	H	L	Dout	High-Z	Lower byte read
L	H	L	L	H	High-Z	Dout	Upper byte read
L	L	X	L	L	Din	Din	Write
L	L	X	H	L	Din	High-Z	Lower byte write
L	L	X	L	H	High-Z	Din	Upper byte write
L	H	H	X	X	High-Z	High-Z	Output disable

Note 2. H: V_{IH} L:V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5[*3] to V_{CC}+0.3[*4]	V
Power dissipation	P_T	0.7	W
Operation temperature	Topr	-40 to +85	°C
Storage temperature range	Tstg	-65 to +150	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Note 3. -3.0V for pulse ≤ 30ns (full width at half maximum)
4. Maximum voltage is +4.6V.

DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.2	—	V_{CC}+0.3	V	
Input low voltage	V_{IL}	-0.3	—	0.6	V	5
Ambient temperature range	Ta	-40	—	+85	°C	

Note 5. -3.0V for pulse ≤ 30ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Input leakage current	$\lvert I_{LI} \rvert$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\lvert I_{LO} \rvert$	—	—	1	µA	CS# = V_{IH} or OE# = V_{IH} or WE# = V_{IL} or LB# = UB# = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Operating current	I_{CC}	—	—	10	mA	CS# = V_{IL}, Others = V_{IH}/V_{IL}, $I_{I/O}$ = 0mA
Average operating current	I_{CC1}	—	—	20	mA	Cycle = 55ns, duty =100%, $I_{I/O}$ = 0mA, CS# = V_{IL}, Others = V_{IH}/V_{IL}
		—	—	25	mA	Cycle = 45ns, duty =100%, $I_{I/O}$ = 0mA, CS# = V_{IL}, Others = V_{IH}/V_{IL}
	I_{CC2}	—	—	2.5	mA	Cycle =1µs, duty =100%, $I_{I/O}$ = 0mA CS# ≤ 0.2V, V_{IH} ≥ V_{CC}-0.2V, V_{IL} ≤ 0.2V
Standby current	I_{SB}	—	0.1[*6]	0.3	mA	CS# = V_{IH}, Others = V_{SS} to V_{CC}
Standby current	I_{SB1}	—	0.3[*6]	2	µA	~+25°C; Vin = V_{SS} to V_{CC}, (1) CS# ≥ V_{CC}-0.2V or (2) LB# = UB# ≥ V_{CC}-0.2V, CS# ≤ 0.2V
		—	—	3	µA	~+40°C
		—	—	5	µA	~+70°C
		—	—	7	µA	~+85°C
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = -1mA
	V_{OH2}	V_{CC}-0.2	—	—	V	I_{OH} = -0.1mA
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2mA
	V_{OL2}	—	—	0.2	V	I_{OL} = 0.1mA

Note 6. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25ºC), and not 100% tested.

Capacitance

(Vcc = 2.7V ~ 3.6V, f = 1MHz, Ta = -40 ~ +85°C)

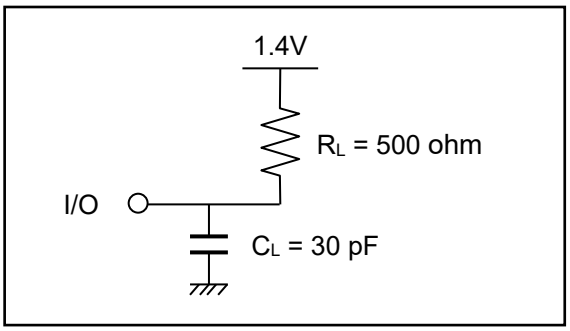
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C in	—	—	8	pF	Vin =0V	7
Input / output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ =0V	7

Note 7. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Vcc = 2.7V ~ 3.6V, Ta = -40 ~ +85°C)

- Input pulse levels: V_{IL} = 0.4V, V_{IH} = 2.4V
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	t_{RC}	45	—	ns	
Address access time	t_{AA}	—	45	ns	
Chip select access time	t_{ACS}	—	45	ns	
Output enable to output valid	t_{OE}	—	22	ns	
Output hold from address change	t_{OH}	10	—	ns	
LB#, UB# access time	t_{BA}	—	45	ns	
Chip select to output in low-Z	t_{CLZ}	10	—	ns	8,9
LB#, UB# enable to low-Z	t_{BLZ}	5	—	ns	8,9
Output enable to output in low-Z	t_{OLZ}	5	—	ns	8,9
Chip deselect to output in high-Z	t_{CHZ}	0	18	ns	8,9,10
LB#, UB# disable to high-Z	t_{BHZ}	0	18	ns	8,9,10
Output disable to output in high-Z	t_{OHZ}	0	18	ns	8,9,10

Note 8. This parameter is sampled and not 100% tested.

9. At any given temperature and voltage condition, t_{CHZ} max is less than t_{CLZ} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

10. t_{CHZ}, t_{BHZ} and t_{OHZ} are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

Write Cycle

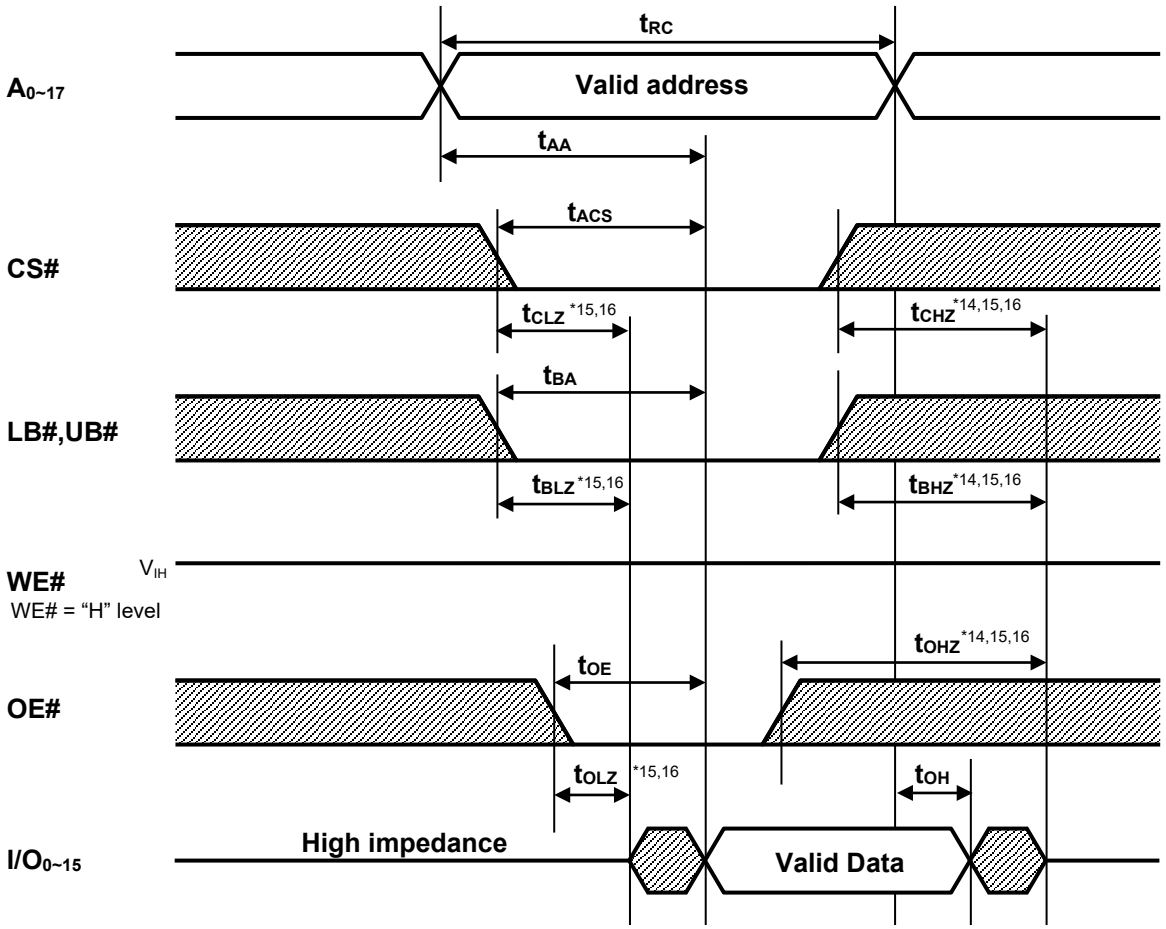
Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	t_{WC}	45	—	ns	
Address valid to write end	t_{AW}	35	—	ns	
Chip select to write end	t_{CW}	35	—	ns	
Write pulse width	t_{WP}	35	—	ns	11
LB#,UB# valid to write end	t_{BW}	35	—	ns	
Address setup time to write start	t_{AS}	0	—	ns	
Write recovery time from write end	t_{WR}	0	—	ns	
Data to write time overlap	t_{DW}	25	—	ns	
Data hold from write end	t_{DH}	0	—	ns	
Output enable from write end	t_{OW}	5	—	ns	12
Output disable to output in high-Z	t_{OHZ}	0	18	ns	12,13
Write to output in high-Z	t_{WHZ}	0	18	ns	12,13

Note 11. t_{WP} is the interval between write start and write end.
A write starts when all of (CS#), (WE#) and (one or both of LB# and UB#) become active.
A write is performed during the overlap of a low CS#, a low WE# and a low LB# or a low UB#.
A write ends when any of (CS#), (WE#) or (one or both of LB# and UB#) becomes inactive.

12. This parameter is sampled and not 100% tested.
13. t_{OHZ} and t_{WHZ} are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

Timing Waveforms

Read Cycle

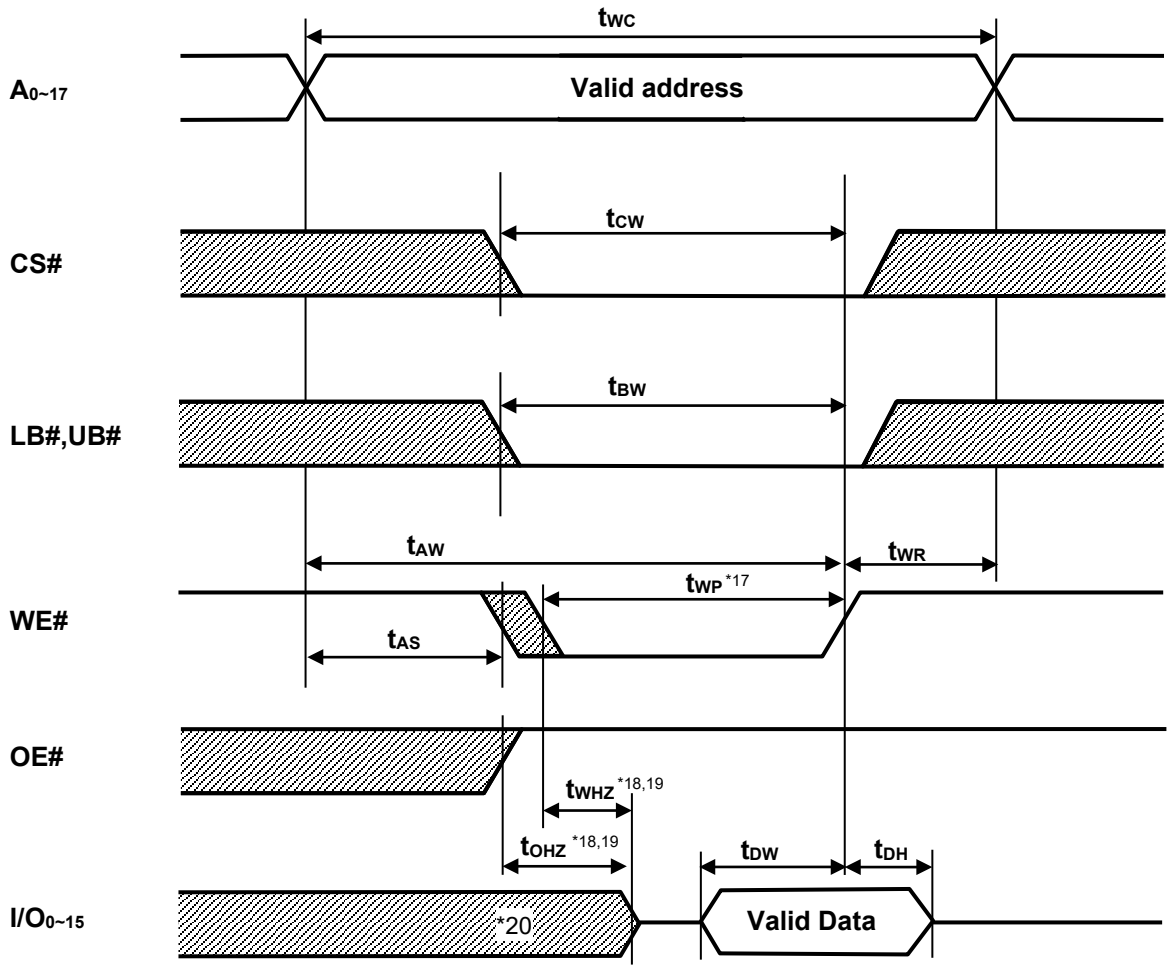


Note 14. t_{CHZ}, t_{BHZ} and t_{OHZ} are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.

15. This parameter is sampled and not 100% tested.

16. At any given temperature and voltage condition, t_{CHZ} max is less than t_{CLZ} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

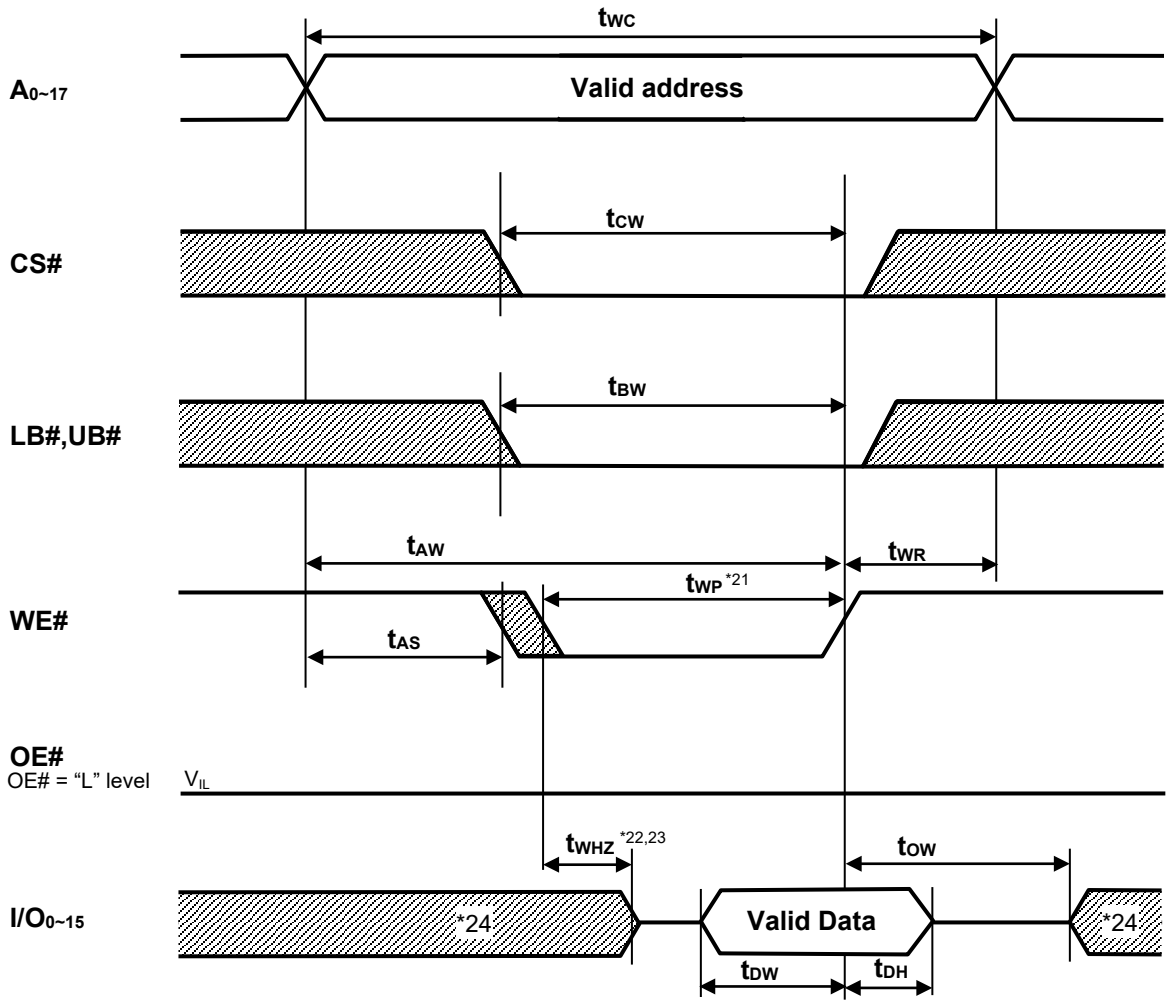
Write Cycle (1) (WE# CLOCK, OE#="H" while writing)



Note 17. t_{WP} is the interval between write start and write end.
A write starts when all of (CS#), (WE#) and (one or both of LB# and UB#) become active.
A write is performed during the overlap of a low CS#, a low WE# and a low LB# or a low UB#.
A write ends when any of (CS#), (WE#) or (one or both of LB# and UB#) becomes inactive.

18. t_{OHZ} and t_{WHZ} are defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.
19. This parameter is sampled and not 100% tested.
20. During this period, I/O pins are in the output state so input signals must not be applied to the I/O pins.

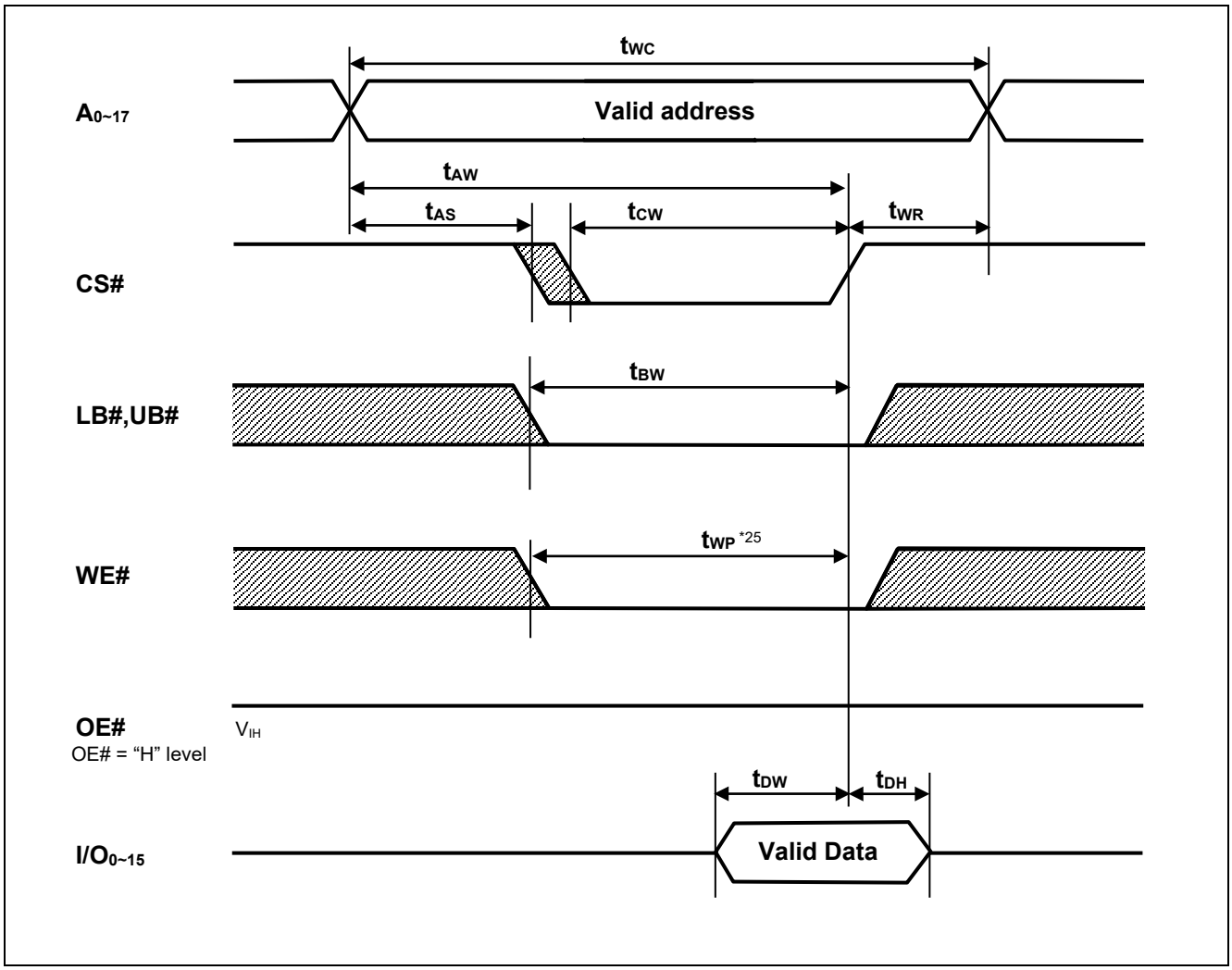
Write Cycle (2) (WE# CLOCK, OE# Low Fixed)



Note 21. t_{WP} is the interval between write start and write end.
A write starts when all of (CS#), (WE#) and (one or both of LB# and UB#) become active.
A write is performed during the overlap of a low CS#, a low WE# and a low LB# or a low UB#.
A write ends when any of (CS#), (WE#) or (one or both of LB# and UB#) becomes inactive.

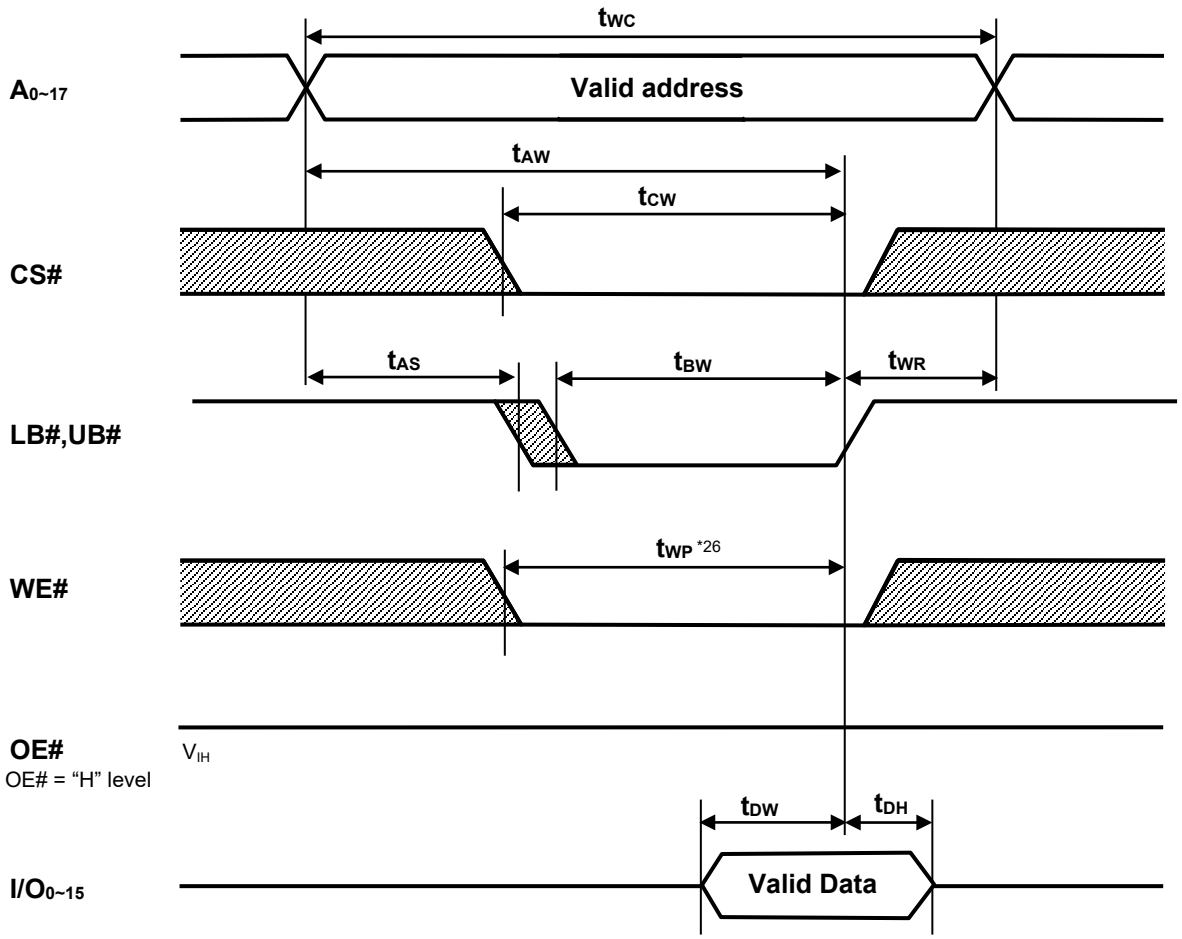
22. t_{WHZ} is defined as the time when the I/O pins enter a high-impedance state and are not referred to the I/O levels.
23. This parameter is sampled and not 100% tested.
24. During this period, I/O pins are in the output state so input signals must not be applied to the I/O pins.

Write Cycle (3) (CS# CLOCK)



Note 25. t_{WP} is the interval between write start and write end.
A write starts when all of (CS#), (WE#) and (one or both of LB# and UB#) become active.
A write is performed during the overlap of a low CS#, a low WE# and a low LB# or a low UB#.
A write ends when any of (CS#), (WE#) or (one or both of LB# and UB#) becomes inactive.

Write Cycle (4) (LB#,UB# CLOCK)



Note 26. t_{WP} is the interval between write start and write end.
A write starts when all of (CS#), (WE#) and (one or both of LB# and UB#) become active.
A write is performed during the overlap of a low CS#, a low WE# and a low LB# or a low UB#.
A write ends when any of (CS#), (WE#) or (one or both of LB# and UB#) becomes inactive.

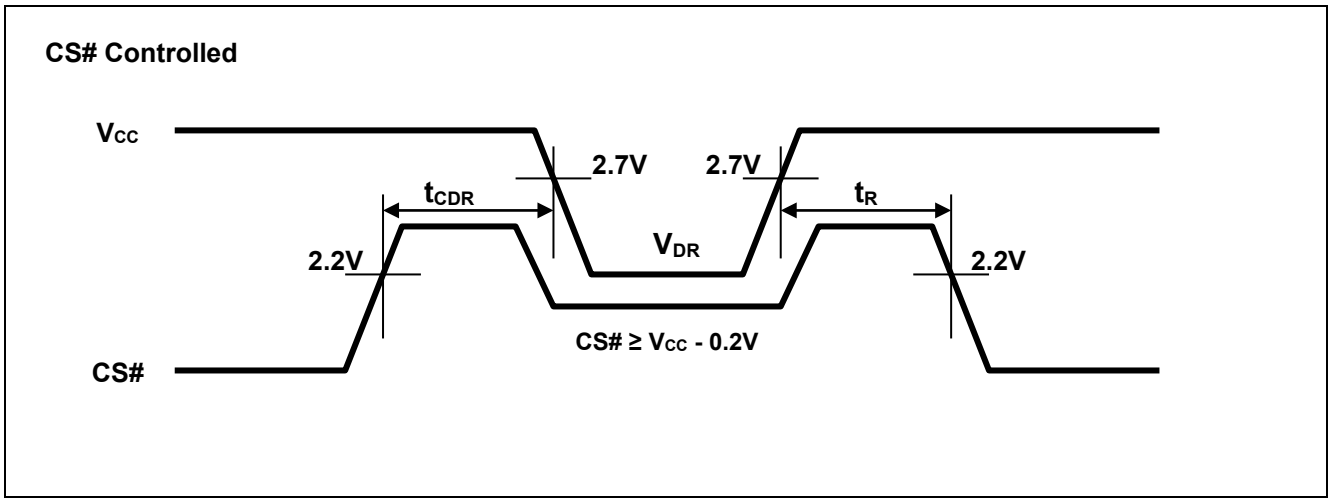
Low V_{CC} Data Retention Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions[*28]	
V_{CC} for data retention	V_{DR}	1.5	—	—	V	Vin ≥ 0V, (1) CS# ≥ V_{CC}-0.2V or (2) LB# = UB# ≥ V_{CC}-0.2V, CS# ≤ 0.2V	
Data retention current	I_{CCDR}	—	0.3[*27]	2	µA	~+25°C	V_{CC}=3.0V, Vin ≥ 0V, (1) CS# ≥ V_{CC}-0.2V or (2) LB# = UB# ≥ V_{CC}-0.2V, CS# ≤ 0.2V
		—	—	3	µA	~+40°C	
		—	—	5	µA	~+70°C	
		—	—	7	µA	~+85°C	
Chip deselect time to data retention	t_{CDR}	0	—	—	ns	See retention waveform.	
Operation recovery time	t_R	5	—	—	ms		

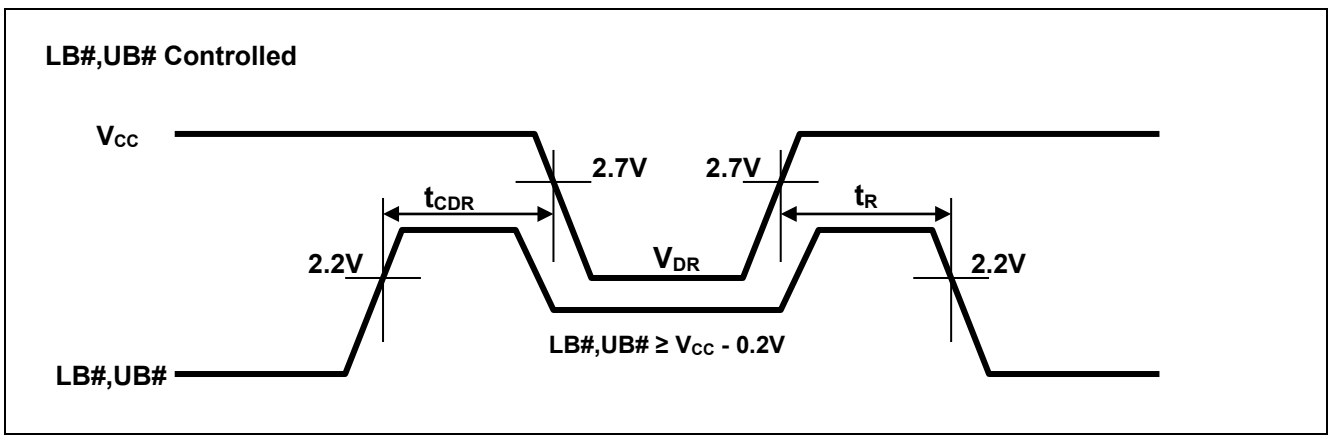
Note 27. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25ºC), and not 100% tested.

28. CS# controls address buffer, WE# buffer, OE# buffer, LB# buffer, UB# buffer and I/O buffer. If CS# controls data retention mode, Vin levels (address, WE#, OE#, LB#,UB#, I/O) can be in the high-impedance state.

Low Vcc Data Retention Timing Waveforms (CS# controlled)



Low Vcc Data Retention Timing Waveforms (LB#,UB# controlled)



Revision History	RMLV0414E Series Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	2014.2.27	—	First edition issued
2.00	2016.1.12	1	Changed section from “Part Name Information” to “Orderable part number information”
2.01	2020.2.20	Last page	Updated the Notice to the latest version
3.00	2021.8.18	1,4,12	Changed the typical value of I_{SB1} and I_{CCDR} from 0.4μA to 0.3μA. Revised orderable part number information

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Renesas Electronics:

RMLV0414EGSB-4S2#HA0 RMLV0414EGSB-4S2#AA0 RMLV0414EGSB-4S2#HA1 RMLV0414EGSB-4S2#AA1