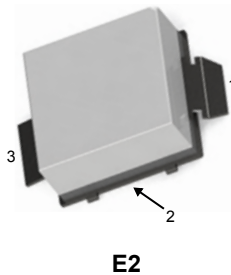


8 W, 28 V, 0.7 to 4.2 GHz RF power LDMOS transistor



Pin connection	
Pin	Connection
1	Drain
2	Source (bottom side)
3	Gate

Features

Order code	Frequency	V _{DD}	P _{OUT}	Gain	Efficiency
RF2L42008CG2	3600 MHz	28 V	8 W	14.5 dB	47%

- High efficiency and linear gain operations
- Integrated ESD protection
- Internally matched for ease of use
- Large positive and negative gate-source voltage range for improved class C operation
- Excellent thermal stability, low HCI drift
- In compliance with the European directive 2002/95/EC

Applications

- Telecom and wideband communications
- Avionics and radar
- 2.45 GHz industrial

Description

The RF2L42008CG2 is a 8 W, 28 V, internally matched LDMOS FET, designed for global positioning system, wideband communications and ISM applications in the frequency range from 0.7 to 4.2 GHz. It can be used in class AB, B or C for all typical modulation formats.



Product status link
RF2L42008CG2

Product summary	
Order code	RF2L42008CG2
Marking	2L42008
Package	E2
Packing	Tape and reel 13"
Base/bulk quantity	300/300

1 Electrical ratings

Table 1. Absolute maximum ratings ($T_C = 25\text{ °C}$)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	65	V
V_{GS}	Gate-source voltage	-6 to 10	V
V_{DD}	Maximum operating voltage	32	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJC}^{(1)}$	Thermal resistance, junction-to-case	3.6	°C/W

1. $T_C = 85\text{ °C}$, $T_J = 200\text{ °C}$, DC test.

Table 3. ESD protection

Symbol	Parameter	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	1B
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS002-2014)	C3

2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Table 4. Static

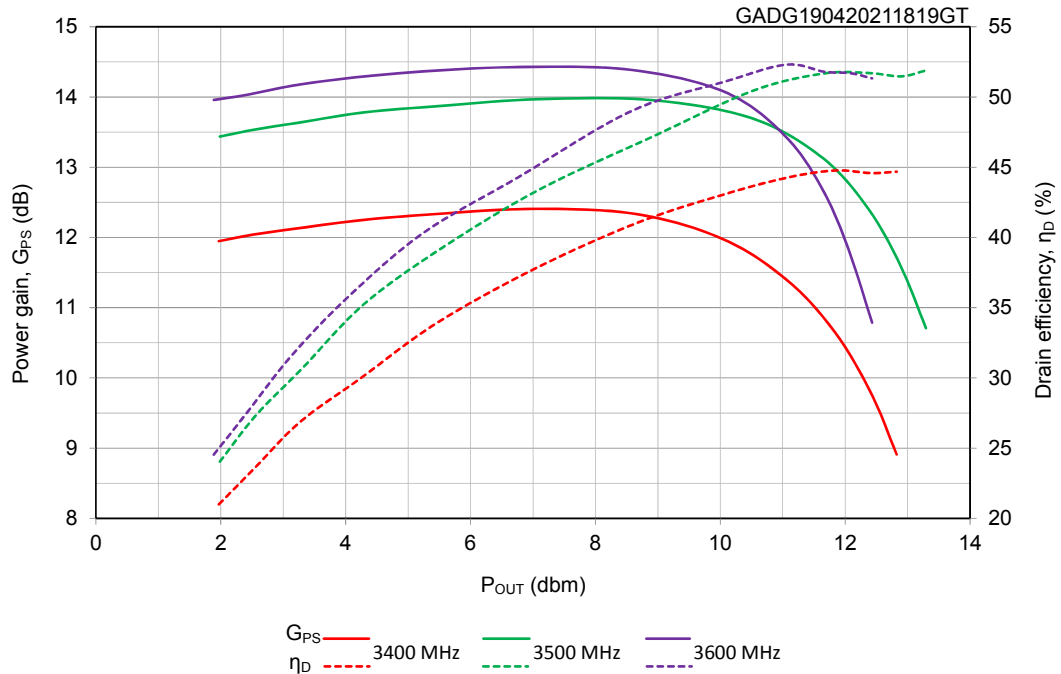
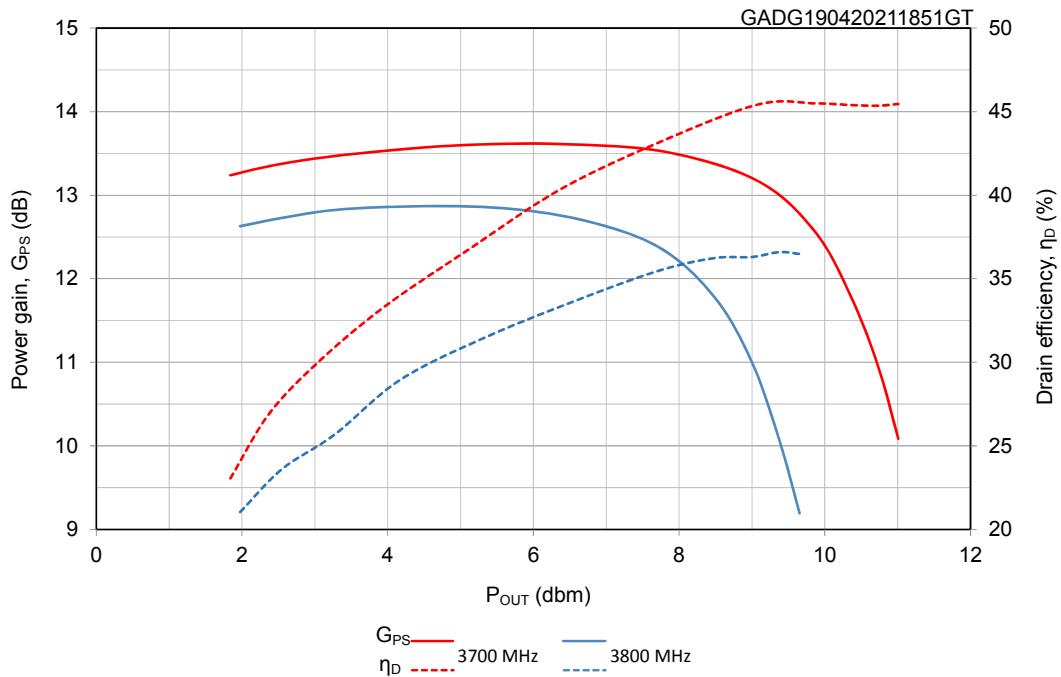
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_{DS} = 100\text{ }\mu\text{A}$	65			V
I_{DSS}	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 28\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 50\text{ V}$				
I_{GSS}	Gate-body leakage current	$V_{GS} = -6/10\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = 28\text{ V}$, $I_{DS} = 300\text{ }\mu\text{A}$	1.75		2.50	V
$V_{GS(Q)}$	Gate quiescent voltage	$V_{DS} = 1\text{ V}$, $I_{DS} = 100\text{ mA}$	2		4	V
$V_{DS(on)}$	Static drain-source on-voltage	$V_{GS} = 10\text{ V}$, $I_{DS} = 800\text{ mA}$			1.1	V
$R_{DS(on)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}$, $V_{DS} = 100\text{ mV}$			1.5	Ω
$I_{DS(on)}$	Static drain-source on-current				2.5	A

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	Frequency		700		4200	MHz
P_{OUT}	Output power	f = 3600 MHz, pulsed CW		8		W
G_{PS}	Power gain			14.5		dB
η_D	Drain efficiency				47	
VSWR	Load mismatch	at 8 W pulsed CW output power, all phases			10:1	

Note: $V_{DD} = 28\text{ V}$, $I_{DQ} = 85\text{ mA}$, pulse width = 100 μs , duty cycle = 10%.

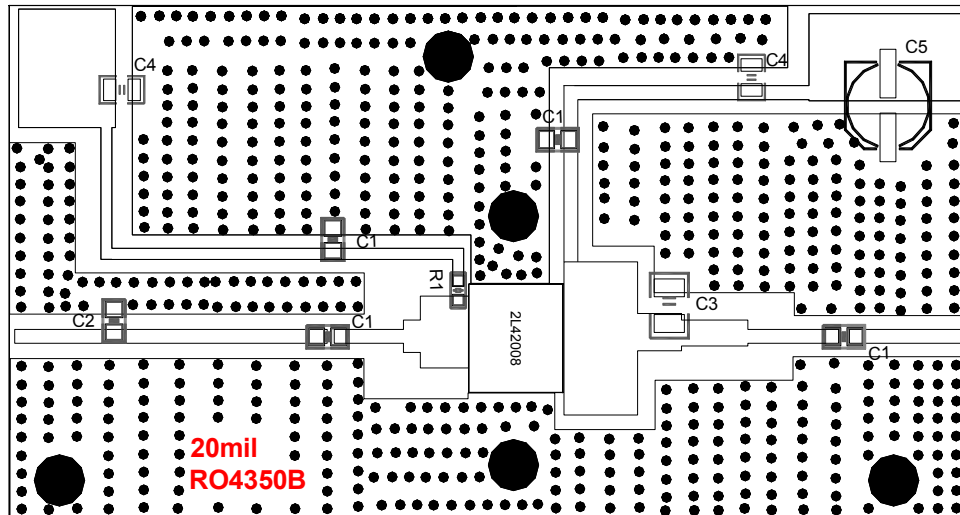
3 Typical performance

Figure 1. Power gain and drain efficiency vs output power (3400 - 3600 MHz)

Figure 2. Power gain and drain efficiency vs output power (3700 - 3800 MHz)


Note: $V_{DD} = 28\text{ V}$, $I_{DQ} = 85\text{ mA}$, pulse width = 100 μs , duty cycle = 10%.

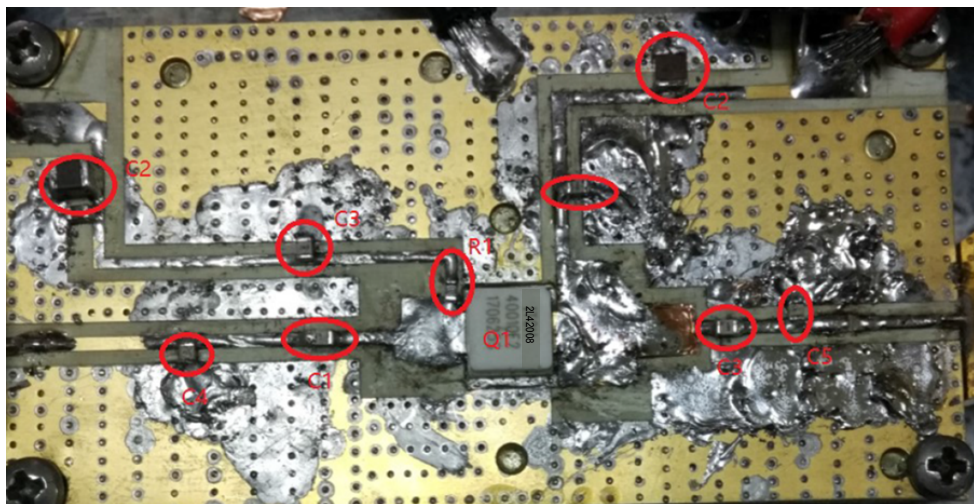
4 Test circuits

Figure 3. Test circuit layout (same PCB with different BOM for each frequency band)



GADG260520201146SA

Figure 4. Test circuit photo (3400 - 3800 MHz)



GADG160320201002SA

Table 6. Components list (3400 - 3800 MHz)

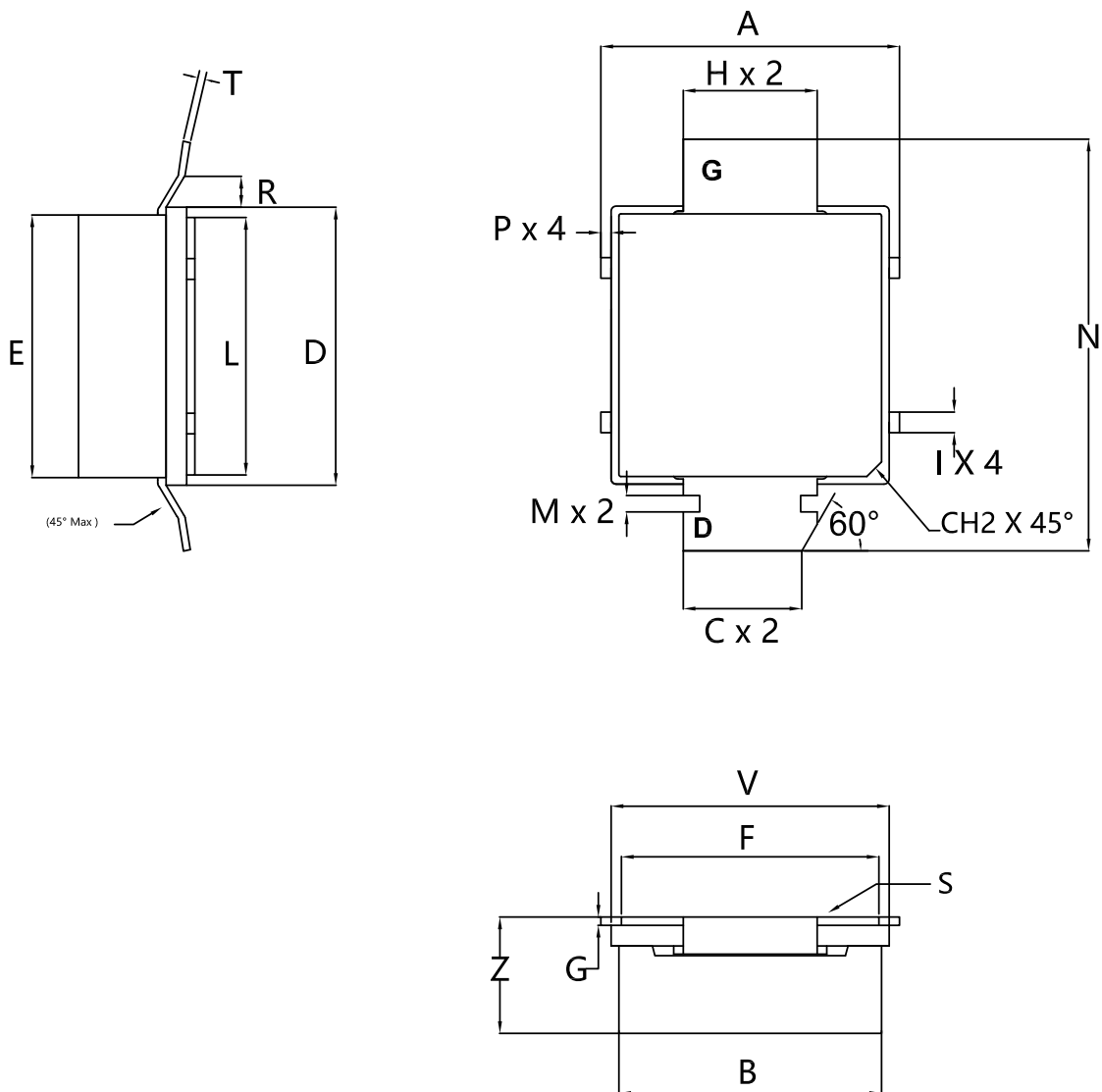
Component	Description	Size	Reference
C1	6.8 pF	0805	ATC600F
C2	0.5 pF	0805	ATC600F
C3	0.3 pF	0805	ATC600F
C4	10 μ F	1206	ceramic multilayer capacitor
C5	100 μ F	0805	aluminum electrolytic capacitors
R1	13 Ω	0805	chip resistor
PCB	0.508 mm (0.020") thick, $\epsilon_r = 3.48$, Rogers RO4350B, 1 oz. copper		

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 E2 package information

Figure 5. E2 package outline



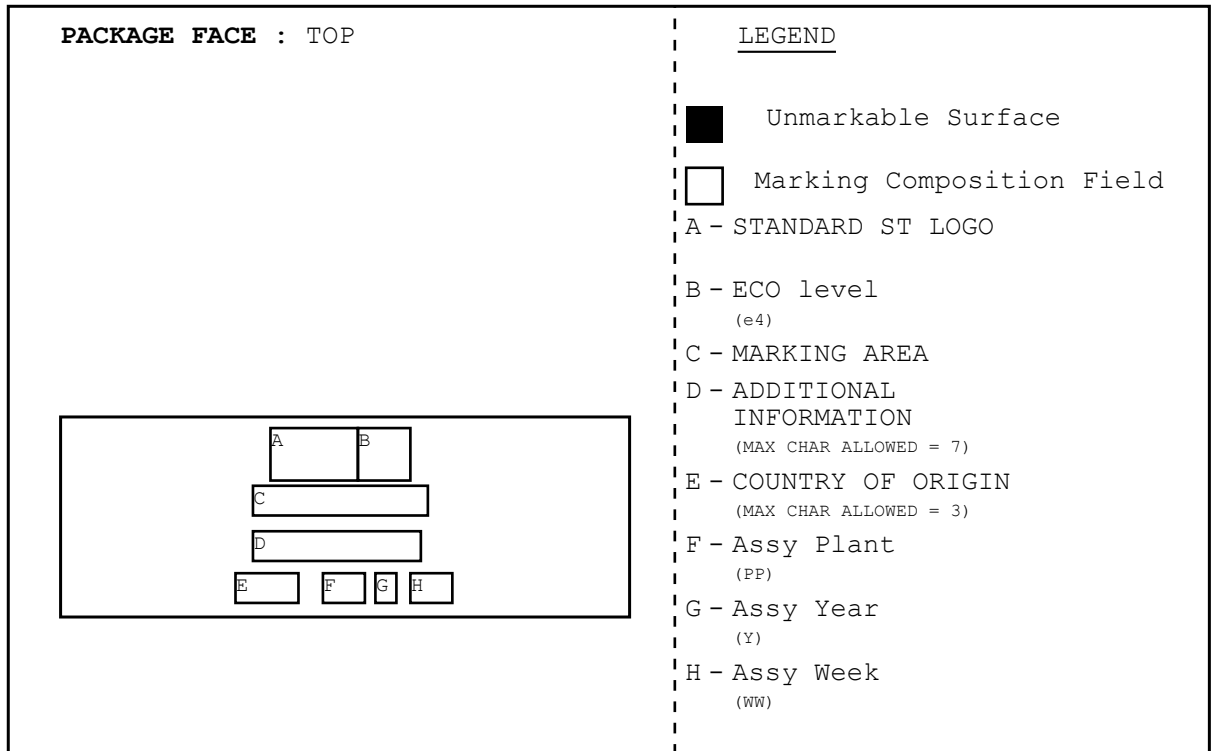
00418523_4

Table 7. E2 mechanical data

Symbol	Millimetres		
	Min.	Typ.	Max.
A			7.37
B	6.35	6.48	6.60
C	2.84	2.92	3.0
D	6.78	6.86	6.94
E	6.35	6.48	6.61
F	6.10	6.35	6.60
G	0.18	0.20	0.23
H	3.23	3.30	3.38
I	0.43	0.51	0.59
L	6.27	6.35	6.43
M	0.33	0.41	0.49
N	10.03	10.16	10.29
P			0.25
R	0.76		1.02
T	0.13	0.18	0.23
V	6.78	6.86	6.94
Z	2.49	2.87	3.25
CH2		0.51	

5.2 Marking information

Figure 6. Marking composition



GADG040220211644GT

Revision history

Table 8. Document revision history

Date	Revision	Changes
18-Jun-2020	1	First release.
20-Apr-2021	2	Updated title, <i>Features</i> and <i>Device summary</i> in cover page. Updated <i>Section 1 Electrical ratings</i> . Updated <i>Section 2 Electrical characteristics</i> . Updated <i>Figure 1. Power gain and drain efficiency vs output power (3400 - 3600 MHz)</i> and <i>Figure 2. Power gain and drain efficiency vs output power (3700 - 3800 MHz)</i> . Updated <i>Section 4 Test circuits</i> . Added <i>Section 5.2 Marking information</i> . Minor text changes.
27-Sep-2021	3	Updated <i>Description</i> in cover page. Minor text changes.

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