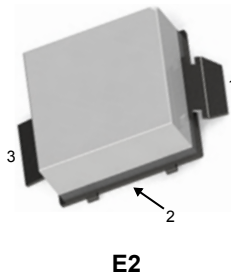


15 W, 28 V, 0.7 to 2.7 GHz RF power LDMOS transistor



Pin connection	
Pin	Connection
1	Drain
2	Source (bottom side)
3	Gate

Features

Order code	Frequency	V _{DD}	P _{OUT}	Gain	Efficiency
RF2L27015CG2	2690 MHz	28 V	15 W	19 dB	53%

- High efficiency and linear gain operations
- Integrated ESD protection
- Internally input matched for ease of use
- Large positive and negative gate-source voltage range for improved class C operation
- Excellent thermal stability, low HCI drift
- In compliance with the European directive 2002/95/EC

Applications

- Telecom and wideband communications
- ISM – 915 MHz and 2.45 GHz
- 915 MHz / 1.3 and 1.5 GHz particle accelerator

Description

The RF2L27015CG2 is a 15 W, 28 V, internally matched LDMOS transistor, designed for Telecom, wideband communications and ISM applications in the frequency range from 0.7 to 2.7 GHz. It can be used in class AB, B or C for all typical modulation formats.



Product status link
RF2L27015CG2

Product summary	
Order code	RF2L27015CG2
Marking	2L27015
Package	E2
Packing	Tape and reel 13"
Base/bulk quantity	300/300

1 Electrical ratings

Table 1. Absolute maximum ratings ($T_C = 25\text{ °C}$)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	-6 to 10	V
V_{DD}	Maximum operating voltage	32	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJC}^{(1)}$	Thermal resistance, junction-to-case	2	°C/W

1. $T_C = 85\text{ °C}$, $T_J = 200\text{ °C}$, DC test.

Table 3. ESD protection

Symbol	Parameter	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	1B
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS002-2014)	C3

2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_{DS} = 100\text{ }\mu\text{A}$	60			V
I_{DSS}	Zero-gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 28\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$				
I_{GSS}	Gate-body leakage current	$V_{GS} = -6/10\text{ V}, V_{DS} = 0\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = 28\text{ V}, I_{DS} = 600\text{ }\mu\text{A}$	1.75		2.50	V
		$V_{DS} = 1\text{ V}, I_{DS} = 600\text{ }\mu\text{A}$				
$V_{GS(Q)}$	Gate quiescent voltage	$V_{DS} = 1\text{ V}, I_{DS} = 180\text{ mA}$		2.65		V
$V_{DS(on)}$	Static drain-source on-voltage	$V_{GS} = 10\text{ V}, I_{DS} = 0.18\text{ A}$			150	mV
		$V_{GS} = 10\text{ V}, I_{DS} = 0.75\text{ A}$			650	
$I_{DS(on)}$	Static drain-source on-current	$V_{GS} = 10\text{ V}, V_{DS} = 100\text{ mV}$			2.5	A
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_{DS} = 0.18\text{ A}$			1	Ω
		$V_{GS} = 10\text{ V}, I_{DS} = 0.75\text{ A}$				

Table 5. Dynamic

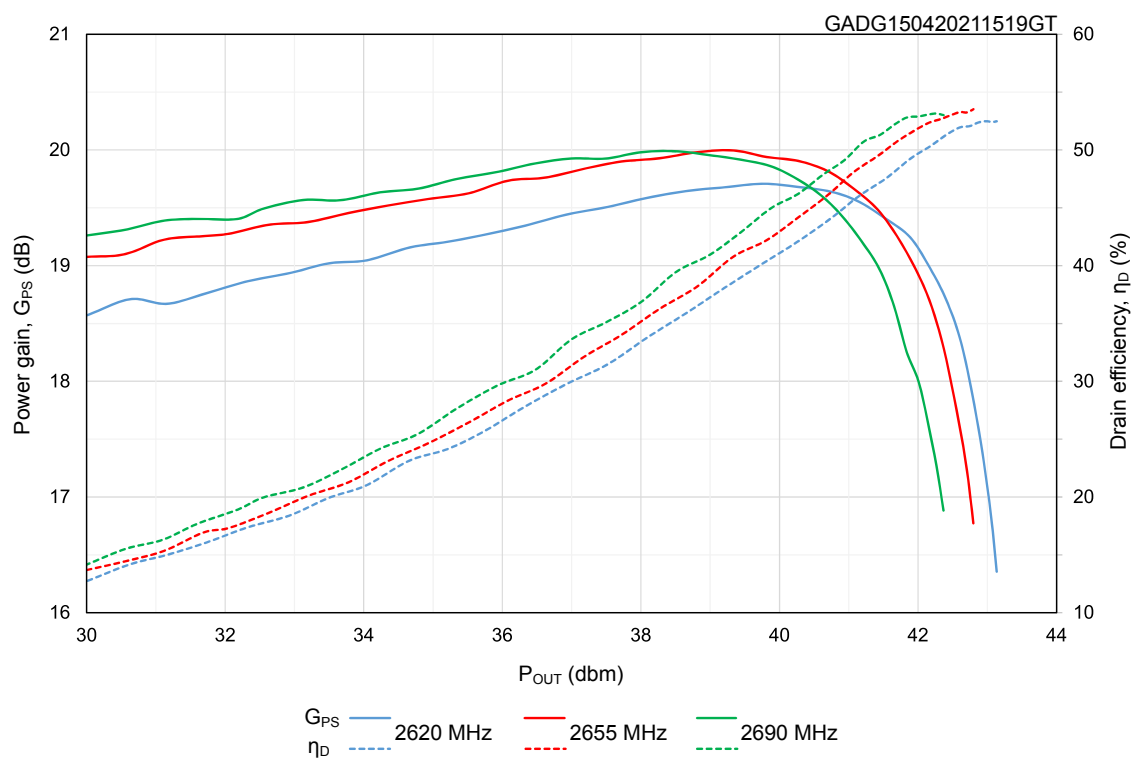
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	Frequency		700		2700	MHz
P_{OUT}	Output power	f = 2690 MHz, at 1dB compression point, pulsed CW		15		W
G_{PS}	Power gain			19		dB
η_D	Drain efficiency			53		%
VSWR	Load mismatch	$P_{OUT} = 15\text{ W}$, pulsed CW, all phases			10:1	

Note: $V_{DD} = 28\text{ V}$, $I_{DQ} = 110\text{ mA}$, $PW = 10\text{ }\mu\text{s}$, duty cycle = 12%.

3 Typical performances

Table 6. Typical performance vs frequency (2620 to 2690 MHz)

f (MHz)	P _{1dB} (dBm)	G _{PS} @ P _{1dB} (dB)	P _{3dB} (dBm)	η _D @P _{3dB} (%)
2620	42.4	18.7	43.1	52.4
2655	41.9	19	42.9	53.5
2690	41.4	18.9	42.3	53

Figure 1. Power gain and drain efficiency vs output power (2620 to 2690 MHz)


Note: $V_{DD} = 28\text{ V}$, $I_{DQ} = 110\text{ mA}$, pulsed CW, pulse width = 10 μs , duty cycle = 12%.

4 Test circuits

Figure 2. Test circuit (same PCB layout with different BOM for each frequency band)

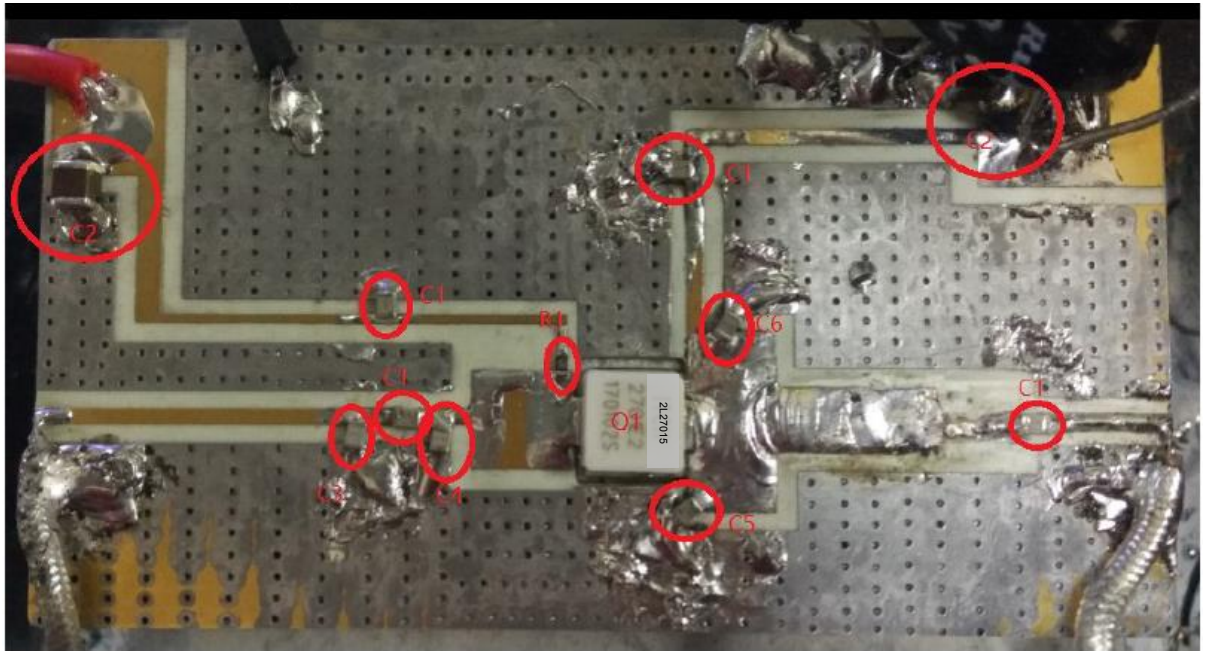


Table 7. List of components (2620 - 2690 MHz frequency band)

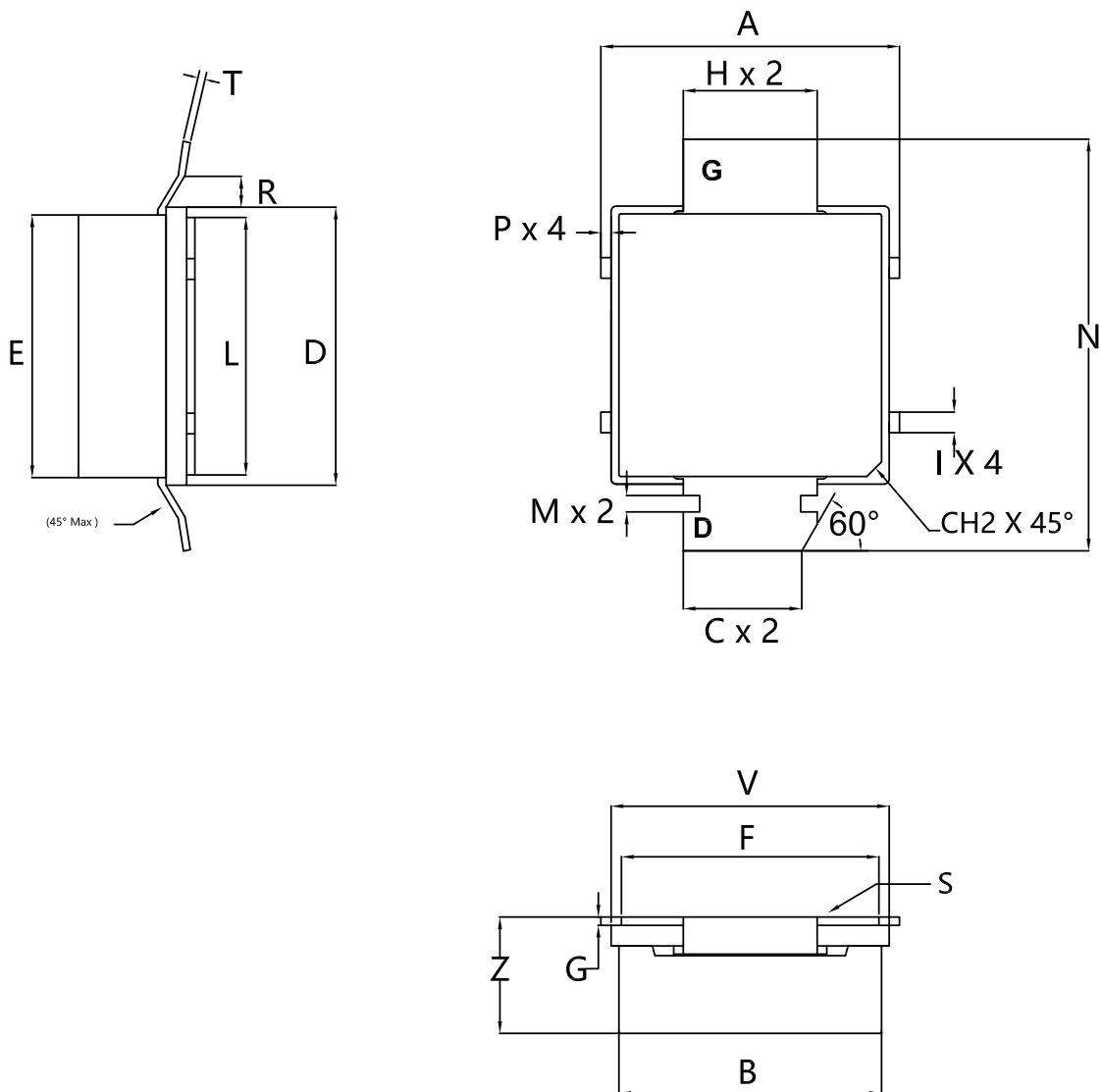
Component	Value	Size	Reference
Q1	RF2L27015CG2		
C1	10 pF	0805	ATC600F
R1	10 Ω	0603	chip resistor
C2	10 μ F	1210	ceramic multilayer capacitor
C3	0.4 pF	0805	ATC600F
C4	1.2 pF	0805	ATC600F
C5	1.2 pF	0805	ATC600F
C6	1.5 pF	0805	ATC600F
PCB	0.508 mm (0.020") thick, $\epsilon_r = 3.48$, Rogers RO4350B, 1 oz. copper		

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 E2 package information

Figure 3. E2 package outline



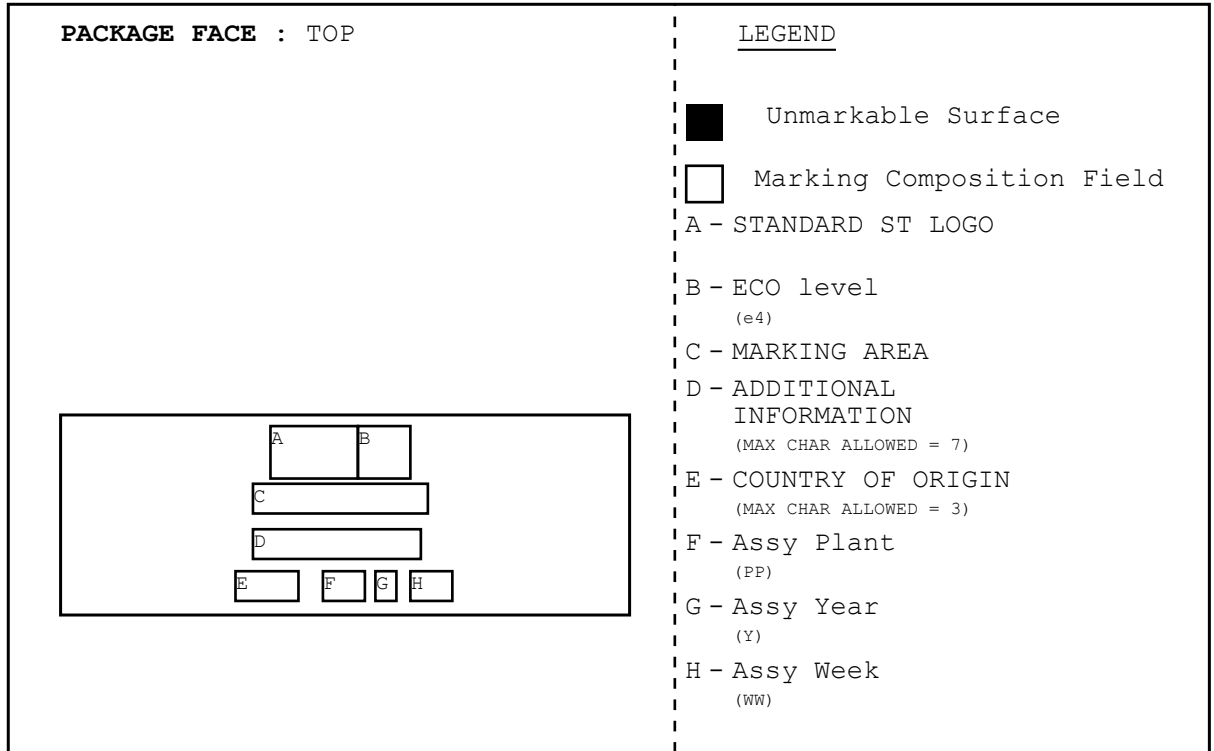
00418523_4

Table 8. E2 mechanical data

Symbol	Millimetres		
	Min.	Typ.	Max.
A			7.37
B	6.35	6.48	6.60
C	2.84	2.92	3.0
D	6.78	6.86	6.94
E	6.35	6.48	6.61
F	6.10	6.35	6.60
G	0.18	0.20	0.23
H	3.23	3.30	3.38
I	0.43	0.51	0.59
L	6.27	6.35	6.43
M	0.33	0.41	0.49
N	10.03	10.16	10.29
P			0.25
R	0.76		1.02
T	0.13	0.18	0.23
V	6.78	6.86	6.94
Z	2.49	2.87	3.25
CH2		0.51	

5.2 Marking information

Figure 4. Marking composition



GADG040220211644GT

Revision history

Table 9. Document revision history

Date	Revision	Changes
10-Jul-2020	1	First release.
19-Apr-2021	2	Updated <i>Features</i> and <i>Device summary</i> in cover page. Updated <i>Section 1 Electrical ratings</i> . Updated <i>Table 4. Static</i> . Updated <i>Figure 1. Power gain and drain efficiency vs output power (2620 to 2690 MHz)</i> . Updated <i>Section 4 Test circuits</i> . Added <i>Section 5.2 Marking information</i> . Minor text changes.
27-Sep-2021	3	Updated <i>Features</i> in cover page. Updated <i>Table 4. Static</i> .

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