



# QPA9143

## 2.3 – 3.8 GHz 100Ω Differential Input Gain Block

### Product Overview

The QPA9143 is a 100Ω differential input to 50Ω single ended output, wideband gain block. It is well suited as the 5G m-MIMO BTS Tx path first gain stage, to directly interface with the DAC of the transceiver, eliminating the need for a discrete balun.

This amplifier delivers exceptional performance with 18 dB of small signal gain and 35 dBm output 3<sup>rd</sup> order intercept (OIP3). The amplifier has excellent gain flatness of 0.5 dB over any 400 MHz bandwidth and a CMRR of 35dB. The amplifier features a shut-down function through V<sub>PD</sub> pin control.

The QPA9143 is optimized over 2.3-3.8GHz band and is housed in a compact 2X2mm SMT package

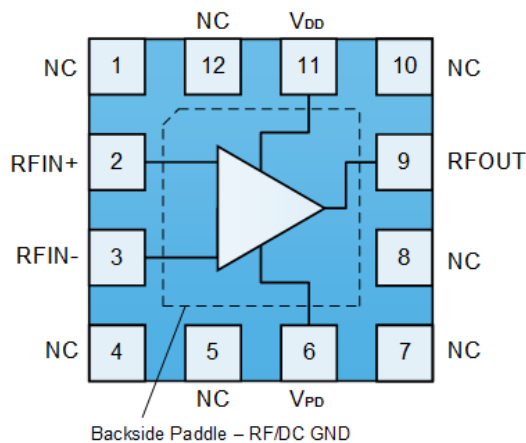


12-pin, 2 x 2 mm SMT Package

### Key Features

- 2.3 – 3.8 GHz Operational Frequency
- 100 Ohm Differential Input
- 50 Ohm Single Ended Output
- +35 dBm OIP3
- 18 dB Gain
- Small 2 x 2 mm SMT Package

### Functional Block Diagram



Top View

### Applications

- 5G m-MIMO
- Mobile Infrastructure
- General Purpose Wireless
- TDD / FDD System

### Ordering Information

Part No.	Description
QPA9143TR7	2500 pcs on 7" reel (standard)
QPA9143EVB-01	Differential Input Evaluation Board

## Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to +150°C
RF Input Power, CW, 50 Ω, T=25 °C	22 dBm
Device Voltage (V <sub>DD</sub> )	7 V
Dissipated Power (P <sub>Diss</sub> )	0.7 W

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability.

## Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Device Voltage (V <sub>DD</sub> )	+3.3	+5	+5.25	V
T <sub>CASE</sub>	-40		+105	°C
T <sub>j</sub> for >10 <sup>6</sup> hours MTTF			+190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

## Electrical Specifications

Parameter	Conditions <sup>(1)</sup>	Min	Typ	Max	Units
Operational Frequency Range		2300		3800	MHz
Test Frequency			2600		MHz
Small Signal Gain	With ideal balun at differential port	16	18	20	dB
Gain Flatness	Any 400 MHz BW within band		0.5		dB
Input Return Loss <sup>(2)</sup>	Differential, 100 Ω		8.5		dB
Output Return Loss			9		dB
Output P1dB		+16	+19.5		dBm
Output IP3	P <sub>out</sub> = -1 dBm/tone, Δf = 1 MHz	+29	+35		dBm
CMRR <sup>(2)</sup>			35		dB
Input Impedance	Differential		100		Ω
Noise Figure	Input balun and trace losses deducted		1.9		dB
Device Current, ON	V <sub>PD</sub> = 0.63 V		70	110	mA
Device Current, OFF	V <sub>PD</sub> = 1.17 V		4		mA
V <sub>PD</sub> , Logic Low		0		0.63	V
V <sub>PD</sub> , Logic High		1.17		V <sub>DD</sub>	V
Switching Time	50% DC to 10/90% RF		70		nsec
Thermal Resistance, θ <sub>Jc</sub>	Junction to case		50		°C/W

Notes:

1. Test conditions unless otherwise noted: V<sub>DD</sub> = +5.0 V, V<sub>PD</sub> = +0.63 V, Temp = +25 °C, 50 Ω system.
2. Calculated from 3 port S-parameters.

## Logic Table

Parameter, V <sub>PD</sub>	High	Low
Device State	OFF	ON

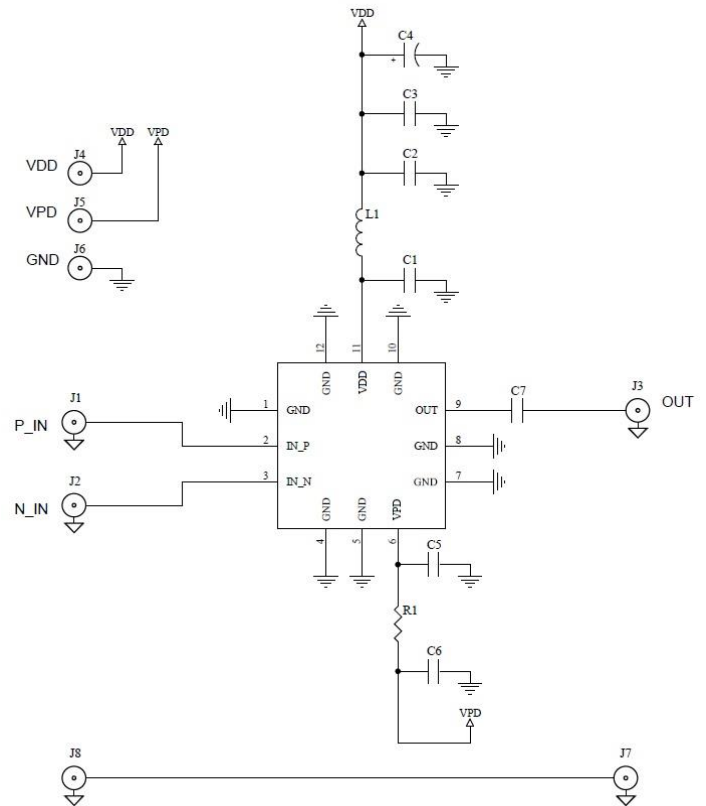
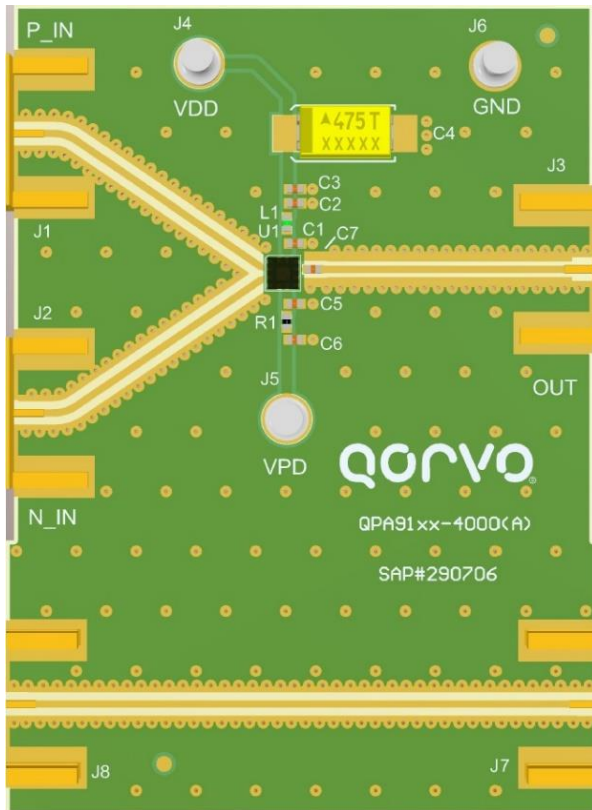
## Typical Performance – QPA9143EVB-01

Parameter	Conditions <sup>(1)</sup>	Typical Value					Units
Frequency		2300	2700	3400	3600	3800	MHz
Gain <sup>(2)</sup>		17.2	18.1	19.2	19.1	18.8	dB
Input Return Loss <sup>(3)</sup>	Differential, 100 Ω	7.0	9.0	10.0	9.4	8.6	dB
Output Return Loss		7.3	9.8	15.0	12.2	8.9	dB
Output P1dB		19.2	19.2	19.7	19.3	19.3	dBm
Output IP3	Pout = -1 dBm/tone, Δf = 1 MHz	35.1	35.2	35.0	34.9	34.5	dBm

**Notes:**

1. Test conditions unless otherwise noted:  $V_{DD} = +5.0\text{ V}$ ,  $V_{PD} = +0.63\text{ V}$ ,  $I_{DD} = 73\text{ mA}$ , Temp = +25 °C, 50 Ω system.
2. With idea balun on differential port.
3. Calculated from 3 port S-Parameters.

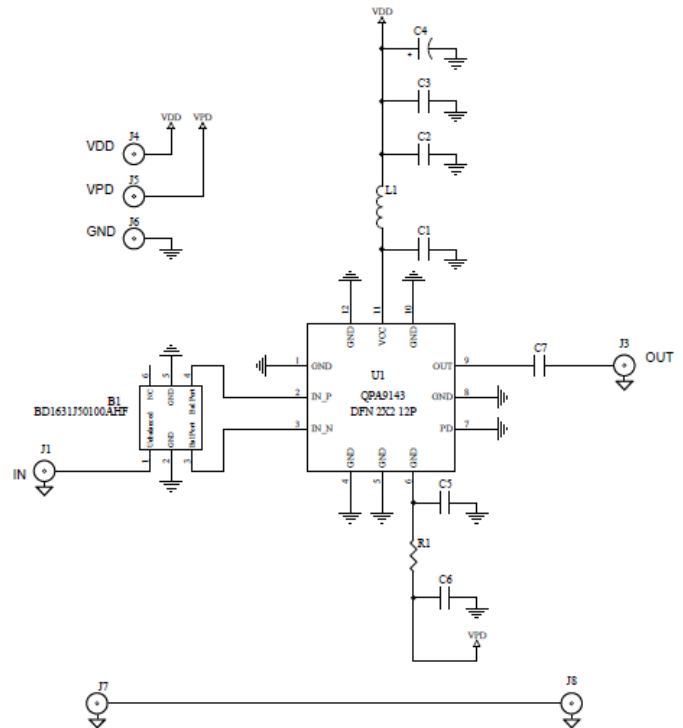
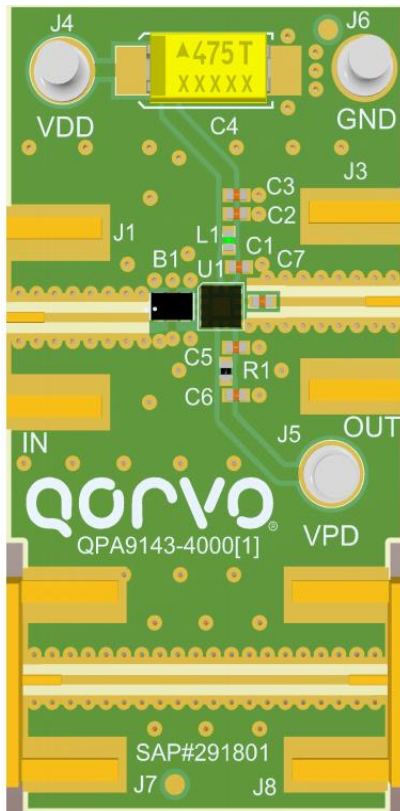
## Evaluation Board - QPA9143EVB-01



## Bill of Materials

Reference Des.	Value	Description	Manuf.	Part Number
n/a	-	Printed Circuit Board	Qorvo	
U1	-	Differential Input Tx Gain Block	Qorvo	QPA9143
C4	10 $\mu$ F	CAP, 20%, 25V, Tantalum, 6032	Cal-Chip	TCMIE106CT
C2	1000 pF	CAP, 10%, 50V, X7R, 0402	Various	
C7	100 pF	CAP, 5%, 50V, C0G, 0402	Murata	GRM1555C1H101JA01D
C3	0.1 $\mu$ F	CAP, 10%, 50V, X5R, 0402	Various	
R1	0 $\Omega$	RES, 1/10W, 0402	Various	
L1	2 nH	IND, Thin Film, 0402	Murata	LQP15MN2N0B02D
J1, J2, J3	-	Conn, SMA F STRT .062"	Cinch Connectivity	142-0701-851

## Evaluation Board with Input Balun

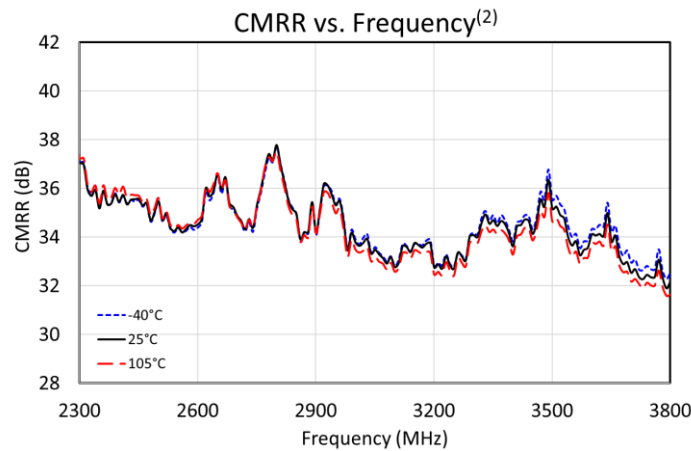
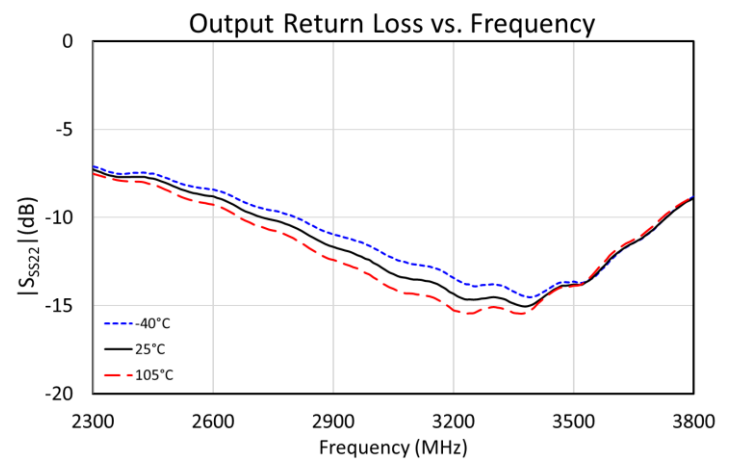
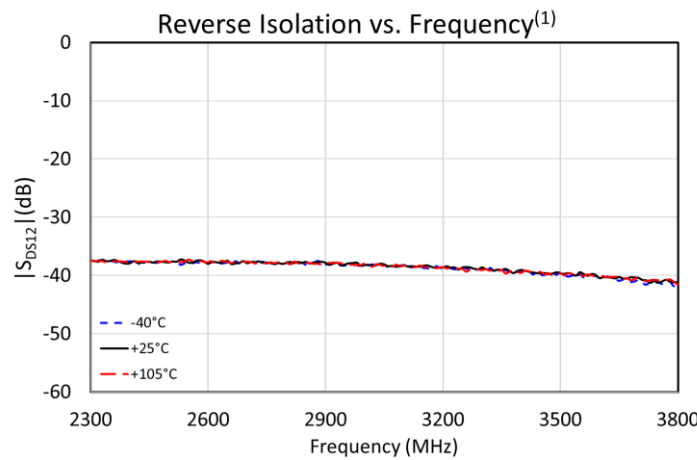
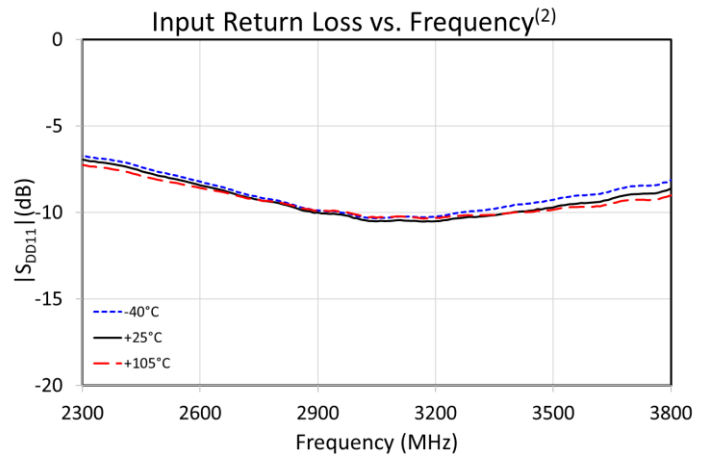
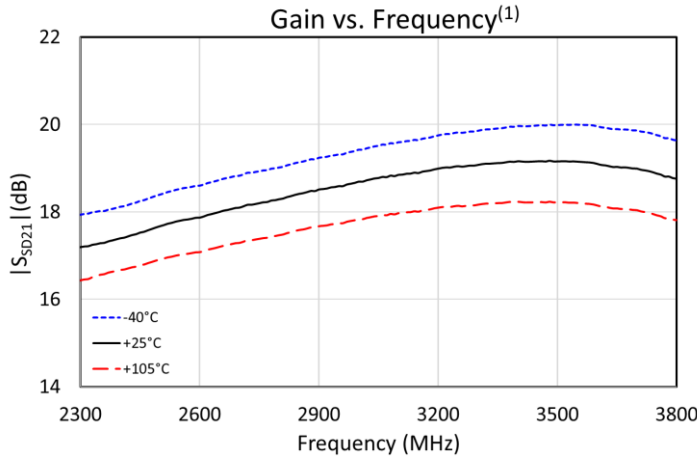


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C2	1000 pF	CAP, 10%, 50V, X7R, 0402	Various	
C7	100 pF	CAP, 5%, 50V, C0G, 0402	Murata	GRM1555C1H101JA01D
C3	0.1 $\mu$ F	CAP, 10%, 50V, X5R, 0402	Various	
R1	0 $\Omega$	RES, 1/10W, 0402	Various	
B1	-	BALUN, RF, 1.6GHz-3.1GHz, 500/100, 0805	Anaren	BD1631J50100AHF
L1	2 nH	IND, Thin Film, 0402	Murata	LQP15MN2N0B02D
J1, J2, J3	-	CON, SMA F STRT .062"	Cinch Connectivity	142-0701-851

## Performance Plots – QPA9143EVB-01

Test conditions unless otherwise noted:  $V_{DD}$  on EVB = +5.0 V,  $V_{PD}$  = +0.63 V, 50 Ω system.

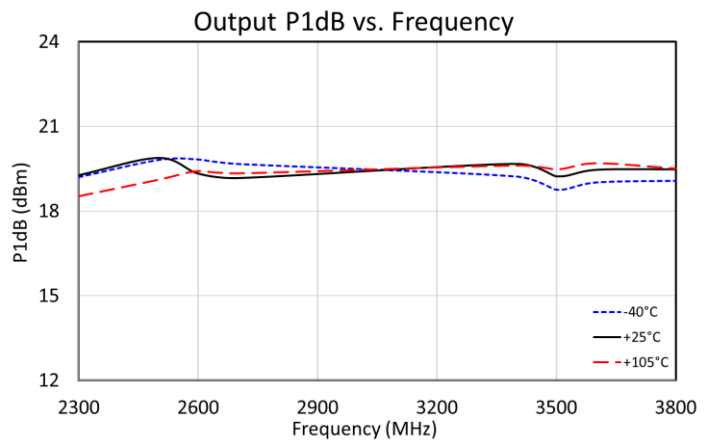
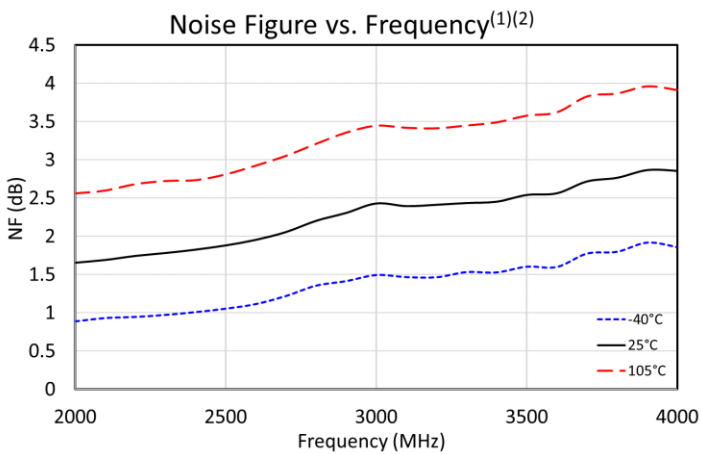
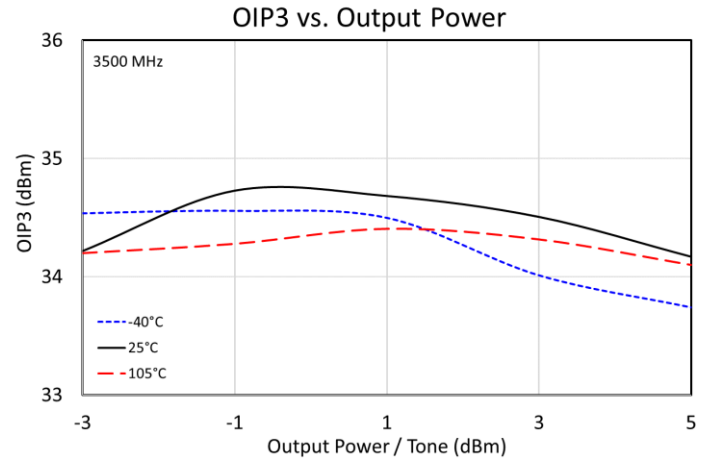
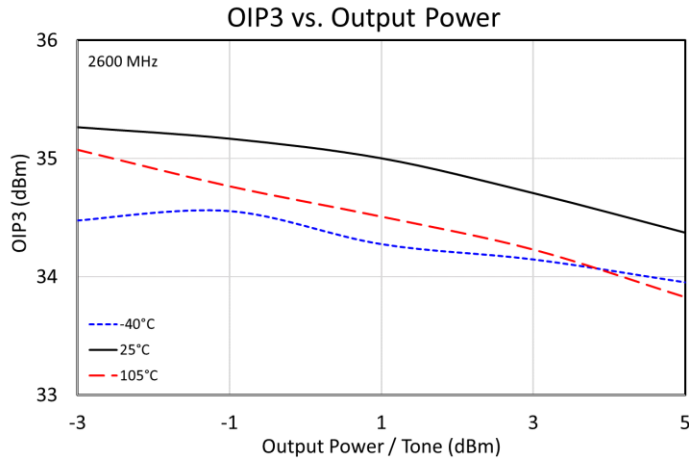


Notes:

1. With ideal balun at differential port
2. Calculated from 3-port S-Parameters.

## Performance Plots – QPA9143EVB-01 (Contd.)

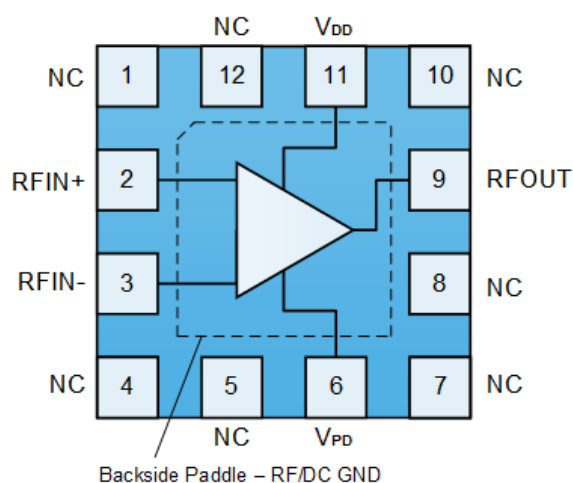
Test conditions unless otherwise noted:  $V_{DD}$  on EVB = +5.0 V,  $V_{PD}$  = +0.63 V. With ideal balun on differential port.



**Notes:**

1. NF measured with Anaren BD1631J50100AHF balun for 2000-3000 MHz and Anaren BD3150N50100AHF balun for 3000-4000 MHz.
2. Trace loss and balun de-embedded in NF vs Frequency

## Pad Configuration and Description



Top View

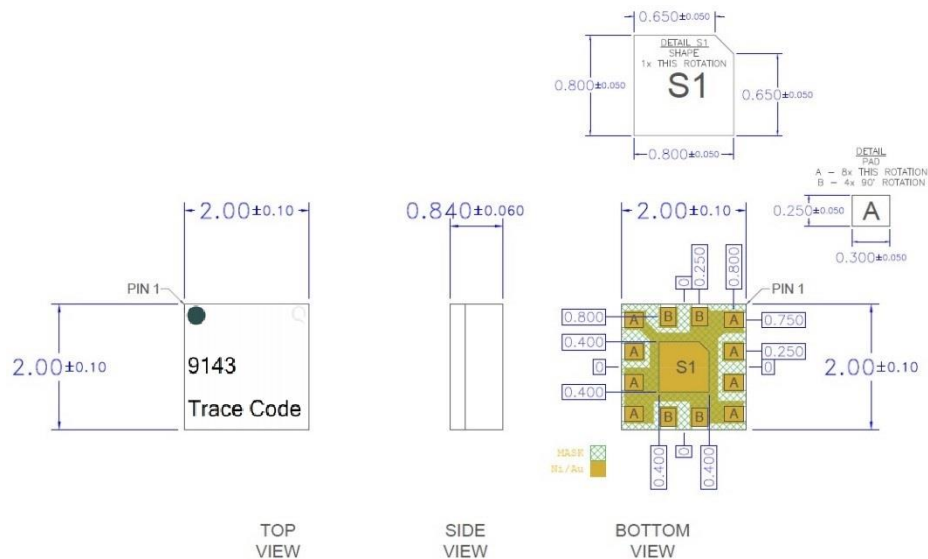
Pad No.	Label	Description
1, 4, 5, 7, 8, 10, 12	NC	No electrical connection internally. It may be left floating or connected to ground. Land pads should be provided for PCB mounting integrity.
2	RFIN+	Differential input +. Requires external DC blocking capacitor if DC is present on this pin.
3	RFIN-	Differential input -. Requires external DC blocking capacitor if DC is present on this pin.
6	V <sub>PD</sub>	Power down amplifier bias voltage (regulated internally).
9	RFOUT	Single-ended output. Internally matched to 50ohm. Requires external DC blocking capacitor.
11	V <sub>DD</sub>	Power supply voltage for amplifier.
Backside Paddle	-	RF/DC Ground, Use recommended via hole pattern to minimize inductance and thermal resistance. See PCB mounting pattern for suggested for suggested PCB layout.



## Package Marking and Dimensions

Marking: Part Number – 9143

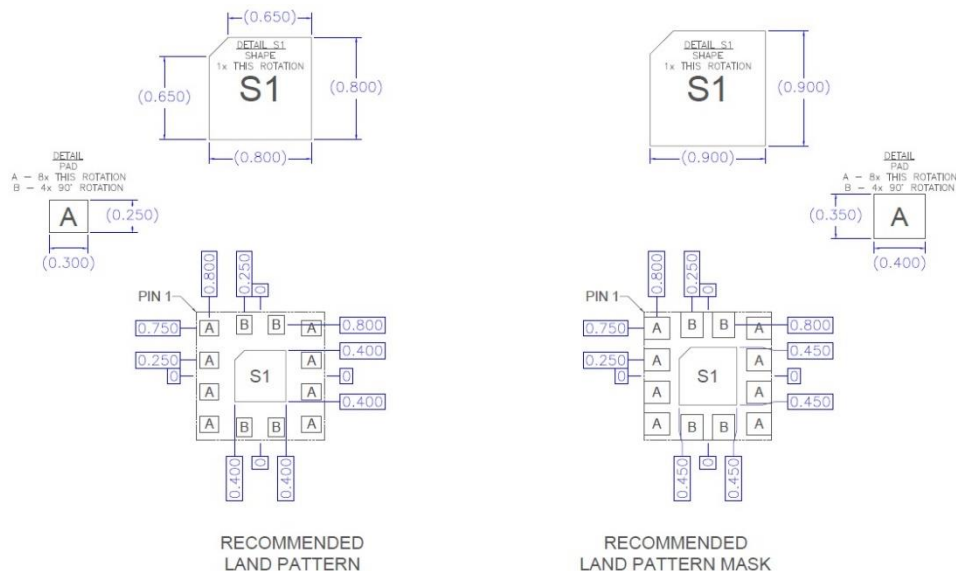
Trace Code – assigned by sub-contractor



### Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. The terminal #1 identifier and terminal numbering conform to SPE-000677.
3. Contact plating: ENEPIG

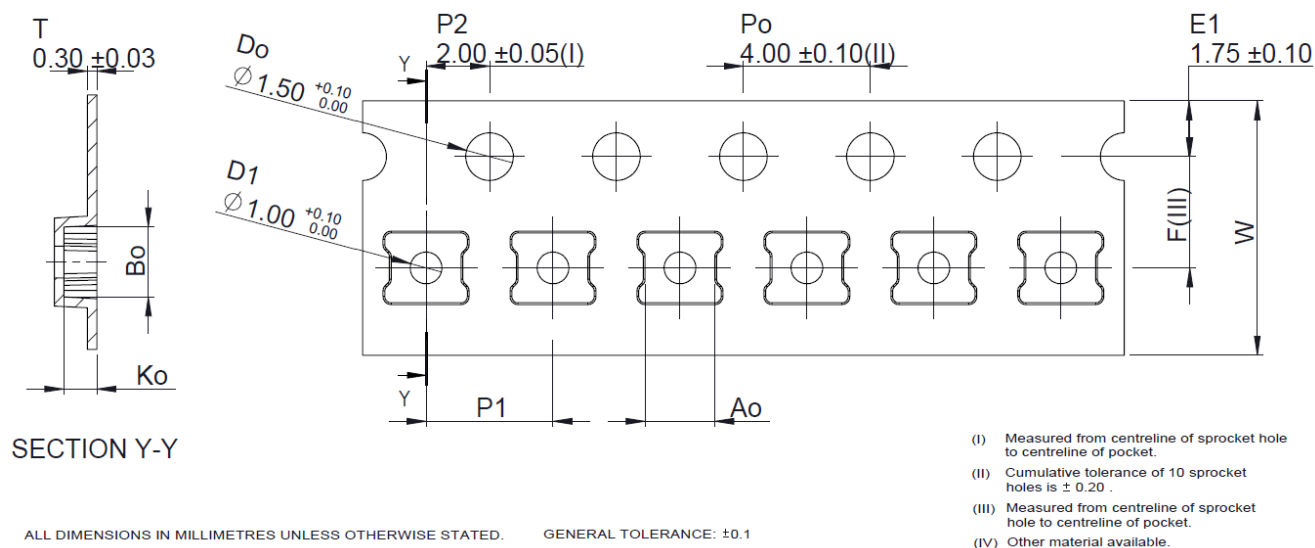
## Recommended PCB Layout Pattern



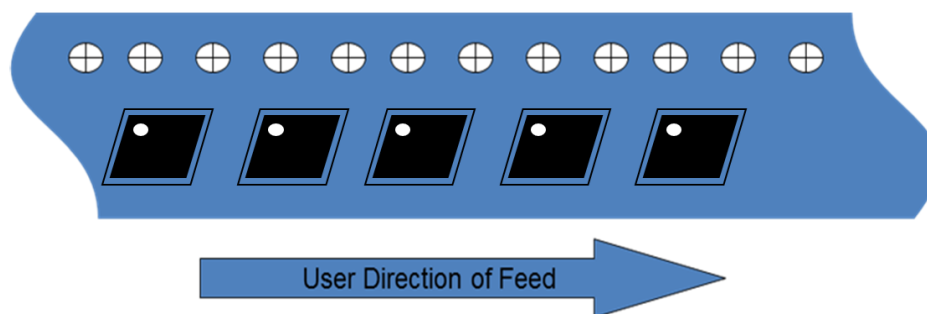
### Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.01").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

## Tape and Reel Information – Carrier and Cover Tape Dimensions

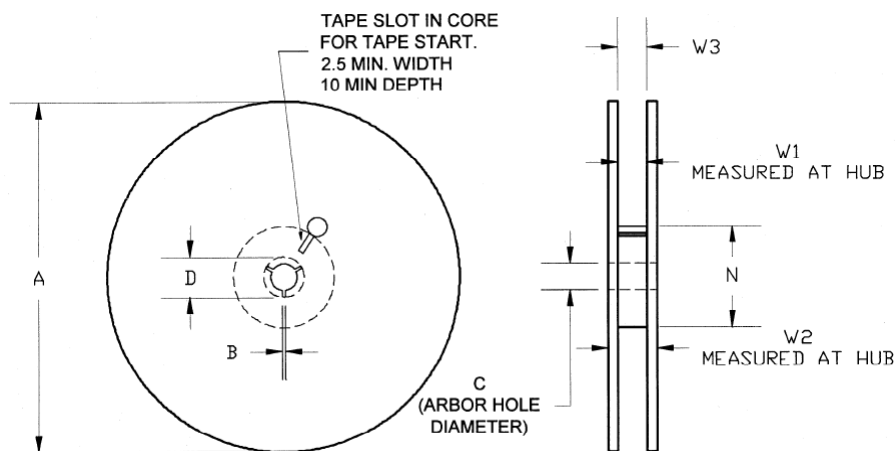


Feature	Measure	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.087	2.20
	Width	B0	0.087	2.20
	Depth	K0	0.041	1.04
	Pitch	P1	0.157	4.00
Centerline Distance	Cavity to Perforation - Length Direction	P2	0.079	2.00
	Cavity to Perforation - Width Direction	F	0.138	3.50
Cover Tape	Width	C	0.362	9.20
Carrier Tape	Width	W	0.315	8.00



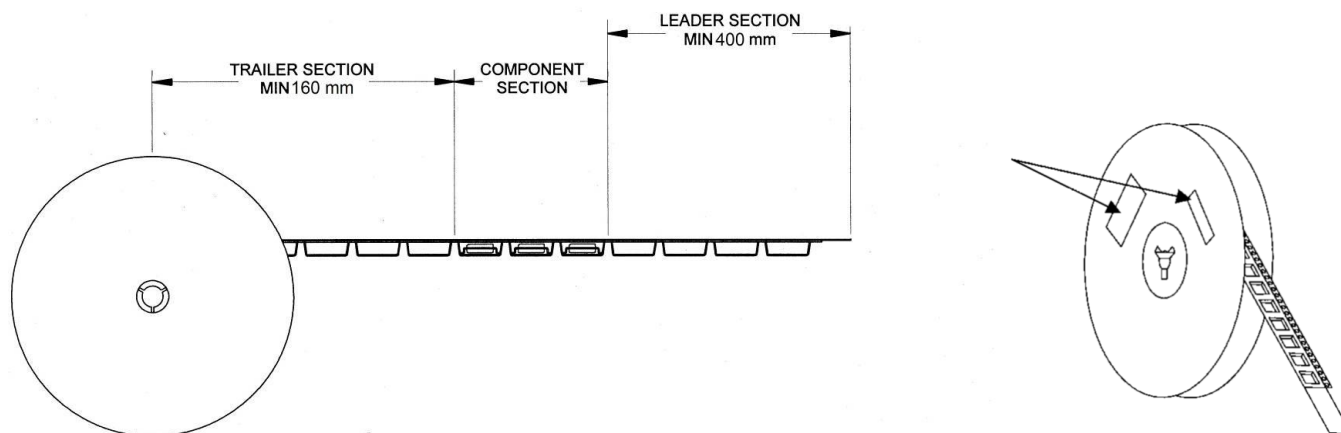
## Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 7" reel.



Feature	Measure	Symbol	Size (in)	Size (mm)
Flange	Diameter	A	6.969	177.0
	Thickness	W2	0.559	14.2
	Space Between Flange	W1	0.346	8.8
Hub	Outer Diameter	N	2.283	58.0
	Arbor Hole Diameter	C	0.512	13.0
	Key Slit Width	B	0.079	2.0
	Key Slit Diameter	D	0.787	20.0

## Tape and Reel Information – Tape Length and Label Placement



### Notes:

1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.

## Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA / JEDEC JS-001-2017
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020E



Caution!  
ESD-Sensitive Device

## Solderability

Compatible with both lead-free (260°C max. reflow temperature) and tin/lead (245°C max. reflow temperature) soldering processes. Solder profiles available upon request.

Contact plating: ENEPIG

## RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- SVHC Free



## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: [www.qorvo.com](http://www.qorvo.com)

Tel: 1-844-890-8163

Email: [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

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