

# NTS0302

2-bit dual supply translating transceiver; open drain; auto direction sensing

Rev. 1 — 17 June 2019

Product data sheet

## 1. General description

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The NTS0302 is a 2-bit, dual supply translating transceiver family with auto direction sensing, that enables bidirectional voltage level translation. It features two 1-bit input-output ports (A and B), one output enable input (OE) and two supply pins ( $V_{CC(A)}$  and  $V_{CC(B)}$ ).  $V_{CC(A)}$  can be supplied at any voltage between 0.95 V and 3.6 V.  $V_{CC(B)}$  can be supplied at any voltage between 1.65 V and 5.5 V. This flexibility makes the device suitable for translating between any of the voltage nodes (0.95 V, 1.2 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins A and OE are referenced to  $V_{CC(A)}$  and pin B is referenced to  $V_{CC(B)}$ . A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state.

## 2. Features and benefits

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- Wide supply voltage range:
  - ◆  $V_{CC(A)}$ : 0.95 V to 3.6 V and  $V_{CC(B)}$ : 1.65 V to 5.5 V
- No power-sequencing required
- Maximum data rate
  - ◆ Open-drain: 2 Mbps
  - ◆ Push-pull: 20 Mbps
- Longer one-shot pulse for driving larger capacitive loads with much reduced ringing and overshoot
- A-side inputs accept voltages up to 3.6 V
- B-side inputs accept voltages up to 5.5 V
- ESD protection:
  - ◆ HBM JESD22-A114E Class 2 exceeds 2000 V for both ports
  - ◆ CDM JESD22-C101E exceeds 1000 V for both ports
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Available in X2SON8 package
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$

## 3. Applications

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- I<sup>2</sup>C/SMBus, UART
- GPIO



## 4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
NTS0302JK	2x[1]	X2SON8	plastic super thin small outline package; no leads; 8 terminals; 1.4 x 1.0 x 0.32 mm body	SOT1986-1

[1] "x" changes based on date code.

### 4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NTS0302JK	NTS0302JKZ	X2SON8	reel 7" q1/t1 *standard mark	10000	T <sub>amb</sub> = -40 °C to +125 °C

## 5. Functional diagram

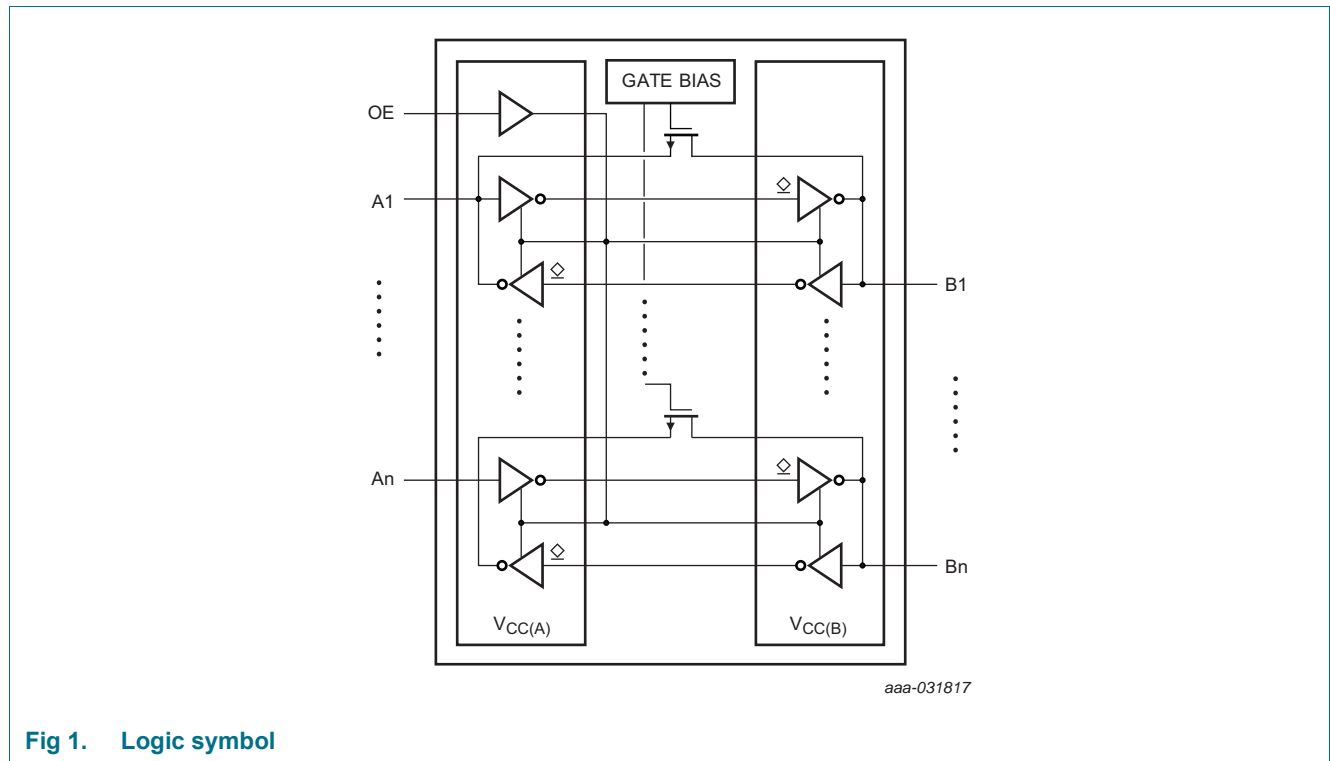
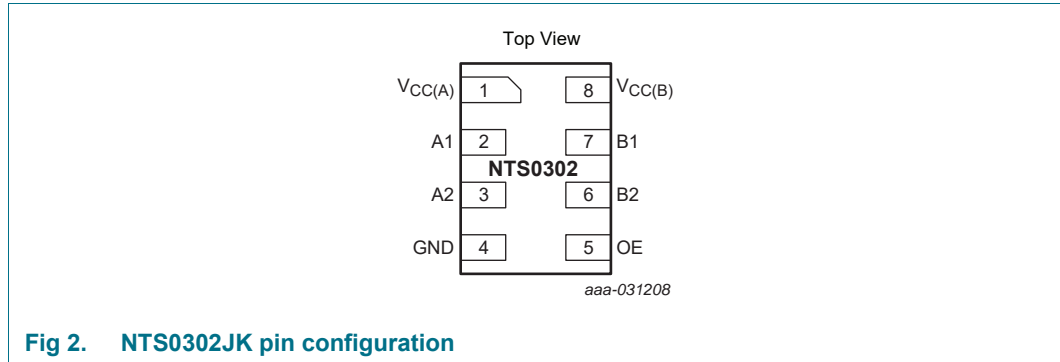


Fig 1. Logic symbol

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

**Table 3. NTS0302 pin description**

Symbol	Pin	Description
$V_{CC(A)}$	1	supply voltage A
A1, A2	2, 3	data input or output (referenced to $V_{CC(A)}$ )
GND	4	ground (0 V)
OE	5	output enable input (active HIGH; referenced to $V_{CC(A)}$ )
B2, B1	6, 7	data input or output (referenced to $V_{CC(B)}$ )
$V_{CC(B)}$	8	supply voltage B

## 7. Functional description

Table 4. Function table<sup>[1]</sup>

Supply voltage		Input	Input/output	
V <sub>CC(A)</sub>	V <sub>CC(B)</sub>	OE	A	B
0.95 V to V <sub>CC(B)</sub>	1.65 V to 5.5 V	L	Z	Z
0.95 V to V <sub>CC(B)</sub>	1.65 V to 5.5 V	H	input or output	output or input
GND <sup>[2]</sup>	GND <sup>[2]</sup>	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] When either V<sub>CC(A)</sub> or V<sub>CC(B)</sub> is at GND level, the device goes into power-down mode.

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC(A)</sub>	supply voltage A		-0.5	+4.6	V
V <sub>CC(B)</sub>	supply voltage B		-0.5	+6.5	V
V <sub>I</sub>	input voltage	A port and OE input <sup>[1][2]</sup>	-0.5	+6.5	V
		B port <sup>[1][2]</sup>	-0.5	+6.5	V
V <sub>O</sub>	output voltage	Active mode <sup>[1][2]</sup>			
		A or B port	-0.5	V <sub>CCO</sub> + 0.5	V
		Power-down or 3-state mode <sup>[1]</sup>			
		A port	-0.5	+4.6	V
	B port	-0.5	+6.5	V	
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CCO</sub> <sup>[2]</sup>	-	±50	mA
I <sub>CC</sub>	supply current	I <sub>CC(A)</sub> or I <sub>CC(B)</sub>	-	100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V<sub>CCO</sub> is the supply voltage associated with the output.

## 9. Recommended operating conditions

Table 6. Recommended operating conditions<sup>[1][2]</sup>

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC(A)</sub>	supply voltage A	<sup>[2]</sup>	0.95	3.6	V
V <sub>CC(B)</sub>	supply voltage B		1.65	5.5	V
V <sub>I_EN</sub>	EN input voltage		-0.3	V <sub>CC(B)</sub> +0.3	V
T <sub>amb</sub>	ambient temperature		-40	+125	°C
T <sub>J</sub>	junction temperature	<sup>[3]</sup>	-40	+125	°C

Table 6. Recommended operating conditions<sup>[1][2]</sup> ...continued

Symbol	Parameter	Conditions	Min	Max	Unit	
$\Delta t/\Delta V$	input transition rise and fall rate	A or B port; push-pull driving				
		$V_{CC(A)} = 0.95\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	[2]	-	10	ns/V
		OE input				
		$V_{CC(A)} = 0.95\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	10	ns/V	

[1] The A and B sides of an unused I/O pair must be held in the same state, both at  $V_{CCI}$  or both at GND.

[2]  $V_{CC(A)}$  must be less than or equal to  $V_{CC(B)}$ .

[3] The  $T_J$  limits shall be supported by proper thermal PCB design taking the power consumption and the thermal resistance as listed in Table 7 into account.

## 10. Thermal characteristics

Table 7. Thermal resistance information

Symbol	Rating	NTS0302JK (X2SON8)
$R_{\theta JA}$	Junction to ambient	174.9 °C/W
$\Psi_{JT}$	Junction to top characterization	15.8 °C/W

## 11. Static characteristics

Table 8. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25\text{ °C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_I$	input leakage current	OE input; $V_I = 0\text{ V to }3.6\text{ V}; V_{CC(A)} = 0.95\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	-	-	$\pm 1$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	A or B port; $V_O = 0\text{ V or }V_{CCO}; V_{CC(A)} = 0.95\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	[1]	-	$\pm 1$	$\mu\text{A}$
$C_I$	input capacitance	OE input; $V_{CC(A)} = 3.3\text{ V}; V_{CC(B)} = 3.3\text{ V}$	-	1	-	pF
$C_{I/O}$	input/output capacitance	A port	-	4	-	pF
		B port	-	7.5	-	pF
		A or B port; $V_{CC(A)} = 3.3\text{ V}; V_{CC(B)} = 3.3\text{ V}$	-	11	-	pF

[1]  $V_{CCO}$  is the supply voltage associated with the output.

Table 9. Typical supply current

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25\text{ °C}$ .<sup>[1]</sup>

$V_{CC(A)}$	$V_{CC(B)}$								Unit
	1.65 V		2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
0.95 V	0.1	0.1	0.1	0.5	0.1	0.5	0.1	3	$\mu\text{A}$
1.2 V	0.1	0.1	0.1	0.5	0.1	0.5	0.1	3	$\mu\text{A}$

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**Table 9. Typical ...continued supply current ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V);  $T_{amb} = 25\text{ }^{\circ}\text{C}$ . [1]

$V_{CC(A)}$	$V_{CC(B)}$								Unit
	1.65 V		2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
1.8 V	-	-	0.1	0.5	0.1	0.5	0.1	3	$\mu\text{A}$
2.5 V	-	-	0.2	0.5	0.1	0.5	0.1	3	$\mu\text{A}$
3.3 V	-	-	-	-	0.1	0.1	0.1	2	$\mu\text{A}$

[1] Device is disabled (OE=0) for table measurements.

**Table 10. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V). [3]

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Max	Min	Max		
$V_{IH}$	HIGH-level input voltage	A port						
		$V_{CC(A)} = 0.95\text{ V to }1.65\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	[1]	$V_{CCI} - 0.2$	-	$V_{CCI} - 0.2$	-	V
		$V_{CC(A)} = 1.65\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$	[1]	$V_{CCI} - 0.4$	-	$V_{CCI} - 0.4$	-	V
		B port						
		$V_{CC(A)} = 0.95\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$	[1]	$V_{CCI} - 0.4$	-	$V_{CCI} - 0.4$	-	V
$V_{IL}$	LOW-level input voltage	OE input						
		$V_{CC(A)} = 0.95\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$		$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V
		A or B port						
		$V_{CC(A)} = 0.95\text{ V to }1.65\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$		-	0.13	-	0.13	V
$V_{OHA}$	HIGH-level output voltage	$V_{CC(A)} = 1.65\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 2.3\text{ V to }5.5\text{ V}$		-	0.15	-	0.15	V
		$I_O = -20\text{ }\mu\text{A}$						
		$V_{CC(B)} = 1.65\text{ V to }5.5\text{ V};$ $V_{CCI} = V_{CC(B)} - 0.4\text{ V}$	[2]					
$V_{OHB}$	HIGH-level output voltage	$V_{CC(A)} = 0.95\text{ V to }1.65\text{ V}$	[2]	$0.65V_{CC(A)}$	-	$0.62V_{CC(A)}$	-	V
		$I_O = -20\text{ }\mu\text{A}$						
		$V_{CC(A)} = 0.95\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V};$ $V_{CCI} = V_{CC(A)} - 0.2\text{ V}$	[2]	$0.8V_{CC(B)}$	-	$0.75V_{CC(B)}$	-	V
$V_{OL}$	LOW-level output voltage	A or B port; $I_O = 1\text{ mA}$	[2]					
		$V_I \leq 0.15\text{ V};$ $V_{CC(A)} = 0.95\text{ V to }3.6\text{ V};$ $V_{CC(B)} = 1.65\text{ V to }5.5\text{ V}$		-	0.30	-	0.30	V

**Table 10. Static characteristics ...continued**At recommended operating conditions; voltages are referenced to GND (ground = 0 V).<sup>[3]</sup>

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Max	Min	Max	
I <sub>I</sub>	input leakage current	OE input; V <sub>I</sub> = 0 V to 3.6 V; V <sub>CC(A)</sub> = 0.95 V to 3.6 V; V <sub>CC(B)</sub> = 1.65 V to 5.5 V	-	±2	-	±12	μA
I <sub>OZ</sub>	OFF-state output current	A or B port; V <sub>O</sub> = 0 V or V <sub>CCO</sub> ; <sup>[2]</sup> V <sub>CC(A)</sub> = 0.95 V to 3.6 V; V <sub>CC(B)</sub> = 1.65 V to 5.5 V	-	±2	-	±12	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = 0 V or V <sub>CCI</sub> ; I <sub>O</sub> = 0 A <sup>[1]</sup>					
		I <sub>CC(A)</sub>					
		V <sub>CC(A)</sub> = 0.95 V to 3.6 V; V <sub>CC(B)</sub> = 1.65 V to 5.5 V	-	2.4	-	15	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	2.2	-	15	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 5.5 V	-	-1	-	-8	μA
		I <sub>CC(B)</sub>					
		V <sub>CC(A)</sub> = 0.95 V to 3.6 V; V <sub>CC(B)</sub> = 1.65 V to 5.5 V	-	18	-	51	μA
		V <sub>CC(A)</sub> = 3.6 V; V <sub>CC(B)</sub> = 0 V	-	-1	-	-5	μA
		V <sub>CC(A)</sub> = 0 V; V <sub>CC(B)</sub> = 5.5 V	-	18	-	46	μA
I <sub>CC(A)</sub> + I <sub>CC(B)</sub>							
V <sub>CC(A)</sub> = 0.95 V to 3.6 V; V <sub>CC(B)</sub> = 1.65 V to 5.5 V	-	14.4	-	59	μA		

[1] V<sub>CCI</sub> is the supply voltage associated with the input.[2] V<sub>CCO</sub> is the supply voltage associated with the output.

[3] Device is disabled (OE=0) for table measurements.

## 12. Dynamic characteristics

**Table 11. Dynamic characteristics for temperature range  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$ <sup>[1]</sup>**

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 5](#); for wave forms, see [Figure 3](#) and [Figure 4](#).

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			1.8 V		3.3 V		5.0 V		
			Min	Max	Min	Max	Min	Max	
<b><math>V_{CC(A)} = 0.95\text{V}</math></b>									
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	20	-	11.1	-	12.3	ns
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	14.8	-	12.5	-	12.2	ns
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	9.2	-	5.2	-	5.2	ns
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	8.8	-	2.9	-	1.4	ns
$t_{en}$	enable time	OE to A; B	-	200	-	200	-	200	ns
$t_{dis}$	disable time	OE to A; no external load <sup>[2]</sup>	-	100	-	100	-	100	ns
		OE to B; no external load <sup>[2]</sup>	-	100	-	100	-	100	ns
		OE to A	-	250	-	250	-	250	ns
		OE to B	-	220	-	220	-	220	ns
$t_{TLH}$	LOW to HIGH output transition time	A port	6.0	15.3	2.2	15.1	1.8	11.1	ns
		B port	6.0	17.0	4.0	14.0	4.0	20.0	ns
$t_{THL}$	HIGH to LOW output transition time	A port	0.9	18.0	0.7	9.0	0.6	9.0	ns
		B port	1.6	22.0	2.8	10.7	3.2	14.2	ns
$t_W$	pulse width	data inputs	49	-	49	-	49	-	ns
$f_{data}$	data rate	<sup>[3]</sup>	-	20	-	20	-	20	Mbps

[1]  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .

$t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

[2] Delay between OE going LOW and when the outputs are disabled.

[3] Assuming a maximum one-shot accelerator pulse length of 50ns and equal time for 1 and 0 bit information.



2-bit dual supply translating transceiver; open drain; auto direction sensing

**Table 12. Dynamic characteristics for temperature range  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$  [1]**

Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 5](#); for wave forms, see [Figure 3](#) and [Figure 4](#).

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			2.5 V		3.3 V		5.0 V		
			Min	Max	Min	Max	Min	Max	
<b><math>V_{CC(A)} = 1.8\text{ V}</math></b>									
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	5.8	-	5.9	-	7.3	ns
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	8.5	-	8.5	-	8.8	ns
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	5.5	-	5.7	-	5.9	ns
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	6.7	-	5.7	-	1.4	ns
$t_{en}$	enable time	OE to A; B	-	200	-	200	-	200	ns
$t_{dis}$	disable time	OE to A; no external load [2]	-	100	-	100	-	100	ns
		OE to B; no external load [2]	-	100	-	100	-	100	ns
		OE to A	-	250	-	250	-	250	ns
		OE to B	-	220	-	220	-	220	ns
$t_{TLH}$	LOW to HIGH output transition time	A port	3.2	11.9	1.2	11.7	1.1	9.5	ns
		B port	3.3	13.5	2.7	14.5	2.7	13.5	ns
$t_{THL}$	HIGH to LOW output transition time	A port	1.2	7.4	1.0	7.5	1.0	16.7	ns
		B port	2.6	9.5	2.2	9.4	2.8	12.5	ns
$t_W$	pulse width	data inputs	49	-	49	-	49	-	ns
$f_{data}$	data rate	[3]	-	20	-	20	-	20	Mbps
<b><math>V_{CC(A)} = 2.5\text{ V}</math></b>									
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	4.0	-	4.2	-	4.3	ns
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	4.4	-	5.2	-	5.5	ns
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	3.8	-	4.5	-	5.4	ns
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	3.2	-	2.0	-	1.5	ns
$t_{en}$	enable time	OE to A; B	-	200	-	200	-	200	ns
$t_{dis}$	disable time	OE to A; no external load [2]	-	100	-	100	-	100	ns
		OE to B; no external load [2]	-	100	-	100	-	100	ns
		OE to A	-	220	-	220	-	220	ns
		OE to B	-	220	-	220	-	220	ns
$t_{TLH}$	LOW to HIGH output transition time	A port	2.8	10	1.4	8.3	1.2	7.8	ns
		B port	3.2	10.4	2.9	15.5	2.4	16.9	ns
$t_{THL}$	HIGH to LOW output transition time	A port	1.0	7.2	1.0	6.9	1.0	6.7	ns
		B port	2.2	9.8	2.4	8.4	2.6	8.3	ns

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**Table 12. Dynamic characteristics for temperature range  $-40\text{ }^{\circ}\text{C}$  to  $+125\text{ }^{\circ}\text{C}$**  [\[1\]](#) ...continued  
 Voltages are referenced to GND (ground = 0 V); for test circuit, see [Figure 5](#); for wave forms, see [Figure 3](#) and [Figure 4](#).

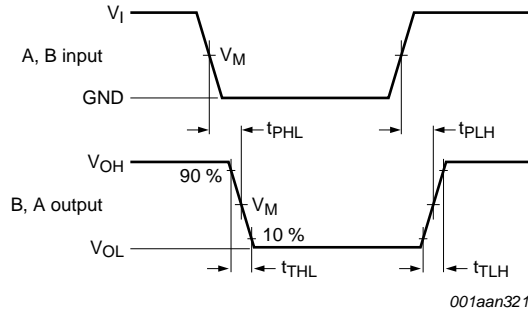
Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			2.5 V		3.3 V		5.0 V		
			Min	Max	Min	Max	Min	Max	
$t_W$	pulse width	data inputs	49	-	49	-	49	-	ns
$f_{data}$	data rate	<a href="#">[3]</a>	-	20	-	20	-	20	Mbps
<b><math>V_{CC(A)} = 3.3\text{ V}</math></b>									
$t_{PHL}$	HIGH to LOW propagation delay	A to B	-	-	-	3.0	-	3.9	ns
$t_{PLH}$	LOW to HIGH propagation delay	A to B	-	-	-	5.3	-	5.5	ns
$t_{PHL}$	HIGH to LOW propagation delay	B to A	-	-	-	3.2	-	4.2	ns
$t_{PLH}$	LOW to HIGH propagation delay	B to A	-	-	-	3.2	-	3.3	ns
$t_{en}$	enable time	OE to A; B	-	-	-	200	-	200	ns
$t_{dis}$	disable time	OE to A; no external load <a href="#">[2]</a>	-	-	-	100	-	100	ns
		OE to B; no external load <a href="#">[2]</a>	-	-	-	100	-	100	ns
		OE to A	-	-	-	280	-	280	ns
		OE to B	-	-	-	220	-	220	ns
$t_{TLH}$	LOW to HIGH output transition time	A port	-	-	1.2	13.1	1.1	7.4	ns
		B port	-	-	2.5	14.2	2.1	16.0	ns
$t_{THL}$	HIGH to LOW output transition time	A port	-	-	1.0	6.8	1.0	6.3	ns
		B port	-	-	2.3	9.3	2.4	9.5	ns
$t_W$	pulse width	data inputs	-	-	49	-	49	-	ns
$f_{data}$	data rate	<a href="#">[3]</a>	-	-	-	20	-	20	Mbps

[1]  $t_{en}$  is the same as  $t_{PZL}$  and  $t_{PZH}$ .  
 $t_{dis}$  is the same as  $t_{PLZ}$  and  $t_{PHZ}$ .

[2] Delay between OE going LOW and when the outputs are disabled.

[3] Assuming a maximum one-shot accelerator pulse length of 50ns and equal time for 1 and 0 bit information.

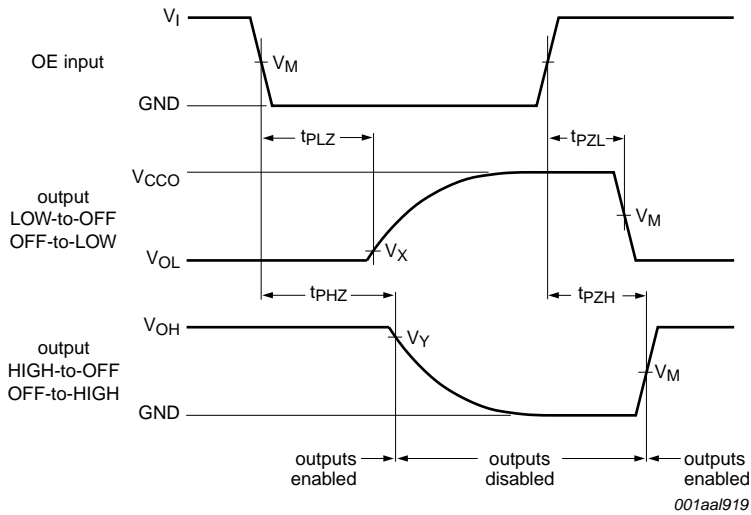
13. Waveforms



Measurement points are given in [Table 13](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 3. The data input (A, B) to data output (B, A) propagation delay times**



Measurement points are given in [Table 13](#).

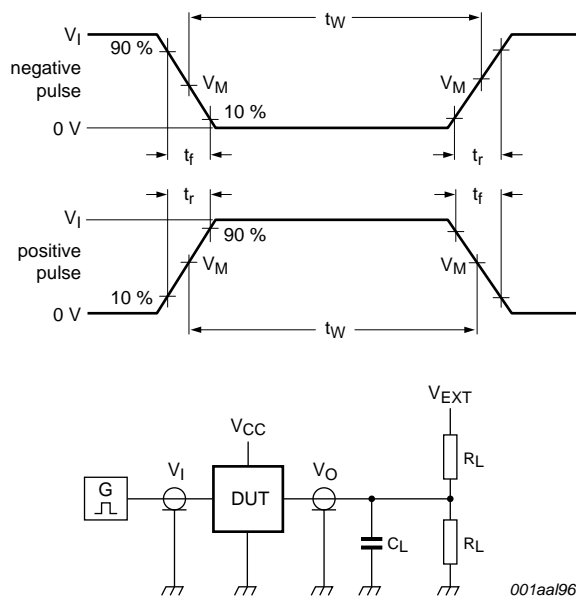
$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 4. Enable and disable times**

Table 13. Measurement points<sup>[1][2]</sup>

Supply voltage	Input	Output		
V <sub>CCO</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
0.95 V	0.5V <sub>CCI</sub>	0.5V <sub>CCO</sub>	V <sub>OL</sub> + 0.1 V	V <sub>OH</sub> - 0.1 V
1.8 V ± 0.15 V	0.5V <sub>CCI</sub>	0.5V <sub>CCO</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V
2.5 V ± 0.2 V	0.5V <sub>CCI</sub>	0.5V <sub>CCO</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V
3.3 V ± 0.3 V	0.5V <sub>CCI</sub>	0.5V <sub>CCO</sub>	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V
5.0 V ± 0.5 V	0.5V <sub>CCI</sub>	0.5V <sub>CCO</sub>	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V

- [1] V<sub>CCI</sub> is the supply voltage associated with the input.
- [2] V<sub>CCO</sub> is the supply voltage associated with the output.



Test data is given in Table 14.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z<sub>O</sub> = 50 Ω; dV/dt ≥ 1.0 V/ns.

R<sub>L</sub> = Load resistance.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

V<sub>EXT</sub> = External voltage for measuring switching times.

Fig 5. Test circuit for measuring switching times

Table 14. Test data

Supply voltage		Input		Load		V <sub>EXT</sub>		
V <sub>CC(A)</sub>	V <sub>CC(B)</sub>	V <sub>I</sub> <sup>[1]</sup>	Δt/ΔV	C <sub>L</sub>	R <sub>L</sub> <sup>[2]</sup>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PZH</sub> , t <sub>PHZ</sub>	t <sub>PZL</sub> , t <sub>PLZ</sub> <sup>[3]</sup>
0.95 V to 3.6 V	1.65 V to 5.5 V	V <sub>CCI</sub>	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	2V <sub>CCO</sub>

- [1] V<sub>CCI</sub> is the supply voltage associated with the input.
- [2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R<sub>L</sub> = 1 MΩ. For measuring enable and disable times, R<sub>L</sub> = 50 KΩ.
- [3] V<sub>CCO</sub> is the supply voltage associated with the output.

## 14. Application information

### 14.1 Applications

Voltage level-translation applications. The NTS0302 can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is primarily targeted at I<sup>2</sup>C or 2-wire which use open-drain drivers. It may also be used in applications where push-pull drivers are connected to the ports, however the NTB010x or the newer lower voltage NTB030x may be more suitable.

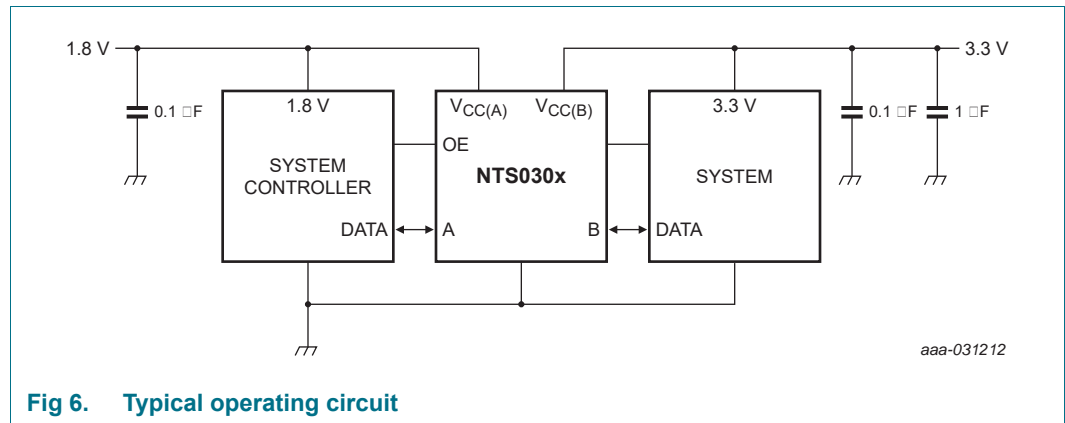


Fig 6. Typical operating circuit

### 14.2 Architecture

The architecture of the NTS0302 is shown in Figure 7. The device does not require an extra input signal to control the direction of data flow from A to B or B to A.

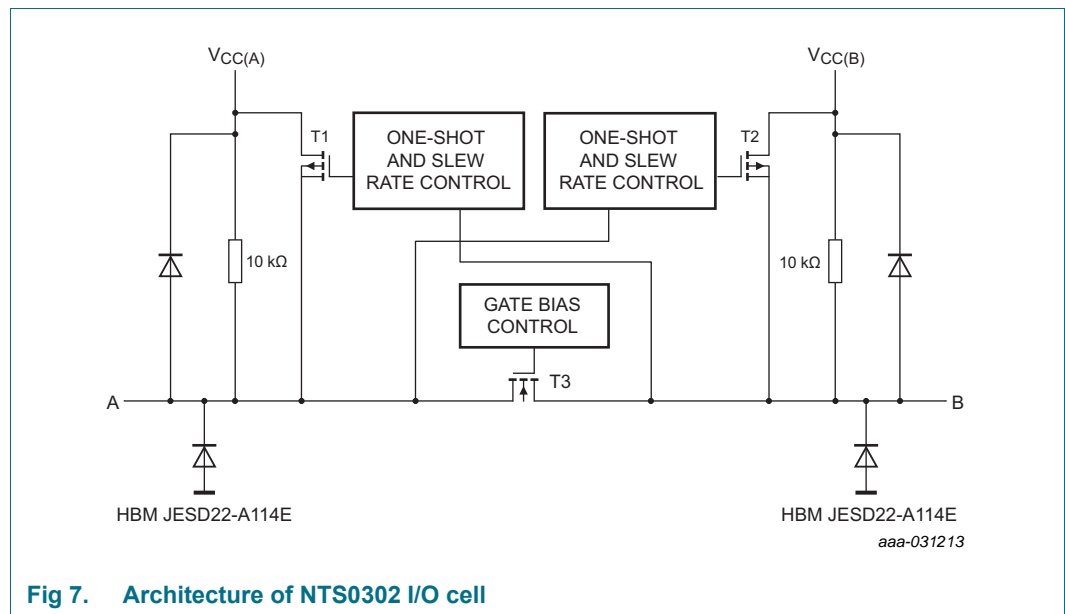


Fig 7. Architecture of NTS0302 I/O cell

The NTS0302 is a “switch” type voltage translator using two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.

2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the  $V_{CC}$  level of the low-voltage side. During a LOW-to-HIGH transition, the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2). It bypasses the 10 k $\Omega$  pull-up resistors and increases the current drive capability. The one-shot is activated once the input transition reaches approximately  $V_{CCI}/2$ ; it is deactivated approximately 50 ns after the output reaches  $V_{CCO}/2$ . During the acceleration time, the driver output resistance is between approximately 50  $\Omega$  and 70  $\Omega$ . To avoid signal contention and minimize dynamic  $I_{CC}$ , the user should wait for the one-shot circuit to turn-off before applying a signal in the opposite direction. Pull-up resistors are included in the device for DC current sourcing capability.

### 14.3 Input driver requirements

As the NTS0302 is a switch type translator, properties of the input driver directly affect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system. The max data rate, HIGH-to-LOW output transition time ( $t_{THL}$ ), and propagation delay ( $t_{PHL}$ ), are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the data sheet assume a driver with output impedance below 50  $\Omega$  is used.

### 14.4 Output load considerations

The maximum lumped capacitive load that can be driven is dependent upon the one-shot pulse duration. In cases with very heavy capacitive loading, there is a risk that the output does not reach the positive rail within the one-shot pulse duration.

To avoid excessive capacitive loading and to ensure correct triggering of the one-shot, use short trace lengths and low capacitance connectors on NTS0302 PCB layouts. The length of the PCB trace should be such that the round-trip delay of any reflection is within the one-shot pulse duration (approximately 50 ns). It ensures low impedance termination and avoids output signal oscillations and one-shot retriggering.

### 14.5 Output single shot slew rate control

Integrated slew-rate control and timed increase of the one-shot driver output current reduce EMI. An additional comparator circuit on the  $V_{OUT}$  side starts to reduce the one-shot driver current when  $V_{OUT} > 0.65V_{OUT}$  with a slight delay, so it can safely drive the output voltage to a safe high-level while at the same time reducing the driver strength early enough to reduce overshoots.

### 14.6 Power-up

During operation,  $V_{CC(A)}$  must never be higher than  $V_{CC(B)}$ . However, during power-up,  $V_{CC(A)} \geq V_{CC(B)}$  does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The NTS0302 includes circuitry that disables all output ports when either  $V_{CC(A)}$  or  $V_{CC(B)}$  is switched off.

### 14.7 Enable and disable

An output enable input (OE) is used to disable the device. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time ( $t_{dis}$  with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time ( $t_{en}$ ) indicates the amount of time the user must allow for one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor. The current-sourcing capability of the driver determines the minimum value of the resistor.

### 14.8 Pull-up or pull-down resistors on I/Os lines

The A port I/O has an internal 10 k $\Omega$  pull-up resistor to  $V_{CC(A)}$ . The B port I/O has an internal 10 k $\Omega$  pull-up resistor to  $V_{CC(B)}$ . If a smaller value of pull-up resistor is required, add an external resistor in parallel to the internal 10 k $\Omega$ . This pull-up resistor affects the  $V_{OL}$  level. When OE goes LOW, the internal pull-ups of the NTS0302 are disabled.

### 14.9 ESD protection on I/Os lines

The NTS0302 contains rail to rail ESD protection structures connecting the A and B I/O to their respective supply. As a consequence, if a supply pin is pulled LOW, the related I/Os are also pulled LOW through the upper ESD protection diode and the 10 k $\Omega$  pull-up resistor.

15. Package outline

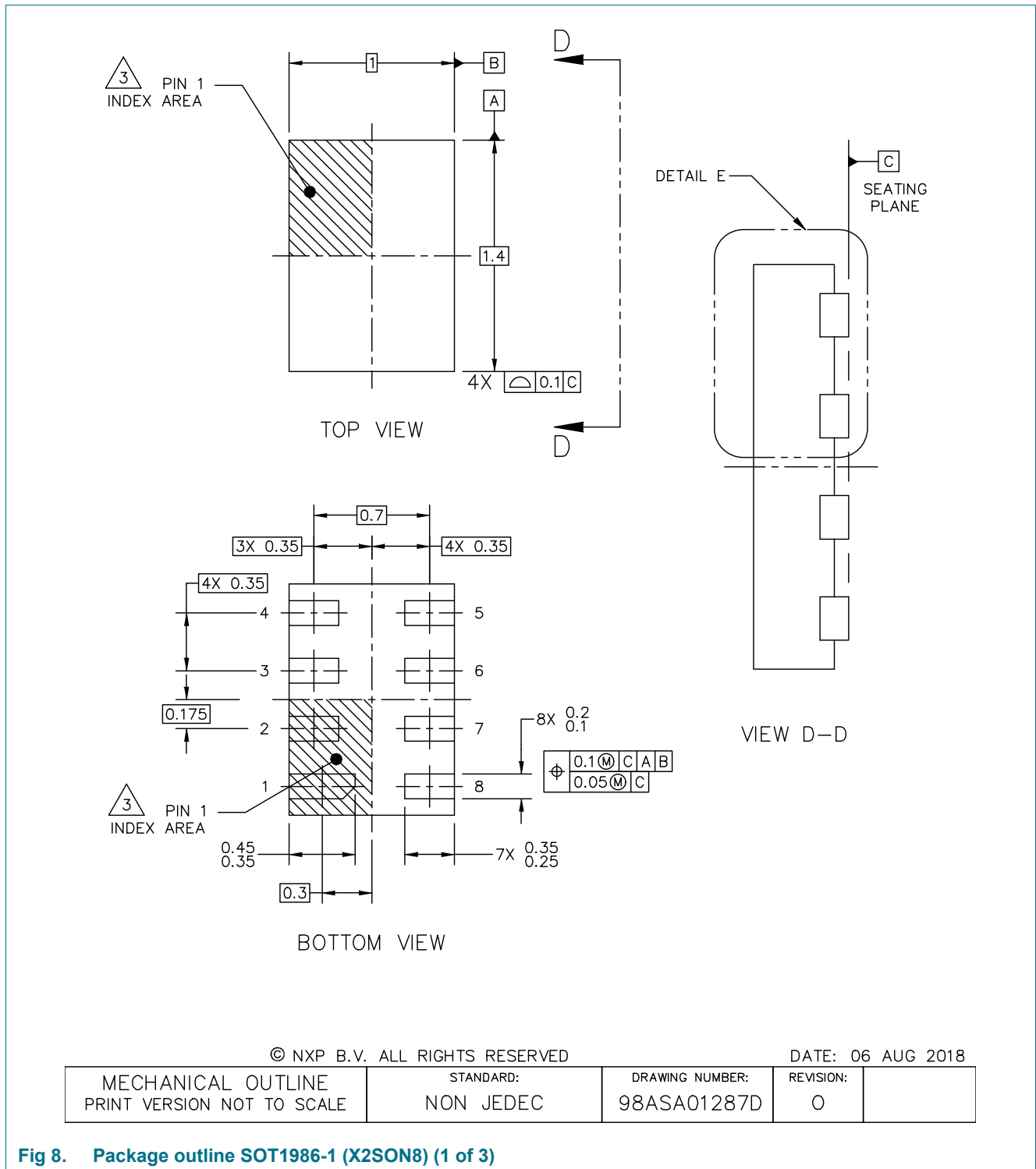
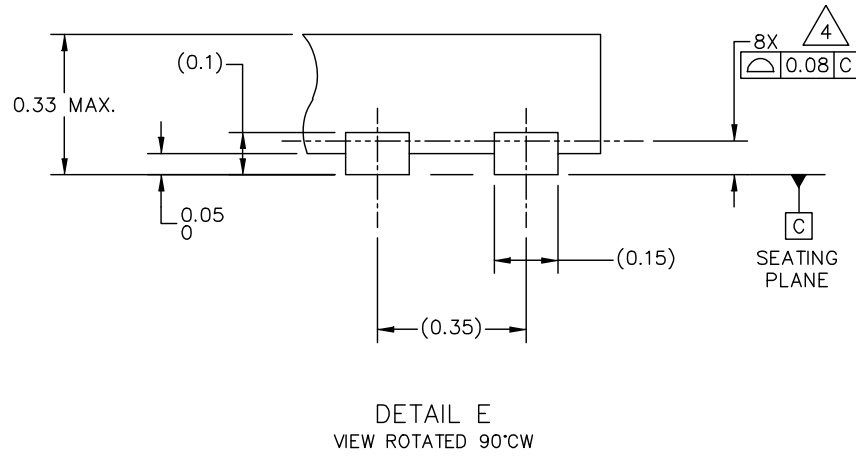


Fig 8. Package outline SOT1986-1 (X2SON8) (1 of 3)





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Fig 9. Package outline SOT1986-1 (X2SON8) (2 of 3)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS.

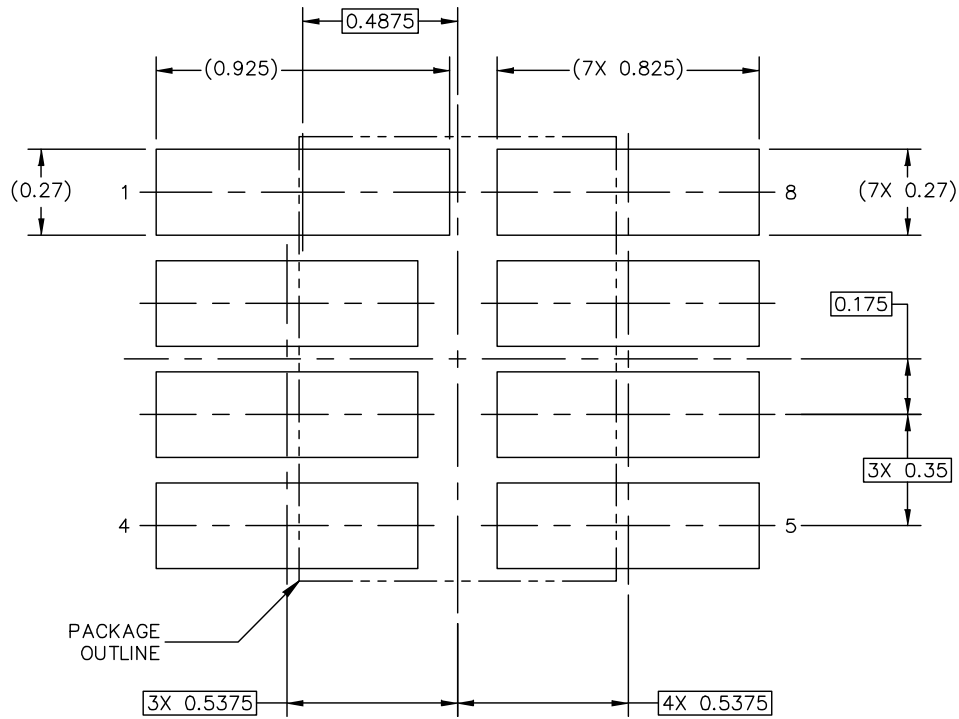
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Fig 10. Package outline SOT1986-1 (X2SON8) (3 of 3)

16. Soldering



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

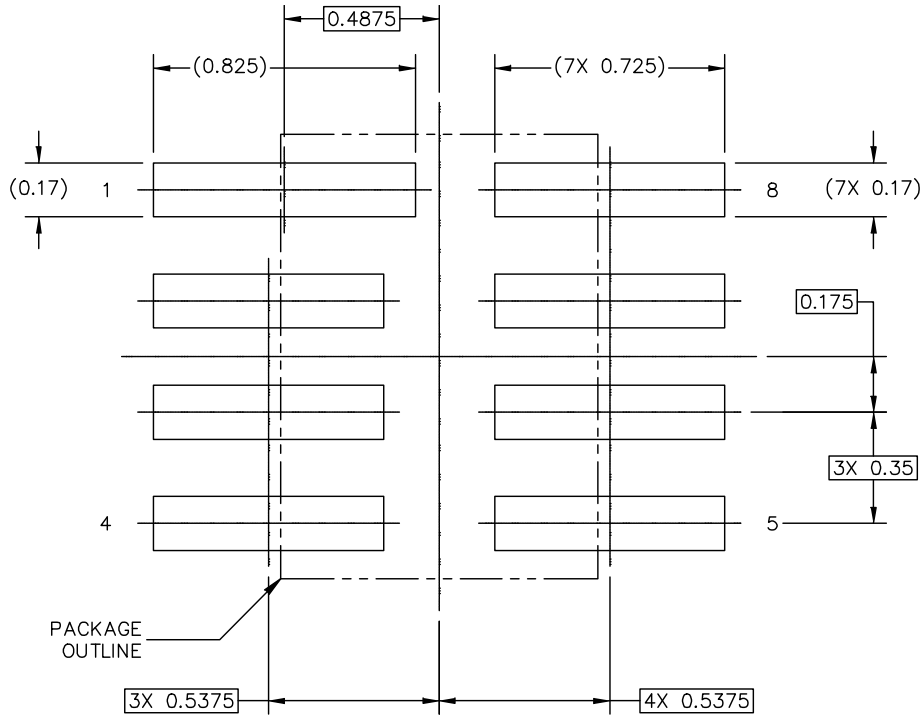
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Fig 11. Soldering footprint for SOT1986-1 (X2SON8) 1 of 3



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

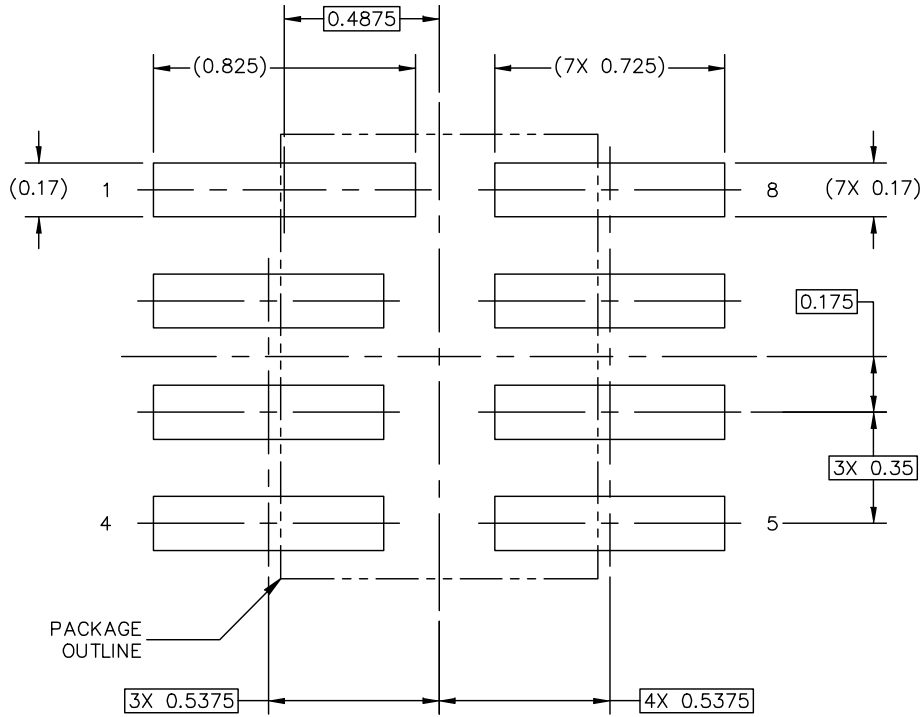
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Fig 12. Soldering footprint for SOT1986-1 (X2SON8) 2 of 3



STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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Fig 13. Soldering footprint for SOT1986-1 (X2SON8) 3 of 3

## 17. Abbreviations

Table 15. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
GPIO	General Purpose Input Output
HBM	Human Body Model
I <sup>2</sup> C	Inter-Integrated Circuit
IEC	International Electrotechnical Commission
MM	Machine Model
PCB	Printed-Circuit Board
PMOS	Positive Metal Oxide Semiconductor
SMBus	System Management Bus
UART	Universal Asynchronous Receiver Transmitter

## 18. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NTS0302 v.1.0	20190617	Product data sheet	-	-

## 19. Legal information

### 19.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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