

DDR4 SDRAM RDIMM Addendum

MTA36ASF8G72PZ – 64GB

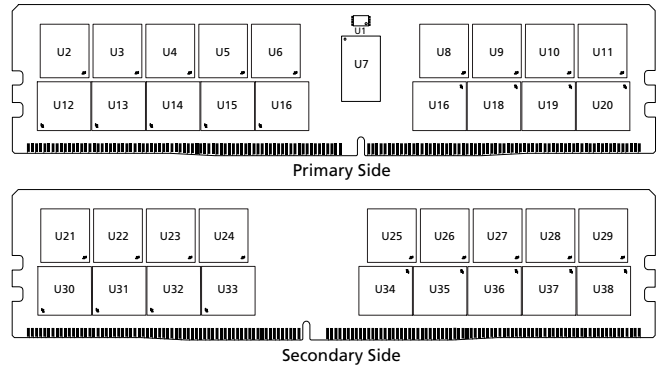
Introduction

Information provided here is in addition to or supercedes information provided in the Micron DDR4 RDIMM Core data sheet.

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- Features and specifications supported in the Micron DDR4 RDIMM Core data sheet
- 288-pin, registered dual in-line memory module (RDIMM)
- Fast data transfer rates: PC4-3200, PC4-2933
- 64GB (8 Gig x 72)
- Dual-rank
- 16 internal banks; 4 groups of 4 banks each

Figure 1: 288-Pin RDIMM (MO-309, R/C-B3)



Options

- Operating temperature
 - Commercial ($0^{\circ}\text{C} \leq T_{\text{OPER}} \leq 95^{\circ}\text{C}$)
- Package
 - 288-pin DIMM (halogen-free)
- Frequency/CAS latency
 - 0.625ns @ CL = 22 (DDR4-3200)
 - 0.682ns @ CL = 21 (DDR4-2933)

Marking

None
Z
-3G2
-2G9

Table 1: Addressing

Parameter	64GB
Row address	256K A[17:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	16Gb (4 Gig x 4), 16 banks
Module rank address	2 CS_n[1:0]



Table 2: Part Numbers and Timing Parameters – 64GB Modules

Base device: MT40A4G4,¹ 16Gb DDR4 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (CL-nRCD-nRP)
MTA36ASF8G72PZ-3G2__	64GB	8 Gig x 72	25.6 GB/s	0.625ns/3200 MT/s	22-22-22
MTA36ASF8G72PZ-2G9__	64GB	8 Gig x 72	23.47 GB/s	0.682ns/2933 MT/s	21-21-21

- Notes:
1. The data sheet for the base device can be found on micron.com.
 2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA36ASF8G72PZ-3G2B2.

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DQ Map

Table 3: Component-to-Module DQ Map Front (R/C-B3)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U2	0	7	155	U3	0	15	166
	1	5	148		1	13	159
	2	6	10		2	14	21
	3	4	3		3	12	14
U4	0	23	177	U5	0	31	188
	1	21	170		1	29	181
	2	22	32		2	30	43
	3	20	25		3	28	36
U6	0	CB7	199	U8	0	39	247
	1	CB5	192		1	37	240
	2	CB6	54		2	38	102
	3	CB4	47		3	36	95
U9	0	47	258	U10	0	55	269
	1	45	251		1	53	262
	2	46	113		2	54	124
	3	44	106		3	52	117
U11	0	63	280	U12	0	3	157
	1	61	273		1	1	150
	2	62	135		2	2	12
	3	60	128		3	0	5
U13	0	10	23	U14	0	16	27
	1	9	161		1	18	34
	2	11	168		2	17	172
	3	8	16		3	19	179
U15	0	24	38	U16	0	CB0	49
	1	26	45		1	CB2	56
	2	25	183		2	CB1	194
	3	27	190		3	CB3	201
U17	0	32	97	U18	0	41	253
	1	34	104		1	42	115
	2	33	242		2	40	108
	3	35	249		3	43	260



Table 3: Component-to-Module DQ Map Front (R/C-B3) (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U19	0	51	271	U20	0	59	282
	1	49	264		1	57	275
	2	50	126		2	58	137
	3	48	119		3	56	130

Table 4: Component-to-Module DQ Map Back (R/C-B3)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U21	0	61	273	U22	0	53	262
	1	63	280		1	55	269
	2	60	128		2	52	117
	3	62	135		3	54	124
U23	0	45	251	U24	0	37	240
	1	47	258		1	39	247
	2	44	106		2	36	95
	3	46	113		3	38	102
U25	0	CB5	192	U26	0	29	181
	1	CB7	199		1	31	188
	2	CB4	47		2	28	36
	3	CB6	54		3	30	43
U27	0	21	170	U28	0	13	159
	1	23	177		1	15	166
	2	20	25		2	12	14
	3	22	32		3	14	21
U29	0	5	148	U30	0	57	275
	1	7	155		1	59	282
	2	4	3		2	56	130
	3	6	10		3	58	137
U31	0	49	264	U32	0	42	115
	1	51	271		1	41	253
	2	48	119		2	43	260
	3	50	126		3	40	108



Table 4: Component-to-Module DQ Map Back (R/C-B3) (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U33	0	34	104	U34	0	CB2	56
	1	32	97		1	CB0	49
	2	35	249		2	CB3	201
	3	33	242		3	CB1	194
U35	0	26	45	U36	0	18	34
	1	24	38		1	16	27
	2	27	190		2	19	179
	3	25	183		3	17	172
U37	0	9	161	U38	0	1	150
	1	10	23		1	3	157
	2	8	16		2	0	5
	3	11	168		3	2	12

I_{DD} Specifications

Table 5: DDR4 I_{DD} Specifications and Conditions (0° ≤ T_C ≤ 85°) – 64GB (Die Revision E)

Values are for the MT40A4G4 DDR4 SDRAM only and are computed from values specified in the 16Gb (4 Gig x 4) component data sheet

Parameter	Symbol	3200	2933	Units
One bank ACTIVATE-PRECHARGE current	I _{DD0} ¹	1674	1656	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I _{pp} current	I _{PP0} ¹	90	90	mA
One bank ACTIVATE-READ-PRECHARGE current	I _{DD1} ¹	1872	1854	mA
Precharge standby current	I _{DD2N} ²	1620	1584	mA
Precharge standby ODT current	I _{DD2NT} ¹	1602	1584	mA
Precharge power-down current	I _{DD2P} ²	1368	1368	mA
Precharge quiet standby current	I _{DD2Q} ²	1512	1512	mA
Active standby current	I _{DD3N} ²	2160	2124	mA
Active standby I _{pp} current	I _{PP3N} ²	72	72	mA
Active power-down current	I _{DD3P} ²	1728	1692	mA
Burst read current	I _{DD4R} ¹	2970	2826	mA
Burst write current	I _{DD4W} ¹	2574	2502	mA
Different logic rank burst refresh current (1x REF)	I _{DD5R} ¹	1908	1908	mA
Different logic rank burst refresh I _{pp} current (1x REF)	I _{PP5R} ¹	108	108	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I _{DD6N (0-85°C)} ²	1908	1908	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I _{DD6E (0-95°C)} ²	4068	4068	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I _{DD6R (0-45°C)} ²	720	720	mA
Auto self refresh current (25°C)	I _{DD6A (25°C)} ²	396	396	mA
Auto self refresh current (45°C)	I _{DD6A (45°C)} ²	720	720	mA
Auto self refresh current (75°C)	I _{DD6A (75°C)} ²	1836	1836	mA
Auto self refresh current (95°C)	I _{DD6A (95°C)} ²	4068	4068	mA
Auto self refresh I _{pp} current (0°C to 95°C)	I _{PP6X} ²	216	216	mA
Bank interleave read current	I _{DD7} ¹	4230	4194	mA
Bank interleave read I _{pp} current	I _{PP7} ¹	324	324	mA
Maximum power-down current	I _{DD8} ²	1296	1296	mA

- Notes:
1. One module rank in the active I_{DD}/I_{pp}, the other rank in I_{DD2P}/I_{PP3N}.
 2. All ranks in this I_{DD}/I_{pp} condition.
 3. When T_C > 85°C, the I_{DD} and I_{pp} values must be derated. Refer to the base device data sheet I_{DD} and I_{pp} specification tables for derating values for the applicable die-revision.

Table 6: DDR4 I_{DD} Specifications and Conditions (0° ≤ T_C ≤ 85°) – 64GB (Die Revision B)

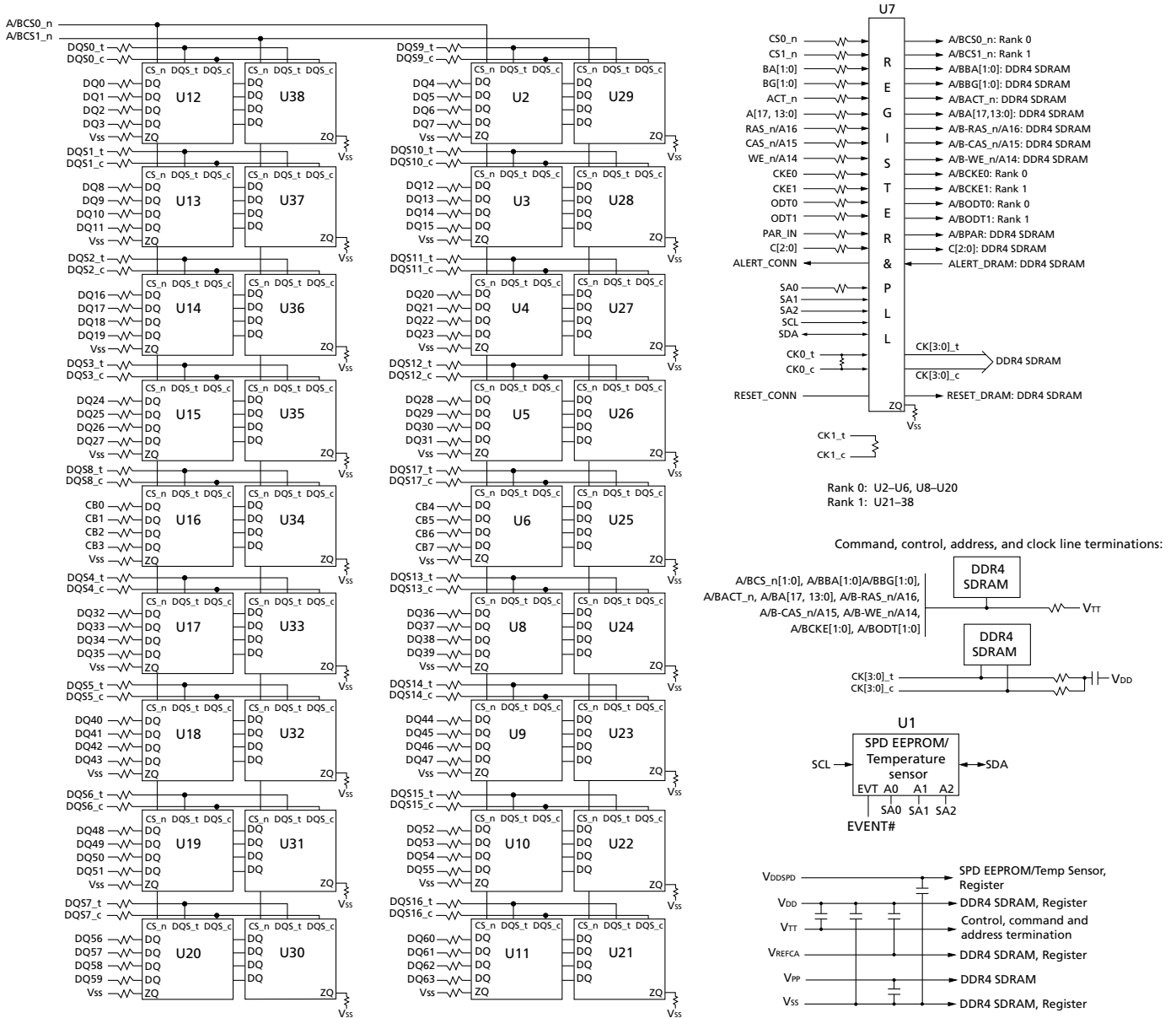
Values are for the MT40A4G4 DDR4 SDRAM only and are computed from values specified in the 16Gb (4 Gig x 4) component data sheet

Parameter	Symbol	3200	2933	Units
One bank ACTIVATE-PRECHARGE current	I _{DD0} ¹	1854	1836	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I _{PP} current	I _{PP0} ¹	126	126	mA
One bank ACTIVATE-READ-PRECHARGE current	I _{DD1} ¹	2034	2016	mA
Precharge standby current	I _{DD2N} ²	1872	1836	mA
Precharge standby ODT current	I _{DD2NT} ¹	1782	1764	mA
Precharge power-down current	I _{DD2P} ²	1548	1548	mA
Precharge quite standby current	I _{DD2Q} ²	1692	1692	mA
Active standby current	I _{DD3N} ²	2808	2772	mA
Active standby I _{PP} current	I _{PP3N} ²	108	108	mA
Active power-down current	I _{DD3P} ²	2484	2448	mA
Burst read current	I _{DD4R} ¹	3870	3726	mA
Burst write current	I _{DD4W} ¹	3726	3600	mA
Different logic rank burst refresh current (1x REF)	I _{DD5R} ¹	2196	2178	mA
Different logic rank burst refresh I _{PP} current (1x REF)	I _{PP5R} ¹	144	144	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I _{DD6N (0-85°C)} ²	2412	2412	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I _{DD6E (0-95°C)} ²	4356	4356	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I _{DD6R (0-45°C)} ²	1044	1044	mA
Auto self refresh current (25°C)	I _{DD6A (25°C)} ²	360	360	mA
Auto self refresh current (45°C)	I _{DD6A (45°C)} ²	1044	1044	mA
Auto self refresh current (75°C)	I _{DD6A (75°C)} ²	2196	2196	mA
Auto self refresh current (95°C)	I _{DD6A (95°C)} ²	4356	4356	mA
Auto self refresh I _{PP} current (0°C to 95°C)	I _{PP6X} ²	396	396	mA
Bank interleave read current	I _{DD7} ¹	5058	4932	mA
Bank interleave read I _{PP} current	I _{PP7} ¹	252	252	mA
Maximum power-down current	I _{DD8} ²	1440	1440	mA

- Notes:
1. One module rank in the active I_{DD}/I_{PP}, the other rank in I_{DD2P}/I_{PP3N}.
 2. All ranks in this I_{DD}/I_{PP} condition.
 3. When T_C > 85°C, the I_{DD} and I_{PP} values must be derated. Refer to the base device data sheet I_{DD} and I_{PP} specification tables for derating values for the applicable die-revision.

Functional Block Diagram

Figure 2: Functional Block Diagram, R/C-B3



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.



64GB (x72, ECC, DR) 288-Pin DDR4 RDIMM Functional Block Diagram

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