# MPM82504

## 16V, Quad 25A, Scalable DC/DC Power Module with PMBus

## DESCRIPTION

The MPM82504 is a quad 25A, scalable, fully integrated power module with a PMBus interface. The device offers a complete power solution that achieves up to 25A per output channel. The MPM82504 has four output channels that can be paralleled to provide 50A, 75A, or 100A of output current for flexible configurations. The device can also operate in parallel with the MPM3695-100 and additional MPM82504 devices to provide a higher output current. The MPM82504 operates at a high efficiency across a wide load range.

The device utilizes MPS's proprietary, multi-phase constant-on-time (MCOT) control, which provides ultra-fast transient response and simple loop compensation. The PMBus interface enables flexible digital configurations and monitoring of key parameters.

Full protection features include over-current protection (OCP), over-voltage protection (OVP), under-voltage protection (UVP), and over-temperature protection (OTP).

The MPM82504 requires a minimal number of readily available external components. It is available in a BGA (15mmx30mmx5.18mm) package.

## FEATURES

- 3.2V to 16V Input Voltage Range with External 3.3V VCC Bias
- 4V to 16V Input Voltage Range with Internal VCC Bias
- 0.5V to 3.3V Output Voltage Range
- Four Parallelable Output Channels with Up to 25A per Channel
- Parallel Operation with Multiple MPM82504 and MPM3695-100 Devices
- Auto-Interleaving for Multi-Phase Operation
- Individual Remote Sense for Each Channel
- PMBus 1.3 Compliant
- Telemetry Readback including $V_{IN}$, $V_{OUT}$, $I_{OUT}$, Temperature, and Faults for Each Channel
- Each Channel Is Configurable via the PMBus:
  - Output Voltage, Soft-Start Time
  - Over-Current, Over-Temperature, Over-Voltage, Under-Voltage, and UVLO Limits
  - PWM Mode and Switching Frequency
- Available in a BGA (15mmx30mmx5.18mm) Package

## APPLICATIONS

- Telecom and Networking Systems
- Industrial Equipment
- Servers and Computing
- FPGA and ASIC Core Power

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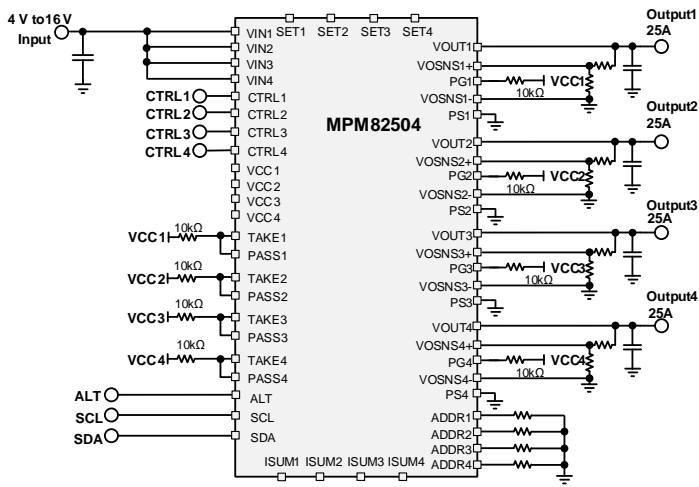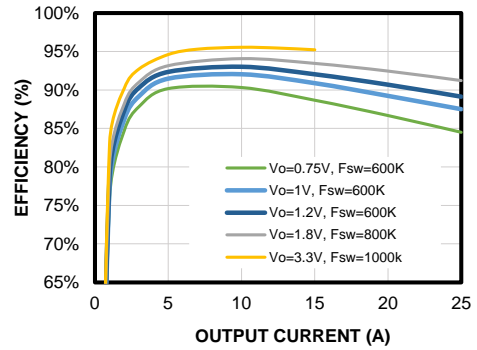
## TYPICAL APPLICATION



**Figure 1: Quad Output Operation**

**Efficiency vs. Output Current**

$V_{IN}$ = 12V, single channel with external 3.3V VCC

# ORDERING INFORMATION

| Part Number* | Package | Top Marking | MSL Rating | Notes |
|---|---|---|---|---|
| MPM82504GBH-xxxx** | BGA-253L (15mmx30mmx5.18mm) | *See Below* | 3 | - |
| MPM82504GBH-0000 | BGA-253L (15mmx30mmx5.18mm) | *See Below* | 3 | Default configuration for quad 25A output |
| MPM82504GBH-0001 | BGA-253L (15mmx30mmx5.18mm) | *See Below* | 3 | Default configuration for dual 50A output |

\* Add –T for tray package (e.g. MPM82504GBH-0000–T).

\*\*Note: The 4-digit "-xxxx" is the configuration code identifier for the register settings stored in the non-volatile memory (NVM). The default configuration code is "-0000". See Table 4, Table 5, Table 6, and Table 7 on pages 52 through 55 for the detailed configuration information and the register map for codes "-0000" and "-0001". Each "x" can be a hexadecimal value between 0 and F. Work with an MPS FAE to create this unique number.

# TOP MARKING

MPSYYWW

MP82504

LLLLLLLLL

M

MPS: MPS prefix
Y: Year code
W: Week code
MP82504: Part number
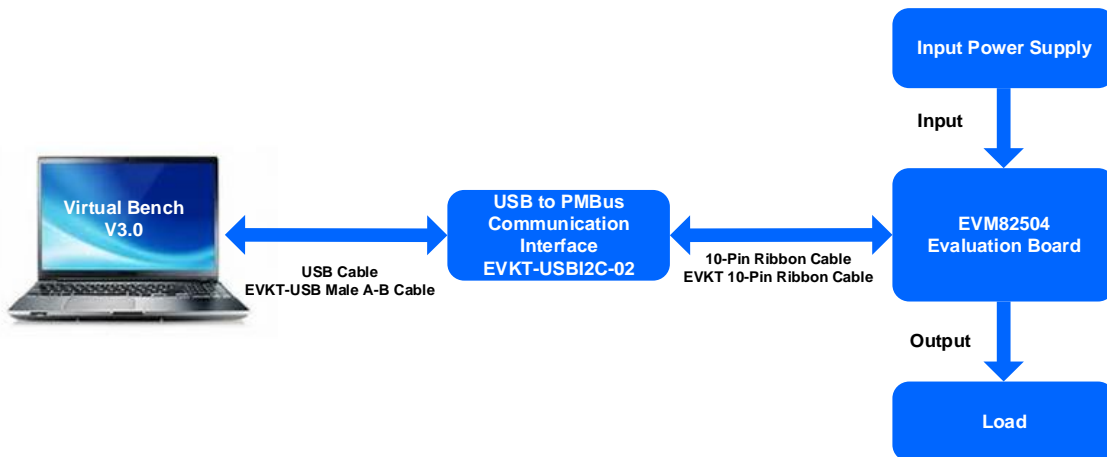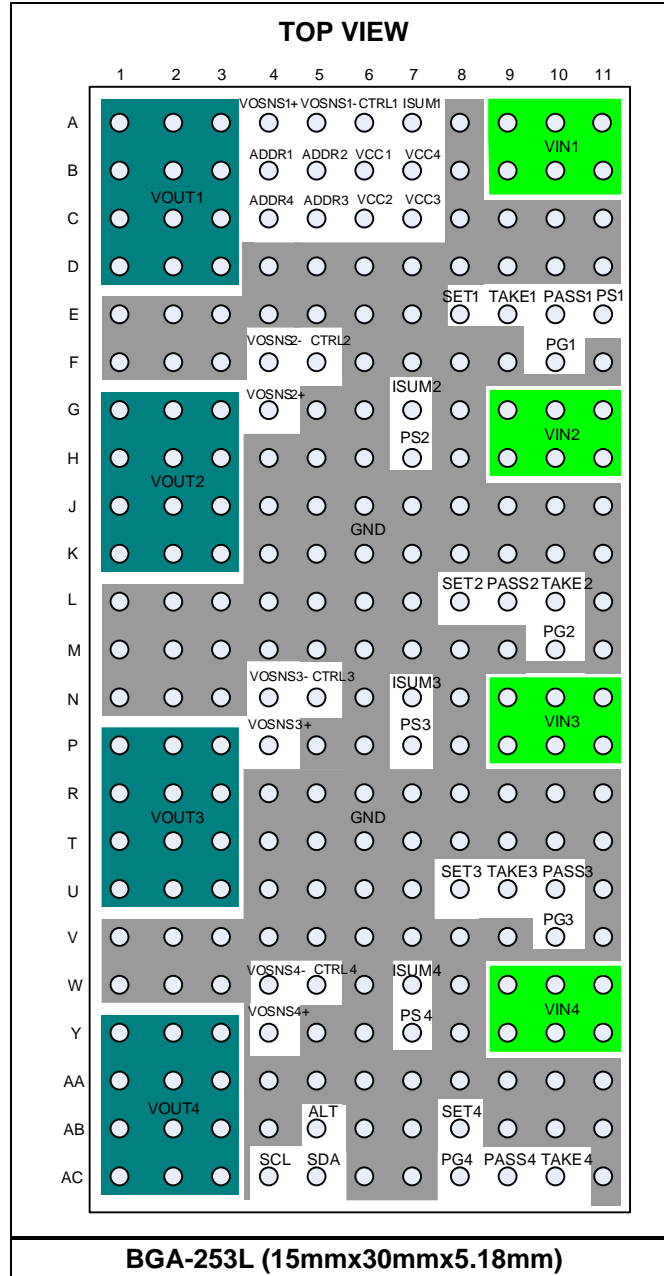LLLLLLLLL: Lot number
M: Module

**Figure 2: Evaluation Board Set-Up**

# PACKAGE REFERENCE



**BGA-253L (15mmx30mmx5.18mm)**

## PIN LIST

**Table 1: Pins A1–E11**

| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|-----|------|-----|------|-----|------|-----|------|-----|------|
| A1 | VOUT1 | B1 | VOUT1 | C1 | VOUT1 | D1 | VOUT1 | E1 | GND |
| A2 | VOUT1 | B2 | VOUT1 | C2 | VOUT1 | D2 | VOUT1 | E2 | GND |
| A3 | VOUT1 | B3 | VOUT1 | C3 | VOUT1 | D3 | VOUT1 | E3 | GND |
| A4 | VOSNS1+ | B4 | ADDR1 | C4 | ADDR4 | D4 | GND | E4 | GND |
| A5 | VOSNS1- | B5 | ADDR2 | C5 | ADDR3 | D5 | GND | E5 | GND |
| A6 | CTRL1 | B6 | VCC1 | C6 | VCC2 | D6 | GND | E6 | GND |
| A7 | ISUM1 | B7 | VCC4 | C7 | VCC3 | D7 | GND | E7 | GND |
| A8 | GND | B8 | GND | C8 | GND | D8 | GND | E8 | SET1 |
| A9 | VIN1 | B9 | VIN1 | C9 | GND | D9 | GND | E9 | TAKE1 |
| A10 | VIN1 | B10 | VIN1 | C10 | GND | D10 | GND | E10 | PASS1 |
| A11 | VIN1 | B11 | VIN1 | C11 | GND | D11 | GND | E11 | PS1 |

**Table 2: Pins F1–K11**

| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|-----|------|-----|------|-----|------|-----|------|-----|------|
| F1 | GND | G1 | VOUT2 | H1 | VOUT2 | J1 | VOUT2 | K1 | VOUT2 |
| F2 | GND | G2 | VOUT2 | H2 | VOUT2 | J2 | VOUT2 | K2 | VOUT2 |
| F3 | GND | G3 | VOUT2 | H3 | VOUT2 | J3 | VOUT2 | K3 | VOUT2 |
| F4 | VOSNS2- | G4 | VOSNS2+ | H4 | GND | J4 | GND | K4 | GND |
| F5 | CTRL2 | G5 | GND | H5 | GND | J5 | GND | K5 | GND |
| F6 | GND | G6 | GND | H6 | GND | J6 | GND | K6 | GND |
| F7 | GND | G7 | ISUM2 | H7 | PS2 | J7 | GND | K7 | GND |
| F8 | GND | G8 | GND | H8 | GND | J8 | GND | K8 | GND |
| F9 | GND | G9 | VIN2 | H9 | VIN2 | J9 | GND | K9 | GND |
| F10 | PG1 | G10 | VIN2 | H10 | VIN2 | J10 | GND | K10 | GND |
| F11 | GND | G11 | VIN2 | H11 | VIN2 | J11 | GND | K11 | GND |

**Table 3: Pins L1–R11**

| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|-----|------|-----|------|-----|------|-----|------|-----|------|
| L1 | GND | M1 | GND | N1 | GND | P1 | VOUT3 | R1 | VOUT3 |
| L2 | GND | M2 | GND | N2 | GND | P2 | VOUT3 | R2 | VOUT3 |
| L3 | GND | M3 | GND | N3 | GND | P3 | VOUT3 | R3 | VOUT3 |
| L4 | GND | M4 | GND | N4 | VOSNS3- | P4 | VOSNS3+ | R4 | GND |
| L5 | GND | M5 | GND | N5 | CTRL3 | P5 | GND | R5 | GND |
| L6 | GND | M6 | GND | N6 | GND | P6 | GND | R6 | GND |
| L7 | GND | M7 | GND | N7 | ISUM3 | P7 | PS3 | R7 | GND |
| L8 | SET2 | M8 | GND | N8 | GND | P8 | GND | R8 | GND |
| L9 | PASS2 | M9 | GND | N9 | VIN3 | P9 | VIN3 | R9 | GND |
| L10 | TAKE2 | M10 | PG2 | N10 | VIN3 | P10 | VIN3 | R10 | GND |

| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|-----|------|-----|------|-----|------|-----|------|-----|------|
| L11 | GND | M11 | GND | N11 | VIN3 | P11 | VIN3 | R11 | GND |

**Table 4: Pins T1–K11**

| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
|-----|------|-----|------|-----|------|-----|------|-----|------|
| T1 | VOUT3 | U1 | VOUT3 | V1 | GND | W1 | GND | Y1 | VOUT4 |
| T2 | VOUT3 | U2 | VOUT3 | V2 | GND | W2 | GND | Y2 | VOUT4 |
| T3 | VOUT3 | U3 | VOUT3 | V3 | GND | W3 | GND | Y3 | VOUT4 |
| T4 | GND | U4 | GND | V4 | GND | W4 | VOSNS4- | Y4 | VOSNS4+ |
| T5 | GND | U5 | GND | V5 | GND | W5 | CTRL4 | Y5 | GND |
| T6 | GND | U6 | GND | V6 | GND | W6 | GND | Y6 | GND |
| T7 | GND | U7 | GND | V7 | GND | W7 | ISUM4 | Y7 | PS4 |
| T8 | GND | U8 | SET3 | V8 | GND | W8 | GND | Y8 | GND |
| T9 | GND | U9 | TAKE3 | V9 | GND | W9 | VIN4 | Y9 | VIN4 |
| T10 | GND | U10 | PASS3 | V10 | PG3 | W10 | VIN4 | Y10 | VIN4 |
| T11 | GND | U11 | GND | V11 | GND | W11 | VIN4 | Y11 | VIN4 |

**Table 4: Pins AA1–AC11**

| Pin | Name | Pin | Name | Pin | Name |
|-----|------|-----|------|-----|------|
| AA1 | VOUT4 | AB1 | VOUT4 | AC1 | VOUT4 |
| AA2 | VOUT4 | AB2 | VOUT4 | AC2 | VOUT4 |
| AA3 | VOUT4 | AB3 | VOUT4 | AC3 | VOUT4 |
| AA4 | GND | AB4 | GND | AC4 | SCL |
| AA5 | GND | AB5 | ALT | AC5 | SDA |
| AA6 | GND | AB6 | GND | AC6 | GND |
| AA7 | GND | AB7 | GND | AC7 | GND |
| AA8 | GND | AB8 | SET4 | AC8 | PG4 |
| AA9 | GND | AB9 | GND | AC9 | PASS4 |
| AA10 | GND | AB10 | GND | AC10 | TAKE4 |
| AA11 | GND | AB11 | GND | AC11 | GND |

## PIN FUNCTIONS [(1)]

| Name | Description |
|---|---|
| VIN1, VIN2, VIN3, VIN4 | **Supply voltage for channels 1 to 4.** These pins provides power to the each channel. Decoupling capacitors must be connected between VINx and GND. |
| VOUT1, VOUT2, VOUT3, VOUT4 | **Module output node for channels 1 to 4.** Connect VOUTx to the PCB with copper. Each output node corresponds with its respective channel. For example, VOUT1 corresponds to channel 1. |
| GND | **Power ground.** Connect all GND pins together on a PCB copper plane. |
| VCC1, VCC2, VCC3, VCC4 | **Internal 3.3V LDO output.** Float the VCC pins for non-parallel channels. Connect the VCC pins of the channels in parallel mode. |
| CTRL1, CTRL2, CTRL3, CTRL4 | **Converter control.** CTRL1–4 are digital inputs that turn the regulators on and off. Drive CTRLx high to turn the corresponding channel on; drive CTRLx low to turn the channel off. Do not float these pins. In parallel operation, connect the CTRL pins of the paralleled channels. |
| VOSNS1-, VOSNS2-, VOSNS3-, VOSNS4- | **Output voltage sense negative return.** Connect this pin directly to the GND sense point of the corresponding channel's load. Short this pin to GND if remote sense is not used. For parallel operation, connect the VOSNSx- pins of the paralleled channels. |
| VOSNS1+, VOSNS2+, VOSNS3+, VOSNS4+ | **Output voltage sense positive return.** Connect this pin to the output voltage ($V_{OUT}$) sense point of the corresponding channel. For parallel operation, connect the VOSNSx+ pins of the paralleled channels. |
| PG1, PG2, PG3, PG4 | **Power good output.** The output of this pin is an open-drain signal. A pull-up resistor must be connected to a DC voltage to pull this pin high if $V_{OUT}$ exceeds 90% of the nominal voltage. There is a delay from PG going low to high. For parallel operation, connect the PG pins of the paralleled channels. |
| PASS1, PASS2, PASS3, PASS4 | **Passes trigger signal to TAKE.** For non-paralleled channels, connect the corresponding PASS pin to the TAKE pin. Connect PASS and TAKE of the previous phase in parallel operation. For more details, see the Typical Application Circuits section on page 55. |
| TAKE1, TAKE2, TAKE3, TAKE4 | **Receives trigger signal from PASS.** For non-paralleled channels, pull this pin to 3.3V and connect the corresponding PASS pin to the TAKE pin. For parallel operation, pull the master channel's TAKE to 3.3V. For more details, see the Typical Application Circuits section on page 55. |
| SET1, SET2, SET3, SET4 | **Set of PWM signal.** Float the SET pins for non-paralleled channels. For parallel operation, connect the SETx pins of the paralleled channels. |
| ISUM1, ISUM2, ISUM3, ISUM4 | **Reference current output.** For non-paralleled channels, float the ISUM pins. For parallel operation, connect ISUM of the paralleled phases together. |
| SCL | **PMBus serial clock.** |
| SDA | **PMBus serial data.** |
| ALT | **PMBus alert.** Open-drain output, active low. A pull-up resistor must be connected to a 3.3V rail. |
| ADDR1, ADDR2, ADDR3, ADDR4 | **PMBus address setting pins.** Connect a resistor between the ADDR pins and GND to set the address for each channel. For parallel operation, select the same address for each channel. |
| PS1, PS2, PS3, PS4 | **Phase-shedding pins.** With proper PMBus setting, pull this pin high to enable a slave phase. Pull this pin low to disable a slave phase for multi-phase operation. Connect this pin of the master phase to GND, and float the pins of the slave phase(s). |

**Note:**

1) See the Pin List section on page 5 for all pins.

## ABSOLUTE MAXIMUM RATINGS [2]

Supply voltage ($V_{IN}$) ..................................... 18V
$V_{OUT}$ .............................................-0.3V to +5V
$V_{CC}$ .................................................... 4.5V
$V_{CC}$ (1s) [3] .......................................... 6V
All other pins ...............................-0.3V to +4.3V
All other pins (1s) [3] ...................................... 6V
Continuous power dissipation ($T_A$ = 25°C) [4]
............................................................. 24.95W
Junction temperature ................................170°C
Storage temperature............... -65°C to +170°C

### ESD Ratings

Human body model (HBM) ................... ±1000V
Charged device model (CDM).................±750V

### Recommended Operating Conditions [5]

Supply voltage ($V_{IN}$) ............................4V to 16V
Supply voltage ($V_{IN}$) [6].....................3.2V to 16V
Output voltage ($V_{OUT}$).....................0.5V to 3.3V
External $V_{CC}$ bias ...............................3V to 3.6V
Operating junction temp ($T_J$) .... -40°C to +125°C

### Thermal Resistance $\theta_{JA}$ $\theta_{JC}$

BGA-253L (15mmx30mmx5.18mm)
EVM82504-BH-00A [7] ..........5.77 ....0.74 . °C/W
JESD51-7 [8] ........................10.3 .....7.7 .. °C/W

**Notes:**

2) Exceeding these ratings may damage the device.
3) Voltage rating during MTP programming.
4) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J$ (MAX), the junction-to-ambient thermal resistance, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D$ (MAX) = ($T_J$ (MAX) - $T_A$) / $\theta_{JA}$. Exceeding the maximum allowable power dissipation can produce an excessive die temperature.
5) The device is not guaranteed to function outside of its operating conditions.
6) The output range is guaranteed with an external 3.3V VCC. Writing to the MTP memory is not supported with an external 3.3V VCC bias.
7) Measured on EVM82504-BH-00A, 6-layer PCB,13.5cmx10cm.
8) The value of $\theta_{JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

# ELECTRICAL CHARACTERISTICS

**$V_{IN}$ = 12V, $T_J$ = -40°C to +125°C [9], unless otherwise noted.**

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **VIN Supply Current** | | | | | | |
| Shutdown supply current | $I_{IN}$ | $V_{CTRL}$ = 0V, single channel | | 2.5 | 4 | mA |
| **Input Voltage** | | | | | | |
| Input voltage | $V_{IN}$ | Internal VCC | 4 | | 16 | V |
| | | With external 3.3V VCC | 3.2 | | 16 | V |
| **Output Voltage** | | | | | | |
| Output voltage range [10] | $V_{OUT\_RANGE}$ | | 0.5 | | 3.3 | V |
| Load regulation [10] | $V_{OUT\_DC\_LOAD}$ | $I_{OUT}$ from 0A to 25A | | ±0.5% | | $V_{OUT}$ |
| Line regulation [10] | $V_{OUT\_DC\_LINE}$ | $V_{IN}$ from 4V to 16V, $I_{OUT}$ = 25A | | ±0.5% | | $V_{OUT}$ |
| **Current Limit** | | | | | | |
| Valley current limit | $I_{LIM}$ | Single channel, D7h = 0x12 | | 27 | | A |
| Min valley current limit configurable value [10] | | Single channel | | 1.5 | | A |
| Max valley current limit configurable value [10] | | Single channel | | 27 | | A |
| Low-side negative current limit in OVP | $I_{LIM\_NEG\_OVP}$ | Single channel | | -13 | | A |
| **CTRL** | | | | | | |
| CTRL on threshold | $CTRL_{ON}$ | | 2.2 | | | V |
| CTRL off threshold | $CTRL_{OFF}$ | | | | 1.2 | V |
| **Timing and Frequency** | | | | | | |
| Switching frequency [10] | $f_{SW}$ | Single channel | | 600 | | kHz |
| Minimum on time [10] | $t_{ON\_MIN}$ | $f_{SW}$ = 1000kHz, $V_{OUT}$ = 0.6V | | 50 | | ns |
| Minimum off time [10] | $t_{OFF\_MIN}$ | $V_{FB}$ = 480mV | | 220 | | ns |
| **Output Over-Voltage Protection (OVP) and Under-Voltage Protection (UVP)** | | | | | | |
| OVP threshold | $V_{OVP}$ | D4h, bits[1:0] = 00 | 111% | 115% | 119% | $V_{REF}$ |
| UVP threshold | $V_{UVP}$ | D9h, bits[3:2] = 10 | 75% | 79% | 83% | $V_{REF}$ |
| Max configurable OVP threshold | $V_{OVP\_MAX}$ | D4h, bits[1:0] = 11 | 126% | 130% | 134% | $V_{REF}$ |
| Min configurable OVP threshold | $V_{OVP\_MIN}$ | D4h, bits[1:0] = 00 | 111% | 115% | 119% | $V_{REF}$ |
| Max configurable UVP threshold | $V_{UVP\_MAX}$ | D9h, bits[3:2] = 11 | 80% | 84% | 88% | $V_{REF}$ |
| Min configurable UVP threshold | $V_{UVP\_MIN}$ | D9h, bits[3:2] = 00 | 65% | 69% | 73% | $V_{REF}$ |
| **Analog-to-Digital Converter (ADC)** [10] | | | | | | |
| Voltage range | | | 0 | | 1.28 | V |
| ADC resolution | | | | 10 | | bits |
| DNL | | | | 1 | | LSB |

## ELECTRICAL CHARACTERISTICS *(continued)*

$V_{IN}$ = 12V, $T_J$ = -40°C to +125°C [9], unless otherwise noted.

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Digital-to-Analog Converter (DAC) (Feedback Voltage)** | | | | | | |
| Range [10] | | | 450 | 600 | 672 | mV |
| Feedback voltage | $V_{FB}$ | 21h, bits[11:0] = 0x0258h; 29h, bits[9:0] = 0x01F4h | 594 | 600 | 606 | mV |
| Resolution | | Per LSB | | 2 | | mV |
| Feedback voltage with margin high [10] | $V_{FB\_MG\_HIGH}$ | | | 672 | | mV |
| Feedback voltage with margin low [10] | $V_{FB\_MG\_LOW}$ | | | 450 | | mV |
| **Soft Start and Turn-On/Off Delay** | | | | | | |
| Soft-start time [10] | $t_{SS}$ | 61h, bits[2:0] = 3b'001 | | 2 | | ms |
| Turn-on delay | $t_{ON\_DELAY}$ | 60h, bits[7:0] = 0x00h | | 0 | | ms |
| Turn-off delay | $t_{OFF\_DELAY}$ | 64h, bits[7:0] = 0x00h | | 0 | | ms |
| **Error Amplifier (EA)** | | | | | | |
| Feedback current | $I_{FB}$ | $V_{FB}$ = $V_{REF}$ ($V_{FB}$ is the potential between VOSNS+ and VOSNS-) | | 50 | 100 | nA |
| **Soft Shutdown** | | | | | | |
| Soft shutdown discharge FET | $R_{ON\_DISCH}$ | Single channel | | 60 | | Ω |
| **Under-Voltage Lockout (UVLO)** | | | | | | |
| VCC UVLO rising threshold | $VCC_{VTH}$ | | 2.6 | 2.75 | 2.9 | V |
| VCC UVLO threshold hysteresis | $VCC_{HYS}$ | | | 250 | | mV |
| Min input configurable turn-on voltage | $V_{IN\_ON\_MIN}$ | VCC = 3.3V | 2.65 | 2.9 | 3.1 | V |
| Max input configurable turn-on voltage | $V_{IN\_ON\_MAX}$ | | 16 | 16.5 | 17 | V |
| Min input configurable turn-off voltage | $V_{IN\_OFF\_MIN}$ | VCC = 3.3V | | 2.75 | | V |
| Max input configurable turn-off voltage [10] | $V_{IN\_OFF\_MAX}$ | | | 15.75 | | V |
| **Power Good (PG)** | | | | | | |
| PG high threshold | $PG_{VTH\_HI}$ | $V_{FB}$ from low to high, D9h, bits[1:0] = 01 | | 94% | | $V_{REF}$ |
| PG low threshold | $PG_{VTH\_LO}$ | $V_{FB}$ from high to low, D9h, bits[3:2] = 10 | | 79% | | $V_{REF}$ |
| PG low-to-high delay | $t_{PGTD}$ | D1h, bits[5:2] = 0000 | | 2 | | ms |
| PG sink current capability | $V_{PG}$ | $I_{PG}$ = 10mA | | | 0.3 | V |
| PG leakage current | $I_{PG\_LEAK}$ | $V_{PG}$ = 3V | | 1.5 | | µA |

## ELECTRICAL CHARACTERISTICS *(continued)*

$V_{IN}$ = 12V, $T_J$ = -40°C to +125°C [9], unless otherwise noted.

| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| PG low-level output voltage | $V_{OL\_100}$ | $V_{IN}$ = 0V, pull PGOOD up to 3.3V through a 100kΩ resistor, $T_J$ = 25°C | | 600 | 720 | mV |
| | $V_{OL\_10}$ | $V_{IN}$ = 0V, pull PGOOD up to 3.3V through a 10kΩ resistor, $T_J$ = 25°C | | 700 | 820 | |
| **Thermal Protection (TP)** | | | | | | |
| TP fault rising threshold [10] | $T_{SD\_RISE}$ | 4Fh = 0x96h | | 150 | | °C |
| TP fault falling threshold [10] | $T_{SD\_FALL}$ | 4Fh = 0096h; D6h, bits[2:1] = 01 | | 125 | | °C |
| TP warning rising threshold [10] | $T_{WARN\_RISE}$ | 51h = 0x7dh | | 125 | | °C |
| TP warning falling threshold [10] | $T_{WARN\_FALL}$ | 51h = 0x7dh; D6h, bits[2:1] = 01 | | 100 | | °C |
| Min TP warning temp [10] | $T_{SD\_WARN\_MIN}$ | | | 35 | | °C |
| Max TP warning temp [10] | $T_{SD\_WARN\_MAX}$ | | | 160 | | °C |
| **Monitoring Parameters** | | | | | | |
| Output voltage monitor accuracy [10] | | $V_{OUT}$ = 0.6V | 0.588 | 0.6 | 0.612 | V |
| Input voltage monitor accuracy | | | 11.76 | 12 | 12.24 | V |
| **PMBus DC Characteristics (SDA, SCL, ALERT, CTRL)** [10] | | | | | | |
| Input high voltage | $V_{IH}$ | | | | 2.1 | V |
| Input low voltage | $V_{IL}$ | | 0.8 | | | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 1mA | | | 0.4 | V |
| Input leakage current | $I_{LEAK}$ | SDA, SCL, ALERT = 3.3V | -10 | | +10 | µA |
| Maximum voltage (SDA, SCL, ALERT, CTRL) | $V_{MAX}$ | Transient voltage including ringing | -0.3 | 3.3 | +3.6 | V |
| Pin capacitance on SDA,SCL | $C_{PIN}$ | | | | 10 | pF |
| **PMBus Timing Characteristics** [10] | | | | | | |
| Min operating frequency | | | | 10 | | kHz |
| Max operating frequency | | | | 1000 | | kHz |
| Bus free time | | Between stop and start condition | 4.7 | | | µs |
| Holding time | | | 4.0 | | | µs |
| Repeated start condition set-up time | | | 4.7 | | | µs |
| Stop condition set-up time | | | 4.0 | | | µs |
| Data hold time | | | 300 | | | ns |
| Data set-up time | | | 250 | | | ns |
| Clock low timeout | | | 25 | | 35 | ms |
| Clock low period | | | 4.7 | | | µs |
| Clock high period | | | 4.0 | | 50 | µs |

# ELECTRICAL CHARACTERISTICS *(continued)*

**$V_{IN}$ = 12V, $T_J$ = -40°C to +125°C [9], unless otherwise noted.**

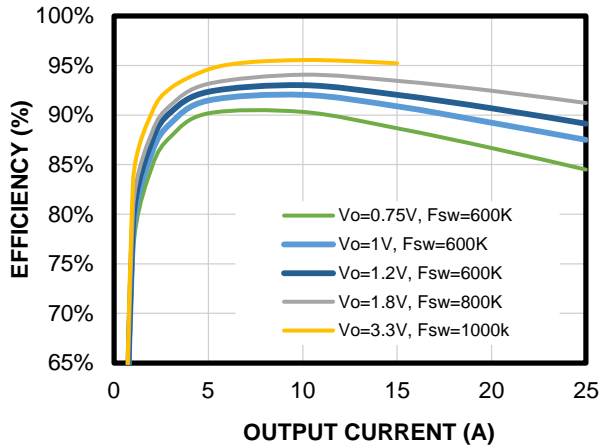| Parameters | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Clock/data falling time | | | | | 300 | ns |
| Clock/data rising time | | | | | 1000 | ns |

**Notes:**

9) Guaranteed by over-temperature (OT) correlation. Not tested in production.
10) Guaranteed by sample characterization. Not tested in production.

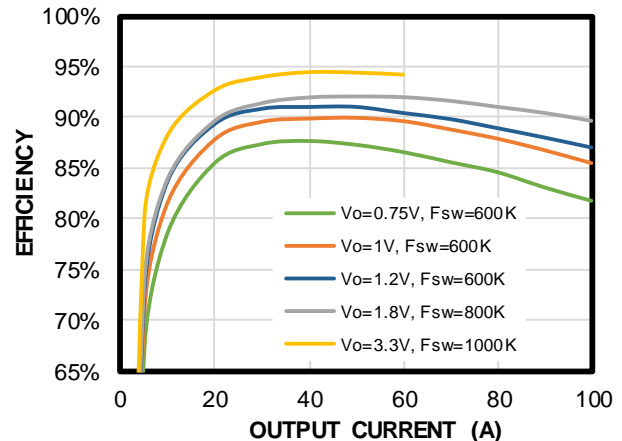# TYPICAL PERFORMANCE CHARACTERISTICS

**V_IN = 12V, T_A = 25°C, unless otherwise noted.**

### Efficiency vs. Output Current
V_IN = 12V, single channel with external 3.3V VCC



### Efficiency vs. Output Current
V_IN = 12V, single channel with internal 3.3V VCC
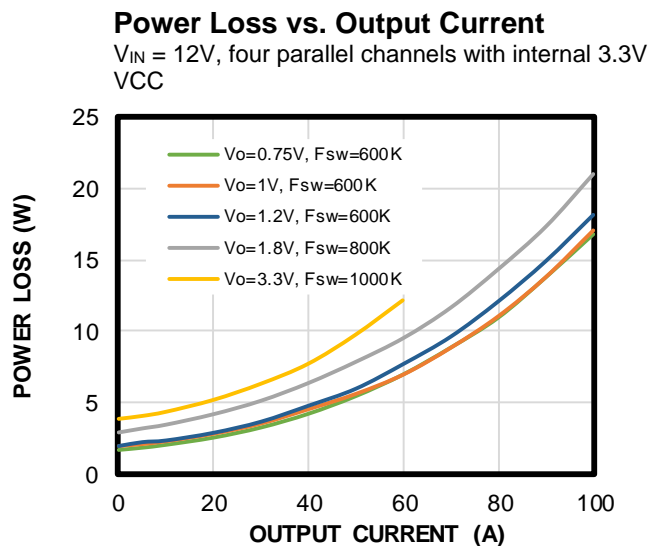


### Efficiency vs. Output Current
V_IN = 5V, single channel with external 3.3V VCC



### Efficiency vs. Output Current
V_IN = 5V, single channel with internal 3.3V VCC



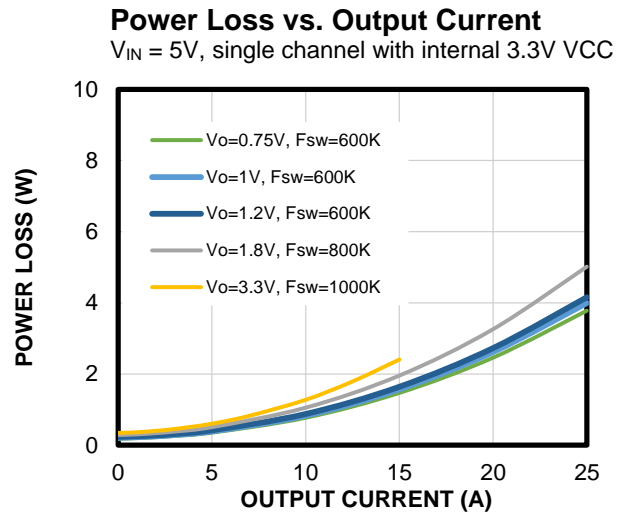### Efficiency vs. Output Current
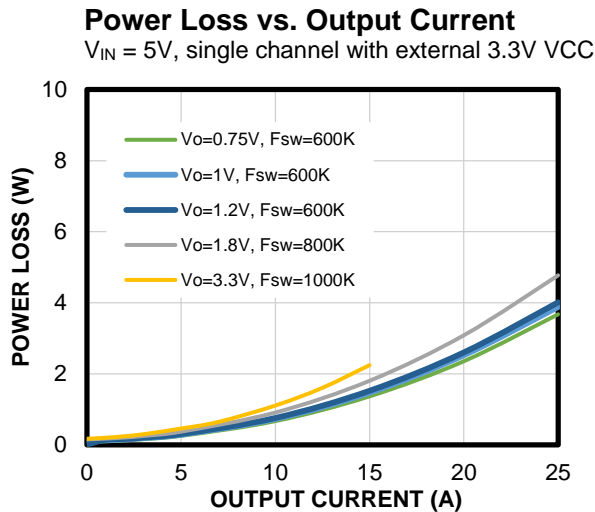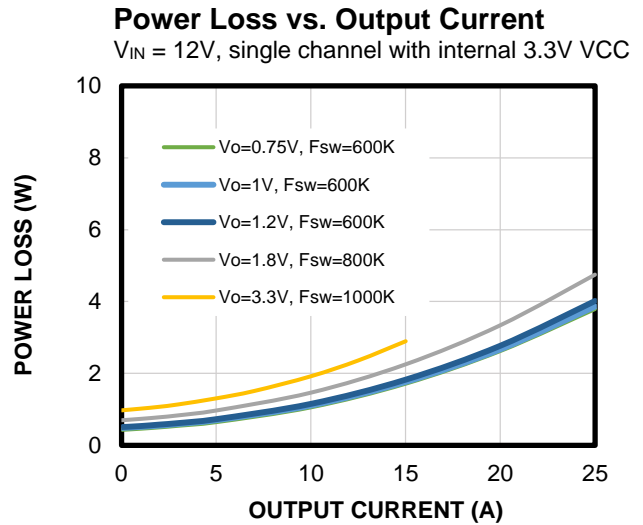V_IN = 12V, four parallel channels with external 3.3V VCC



### Efficiency vs. Output Current
V_IN = 12V, four parallel channels with internal 3.3V VCC

# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN}$ = 12V, $T_A$ = 25°C, unless otherwise noted.

### Power Loss vs. Output Current
$V_{IN}$ = 12V, single channel with external 3.3V VCC



### Power Loss vs. Output Current
$V_{IN}$ = 12V, single channel with internal 3.3V VCC



### Power Loss vs. Output Current
$V_{IN}$ = 5V, single channel with external 3.3V VCC



### Power Loss vs. Output Current
$V_{IN}$ = 5V, single channel with internal 3.3V VCC



### Power Loss vs. Output Current
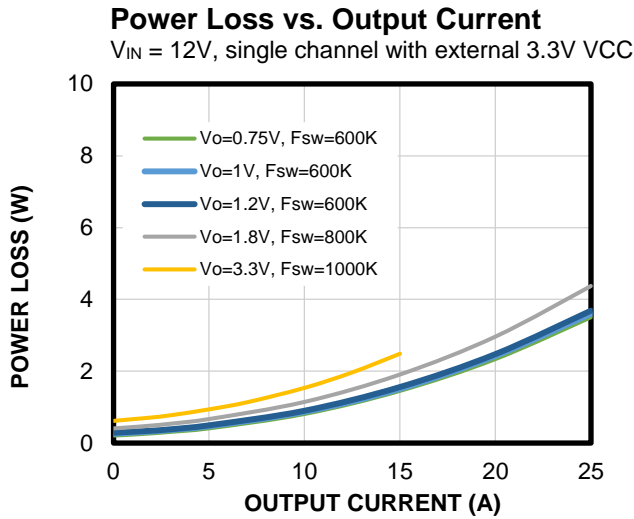$V_{IN}$ = 12V, four parallel channels with external 3.3V VCC



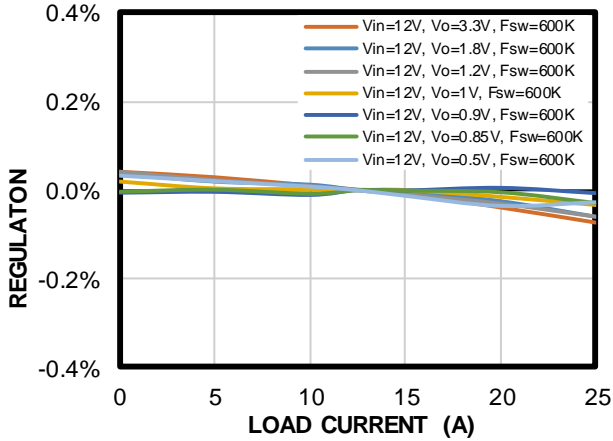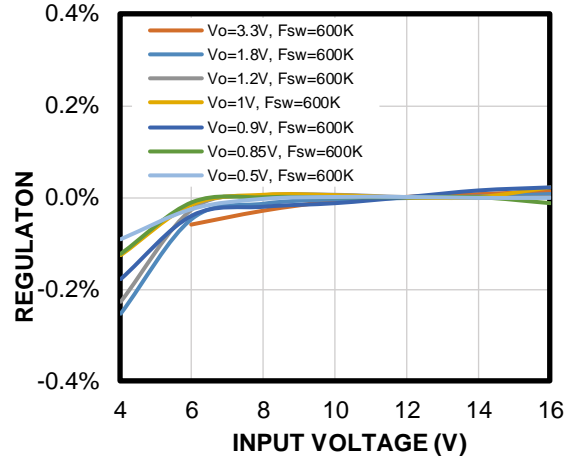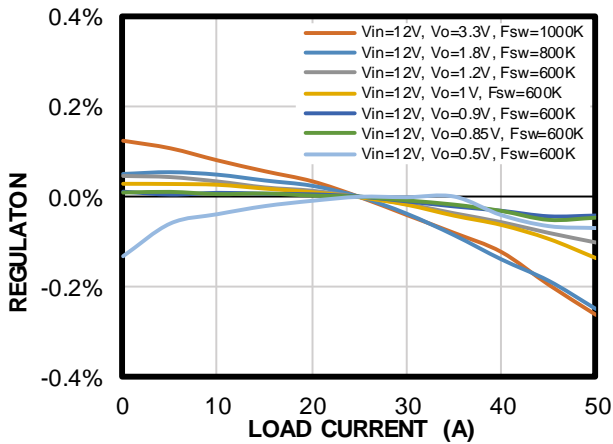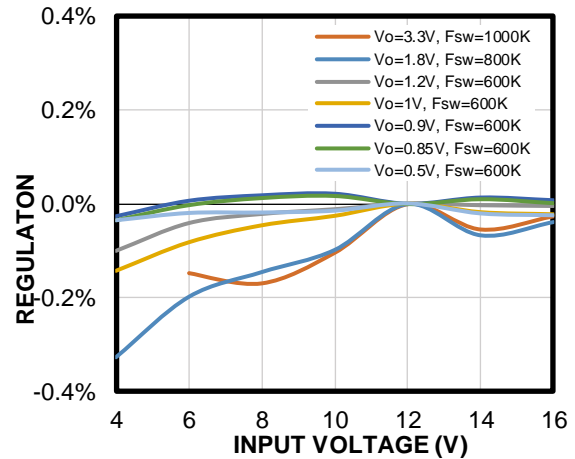### Power Loss vs. Output Current
$V_{IN}$ = 12V, four parallel channels with internal 3.3V VCC
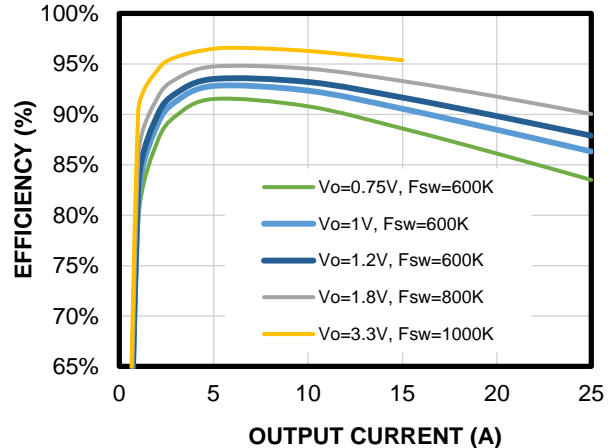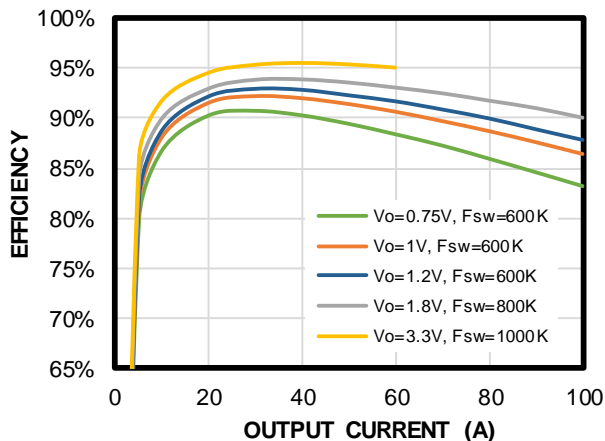
# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

**V<sub>IN</sub> = 12V, T<sub>A</sub> = 25°C, unless otherwise noted.**

$V_{IN}$ = 12V, $T_A$ = 25°C, unless otherwise noted.

### Load Regulation vs. Load Current
Single channel, $f_{SW}$ = 600kΩ

### Line Regulation vs. Input Voltage
Single channel, full load

### Load Regulation vs. Load Current
Two parallel channels, $V_{IN}$ = 12V

### Line Regulation vs. Input Voltage
Two parallel channels, full load

### Load Regulation vs. Output Current
Three parallel channels, $V_{IN}$ = 12V
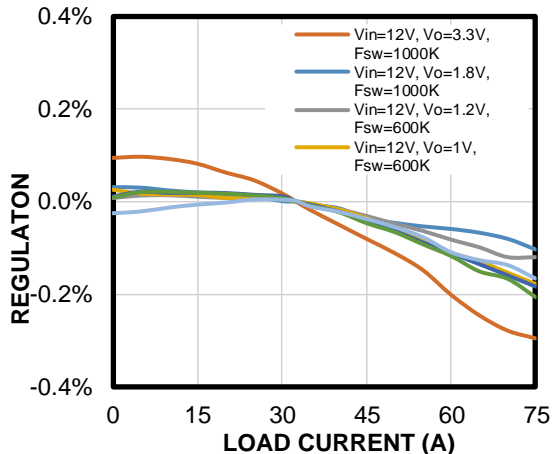
### Line Regulation vs. Input Voltage
Three parallel channels, full load
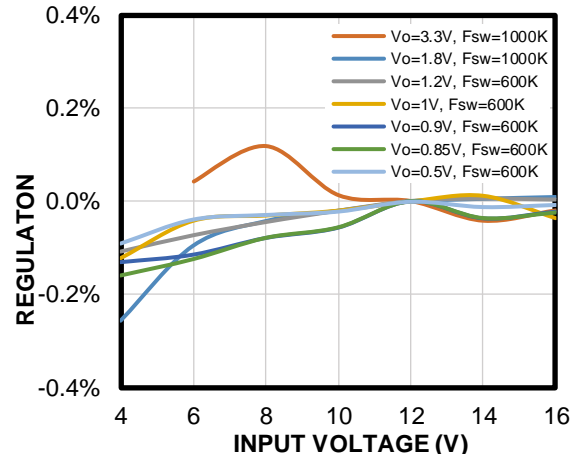
# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN}$ = 12V, $T_A$ = 25°C, unless otherwise noted.

### Load Regulation vs. Load Current
$V_{IN}$ = 12V, four parallel channels
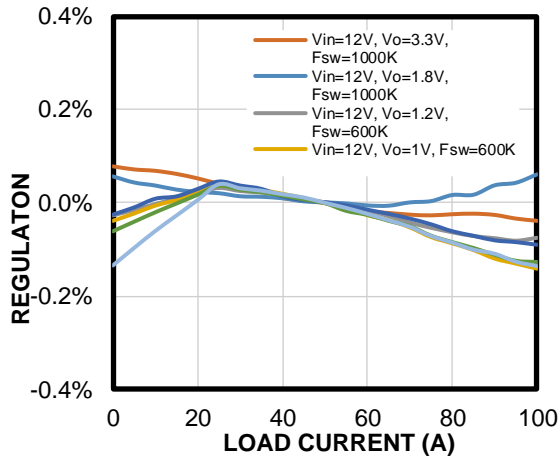
### Line Regulation vs. Input Voltage
Four parallel channels, full load
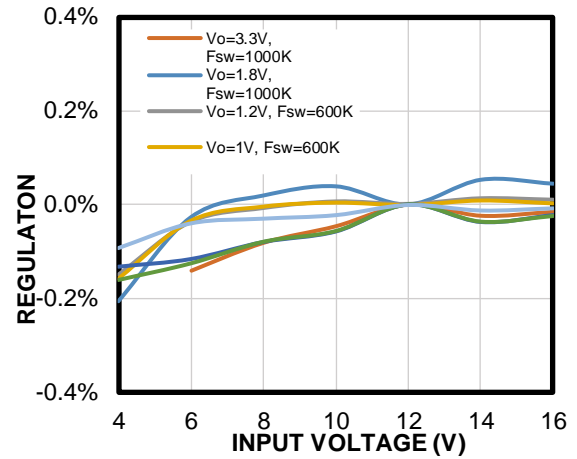
### Package Derating without Air Cooling
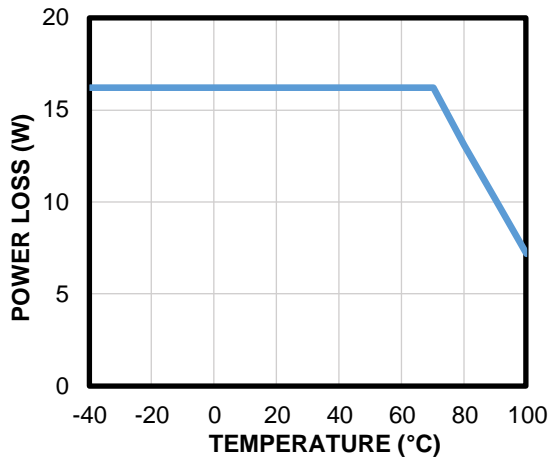
# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN}$ = 12V, single channel, $f_{SW}$ = 600kHz, $T_A$ = 25°C, unless otherwise noted.

**Steady Ripple**
$V_{OUT}$ = 1.2V, $I_{OUT}$ = 0A,
$C_{OUT}$: 6 x 47µF + 330µF
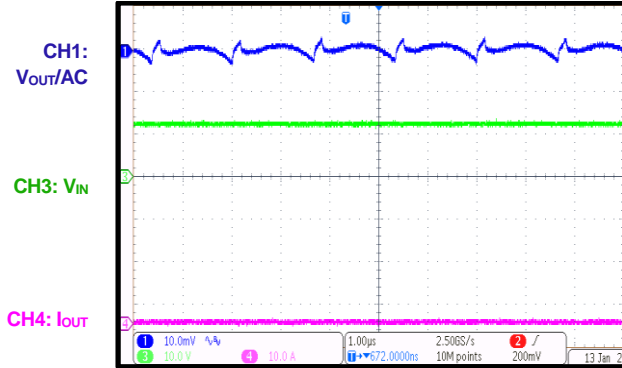
**Steady Ripple**
$V_{OUT}$ = 1.2V, $I_{OUT}$ = 25A,
$C_{OUT}$: 6 x 47µF + 330µF
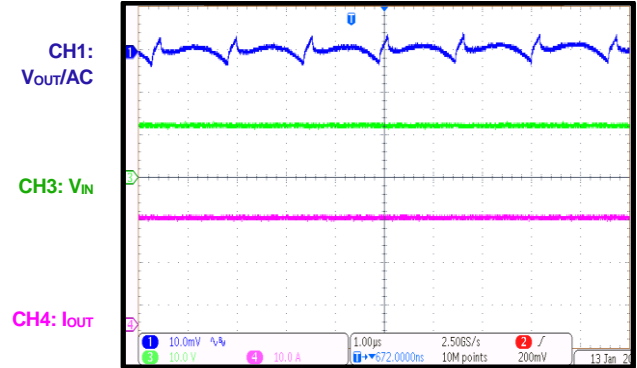
**Steady Ripple**
$V_{OUT}$ = 1V, $I_{OUT}$ = 0A, $C_{OUT}$: 6 x 47µF + 330µF
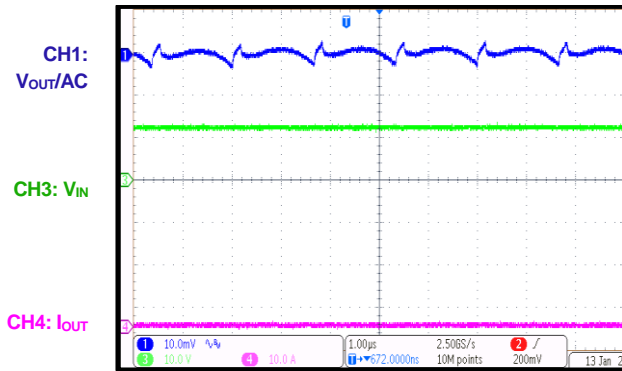
**Steady Ripple**
$V_{OUT}$ = 1V, $I_{OUT}$ = 25A, $C_{OUT}$: 6 x 47µF + 330µF
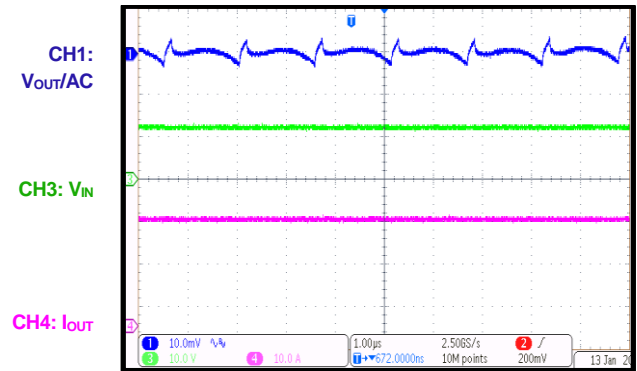
**Steady Ripple**
$V_{OUT}$ = 0.8V, $I_{OUT}$ = 0A,
$C_{OUT}$: 6 x 47µF + 330µF
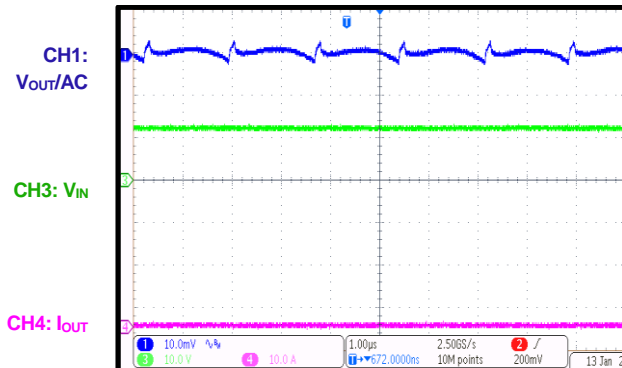
**Steady Ripple**
$V_{OUT}$ = 0.8V, $I_{OUT}$ = 25A,
$C_{OUT}$: 6 x 47µF + 330µF
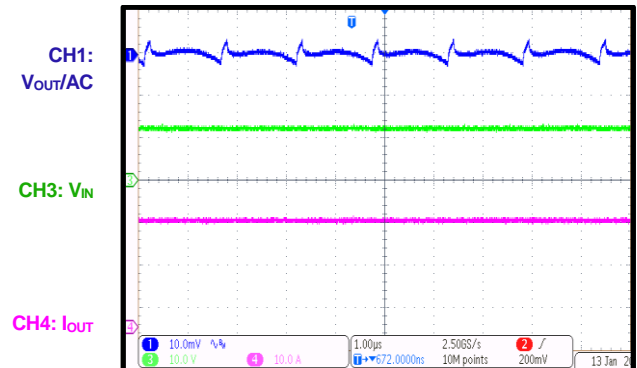
# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN}$ = 12V, single channel, $f_{SW}$ = 600kHz, $T_A$ = 25°C, unless otherwise noted.

### Start-Up through VIN
$V_{OUT}$ = 1.2V, $I_{OUT}$ = 0A
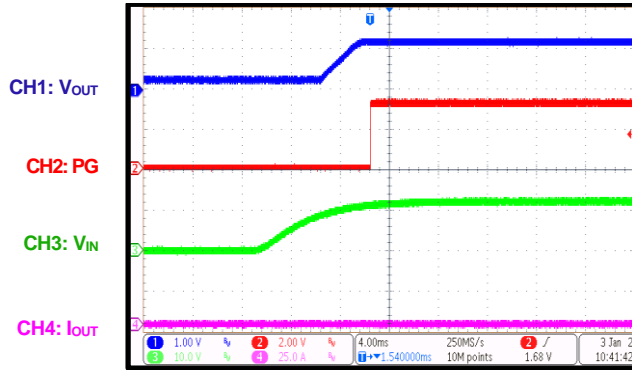


### Start-Up through VIN
$V_{OUT}$ = 1.2V, $I_{OUT}$ = 25A
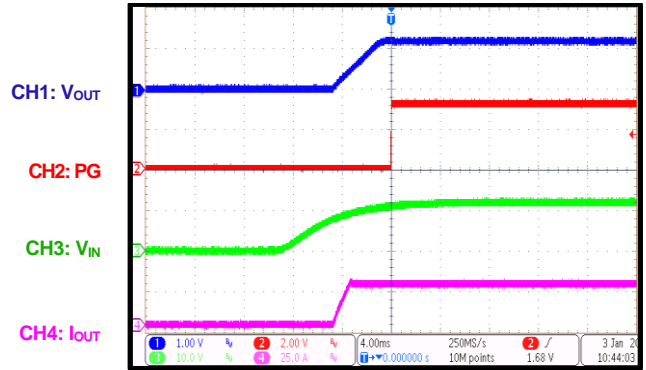


### Shutdown through VIN
$V_{OUT}$ = 1.2V, $I_{OUT}$ = 0A
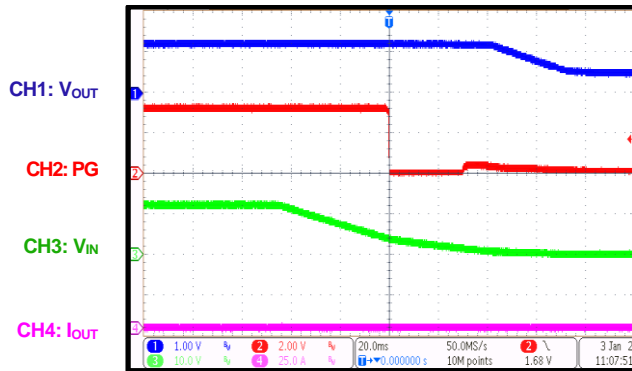


### Shutdown through VIN
$V_{OUT}$ = 1.2V, $I_{OUT}$ = 25A
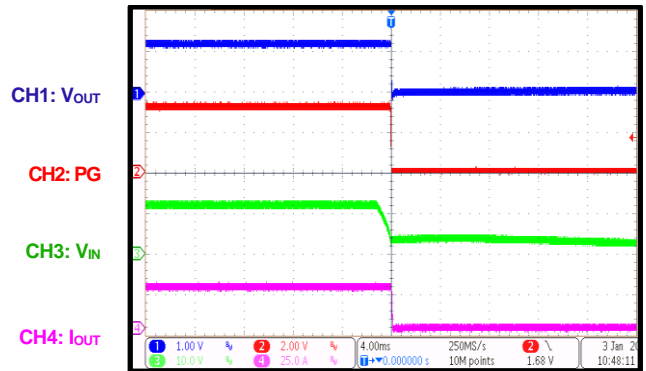


### SCP
$V_{OUT}$ = 1.2V
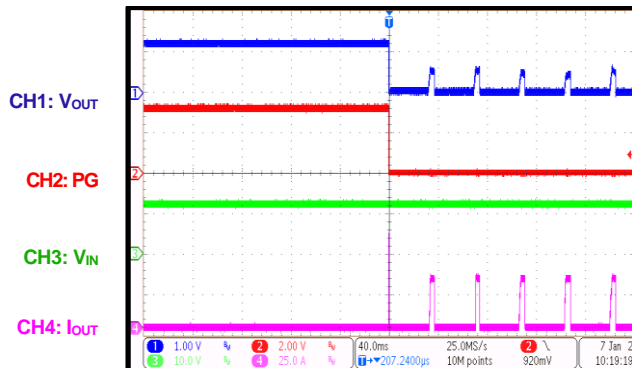


### Transient
$V_{OUT1}$ = 1.2V, step: 0A to 10A, $f_{SW}$ = 600kHz, slew rate = 10A/µS, RAMP = 15.1mV, $C_{OUT}$ = 10 x 47µF MLCC + 2 x 330µF POSCAP capacitor, undershoot = -27mV, overshoot = 29mV
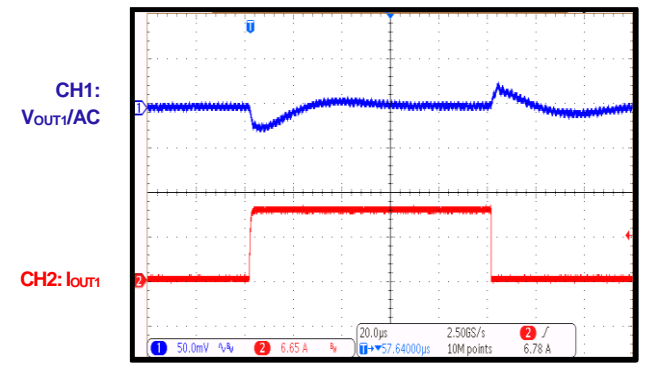
# TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

$V_{IN}$ = 12V, quad channel, $f_{SW}$ = 600kHz, $T_A$ = 25°C, unless otherwise noted.

**Steady Ripple**
$V_{OUT1/2/3/4}$ = 1.2V, $I_{OUT1/2/3/4}$ = 0A,
$C_{OUT}$ per output: 6 x 47µF + 330µF
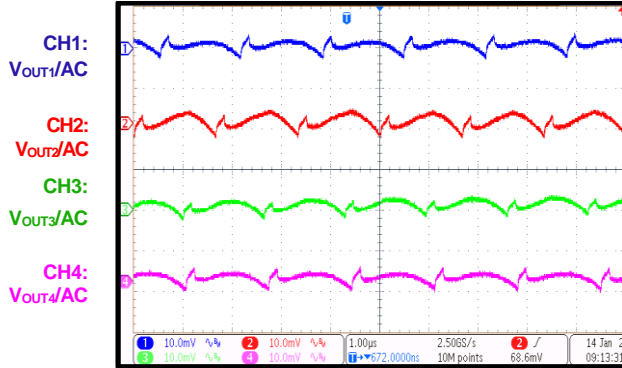
**Steady Ripple**
$V_{OUT1/2/3/4}$ = 1.2V, $I_{OUT1/2/3/4}$ = 25A,
$C_{OUT}$ per output: 6 x 47µF + 330µF
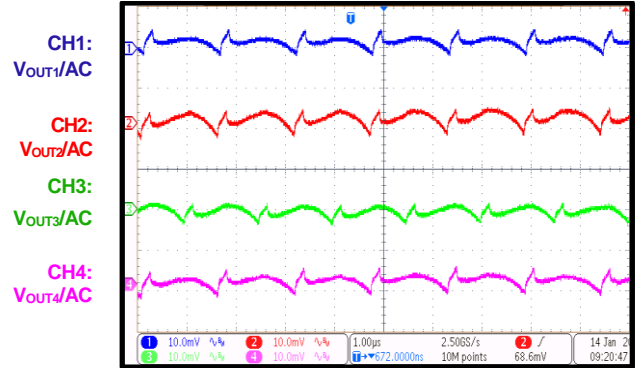
**Start-Up through VIN**
$V_{OUT1/2/3/4}$ = 1.2V, $I_{OUT1/2/3/4}$ = 0A
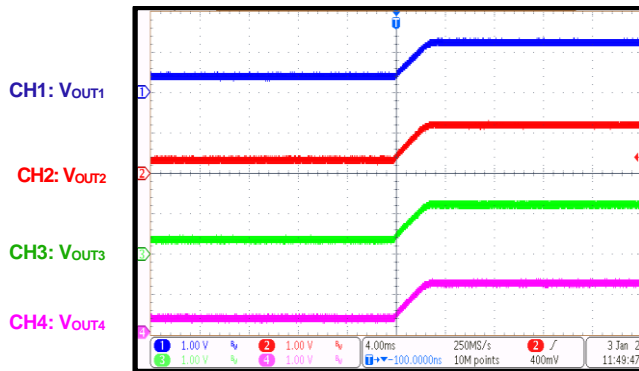
**Start-Up through VIN**
$V_{OUT1/2/3/4}$ = 1.2V, $I_{OUT1/2/3/4}$ = 25A
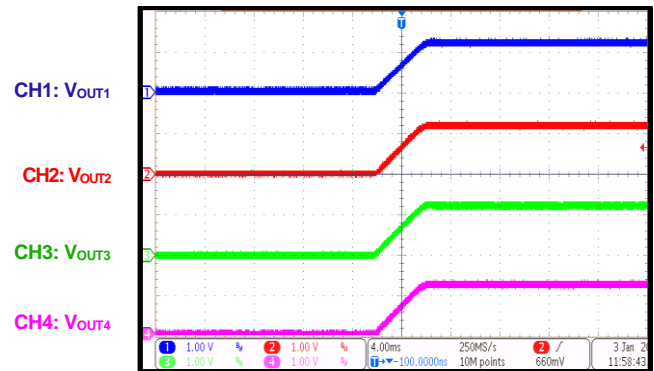
**Shutdown through VIN**
$V_{OUT1/2/3/4}$ = 1.2V, $I_{OUT1/2/3/4}$ = 0A
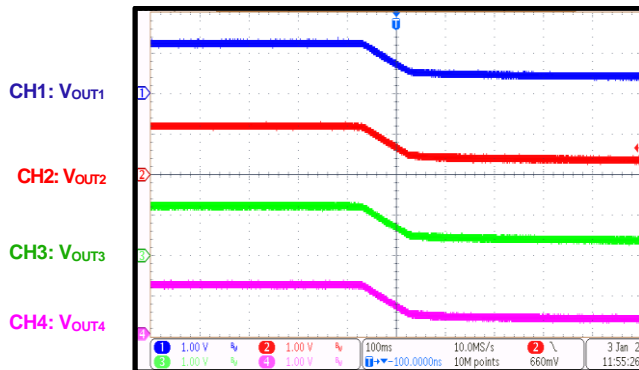
**Shutdown through VIN**
$V_{OUT1/2/3/4}$ = 1.2V, $I_{OUT1/2/3/4}$ = 25A
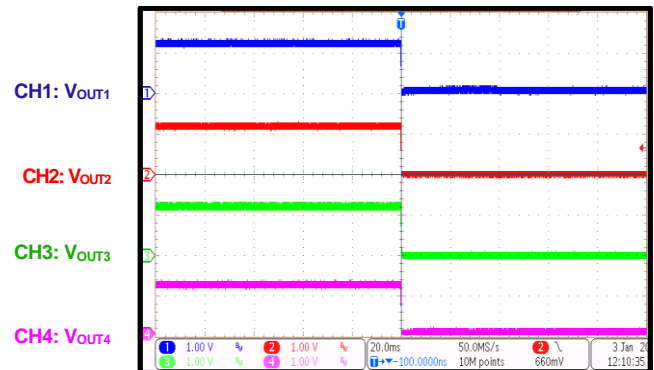
# FUNCTIONAL BLOCK DIAGRAM
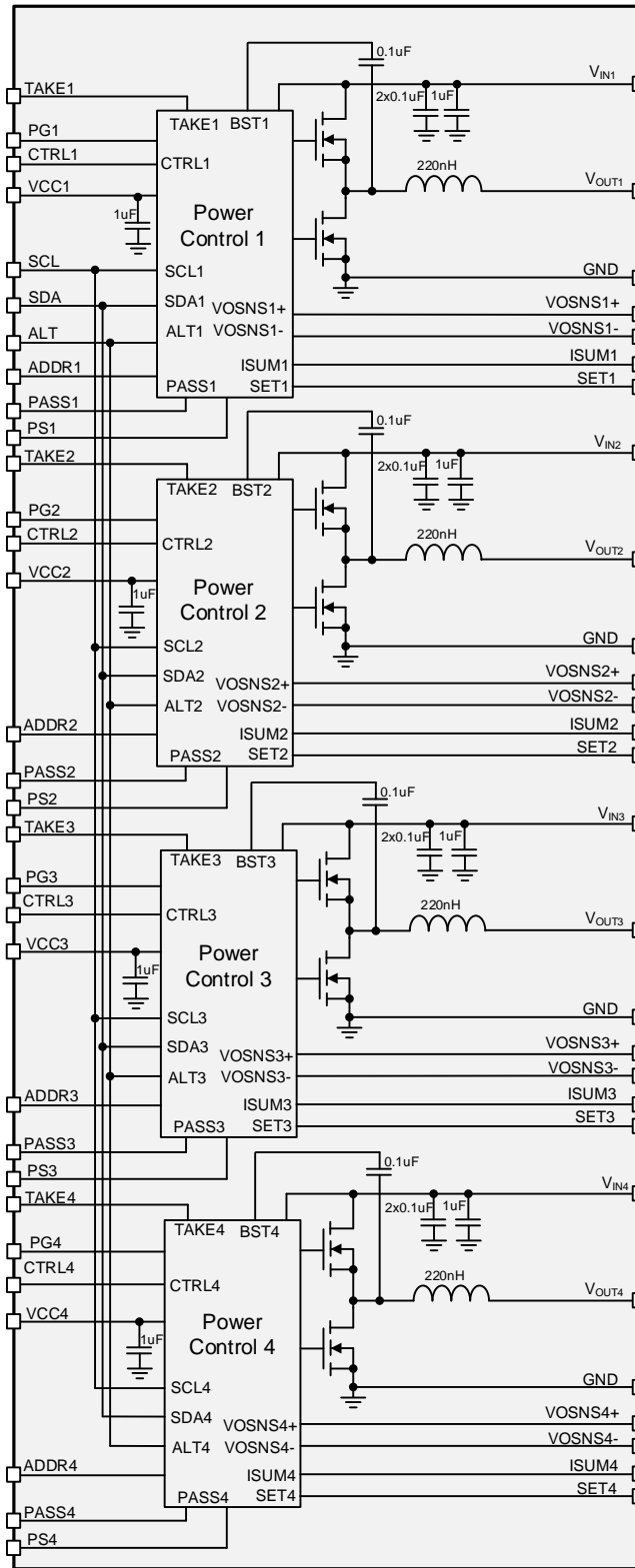


**Figure 3: Functional Block Diagram**
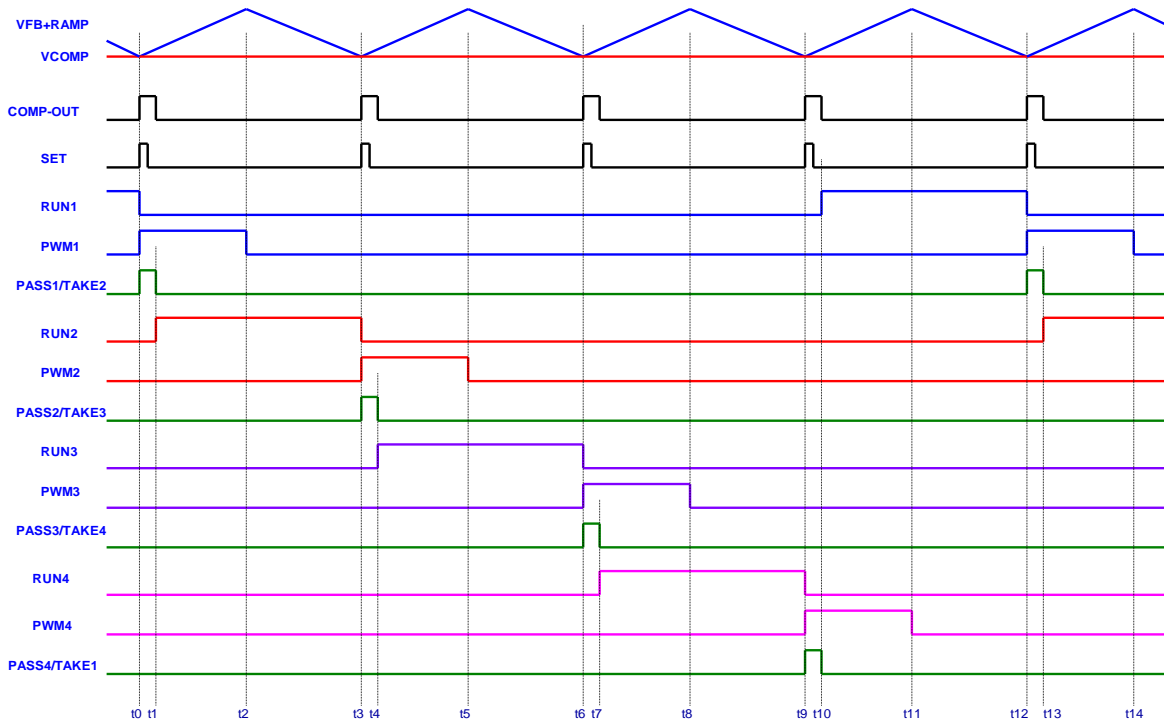
**Figure 4: Multi-Phase Operation Timing Diagram (Steady State)**
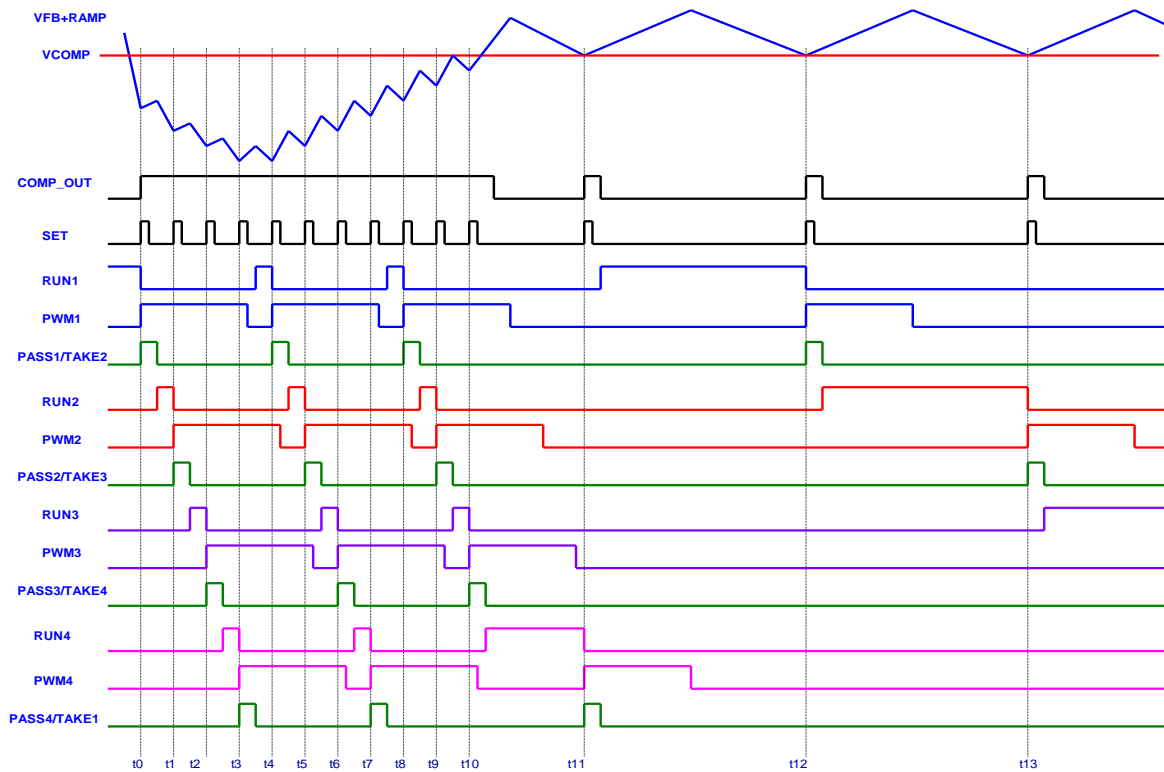
**Figure 5: Multi-Phase Operation Timing Diagram (Transient)**

# OPERATION

The MPM82504 is a fully integrated power module with four outputs. It provides up to 25A of continuous output current in a compact BGA (15mmx30mmx5.18mm) package.

For applications that require more than 25A, the MPM82504's four channels can be connected in parallel to deliver an output current up to 100A. For applications that require more than 100A, the MPM82504 can be connected to another MPM82504 in parallel, or it can be connected to the MPM3695-100.

The MPM82504 employs multi-phase constant-on-time (MCOT) control to provide a fast transient response. Internal ramp compensation guarantees stable operation for applications using zero-ESR ceramic output capacitors.

## Poly-Phase Architecture

The MPM82504 integrates four sets of half-bridges with a power controller in each power module. During single-channel operation, the four channels function independently. In parallel operation, the phases of parallel channels are phase-shifted to minimize the output voltage ripple. For parallel operation, one of the internal phases must be configured as the master phase, while the other phases are slave phases.

## Parallel Operation

In a parallel configuration, one master channel (and one or more slave channels) are connected in parallel. The output current ($I_{OUT}$) is equally shared among all MPM82504 channels with active current balancing. In parallel operation, each switching period is divided by up to 8 interleaved phases with a phase shift of 45 degrees. The master module's TAKE pin must be pulled up to a 3.3V voltage source through a resistor. The MPM82504 detects its master/slave configuration by monitoring the state of the TAKE pin during start-up.

## MCOT Operation: Master Phase

A master phase performs the following functions:

- Accepts both write and read commands through the PMBus from a host.

- Generates the SET signal.

- Manages start-up, shutdown, and all the protection functions.

- Monitors fault alerts from the slave phases through the PG pin.

- Generates the first on pulse.

- Generates the on pulse when receiving RUN and SET signals.

- Dynamically adjusts its on time to ensure equal current sharing.

- Generates the PASS signal.

## MCOT Operation: Slave Phases

The slave phases perform the following functions:

- Accept write commands through the PMBus from a host.

- Take a SET signal from a master phase.

- Start the on pulse when receiving RUN and SET signals.

- Dynamically adjust their on time to ensure equal current sharing on their own phase based on the per-phase and total current.

- Generate the PASS signal.

Figure 4 on page 21 shows MCOT operation. At t0, a SET pulse is generated by the master phase when ($V_{FB}$ + RAMP) drops below the reference level ($V_{COMP}$). All the phases receive this SET signal, but only the phase that has an active RUN signal (i.e. the master) takes action. Then the master turns on the high-side MOSFET (HS-FET). Meanwhile, the MPM82504 generates a fixed-width pulse on the PASS pin, and passes it to the TAKE pin from the first slave (Slave 1).

At t1, the falling edge of the TAKE pin from Slave 1 activates the RUN signal. This means that Slave 1 waits for the SET signal to turn on its HS-FET.

At t2, the PWM signal on time from the master phase expires, and the HS-FET turns off. The PWM signal on time is fixed for a given input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and switching frequency ($f_{SW}$). The on time for each phase is fine-tuned based on the per-phase and total current to ensure equal current sharing among phases.

At t3, ($V_{FB}$ + RAMP) drops below the reference level ($V_{COMP}$) in the master phase again. Slave 1 has an active RUN signal, so it turns on its HS-FET. All other phases ignore this SET signal. Meanwhile, Slave 1 generates a fixed-width pulse on the PASS pin, and passes it to the TAKE pin of Slave 2. The MPM82504 repeats this process for each phase to turn the HS-FETs on one by one for a fixed on time.

The MPM82504 uses MCOT control to achieve a fast load transient response (see Figure 5 on page 21). The SET signal is generated more frequently during a load transient than during steady state. Consequently, energy is delivered to the load at a higher rate, which minimizes the output deviation during a load transient event. The SET pulses can be generated with a minimum 50ns interval, meaning the next phase can be turned on about 50ns after the previous phase turns on.

### RAMP Compensation

The MPM82504 operates with zero-ESR ceramic output capacitors by using internal RAMP compensation. A triangular RAMP signal is generated internally, then superimposed onto the FB signal.

The triangular RAMP signal starts to rise once ($V_{FB}$ + RAMP) drops below the reference signal, and a SET pulse is generated. The RAMP signal rise time is fixed. The amplitude of the RAMP compensation is selectable through register D0h, bits[3:1] to support a wide range of operation configurations.

There is a tradeoff between stability and load transient response. A larger RAMP signal provides better stability but slower load transient response, and vice versa. Optimize RAMP compensation selection based on the design criteria for each application (see Table 5 on page 24).

### Phase-Shedding Operation

For multi-phase operation, the slave phases can be enabled or disabled through the PMBus or PSx pin. The phase-shedding function is disabled in the master phase to ensure proper operation. If phase-shedding is controlled through the PMBus, then register E5h, bit[0] is used. If E5h, bit[0] = 1b'0, the slave phases are enabled. If E5h, bit[0] = 1b'1, the slave phases are disabled.

If phase-shedding is controlled through the PS pin, the E5h[1] command must be set to 1b'1. If PSx is pulled high, the slave phases are enabled. If PSx is pulled low, the slave phases are disabled.

**Table 5: Recommended RAMP and Resistor Divider Values**

| Parallel Mode | $V_{IN}$ (V) | $V_{OUT}$ (V) | $f_{SW}$ (kHz) | RAMP (mV) | Upper Divider (kΩ) | Lower Divider (kΩ) | $C_{FF}$ (nF) |
|---|---|---|---|---|---|---|---|
| Single channel | 12 | 0.75 | 600 | 27 | 1 | 4.02 | 22 |
| Single channel | 12 | 1 | 600 | 27 | 1 | 1.5 | 22 |
| Single channel | 12 | 1.2 | 600 | 27 | 1 | 1 | 22 |
| Single channel | 12 | 1.8 | 800 | 27 | 2 | 1 | 22 |
| Single channel | 12 | 3.3 | 1000 | 27 | 4.53 | 1 | 22 |
| Two paralleled channels | 12 | 0.75 | 600 | 41 | 1 | 4.02 | 22 |
| Two paralleled channels | 12 | 1 | 600 | 41 | 1 | 1.5 | 22 |
| Two paralleled channels | 12 | 1.2 | 600 | 41 | 1 | 1 | 22 |
| Two paralleled channels | 12 | 1.8 | 800 | 68 | 2 | 1 | 22 |
| Two paralleled channels | 12 | 3.3 | 1000 | 68 | 4.53 | 1 | 22 |
| Three paralleled channels | 12 | 0.75 | 600 | 41 | 1 | 4.02 | 22 |
| Three paralleled channels | 12 | 1 | 600 | 41 | 1 | 1.5 | 22 |
| Three paralleled channels | 12 | 1.2 | 600 | 41 | 1 | 1 | 22 |
| Three paralleled channels | 12 | 1.8 | 800 | 68 | 2 | 1 | 22 |
| Three paralleled channels | 12 | 3.3 | 1000 | 68 | 4.53 | 1 | 22 |
| Four paralleled channels | 12 | 0.75 | 600 | 41 | 1 | 4.02 | 22 |
| Four paralleled channels | 12 | 1 | 600 | 41 | 1 | 1.5 | 22 |
| Four paralleled channels | 12 | 1.2 | 600 | 41 | 1 | 1 | 22 |
| Four paralleled channels | 12 | 1.8 | 800 | 68 | 2 | 1 | 22 |
| Four paralleled channels | 12 | 3.3 | 1000 | 68 | 4.53 | 1 | 22 |

# PMBUS INTERFACE

## PMBus Serial Interface Description

The Power Management Bus (PMBus) is an open-standard, power management protocol that defines a means of communication with power conversion and other devices.

The PMBus is a two-wire, bidirectional, serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled up to a bus voltage when they are in an idle state. When connecting to the lines, a master device generates the SCL signal and device address, then arranges the communication sequence. The MPM82504 is a PMBus slave device that supports both standard mode (100kHz) and fast modes (400kHz and 1000kHz).

## Slave Address

A unique address should be set for each slave device that is connected to the same PMBus. The ADDR pin configures the address for the MPM82504. There is a 10µA current flowing out of the ADDR pin. Connect a resistor between the ADDR pin and AGND to set the ADDR voltage. The internal analog-to-digital converter (ADC) converts the pin voltage of the ADDR pin to set the PMBus address. A maximum of 16 addresses can be set by the ADDR pin. Table 6 lists the PMBus address for different resistor values. MFR_ADDR_PMBUS (D3h) can be used to digitally set the PMBus address.

For multi-phase configuration, the slave phases can share the same address as the master, or they can have different addresses, depending on the application requirements. The slave phases can only accept write commands, which means they cannot accept read commands from the PMBus master. However, the master phase can accept both write and read commands from the PMBus master.

## Start and Stop Conditions

Start and stop conditions are signaled by the master device to indicate the beginning and the end of the PMBus transfer. A start (S) condition is defined as the SDA signal transitioning from high to low while SCL is high. A stop (P) condition is defined as the SDA signal transitioning from low to high while SCL is high (see Figure 6 on page 26).

**Table 6: PMBus Address vs. ADDR Resistor**

| R$_{ADDR}$ (kΩ) | Slave Address |
|---|---|
| 4.99 | 30h |
| 15 | 31h |
| 24.9 | 32h |
| 34.8 | 33h |
| 45.3 | 34h |
| 54.9 | 35h |
| 64.9 | 36h |
| 75 | 37h |
| 84.5 | 38h |
| 95.3 | 39h |
| 105 | 3Ah |
| 115 | 3Bh |
| 124 | 3Ch |
| 133 | 3Dh |
| 147 | 3Eh |
| 154 | 3Fh |

The master then generates the SCL clocks, and transmits the device address and the read/write (R/W) direction bit on the SDA line. Data is transferred in 8-bit bytes by the SDA line. Each byte of data must be followed by an acknowledge (ACK) bit.

## PMBus Update Sequence

The MPM82504 requires a start condition, a valid PMBus address, a register address byte, and a data byte for a single data update. After receiving each byte, the MPM82504 acknowledges this process by pulling the SDA line low during the high period of a single clock pulse. A valid PMBus address selects the MPM82504. The MPM82504 performs an update on the falling edge of the LSB byte.

## Protocol Usage

All PMBus transactions are accomplished using defined bus protocols. The following protocols can be implemented:

- Send byte with packet error checking (PEC)
- Receive byte with PEC
- Write byte with PEC
- Read byte with PEC
- Write word with PEC
- Read word with PEC

- Block read with PEC

## PMBus Message Format

Figure 7 on page 27 shows the message formats. Unshaded cells indicate that the bus host is actively driving the bus, while shaded cells indicate that the MPM82504 is driving the bus. The symbols are defined below:

- S = Start condition
- Sr = Repeated start condition
- P = Stop condition
- R = Read bit
- $\overline{W}$ = Write bit
- A = Acknowledge bit (0)
- $\overline{A}$ = Acknowledge bit (1)

A represents the acknowledge (ACK) bit. The ACK bit is typically active low (logic 0) if the transmitted byte is successfully received by a device. However, when the receiving device is the bus master, the ACK bit for the last byte read is a logic 1, which is indicated with $\overline{A}$.

## Packet Error Checking (PEC)

The MPM82504's PMBus interface supports the use of the packet error checking (PEC) byte. The PEC byte is transmitted by the MPM82504 during a read transaction, or sent by the bus host to the MPM82504 during a write transaction.

The PEC byte detects errors during a bus transaction, depending on whether the transaction is a read or a write. If the host determines that the PEC byte read during a read transaction is incorrect, it can decide to repeat the read if necessary. If the MPM82504

determines that the PEC byte sent during a write transaction is incorrect, it ignores the command (does not execute it) and sets a status flag. Within a group command, the host can choose to send or not send a PEC byte as part of the message to the MPM82504.

## PMBus Alert Response Address (ARA)

The PMBus alert response address (ARA) is a special address that can be used by the bus host to locate any devices with which it can communicate. A host typically uses a hardware interrupt pin to monitor the PMBus ALERT pins from a number of devices. When the host interrupt occurs, the host issues a message on the bus using the PMBus receive byte, or the received byte with PEC protocol.

The special address used by the host is 0x0C. Any devices that have a PMBus alert signal return their own 7-bit address as the 7MSB of the data byte. The LSB value is not used and can be either 1 or 0. The host reads the device address from the received data byte and proceeds to handle the alert condition.

More than one device may have an active PMBus alert signal and attempt to communicate with the host. In this case, the device with the lowest address dominates the bus and succeeds in transmitting its address to the host. The device that succeeds disables its PMBus alert signal. If the host sees that the PMBus alert signal is still low, it continues to read addresses until all devices have successfully transmitted their addresses.
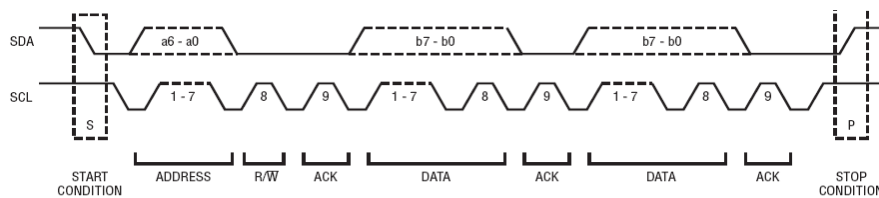


**Figure 6: Data Transfer through the PMBus**

a) Send Byte and Send Byte with PEC

| 1 | 7 | 1 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Data Byte | A | P |

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Data Byte | A | PEC | A | P |

b) Receive Byte and Receive Byte with PEC

| 1 | 7 | 1 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| S | Slave Address | Rd | A | Data Byte | A | P |

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Rd | A | Data Byte | A | PEC | A | P |

c) Write Byte and Write Byte with PEC

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Command Code | A | Data Byte | A | P |

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Command Code | A | Data Byte | A | PEC | A | P |

d) Write Word and Write Word with PEC

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Command Code | A | Data Byte Low | A | Data Byte High | A | P |

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Command Code | A | Data Byte Low | A | Data Byte High | A | PEC | A | P |

e) Read Byte and Read Byte with PEC

| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Command Code | A | S | Slave Address | Rd | A | Data Byte | A | P |

| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Command Code | A | S | Slave Address | Rd | A | Data Byte | A | PEC | A | P |

f) Read Word and Read Word with PEC

| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Command Code | A | S | Slave Address | Rd | A | Data Byte Low | A |

| 8 | 1 | 1 |
|---|---|---|
| Data Byte High | A | P |

| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Command Code | A | S | Slave Address | Rd | A | Data Byte Low | A |

| 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|
| Data Byte High | A | PEC | A | P |

g) Block Read with PEC

| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Command Code | A | S | Slave Address | Rd | A | Byte Count = N | A | … |

| 8 | 1 | 8 | 1 | … | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|
| Data Byte1 | A | Data Byte 2 | A | … | Data Byte N | A | P |

| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | Command Code | A | S | Slave Address | Rd | A | Byte Count = N | A | … |

| 8 | 1 | 8 | 1 | … | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|
| Data Byte1 | A | Data Byte 2 | A | … | Data Byte N | A | PEC | A | P |

**Figure 7: PMBus Message Format**

## Data and Numerical Formats

The MPM82504 uses a direct internal format to represent real-world values such as voltage, current, power, and temperature except register 8Dh.

All numbers with no suffix in this document are decimals, unless explicitly designated otherwise.

Numbers in binary format are indicated by the prefix "n'b", where n is the binary count. For example, 5'b01010 indicates a 5-bit binary data where the data is 01010.

The suffix "h" indicates a hexadecimal format, which is generally used for the register address number in this document.

The symbol "0x" indicates a hexadecimal format, which is used for the value in the register. For example, 0xA3 is a 1-byte number with a hexadecimal value of A3.

## PMBus Communication Failure

A data transmission fault occurs when data is not properly transferred between the devices. There are several data transmission faults:

- Sending too little data
- Reading too little data
- Sending too many bytes
- Reading too many bytes
- Improperly set read bit in the address byte
- Unsupported command code

## PMBus Reporting and Status Monitoring

The MPM82504 supports real-time monitoring for some operation parameters and statuses with the PMBus interface (see Table 7).

**Table 7: PMBus Monitored Parameters and Statuses**

| Parameter/Status | PMBus |
|:---|:---:|
| $V_{OUT}$ | 1.25mV/LSB |
| $I_{OUT}$ | 62.5mA/LSB |
| Temperature | 1°C/LSB |
| $V_{IN}$ | 25mV/LSB |
| $V_{IN}$ over-voltage (OV) | ✓ |
| $V_{IN}$ under-voltage (UV) | ✓ |
| $V_{IN}$ OV warning | ✓ |
| $V_{IN}$ UV warning | ✓ |
| $V_{OUT}$ OV | ✓ |
| $V_{OUT}$ UV | ✓ |
| Over-temperature (OT) | ✓ |
| OT warning | ✓ |
| $V_{OUT}$ over-current (OC) | ✓ |
| $V_{OUT}$ OC warning | ✓ |

## MTP Programming

The MPM82504 has a built-in multiple-time programmable (MTP) memory to store user configurations. The standard command register STORE_USER_ALL (15h) is not supported by the MPM82504. Instead, the MTP cells can be configured using the following command combination:

1. E7h (2000h)
2. E7h (1000h)
3. E7h (4000h)

In the GUI, the above commands are integrated together and named STORE_USER_ALL. Though the MPM82504 does not directly support the 15h command, the device can accept the 15h command from MPS's GUI. The GUI can be downloaded from the MPS website.

When the MTP is being configured, the VCC voltage may go up as high as 5V. Ensure that VCC is connected to circuits that can withstand this voltage. MTP configuration typically takes about 300ms.

## REGISTER MAP

| Name | Page [11] | Code | Type | Bytes | Default Value (Configuration Code: 0000) | MTP |
|------|-----------|------|------|-------|------------------------------------------|-----|
| OPERATION | 1 | 01h | R/W with PEC | 1 | 0x80 | ✓ |
| ON_OFF_CONFIG | 1 | 02h | R/W with PEC | 1 | 0x1e | ✓ |
| CLEAR_FAULTS | 1 | 03h | Send byte with PEC | 0 | - | - |
| WRITE_PROTECT | 1 | 10h | R/W with PEC | 1 | 0x00 | ✓ |
| STORE_USER_ALL | 1 | 15h | Send byte with PEC | 0 | - | - |
| RESTORE_USER_ALL | 1 | 16h | Send byte with PEC | 0 | - | - |
| CAPABILITY | 1 | 19h | R with PEC | 1 | 0xB0 | - |
| VOUT_MODE | 1 | 20h | R with PEC | 1 | 0x40 | - |
| VOUT_COMMAND | 1 | 21h | R/W with PEC | 2 | 0x01A9 (0.85V) | ✓ |
| VOUT_MAX | 1 | 24h | R/W with PEC | 2 | 0x0BB8 (6V) | ✓ |
| VOUT_MARGIN_HIGH | 1 | 25h | R/W with PEC | 2 | 0x02A0 (1.344V) | ✓ |
| VOUT_MARGIN_LOW | 1 | 26h | R/W with PEC | 2 | 0x01FE (1.02V) | ✓ |
| VOUT_SCALE_LOOP | 1 | 29h | R/W with PEC | 2 | 0x02C2 (0.706) | ✓ |
| VOUT_MIN | 1 | 2Bh | R/W with PEC | 2 | 0x00FA (0.5V) | ✓ |
| VIN_ON | 1 | 35h | R/W with PEC | 2 | 0x0012 (4.5V) | ✓ |
| VIN_OFF | 1 | 36h | R/W with PEC | 2 | 0x000B (2.75V) | ✓ |
| OT_FAULT_LIMIT | 1 | 4Fh | R/W with PEC | 2 | 0x00A0 (160°C) | ✓ |
| OT_WARN_LIMIT | 1 | 51h | R/W with PEC | 2 | 0x008C (140°C) | ✓ |
| VIN_OV_FAULT_LIMIT | 1 | 55h | R/W with PEC | 2 | 0x0024 (18V) | ✓ |
| VIN_OV_WARN_LIMIT | 1 | 57h | R/W with PEC | 2 | 0x0022 (17V) | ✓ |
| VIN_UV_WARN_LIMIT | 1 | 58h | R/W with PEC | 2 | 0x0001 (0.25V) | ✓ |
| TON_DELAY | 1 | 60h | R/W with PEC | 2 | 0x0000 (0ms) | ✓ |
| TON_RISE | 1 | 61h | R/W with PEC | 2 | 0x0002 (4ms) | ✓ |
| TOFF_DELAY | 1 | 64h | R/W with PEC | 2 | 0x0000 (0ms) | ✓ |
| STATUS_BYTE | 1 | 78h | R with PEC | 1 | - | - |
| STATUS_WORD | 1 | 79h | R with PEC | 2 | - | - |
| STATUS_VOUT | 1 | 7Ah | R with PEC | 1 | - | - |
| STATUS_IOUT | 1 | 7Bh | R with PEC | 1 | - | - |
| STATUS_INPUT | 1 | 7Ch | R with PEC | 1 | - | - |
| STATUS_TEMPERATURE | 1 | 7Dh | R with PEC | 1 | - | - |
| STATUS_CML | 1 | 7Eh | R with PEC | 1 | - | - |
| READ_VIN | 1 | 88h | R with PEC | 2 | - | - |
| READ_VOUT | 1 | 8Bh | R with PEC | 2 | - | - |
| READ_IOUT | 1 | 8Ch | R with PEC | 2 | - | - |
| READ_TEMPERATURE_1 | 1 | 8Dh | R with PEC | 2 | - | - |
| MFR_CTRL_COMP | 1 | D0h | R/W with PEC | 1 | 0x0D | ✓ |
| MFR_CTRL_VOUT | 1 | D1h | R/W with PEC | 1 | 0x00 | ✓ |
| MFR_CTRL_OPS | 1 | D2h | R/W with PEC | 1 | 0x03 | ✓ |
| MFR_ADDR_PMBUS | 1 | D3h | R/W with PEC | 1 | 0x30 | ✓ |
| MFR_VOUT_FAULT_LIMIT | 1 | D4h | R/W with PEC | 1 | 0x03 | ✓ |
| MFR_OVP_NOCP_SET | 1 | D5h | R/W with PEC | 1 | 0x02 | ✓ |
| MFR_OT_OC_SET | 1 | D6h | R/W with PEC | 1 | 0x09 | ✓ |
| MFR_OC_PHASE_LIMIT | 1 | D7h | R/W with PEC | 1 | 0x11 | ✓ |
| MFR_PGOOD_ON_OFF_LIMIT | 1 | D9h | R/W with PEC | 1 | 0x00 | ✓ |
| MFR_VOUT_STEP | 1 | DAh | R/W with PEC | 1 | 0x04 | ✓ |
| MFR_LOW_POWER | 1 | E5h | R/W with PEC | 1 | 0x00 | ✓ |
| MFR_CTRL | 1 | EAh | R/W with PEC | 2 | 0x72 bit[9] = 1, bit[3] = 0 | ✓ |

**Notes:**

11) The registers of Pages 1–4 are the same, but the default values may be different.

## OPERATION (01h)

The OPERATION command is a paged register. This command turns the converter output on and off in conjunction with input from the CTRL pin. It also sets $V_{OUT}$ to the upper or lower margin voltages. The device remains in the commanded operating mode until a subsequent OPERATION command (or a change in the state of the CTRL pin) instructs the converter to change to another mode.

This command can re-enable the converter after a fault-triggered shutdown. Writing an off command followed by an on command clears all faults. Writing only an on command after a fault-triggered shutdown does not clear the fault registers. See the Default MTP Configuration section on page 47 for the default values.

| Command | OPERATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R | R |
| Function | | | | | | | X | |

| Bits[7:6] | Bits[5:4] | Bits[3:2] | Bits[1:0] | On/Off | Margin State | 01h |
|---|---|---|---|---|---|---|
| 00 | xx | xx | xx | Immediate off | N/A | 0x00 |
| 01 | xx | xx | xx | Soft shutdown | N/A | 0x60 |
| 10 | 00 | xx | xx | On | Off | 0x80 |
| 10 | 01 | 01 | xx | On | Margin low (ignore fault) | 0x94 |
| 10 | 01 | 10 | xx | On | Margin low (act on fault) | 0x98 |
| 10 | 10 | 01 | xx | On | Margin high (ignore fault) | 0xA4 |
| 10 | 10 | 10 | xx | On | Margin high (act on fault) | 0xA8 |

## ON_OFF_CONFIG (02h)

The ON_OFF_CONFIG command configures the combination of CTRL pin input and PMBus commands required to turn the converter on and off. This includes how the converter responds when $V_{IN}$ is applied.

| Command | ON_OFF_CONFIG | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R/W | R/W | R/W | R/W | R |
| Function | X | | | ON | OP | CTRL | POL_CTRL | DELAY |

### ON

The ON bit sets the default to either operate whenever $V_{IN}$ is present, or for the on/off operation to be controlled by the CTRL pin and PMBus commands.

| Bit[4] Value | Description |
|---|---|
| 0 | The converter starts up any time $V_{IN}$ is present, regardless of state of the CTRL pin. |
| 1 | The converter does not start up unless commanded by the CTRL pin and OPERATION command (as configured in bits[3:0]). |

### OP

This OP bit controls how the converter responds to the OPERATION commands.

| Bit[3] Value | Description |
|---|---|
| 0 | The converter ignores the ON bit in the OPERATION command from the PMBus. |
| 1 | The converter responds to the ON bit in the OPERATION command from the PMBus. |

## CTRL

The CTRL bit controls how the converter responds to the CTRL pin.

| Bit[2] Value | Description |
|---|---|
| 0 | The converter ignores the CTRL pin (the device turning on and off is only controlled by the OPERATION command). |
| 1 | The converter requires the CTRL pin to be asserted to start up. Depending on bit[3] (OP), the OPERATION command may also be required to instruct the converter to start up. |

## POL_CTRL

The POL_CTRL bit sets the polarity of the CTRL pin. This function is disabled.

| Bit[1] Value | Description |
|---|---|
| 0 | Active low (pull the CTRL pin low to start the converter). |
| 1 | Active high (pull the CTRL pin high to start the converter). |

## DELAY

The DELAY bit sets the shutdown action when the converter is commanded off through the PMBus. This bit is read-only and cannot be modified by the end user.

| Bit[0] Value | Description |
|---|---|
| 0 | The device uses the configured turn off delay and fall time. |

## CLEAR_FAULTS (03h)

The CLEAR_FAULTS command resets all stored warning and fault flags. If a fault or warning condition still exists when the CLEAR_FAULTS command is issued, the ALT# signal may not be cleared, or it is re-asserted almost immediately. Issuing a CLEAR_FAULTS command does not cause the converter to restart in the event of a fault shutdown. To restart the device, issue an OPERATION on command after the fault condition is cleared. This command uses the PMBus to send the byte protocol.

## WRITE_PROTECT (10h)

The WRITE_PROTECT command controls writing to the converter. The provides protection against accidental changes.

All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings.

| Bits[7:0] Value | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Enables writes to all commands. |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Disables all writes except to the WRITE_PROTECT, OPERATION, PAGE, ON_OFF_CONFIG, and VOUT_COMMAND commands. |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | Disables all writes except to the WRITE_PROTECT, OPERATION, and PAGE commands. |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Disables all writes except to the WRITE_PROTECT command. |

When 10h is set to a value other than 0x00 to configure the MTP, register 15h can only be set through MPS's GUI. The MTP's E7h command cannot be used. For more details, see the MTP Programming section on page 28.

The default value for this register is 0x00.

## STORE_USER_ALL (15h)

The STORE_USER_ALL command writes the data from the registers to the internal MTP(s). This occurs when the MPM82504 receives a STORE_USER_ALL command from the PMBus interface. The MPM82504 does not support the 15h command via the MTP. However, the device can accept the 15h command from MPS's GUI. For more details, see the MTP Programming section on page 28.

The following registers can be stored using STORE_USER_ALL:

- OPERATION (01h)
- ON_OFF_CONFIG (02h)
- WRITE_PROTECT (10h)
- VOUT_COMMAND (21h)
- VOUT_MAX (24h)
- VOUT_MARGIN_HIGH (25h)
- VOUT_MARGIN_LOW (26h)
- VOUT_SCALE_LOOP (29h)
- VOUT_MIN (2Bh)
- VIN_ON (35h)
- VIN_OFF (36h)
- OT_FAULT_LIMIT (4Fh)
- OT_WARN_LIMIT (51h)
- VIN_OV_FAULT_LIMIT (55h)
- VIN_OV_WARN_LIMIT (57h)
- VIN_UV_WARN_LIMIT (58h)
- TON_DELAY (60h)
- TON_RISE (61h)
- TOFF_DELAY (64h)
- MFR_CTRL_COMP (D0h)
- MFR_CTRL_VOUT (D1h)
- MFR_CTRL_OPS (D2h)
- MFR_ADDR_PMBUS (D3h)
- MFR_VOUT_FAULT_LIMIT (D4h)
- MFR_OVP_NOCP_SET (D5h)
- MFR_OT_OC_SET (D6h)
- MFR_OC_PHASE_LIMIT (D7h)
- MFR_PGOOD_ON_OFF_LIMIT (D9h)
- MFR_VOUT_STEP (DAh)
- MFR_LOW_POWER (E5h)
- MFR_CTRL (EAh)

### RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the MPM82504 to copy the entire contents of the MTP values to the matching locations in the registers. The values in the registers are overwritten by the value retrieved from the MTP. Any items in the MTP that do not have matching locations in the operating memory are ignored.

This command can be used while the MPM82504 is operating, but the device may be unresponsive.

This command is write-only.

### CAPABILITY (19h)

The CAPABILITY command returns information about the PMBus functions supported by the MPM82504. This command is read with the PMBus read byte protocol.

| Command | CAPABILITY | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | PEC | MAX_BUS_SPEED | | ALERT | X | | | |
| Default Value | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| Details | PEC supported, max speed 1MHz, supports PMBus alert and ARA | | | | | | | |

| Bits[6:5] Value | | Meaning |
|---|---|---|
| 0 | 0 | The maximum supported bus speed is 100kHz. |
| 0 | 1 | The maximum supported bus speed is 1MHz. |
| 1 | 0 | The maximum supported bus speed is 400kHz. |
| 1 | 1 | Reserved. |

The default value for this register is 0xB0.

### VOUT_MODE (20h)

The VOUT_MODE command reads and commands $V_{OUT}$. The 3MSB are used to determine the data format (only direct format is supported), and the remaining 5 bits represent the exponent used in the $V_{OUT}$ read/write commands.

The default value for this register is 0x40.

### VOUT_COMMAND (21h)

The VOUT_COMMAND command sets $V_{OUT}$. To calculate the feedback reference voltage, multiply VOUT_COMMAND by VOUT_SCALE_LOOP.

For more details, see the Setting the Output Voltage section on page 52.

| Command | VOUT_COMMAND | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | X | | | | 2mV/LSB | | | | | | | | | | | |

The value is unsigned, and 1LSB = 2mV. See the Default MTP Configuration section on page 47 for the default values.

## VOUT_MAX (24h)

The VOUT_MAX command sets an upper limit on $V_{OUT}$, regardless of any other commands or combinations. VOUT_MAX provides a safeguard against a user accidentally setting $V_{OUT}$ too high. It does not replace over-voltage protection (OVP).

| Command | VOUT_MAX | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | X | | | | 2mV/LSB | | | | | | | | | | | |

If an attempt is made to set $V_{OUT}$ at a level that exceeds VOUT_MAX, the device takes the following actions:

1. The commanded $V_{OUT}$ is set to VOUT_MAX.

2. The VOUT bit is set in STATUS_WORD.

3. The VOUT_MAX_MIN warning bit is set in the STATUS_VOUT register.

4. The device notifies the host.

The value is unsigned and 1LSB = 2mV. The maximum value of VOUT_MAX is 6V. See the Default MTP Configuration section on page 47 for the default values.

## VOUT_MARGIN_HIGH (25h)

| Command | VOUT_MARGIN_HIGH | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | X | | | | 2mV/LSB | | | | | | | | | | | |

The value is unsigned and 1LSB = 2mV. See the Default MTP Configuration section on page 47 for the default values.

## VOUT_MARGIN_LOW (26h)

| Command | VOUT_MARGIN_LOW | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | X | | | | 2mV/LSB | | | | | | | | | | | |

The value is unsigned and 1LSB = 2mV. See the Default MTP Configuration section on page 47 for the default values.

## VOUT_SCALE_LOOP (29h)

The VOUT_SCALE_LOOP command sets the feedback resistor divider ratio, which is equal to $V_{FB} / V_{OUT}$. This command should match the actual value of the feedback resistor divider, regardless of whether it is an external or internal feedback resistor divider.

| Command | VOUT_SCALE_LOOP | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | X | | | | | | 0.001/LSB | | | | | | | | | |

The value is unsigned and 1LSB = 0.001. See the Default MTP Configuration section on page 47 for the default values.

## VOUT_MIN (2Bh)

The VOUT_MIN command sets a lower limit on the converter's $V_{OUT}$, regardless of any other commands or combinations. VOUT_MIN provides a safeguard against a user accidentally setting $V_{OUT}$ too low. It does not replace under-voltage protection (UVP).

| Command | VOUT_MIN | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | X | | | | 2mV/LSB | | | | | | | | | | | |

If an attempt is made to set $V_{OUT}$ below VOUT_MIN, the device takes the following actions:

1. The commanded $V_{OUT}$ is set to VOUT_MIN.

2. The VOUT bit is set in STATUS_WORD.

3. The VOUT_MAX_MIN warning bit is set in the STATUS_VOUT register.

4. The device notifies the host.

The minimum value for VOUT_MIN is 0.5V. See the Default MTP Configuration section on page 47 for the default values.

## VIN_ON (35h)

The VIN_ON command sets the $V_{IN}$ value at which the converter starts to run if all other required start-up conditions are met. VIN_ON should be always set above VIN_OFF with a sufficient margin so that there is no bouncing between VIN_ON and VIN_OFF during power conversion.

| Command | VIN_ON | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | X | | | | | | | | | | 250mV/LSB | | | | | |

The value is unsigned and 1LSB = 250mV. See the Default MTP Configuration section on page 47 for the default values.

## VIN_OFF (36h)

The VIN_OFF command sets the $V_{IN}$ value at which the converter turns off. VIN_OFF should be set below VIN_ON with a sufficient margin so that there is no bouncing between VIN_OFF and VIN_ON during power conversion.

| Command | VIN_OFF | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | X | | | | | | | | | | 250mV/LSB | | | | | |

The value is unsigned and 1LSB = 250mV. See the Default MTP Configuration section on page 47 for the default values.

## OT_FAULT_LIMIT (4Fh)

The OT_FAULT_LIMIT command configures (or reads) the threshold for over-temperature (OT) fault detection. If the measured temperature exceeds this value, an OT fault is triggered. The MPM82504 resumes normal operation after OTP based on OT_RESPONSE in register MFR_OT_OC_SET (D6h). OT fault flags are set in STATUS_BYTE (78h) and STATUS_WORD (79h), and the ALT# signal is asserted. After the measured temperature falls below the value in this register, the MOSFET may switch back on with the OPERATION command when the part works in latch-off mode. The minimum temperature fault detection time should be shorter than 20ms. The temperature range is between 0°C and 255°C.

If an OT fault occurs when the temperature exceeds this register value, the MPM82504 attempts to auto-retry once the temperature drops 20°C below this register value.

| Command | OT_FAULT_LIMIT | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | X | | | | | | | | 1°C/LSB | | | | | | | |

The value is unsigned and 1LSB = 1°C. See the Default MTP Configuration section on page 47 for the default values.

OT_FAULT_LIMIT should be set below 160°C. If OT_FAULT_LIMIT is set above 160°C, the register value is ignored and the MPM82504 enters thermal shutdown if the junction temperature reaches 160°C.

Table 8 shows the relationship between the direct values and real-world values.

**Table 8: Direct vs. Real-World OT Values**

| Direct Value | Real-World Value (°C) |
|---|---|
| 0000 0000 | 0 |
| 0000 0001 | 1 |
| 1111 1111 | 255 |

## OT_WARN_LIMIT (51h)

The OT_WARN_LIMIT command configures (or reads) the threshold for over-temperature (OT) warning detection. If the sensed temperature exceeds this value, an OT warning is triggered, the OT warning flags are set in STATUS_BYTE (78h) and STATUS_WORD (79h), and the ALT# signal is asserted. The minimum temperature warning detection time should be shorter than 20ms.

| Command | OT_ WARN_LIMIT | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | X | | | | | | | | 1°C/LSB | | | | | | | |

The value is unsigned and 1LSB = 1°C. See the Default MTP Configuration section on page 47 for the default values.

OT_WARN_LIMIT should be set below 160°C. The relationship between the direct value and real-word values are the same as OT_FAULT_LIMIT.

### VIN_OV_FAULT_LIMIT (55h)

The VIN_OV_FAULT_LIMIT command configures (or reads) the threshold for $V_{IN}$ over-voltage (OV) fault detection. If $V_{IN}$ exceeds the value in this register, then the $V_{IN}$ OV fault flags are set in their respective registers and the MPM82504 disables the power stage. If $V_{IN}$ drops below VIN_OV_FAULT_LIMIT, the MPM82504 resumes normal operation.

| Command | VIN_OV_FAULT_LIMIT | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | X | | | | | | | | | | 500mV/LSB | | | | | |

The value is unsigned and 1LSB = 500mV. See the Default MTP Configuration section on page 47 for the default values.

VIN_OV_FAULT_LIMIT should not be set above 18V.

### VIN_OV_WARN_LIMIT (57h)

The VIN_OV_WARN_LIMIT command configures (or reads) the threshold for $V_{IN}$ over-voltage (OV) warning detection. If $V_{IN}$ exceeds the value in this register, then $V_{IN}$ OV warning flags are set in the respective registers and the ALT# signal is asserted.

| Command | VIN_OV_ WARN_LIMIT | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | X | | | | | | | | | | 500mV/LSB | | | | | |

The value is unsigned and 1LSB = 500mV. See the Default MTP Configuration section on page 47 for the default values.

VIN_OV_WARN_LIMIT should not exceed 17V.

### VIN_UV_WARN_LIMIT (58h)

The VIN_UV_WARN_LIMIT command configures (or reads) the threshold for $V_{IN}$ under-voltage (UV) fault detection. If $V_{IN}$ falls below the value in this register, then the $V_{IN}$ UV warning flags are set in the respective registers and the ALT# signal is asserted.

| Command | VIN_UV_ WARN_LIMIT | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | X | | | | | | | | | | 250mV/LSB | | | | | |

The value is unsigned and 1LSB = 250mV. See the Default MTP Configuration section on page 47 for the default values.

### TON_DELAY (60h)

The TON_DELAY command sets the time (in ms) from when a start condition is received (as configured by the ON_OFF_CONFIG command) until $V_{OUT}$ starts to rise.

| Command | TON_DELAY | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | X | | | | | | | | 4ms/LSB | | | | | | | |

The value is unsigned and 1LSB = 4ms. The maximum value is FFh (1020ms). See the Default MTP Configuration section on page 47 for the default values.

## TON_RISE (61h)

The TON_RISE command sets the soft-start time (in ms) from when $V_{OUT}$ starts to rise until the voltage has reached the regulation point.

| Command | TON_DELAY | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|---|---|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | X | | | | | | | | | | | | | 1ms/LSB | | |

The only supported values are listed below:

- 3'b000: 1ms
- 3'b001: 2ms
- 3'b010: 4ms
- 3'b011: 8ms
- 3'b100 and up: 16ms

See the Default MTP Configuration section on page 47 for the default values.

## TOFF_DELAY (64h)

The TOFF_DELAY command sets the time (in ms) from EN turning off to when $V_{OUT}$ starts to fall.

| Command | TOFF_DELAY | | | | | | | | | | | | | | | |
|---------|----|----|----|----|----|----|---|---|-----|-----|-----|-----|-----|-----|-----|-----|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | X | | | | | | | | 4ms/LSB | | | | | | | |

The value is unsigned and 1LSB = 4ms. The maximum value is FFh (1020ms). See the Default MTP Configuration section on page 47 for the default values.

## STATUS_BYTE (78h)

The STATUS_BYTE command returns the value of a number of flags indicating the state of the MPM82504. Access to this command uses the read byte protocol. To clear the bits in this register, the underlying fault must be removed and a CLEAR_FAULTS command must be issued.

| Bits | Name | Behavior | Description |
|------|------|----------|-------------|
| 7 | RESERVED | N/A | Always reads as 0. |
| 6 | OFF | Live | 0: The device is enabled<br>1: The device is disabled. This may be due to a $V_{IN}$ under-voltage (UV) or over-voltage fault (OV), or from receiving an OPERATION off command |
| 5 | VOUT_OV | Latch | 0: No $V_{OUT}$ OV fault has occurred<br>1: A $V_{OUT}$ OV fault has occurred |
| 4 | IOUT_OC_FAULT | Latch | 0: No over-current (OC) fault has occurred<br>1: An OC fault has occurred |
| 3 | VIN_UV | N/A | Not supported, always reads as 0. |
| 2 | OT_FAULT_WARN | Latch | 0: No over-temperature (OT) warning or fault has occurred<br>1: An OT warning or fault has occurred |

| 1 | COMM_ERROR | Latch | 0: No communication error has occurred<br>1: A communication error has occurred |
| 0 | NONE_OF_THE_ ABOVE | Latch | 0: No other fault or warning has occurred<br>1: A fault or warning not listed in bits[7:1] has occurred |

## STATUS_WORD (79h)

The STATUS_WORD command returns the value of certain flags indicating the state of the MPM82504. To clear the bits in this register, the underlying fault must first be removed, then issue a CLEAR_FAULTS command.

| Bits | Name | Behavior | Description |
| --- | --- | --- | --- |
| 15 | VOUT_STATUS | Latch | 0: No $V_{OUT}$ fault or warning has occurred<br>1: A $V_{OUT}$ fault or warning has occurred |
| 14 | IOUT_STATUS | Latch | 0: No $I_{OUT}$ fault has occurred<br>1: An $I_{OUT}$ fault has occurred |
| 13 | VIN_STATUS | Latch | 0: No $V_{IN}$ fault has occurred<br>1: A $V_{IN}$ fault has occurred. When $V_{IN}$ starts up, the initial flag is set to 1 before $V_{IN}$ exceeds the under-voltage lockout (UVLO) threshold. This bit is cleared once $V_{IN}$ exceeds the threshold |
| 12 | MFR_STATUS | N/A | Always reads as 0. |
| 11 | POWER_GOOD# | Live | 0: A power good (PG) signal is asserted<br>1: A PG signal is not asserted |
| 10 | RESERVED | N/A | Always reads as 0. |
| 9 | RESERVED | N/A | Always reads as 0. |
| 8 | UNKNOWN | Latch | 0: No other fault has occurred<br>1: A fault type not specified in bits[15:1] has been detected. |
| Low Byte | STATUS_BYTE | N/A | See the description for STATUS_BYTE (78h) on page 38. |

## STATUS_VOUT (7Ah)

The STATUS_VOUT command returns 1 data byte with fault-related information.

| Bits | Name | Behavior | Description |
| --- | --- | --- | --- |
| 7 | VOUT_OV_FAULT | Latch | 0: No $V_{OUT}$ over-voltage (OV) fault has occurred<br>1: A $V_{OUT}$ OV fault has occurred |
| 6 | RESERVED | Latch | Always reads as 0. |
| 5 | RESERVED | Latch | Always reads as 0. |
| 4 | VOUT_UV_FAULT | Latch | 0: No $V_{OUT}$ under-voltage (UV) fault has occurred<br>1: A $V_{OUT}$ UV fault has occurred |
| 3 | VOUT_MAX_MIN | Latch | 0: No VOUT_MAX or VOUT_MIN warning has occurred<br>1: An attempt has been made to set $V_{OUT}$ to a value above VOUT_MAX or below VOUT_MIN |
| 2 | RESERVED | N/A | Always reads as 0. |
| 1 | RESERVED | N/A | Always reads as 0. |
| 0 | UNKNOWN | Latch | 0: No other fault has occurred<br>1: A fault type not specified in bits[7:1] has occurred |

## STATUS_IOUT (7Bh)

| Command | STATUS_IOUT | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | IOUT_OC | IOUT_OC and VOUT_UV | IOUT_OC_WARNING | X | | | | |

## STATUS_INPUT (7Ch)

The STATUS_INPUT command returns the value of flags indicating the device's $V_{IN}$ status. To clear the bits in this register, the underlying fault or warning must first be removed, then issue a CLEAR_FAULTS command.

| Bits | Name | Behavior | Description |
|---|---|---|---|
| 7 | VIN_OV_FAULT | R/Latch | 0: No over-voltage (OV) condition has been detected on the OV pin<br>1: An OV condition has been detected on the OV pin |
| 6 | VIN_OV_WARN | R/Latch | 0: No over-voltage (OV) condition has been detected on the VIN pin<br>1: An OV condition has been detected on the VIN pin |
| 5 | VIN_UV_WARN | R/Latch | 0: No under-voltage (UV) condition has been detected on the VIN pin<br>1: An UV condition has been detected on the VIN pin |
| 4:0 | RESERVED | R | Always reads as 0000. |

## STATUS_TEMPERATURE (7Dh)

The STATUS_TEMPERATURE command returns the value of flags indicating an over-temperature (OT) fault or warning. To clear the bits in this register, the underlying fault should be removed, and a CLEAR_FAULTS command must be issued.

| Bits | Name | Behavior | Description |
|---|---|---|---|
| 7 | OT_FAULT | R/Latch | 0: No over-temperature (OT) fault has occurred<br>1: An OT fault has occurred |
| 6 | OT_WARNING | R/Latch | 0: No over-temperature (OT) warning has occurred<br>1: An OT warning has occurred |
| 5:0 | RESERVED | R | Always reads as 0. |

## STATUS_CML (7Eh)

| Command | STATUS_CML | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Function | Invalid or unsupported command | Invalid or unsupported data | X | Memory fault detected | X | X | Other fault | Memory busy |

## READ_VIN (88h)

The READ_VIN command returns the 10-bit measured $V_{IN}$ value.

| Command | READ_VIN | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | X | | | | | | 25mV/LSB | | | | | | | | | |

### READ_VOUT (8Bh)

The READ_VOUT command returns the 13-bit measured $V_{OUT}$ value.

| Command | READ_VOUT | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | X | | | 1.25mV/LSB | | | | | | | | | | | | |

### READ_IOUT (8Ch)

The READ_IOUT command returns the 14-bit measured $I_{OUT}$ value. This value is also compared to IOUT_OC_FAULT_LIMIT and IOUT_OC_WARN_LIMIT, and affects STATUS_IOUT.

| Command | READ_IOUT | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Direct | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R | R |
| Function | X | | 62.5mA/LSB | | | | | | | | | | | | | |

### READ_TEMPERATURE_1 (8Dh)

The READ_TEMPERATURE_1 command returns the internal sensed temperature. This value is also used internally for over-temperature (OT) fault and warning detection. This value ranges between 40°C and 215°C.

| Command | READ_TEMPERATURE_1 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Format | Two's complement integer | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | X | | | | | | | 1°C/LSB | | | | | | | | |

READ_TEMPERATURE_1 is a 2-byte, two's complement integer. Bit[9] is the signed bit.

Table 9 shows the relationship between the direct values and real-world values.

**Table 9: Direct vs. Real-World Values**

| Sign | Direct Value | Real-World Value (°C) |
|---|---|---|
| 0 | 0 0000 0000 | 0 |
| 0 | 0 0000 0001 | +1 |
| 0 | 1 1111 1111 | +511 |
| 1 | 0 0000 0001 | -511 |
| 1 | 1 1111 1111 | -1 |

### PMBUS_REVISION (98h)

The PMBUS_REVISION command returns the PMBus protocol revision to which the device is compliant. Access to this command uses the read byte protocol. Bits[7:4] indicate the PMBus revision of specification Part I to which the device is compliant. Bits[3:0] indicate the revision of specification Part II to which the device is compliant.

| Command | PMBUS_REVISION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Format | Unsigned binary | | | | | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R | R | R | R | R | R | R | R |

Bits[7:4] always reads as 4'b0011 to indicate PMBus specification Part I, Revision 1.3.

Bits[3:0] always reads as 4'b0011 to indicate PMBus specification Part II, Revision 1.3.

## MFR_CTRL_COMP (D0h)

The MFR_CTRL_COMP command adjusts loop compensation.

| Bits | Name | Access | Behavior | Description |
|------|------|--------|----------|-------------|
| 7:5 | RESERVED | R/W | Live | Reserved. |
| 4 | CFF | R/W | Live | Sets the feed-forward capacitance ($C_{FF}$) when an internal feedback resistor divider is selected.<br><br>0: 20pF<br>1: 50pF |
| 3:1 | RAMP | R/W | Live | Sets the internal ramp compensation to stabilize the loop. The actual ramp amplitude is related to the selection from register EAh, bit[3]. See the table below for more details.<br><br><table><tr><td>EAh, Bit[3] = 0 (Single-Phase)</td><td>EAh, Bit[3] = 1 (Multi-Phase)</td></tr><tr><td>000: 5.6mV RAMP</td><td>000: 8.6mV RAMP</td></tr><tr><td>001: 9.8mV RAMP</td><td>001: 15mV RAMP</td></tr><tr><td>010: 18mV RAMP</td><td>010: 27mV RAMP</td></tr><tr><td>011: 30mV RAMP</td><td>011: 45mV RAMP</td></tr><tr><td>100: 8.5mV RAMP</td><td>100: 13mV RAMP</td></tr><tr><td>101: 15.1mV RAMP</td><td>101: 23mV RAMP</td></tr><tr><td>110: 27mV RAMP</td><td>110: 41mV RAMP</td></tr><tr><td>111: 44mV RAMP</td><td>111: 68mV RAMP</td></tr></table> |
| 0 | SLAVE_ FAULT_ DETECTION | R/W | Live | Enables the slave fault detection function through the PG pin.<br><br>0: Slave-phase fault detection is enabled<br>1: Slave-phase fault detection is disabled |

See the Default MTP Configuration section on page 47 for the default values.

## MFR_CTRL_VOUT (D1h)

The MFR_CTRL_VOUT command adjusts the MPM82504's $V_{OUT}$ behaviors.

| Bits | Name | Access | Behavior | Description |
|------|------|--------|----------|-------------|
| 7 | RESERVED | R/W | Live | Reserved. |
| 6 | VO_ DISCHARGE | R/W | Live | Enables active $V_{OUT}$ discharging when the MPM82504 is commanded to turn off through CTRL or an OPERATION off command.<br><br>1: $V_{OUT}$ discharges at CTRL low<br>0: No active $V_{OUT}$ discharging |
| 5:2 | PG_DELAY | R/W | Live | Set the PG pull-high time after soft-start finishes.<br><br>0000: 2ms<br>0001: 3ms<br>…………..<br>1110: 16ms<br>1111: 1ms |
| 1:0 | VO_RANGE | R/W | Live | Chooses the voltage divider radio.<br><br>00: External voltage divider<br>01: Internal voltage divider: $V_{REF}$ / $V_{OUT}$ = 0.4V to 1.344V<br>10: Internal voltage divider: $V_{REF}$ / $V_{OUT}$ = 0.7V to 2.688V<br>11: Internal voltage divider: $V_{REF}$ / $V_{OUT}$ = 1.3V to 5.376V |

See the Default MTP Configuration section on page 47 for the default values.

## MFR_CTRL_OPS (D2h)

The MFR_CTRL_OPS command sets the switching frequency ($f_{SW}$) and light-load operation mode.

| Bits | Name | Access | Behavior | Description |
|------|------|--------|----------|-------------|
| 7:3 | RESERVED | N/A | N/A | Reserved, |
| 2:1 | SWITCHING_ FREQUENCY | R/W | Live | 00: Set $f_{SW}$ to 400kHz<br>01: Set $f_{SW}$ to 600kHz<br>10: Set $f_{SW}$ to 800kHz<br>11: Set $f_{SW}$ to 1000kHz |
| 0 | SKIP_CCM(SYNC) | R/W | Live | 0: Pulse-skip mode at light loads<br>1: Forced continuous conduction mode (FCCM) at light loads |

See the Default MTP Configuration section on page 47 for the default values.

## MFR_ADDR_PMBUS (D3h)

| Command | MFR_ADDR_PMBUS | | | | | | | |
|---------|------|------|------|------|------|------|------|------|
| Format | Direct | | | | | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Access | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Function | ENABLE | ADDR | | | | | | |

| Bits | Name | Description |
|------|------|-------------|
| 7 | ENABLE | 1: The address is determined by bits[6:0] of this command<br>0: The address is determined by the ADDR pin |
| 6:0 | ADDR | Determines the PMBus address if bit[7] of this command is set to 1. |

See the Default MTP Configuration section on page 47 for the default values.

## MFR_VOUT_FAULT_LIMIT (D4h)

The MFR_VOUT_FAULT_LIMIT command sets the thresholds for over-voltage protection (OVP).

| Bits | Name | Access | Behavior | Description |
|------|------|--------|----------|-------------|
| 7:4 | RESERVED | N/A | N/A | Reserved. |
| 3:2 | OV_EXIT_TH | R/W | Live | 00: 10% of $V_{REF}$<br>01: 50% of $V_{REF}$<br>10: 80% of $V_{REF}$<br>11: 102.5% of $V_{REF}$ |
| 1:0 | OV_ENTER_TH | R/W | Live | 00: 115% of $V_{REF}$<br>01: 120% of $V_{REF}$<br>10: 125% of $V_{REF}$<br>11: 130% of $V_{REF}$ |

All OVP thresholds are relative to the reference voltage.

See the Default MTP Configuration section on page 47 for the default values.

## MFR_OVP_NOCP_SET (D5h)

The MFR_OVP_NOCP_SET command sets the $V_{OUT}$ over-voltage protection (OVP) responses and the delay time of negative over-current protection (NOCP).

| Bits | Name | Access | Behavior | Description |
|------|------|--------|----------|-------------|
| 7:4 | RESERVED | N/A | N/A | Reserved. |
| 3 | DELAY_NOCP | R/W | Live | 0: 100ns delay after NOCP<br>1: 200ns delay after NOCP |
| 2 | RESERVED | N/A | N/A | Reserved. |
| 1:0 | VOUT_OV_ RESPONSE | R/W | Live | 00: Latch-off mode with $V_{OUT}$ discharging<br>01: Latch-off mode without $V_{OUT}$ discharging in DCM<br>10: Hiccup mode with $V_{OUT}$ discharging<br>11: Hiccup mode without $V_{OUT}$ discharging in DCM |

Bits[1:0] (VOUT_OV_RESPONSE) tell the converter how to respond to a $V_{OUT}$ over-voltage (OV) fault. If an OV fault occurs, the device also does the following:

1. Sets the VOUT_OV bit in STATUS_BYTE.

2. Sets the VOUT bit in STATUS_WORD.

3. Sets the VOUT_OV fault bit in STATUS_VOUT.

4. Notifies the host by asserting the ALERT pin.

The four OV responses are described in greater detail below.

- Latch-off mode with $V_{OUT}$ discharging: If the device reaches the over-voltage (OV) threshold, the LS-FET turns on until it reaches NOCP. Then the LS-FET turns off for a fixed time before turning on again. This process resumes until $V_{FB}$ drops below the OVP exit threshold set by register D4, bits[3:2]. Then the LS-FET turns off. If $V_{FB}$ exceeds the OV entry threshold again, then the LS-FET turns on again to discharge $V_{OUT}$. The converter does not attempt to restart until power is cycled on VIN, VCC, or CTRL.

- Latch-off mode without $V_{OUT}$ discharging (only effective in DCM): If the device reaches the OV entry threshold, the LS-FET turns on. When the inductor current reaches 0A, the converter enters Hi-Z mode (output disabled). The converter stops discharging $V_{OUT}$. The converter does not attempt to restart until power is cycled on VIN, VCC, or CTRL.

- Hiccup mode with $V_{OUT}$ discharging: If the device reaches the OV entry threshold, the LS-FET turns on until the device reaches NOCP. Then the LS-FET turns off for a fixed time before turning on again. This process continues until $V_{FB}$ drops below the OVP exit threshold set by register D4h, bits[3:2]. Then the LS-FET turns off, and a new soft start is initiated.

- Hiccup mode without $V_{OUT}$ discharging: If the device reaches the OV entry threshold, the LS-FET turns on until the device reaches NOCP. Then a new soft start is initiated.

See the Default MTP Configuration section on page 47 for the default values.

## MFR_OT_OC_SET (D6h)

The MFR_OT_OC_SET command sets the over-current protection (OCP) response and the over-temperature protection (OTP) hysteresis. It is a 1-byte command.

| Bits | Name | Access | Description |
|------|------|--------|-------------|
| 7:4 | RESERVED | N/A | Reserved. |

| 3 | OC_RESPONSE | R/W | 0: Latch-off mode<br>1: Retry mode |
|---|---|---|---|
| 2:1 | OT_HYST | R/W | 00: 20°C<br>01: 25°C<br>10: 30°C<br>11: 35°C |
| 0 | OT_RESPONSE | R/W | 0: Latch-off mode<br>1: Retry after the temperature drops by the value set by bits[2:1] of this command |

See the Default MTP Configuration section on page 47 for the default values.

## MFR_OC_PHASE_SET (D7h)

The MFR_OC_PHASE_SET command sets the inductor valley current limit for each individual phase. This is a cycle-by-cycle current limit. After 31 consecutive over-current (OC) cycles, OCP is triggered. This is a 1-byte command.

| Bits | Name | Access | Behavior | Description |
|---|---|---|---|---|
| 7:5 | RESERVED | N/A | N/A | Reserved. |
| 4:0 | OC_LIMIT | R/W | Live | Current limit. 1.5A/LSB. |

The value is unsigned and 1LSB = 1.5A. See the Default MTP Configuration section on page 47 for the default values.

## MFR_PGOOD_ON_OFF_LIMIT (D9h)

The MFR_PGOOD_ON_OFF_LIMIT command sets the PGOOD on and off thresholds.

| Bits | Name | Access | Behavior | Description |
|---|---|---|---|---|
| 7:4 | RESERVED | N/A | N/A | Reserved. |
| 3:2 | PG_OFF | R/W | Live | 00: 69% of $V_{REF}$<br>01: 74% of $V_{REF}$<br>10: 79% of $V_{REF}$<br>11: 84% of $V_{REF}$ |
| 1:0 | PG_ON | R/W | Live | 00: 90% of $V_{REF}$<br>01: 92.5% of $V_{REF}$<br>10: 95% of $V_{REF}$<br>11: 97.5% of $V_{REF}$ |

PG_OFF also sets the under-voltage protection (UVP) threshold. When $V_{FB}$ drops below the PG_OFF level, the MPM82504 triggers UVP. The device responds to UVP the same way it responds to over-current protection (OCP). See the Default MTP Configuration section on page 47 for the default values.

Any fault condition pulls PG low.

## MFR_VOUT_STEP (DAh)

The MFR_VOUT_STEP command sets the $V_{OUT}$ transition slew rate after soft start finishes. It does not determine the $V_{OUT}$ slew rate during soft start. See the Default MTP Configuration section on page 47 for the default values.

| Bits | Name | Access | Behavior | Description |
|---|---|---|---|---|
| 7:4 | RESERVED | N/A | N/A | Reserved. |
| 3:0 | VOUT_STEP | R/W | Live | 0000: 20µs/2mV<br><br>1LSB = 2.5µs/2mV. |

## MFR_LOW_POWER (E5h)

The MFR_LOW_POWER enables the slave phase(s) in multi-phase configuration.

| Bits | Name | Access | Behavior | Description |
|------|------|--------|----------|-------------|
| 7:2 | RESERVED | N/A | N/A | Reserved. |
| 1 | LP_PS# | R/W | Live | 0: Low-power mode is disabled regardless of the PS pin status<br>1: Low-power mode is enabled when PS is low, and is disabled when PS is high |
| 0 | LP_PMBUS | R/W | Live | 0: Low-power mode is disabled<br>1: Low-power mode is enabled |

The slave phase(s) can be enabled or disabled directly via bit[0] of the MFR_LOW_POWER command. When bit[1] set to 1, the slave phase(s) can be enabled or disabled by the PS pin.

The master phase cannot be disabled through this command.

See the Default MTP Configuration section on page 47 for the default values.

## MFR_CTRL (EAh)

The MFR_CTRL command enables certain functions.

| Bits | Name | Access | Behavior | Description |
|------|------|--------|----------|-------------|
| 15:11 | RESERVED | R | Live | For manufacturer use only. |
| 10 | RESERVED | R | Live | For manufacturer use only. |
| 9 | OSM | R/W | Live | Enables output sink mode (OSM).<br><br>0: Enable OSM<br>1: Disable OSM |
| 8:4 | RESERVED | R | Live | For manufacturer use only. |
| 3 | PHASE_ OPERATION | R/W | Live | Selects single-phase or multi-phase operation. This bit affects the actual RAMP amplitude selected through register D0h, bits[3:1]. See the MFR_CTRL_COMP (D0h) section on page 42 for more details.<br><br>0: For single-phase operation<br>1: For multi-phase operation |
| 2:0 | RESERVED | R | Live | For manufacturer use only. |

Only bit[9] (OSM) and bit[3] (PHASE_OPERATION) are user accessible for MFR_CTRL (EAh). All other bits are reserved for manufacturer use only.

See the Default MTP Configuration section on page 47 for the default values.

# DEFAULT MTP CONFIGURATION

**Table 8: 0000 Suffix Code Configuration**

| Items | Channel 1 | Channel 2 | Channel 3 | Channel 4 |
|---|---|---|---|---|
| V$_{OUT}$ set method | External divider | External divider | External divider | External divider |
| V$_{OUT}$ | 0.85V | 0.9V | 1.2V | 1.8V |
| V$_{FB}$ | 0.6V | 0.6V | 0.6V | 0.6V |
| Soft-start delay time | 4ms | 4ms | 4ms | 4ms |
| Parallel mode | Unparalleled | Unparalleled | Unparalleled | Unparalleled |
| Valley current limit | 25.5A | 25.5A | 25.5A | 25.5A |
| Light-load mode | FCCM | FCCM | FCCM | FCCM |
| f$_{SW}$ | 1000kHz | 1000kHz | 1000kHz | 1000kHz |
| RAMP | 27mV | 27mV | 27mV | 27mV |

**Table 9: 0000 Suffix Register Value**

| Suffix Code | Page | Register | Hex Value | Suffix Code | Page | Register | Hex Value |
|---|---|---|---|---|---|---|---|
| 0000 | 1 | 01 | 80 | 0000 | 2 | 01 | 80 |
| 0000 | 1 | 02 | 1E | 0000 | 2 | 02 | 1E |
| 0000 | 1 | 10 | 0 | 0000 | 2 | 10 | 0 |
| 0000 | 1 | 21 | 1A9 | 0000 | 2 | 21 | 1C2 |
| 0000 | 1 | 24 | BB8 | 0000 | 2 | 24 | BB8 |
| 0000 | 1 | 25 | 2A0 | 0000 | 2 | 25 | 2A0 |
| 0000 | 1 | 26 | 1FE | 0000 | 2 | 26 | 1FE |
| 0000 | 1 | 29 | 2C2 | 0000 | 2 | 29 | 29B |
| 0000 | 1 | 2b | FA | 0000 | 2 | 2b | FA |
| 0000 | 1 | 35 | 12 | 0000 | 2 | 35 | 12 |
| 0000 | 1 | 36 | B | 0000 | 2 | 36 | B |
| 0000 | 1 | 46 | FFB | 0000 | 2 | 46 | FFB |
| 0000 | 1 | 4A | FFB | 0000 | 2 | 4A | FFB |
| 0000 | 1 | 4F | A0 | 0000 | 2 | 4F | A0 |
| 0000 | 1 | 51 | 8C | 0000 | 2 | 51 | 8C |
| 0000 | 1 | 55 | 24 | 0000 | 2 | 55 | 24 |
| 0000 | 1 | 57 | 22 | 0000 | 2 | 57 | 22 |
| 0000 | 1 | 58 | 1 | 0000 | 2 | 58 | 1 |
| 0000 | 1 | 60 | 0 | 0000 | 2 | 60 | 0 |
| 0000 | 1 | 61 | 2 | 0000 | 2 | 61 | 2 |
| 0000 | 1 | 64 | 0 | 0000 | 2 | 64 | 0 |
| 0000 | 1 | 9B | 36 | 0000 | 2 | 9B | 36 |
| 0000 | 1 | D0 | F | 0000 | 2 | D0 | F |
| 0000 | 1 | D1 | 0 | 0000 | 2 | D1 | 0 |
| 0000 | 1 | D2 | 7 | 0000 | 2 | D2 | 7 |
| 0000 | 1 | D3 | 30 | 0000 | 2 | D3 | 30 |
| 0000 | 1 | D4 | 3 | 0000 | 2 | D4 | 3 |
| 0000 | 1 | D5 | 2 | 0000 | 2 | D5 | 2 |
| 0000 | 1 | D6 | 9 | 0000 | 2 | D6 | 9 |
| 0000 | 1 | D7 | 11 | 0000 | 2 | D7 | 11 |
| 0000 | 1 | D9 | 0 | 0000 | 2 | D9 | 0 |
| 0000 | 1 | DA | 4 | 0000 | 2 | DA | 4 |
| 0000 | 1 | E5 | 0 | 0000 | 2 | E5 | 0 |

| 0000 | 1 | EA | 0 | 0000 | 2 | EA | 0 |
|------|---|-----|-----|------|---|-----|-----|
| 0000 | 1 | EC | 72 | 0000 | 2 | EC | 72 |
| 0000 | 3 | 01 | 80 | 0000 | 4 | 01 | 80 |
| 0000 | 3 | 02 | 1E | 0000 | 4 | 02 | 1E |
| 0000 | 3 | 10 | 0 | 0000 | 4 | 10 | 0 |
| 0000 | 3 | 21 | 258 | 0000 | 4 | 21 | 384 |
| 0000 | 3 | 24 | BB8 | 0000 | 4 | 24 | BB8 |
| 0000 | 3 | 25 | 2A0 | 0000 | 4 | 25 | 2A0 |
| 0000 | 3 | 26 | 1FE | 0000 | 4 | 26 | 1FE |
| 0000 | 3 | 29 | 1F4 | 0000 | 4 | 29 | 14D |
| 0000 | 3 | 2b | FA | 0000 | 4 | 2b | FA |
| 0000 | 3 | 35 | 12 | 0000 | 4 | 35 | 12 |
| 0000 | 3 | 36 | B | 0000 | 4 | 36 | B |
| 0000 | 3 | 46 | FFB | 0000 | 4 | 46 | FFB |
| 0000 | 3 | 4A | FFB | 0000 | 4 | 4A | FFB |
| 0000 | 3 | 4F | A0 | 0000 | 4 | 4F | A0 |
| 0000 | 3 | 51 | 8C | 0000 | 4 | 51 | 8C |
| 0000 | 3 | 55 | 24 | 0000 | 4 | 55 | 24 |
| 0000 | 3 | 57 | 22 | 0000 | 4 | 57 | 22 |
| 0000 | 3 | 58 | 1 | 0000 | 4 | 58 | 1 |
| 0000 | 3 | 60 | 0 | 0000 | 4 | 60 | 0 |
| 0000 | 3 | 61 | 2 | 0000 | 4 | 61 | 2 |
| 0000 | 3 | 64 | 0 | 0000 | 4 | 64 | 0 |
| 0000 | 3 | 9B | 36 | 0000 | 4 | 9B | 36 |
| 0000 | 3 | D0 | F | 0000 | 4 | D0 | F |
| 0000 | 3 | D1 | 0 | 0000 | 4 | D1 | 0 |
| 0000 | 3 | D2 | 7 | 0000 | 4 | D2 | 7 |
| 0000 | 3 | D3 | 30 | 0000 | 4 | D3 | 30 |
| 0000 | 3 | D4 | 3 | 0000 | 4 | D4 | 3 |
| 0000 | 3 | D5 | 2 | 0000 | 4 | D5 | 2 |
| 0000 | 3 | D6 | 9 | 0000 | 4 | D6 | 9 |
| 0000 | 3 | D7 | 11 | 0000 | 4 | D7 | 11 |
| 0000 | 3 | D9 | 0 | 0000 | 4 | D9 | 0 |
| 0000 | 3 | DA | 4 | 0000 | 4 | DA | 4 |
| 0000 | 3 | E5 | 0 | 0000 | 4 | E5 | 0 |
| 0000 | 3 | EA | 0 | 0000 | 4 | EA | 0 |
| 0000 | 3 | EC | 72 | 0000 | 4 | EC | 72 |

**Table 10: 0001 Suffix Code Configuration**

| Items | Channel 1 | Channel 2 | Channel 3 | Channel 4 |
|---|---|---|---|---|
| V$_{OUT}$ set method | External divider | External divider | External divider | External divider |
| V$_{OUT}$ | 0.85V | 0.85V | 1.2V | 1.2V |
| V$_{FB}$ | 0.6V | 0.6V | 0.6V | 0.6V |
| Soft-start delay time | 4ms | 4ms | 4ms | 4ms |
| Parallel mode | Paralleled | | Paralleled | |
| Valley current limit | 25.5A | 25.5A | 25.5A | 25.5A |
| Light-load mode | FCCM | FCCM | FCCM | FCCM |
| f$_{SW}$ | 1000kHz | 1000kHz | 1000kHz | 1000kHz |
| RAMP | 68mV | 68mV | 68mV | 68mV |

**Table 11: 0001 Suffix Register Value**

| Suffix Code | Page | Register | Hex Value | Suffix Code | Page | Register | Hex Value |
|---|---|---|---|---|---|---|---|
| 0001 | 1 | 01 | 80 | 0001 | 2 | 01 | 80 |
| 0001 | 1 | 02 | 1E | 0001 | 2 | 02 | 1E |
| 0001 | 1 | 10 | 0 | 0001 | 2 | 10 | 0 |
| 0001 | 1 | 21 | 1A9 | 0001 | 2 | 21 | 1A9 |
| 0001 | 1 | 24 | BB8 | 0001 | 2 | 24 | BB8 |
| 0001 | 1 | 25 | 2A0 | 0001 | 2 | 25 | 2A0 |
| 0001 | 1 | 26 | 1FE | 0001 | 2 | 26 | 1FE |
| 0001 | 1 | 29 | 2C2 | 0001 | 2 | 29 | 2C2 |
| 0001 | 1 | 2b | FA | 0001 | 2 | 2b | FA |
| 0001 | 1 | 35 | 12 | 0001 | 2 | 35 | 12 |
| 0001 | 1 | 36 | B | 0001 | 2 | 36 | B |
| 0001 | 1 | 46 | FFB | 0001 | 2 | 46 | FFB |
| 0001 | 1 | 4A | FFB | 0001 | 2 | 4A | FFB |
| 0001 | 1 | 4F | A0 | 0001 | 2 | 4F | A0 |
| 0001 | 1 | 51 | 8C | 0001 | 2 | 51 | 8C |
| 0001 | 1 | 55 | 24 | 0001 | 2 | 55 | 24 |
| 0001 | 1 | 57 | 22 | 0001 | 2 | 57 | 22 |
| 0001 | 1 | 58 | 1 | 0001 | 2 | 58 | 1 |
| 0001 | 1 | 60 | 0 | 0001 | 2 | 60 | 0 |
| 0001 | 1 | 61 | 2 | 0001 | 2 | 61 | 2 |
| 0001 | 1 | 64 | 0 | 0001 | 2 | 64 | 0 |
| 0001 | 1 | 9B | 36 | 0001 | 2 | 9B | 36 |
| 0001 | 1 | D0 | F | 0001 | 2 | D0 | F |
| 0001 | 1 | D1 | 0 | 0001 | 2 | D1 | 0 |
| 0001 | 1 | D2 | 7 | 0001 | 2 | D2 | 7 |
| 0001 | 1 | D3 | 30 | 0001 | 2 | D3 | 30 |
| 0001 | 1 | D4 | 3 | 0001 | 2 | D4 | 3 |
| 0001 | 1 | D5 | 2 | 0001 | 2 | D5 | 2 |
| 0001 | 1 | D6 | 9 | 0001 | 2 | D6 | 9 |
| 0001 | 1 | D7 | 11 | 0001 | 2 | D7 | 11 |
| 0001 | 1 | D9 | 0 | 0001 | 2 | D9 | 0 |
| 0001 | 1 | DA | 4 | 0001 | 2 | DA | 4 |
| 0001 | 1 | E5 | 0 | 0001 | 2 | E5 | 0 |
| 0001 | 1 | EA | 8 | 0001 | 2 | EA | 8 |

| 0001 | 1 | EC | 72 | 0001 | 2 | EC | 72 |
|------|---|----|----|------|---|----|----|
| 0001 | 3 | 01 | 80 | 0001 | 4 | 01 | 80 |
| 0001 | 3 | 02 | 1E | 0001 | 4 | 02 | 1E |
| 0001 | 3 | 10 | 0 | 0001 | 4 | 10 | 0 |
| 0001 | 3 | 21 | 258 | 0001 | 4 | 21 | 258 |
| 0001 | 3 | 24 | BB8 | 0001 | 4 | 24 | BB8 |
| 0001 | 3 | 25 | 2A0 | 0001 | 4 | 25 | 2A0 |
| 0001 | 3 | 26 | 1FE | 0001 | 4 | 26 | 1FE |
| 0001 | 3 | 29 | 1F4 | 0001 | 4 | 29 | 1F4 |
| 0001 | 3 | 2b | FA | 0001 | 4 | 2b | FA |
| 0001 | 3 | 35 | 12 | 0001 | 4 | 35 | 12 |
| 0001 | 3 | 36 | B | 0001 | 4 | 36 | B |
| 0001 | 3 | 46 | FFB | 0001 | 4 | 46 | FFB |
| 0001 | 3 | 4A | FFB | 0001 | 4 | 4A | FFB |
| 0001 | 3 | 4F | A0 | 0001 | 4 | 4F | A0 |
| 0001 | 3 | 51 | 8C | 0001 | 4 | 51 | 8C |
| 0001 | 3 | 55 | 24 | 0001 | 4 | 55 | 24 |
| 0001 | 3 | 57 | 22 | 0001 | 4 | 57 | 22 |
| 0001 | 3 | 58 | 1 | 0001 | 4 | 58 | 1 |
| 0001 | 3 | 60 | 0 | 0001 | 4 | 60 | 0 |
| 0001 | 3 | 61 | 2 | 0001 | 4 | 61 | 2 |
| 0001 | 3 | 64 | 0 | 0001 | 4 | 64 | 0 |
| 0001 | 3 | 9B | 36 | 0001 | 4 | 9B | 36 |
| 0001 | 3 | D0 | F | 0001 | 4 | D0 | F |
| 0001 | 3 | D1 | 0 | 0001 | 4 | D1 | 0 |
| 0001 | 3 | D2 | 7 | 0001 | 4 | D2 | 7 |
| 0001 | 3 | D3 | 30 | 0001 | 4 | D3 | 30 |
| 0001 | 3 | D4 | 3 | 0001 | 4 | D4 | 3 |
| 0001 | 3 | D5 | 2 | 0001 | 4 | D5 | 2 |
| 0001 | 3 | D6 | 9 | 0001 | 4 | D6 | 9 |
| 0001 | 3 | D7 | 11 | 0001 | 4 | D7 | 11 |
| 0001 | 3 | D9 | 0 | 0001 | 4 | D9 | 0 |
| 0001 | 3 | DA | 4 | 0001 | 4 | DA | 4 |
| 0001 | 3 | E5 | 0 | 0001 | 4 | E5 | 0 |
| 0001 | 3 | EA | 8 | 0001 | 4 | EA | 8 |
| 0001 | 3 | EC | 72 | 0001 | 4 | EC | 72 |

# APPLICATION INFORMATION

### Operation Mode Selection

The MPM82504 provides both forced continuous conduction mode (FCCM) and pulse-skip mode (PSM) under light-load conditions. Four switching frequencies are available under light-load conditions. Set the switching frequency (fSW) through the PMBus.

### Setting the Output Voltage

Two feedback resistors are required to set the proper feedback gain. The feedback resistor values ($R_1$ and $R_2$) can be calculated with Equation (1):

$$R_2(k\Omega) = \frac{0.6}{V_{OUT}-0.6} \times R_1(k\Omega) \quad (1)$$

Where $V_{OUT}$ is the output voltage.

The $V_{OUT}$ feedback gain ($G_{FB}$) can be estimated with Equation (2):

$$G_{FB} = \frac{R_2}{R_1+R_2} \quad (2)$$

To optimize the load transient response, a feed-forward capacitor ($C_{FF}$) must be placed in parallel with R1. Table 5 on page 24 lists the values of feedback resistors and feed-forward capacitors for common output voltages.

The MPM82504 offers $V_{OUT}$ configurability through the PMBus. In addition, $V_{OUT}$ can be adjusted through the PMBus by adjusting the internal reference voltage ($V_{REF}$) of the PWM controller.

The reference voltage (typically 0.6V by default) can be adjusted to be between 0.5V and 0.672V. For a given feedback resistor network, the maximum output voltage ($V_{OUT\_MAX}$) can be calculated with Equation (3):

$$V_{OUT\_MAX} = \frac{0.672}{G_{FB}} \quad (3)$$

The minimum output voltage ($V_{OUT\_MIN}$) can be estimated with Equation (4):

$$V_{OUT\_MIN} = \frac{0.5}{G_{FB}} \quad (4)$$

Follow the steps below to configure the output voltage through the PMBus:

1. Calculate $G_{FB}$ with Equation (2), then write this value to the register VOUT_SCALE_LOOP.

2. Write the $V_{OUT}$ settings to the register VOUT_COMMAND.

3. $V_{REF}$ is automatically updated based on the commanded $V_{OUT}$ and $G_{FB}$.

$V_{OUT}$ monitoring through the PMBus is enabled by setting VOUT_SCALE_LOOP to a value that matches $G_{FB}$.

For applications where the PMBus interface is not required, $V_{REF}$ is 0.6V by default, and the MPM82504 operates in analog mode. Calculate the feedback resistor values with Equation (1).

### Soft Start (SS)

The soft-start time ($t_{SS}$) can be configured in register 61h. The minimum $t_{SS}$ is 1ms, but it can also be set to 2ms, 4ms, 8ms, or 16ms.

### Pre-Biased Start-Up

The MPM82504 is designed for monotonic start-up into pre-biased loads. If $V_{OUT}$ is pre-biased to a certain voltage during start-up, both the HS-FET and LS-FET are disabled until the internal $V_{REF}$ exceeds the sensed $V_{OUT}$ at the FB pin.

### Output Voltage Discharge

$V_{OUT}$ discharge mode is enabled if the MPM82504 is disabled through the CTRL pin. In this scenario, both the HS-FET and LS-FET are latched off. A discharge FET connected between SW and GND turns on to discharge the output capacitor. The typical on resistance for the discharge FET is 60Ω. Once the $V_{FB}$ drops below 10% of $V_{REF}$, the discharge FET turns off.

### Current Sense and Over-Current Protection (OCP)

The MPM82504 features on-die current sensing and a configurable inductor valley current limit threshold. The inductor valley over-current limit can be configured through register D7h, which sets the per-phase inductor valley current limit for both single and multi-phase operation.

While the LS-FET is on, the inductor current is sensed and monitored cycle by cycle. The HS-FET does not turn on if an over-current (OC) condition is detected while the LS-FET is on. Therefore, the inductor current is also limited cycle by cycle. If an OC condition remains for 31 consecutive cycles, OCP is triggered.

If $V_{OUT}$ drops below the under-voltage protection (UVP) threshold, the MPM82504 enters OCP immediately.

Once OCP is triggered, MPM82504 either enters hiccup mode or latch-off mode, depending on the register setting. To re-enable the device, cycle the power on VCC or CTRL.

### Negative Inductor Current Limit

When the LS-FET detects a negative current below the limit (about -13A), the LS-FET turns off for a certain period to limit the negative current. This period is set by register D5h, bit[3].

### Under-Voltage Protection (UVP)

The MPM82504 monitors $V_{OUT}$ through the FB pin. UVP is triggered if $V_{FB}$ drops below the UVP threshold. Once UVP is triggered, the MPM82504 enters either hiccup mode or latch-off mode, depending on the register setting. To re-enable the device, cycle the power on VCC or CTRL.

### Over-Voltage Protection (OVP)

Over-voltage protection (OVP) is triggered if $V_{FB}$ exceeds the OVP threshold. See the MFR_VOUT_FAULT_LIMIT (D4h) section on page 43 for more details.

### Output Sinking Mode (OSM)

The MPM82504 enters output sinking mode (OSM) if $V_{OUT}$ exceeds $V_{REF}$ by 5% while simultaneously being below the OVP threshold in PSM. Once OSM is triggered, the MPM82504 runs in FCCM. The device exits OSM once the HS-FET turns back on.

### Over-Temperature Protection (OTP)

The MPM82504 monitors the junction temperature. If over-temperature protection (OTP) is triggered, the device enters either hiccup or latch-off mode, depending on the PMBus selection. To re-enable the device, cycle the power on VCC or CTRL.

### Power Good (PG)

The MPM82504 has an open-drain power good (PG) output. The PG pin must be pulled high to VCC (or a voltage source below 3.6V) through a pull-up resistor (typically 100kΩ). PG is initially pulled low once $V_{IN}$ is applied to the MPM82504. After $V_{FB}$ reaches the threshold set by POWER_GOOD_ON and the delay set by MFR_CTRL_VOUT completes, the PG pin is pulled high.

PG latches low if any fault occurs and a protection is triggered (e.g. UV, OV, OT, UVLO). After PG latches off, it cannot be pulled high again unless a new soft start is initiated.

After PG is pulled high, if below conditions are satisfied, the PG pin is immediate to be pulled low.

1.  The input supply is lower than the threshold set by VIN_OFF;

2.  The input supply fails to power the MPM82504;

3.  EN is pulled low.

### Selecting the Input Capacitor

The buck converter has a discontinuous input current, and requires a capacitor to supply AC current to the step-down module while maintaining the DC input voltage. Use ceramic capacitors for the best performance. When designing the layout, place the input capacitors as close to the VIN pin as possible.

The capacitance can vary significantly with temperature. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable across a wide temperature range.

The capacitors must also have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current with Equation (5):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \qquad (5)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (6):

$$I_{CIN} = \frac{I_{OUT}}{2} \qquad (6)$$

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current.

The input capacitance value determines the converter input voltage ripple. Select a capacitor value that meets any input voltage ripple requirements.

Estimate the input voltage ripple with Equation (7):

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, calculated with Equation (8):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{f_{SW} \times C_{IN}} \quad (8)$$

**Selecting the Output Capacitor**

The output capacitor maintains the DC output voltage. Use ceramic capacitors or POSCAP capacitors. Estimate the output voltage ripple with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times f_{SW} \times C_{OUT}}) \quad (9)$$

When using ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and causes the majority of the output voltage ripple. For simplification, estimate the output voltage ripple with Equation (10):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

The ESR contributes minimally to the output voltage ripple, so an external ramp must be implemented to stabilize the system. Design the external ramp using R4, C4, and the equations above.

When using POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ESR ramp voltage is high enough to stabilize the system, thus eliminating the need for an external ramp. Select a minimum ESR value (about 12mΩ) to ensure stable operation. For simplification, the output ripple can be calculated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (11)$$

## PCB Layout Guidelines

### VINx

Sufficient decoupling capacitors should be placed as close as possible to each set of VINx and GND pins. Sufficient GND vias should be placed around the GND pad of the decoupling capacitors. Avoid placing sensitive signal traces close to the input copper plane and/or vias without sufficient ground shielding. A minimum of two 22µF/25V ceramic capacitors are recommended for each input channel to provide sufficient decoupling.

### VOUTx

Each VOUTx pin should be connected together on a copper plane. Place sufficient vias near the VOUTx pads to provide a current path with minimal parasitic impedance. Combine the corresponding copper planes of the VOUTx pins to enable parallel operation.

### GND

Connect all GND pins of the module on a copper plane. Place sufficient vias close to the GND pins to provide a current return path with minimal thermal resistance and parasitic impedance.

### VOSNSx+ and VOSNSx-

Each pair of VOSNSx+/- pins should be routed as differential signals. In parallel operation, all VOSNSx+ pins of the master and slaves should be connected, and all VOSNSx- pins of the master and slaves should be connected. Avoid routing VOSNSx+/- traces close to the input plane and high-speed signals.

### SETx

In parallel operation, connect the corresponding SETx pins with a minimal trace distance. Avoid routing SETx traces close to the input plane and high-speed signals.

### ISUMx

In parallel operation, connect the corresponding ISUMx pins with a minimal trace distance. Avoid routing ISUMx traces close to the input plane and high-speed signals.
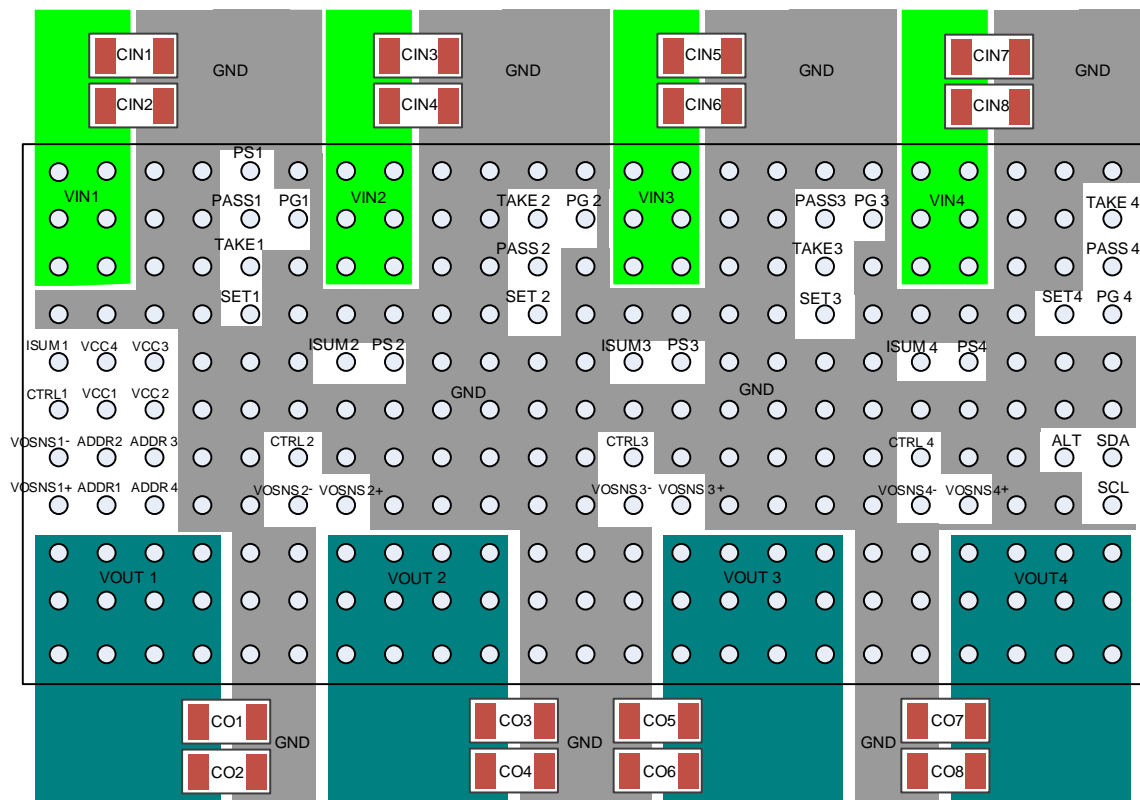


**Figure 8: Layout Example of Quad Output**

# TYPICAL APPLICATION CIRCUITS
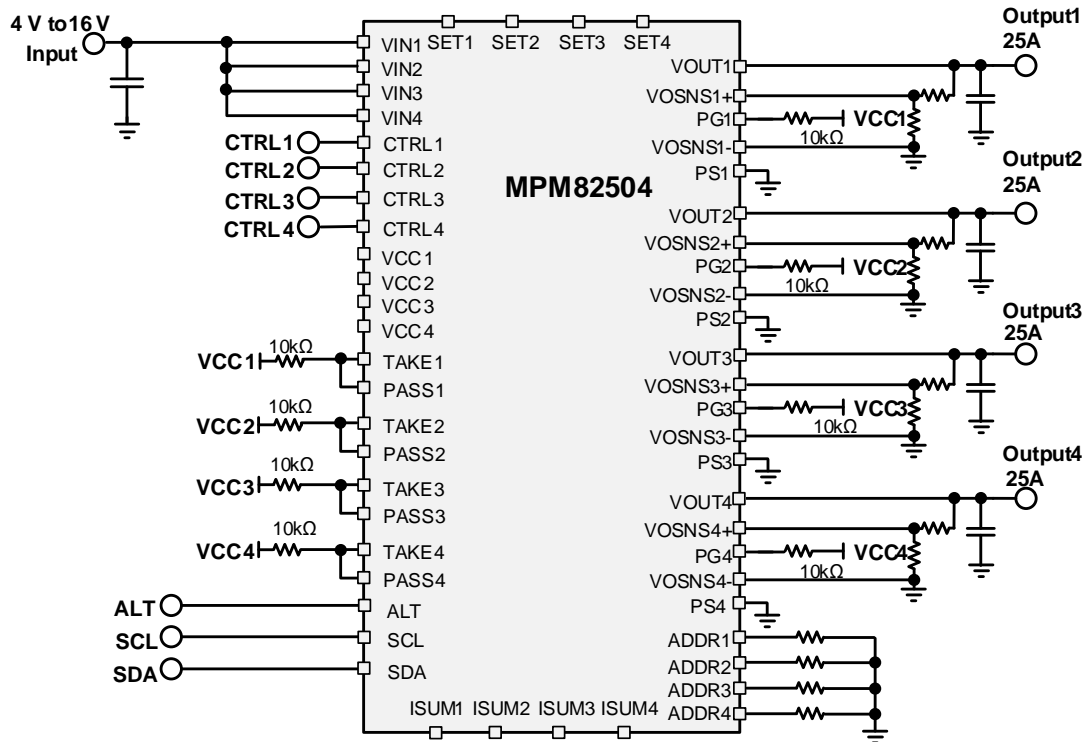


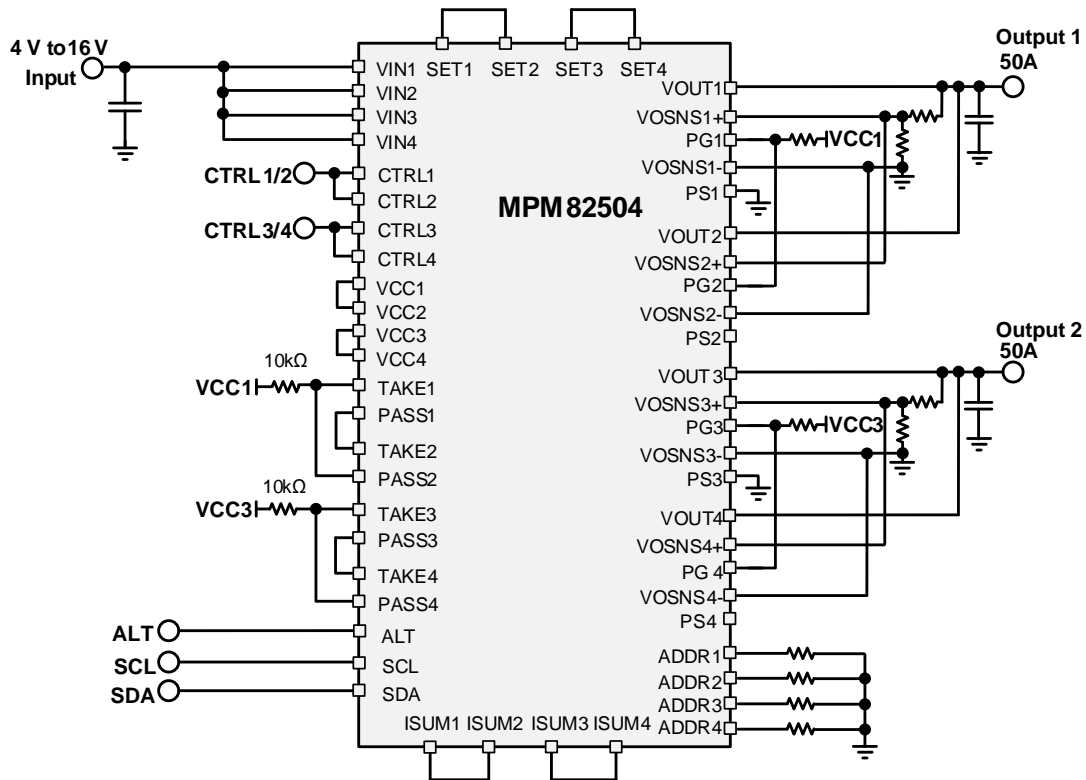**Figure 9: Typical Application Circuit (4V to 16V Input, Quad 25A Output)**



**Figure 10: Typical Application Circuit (4V to 16V Input, Dual 50A Output in Parallel Operation)**

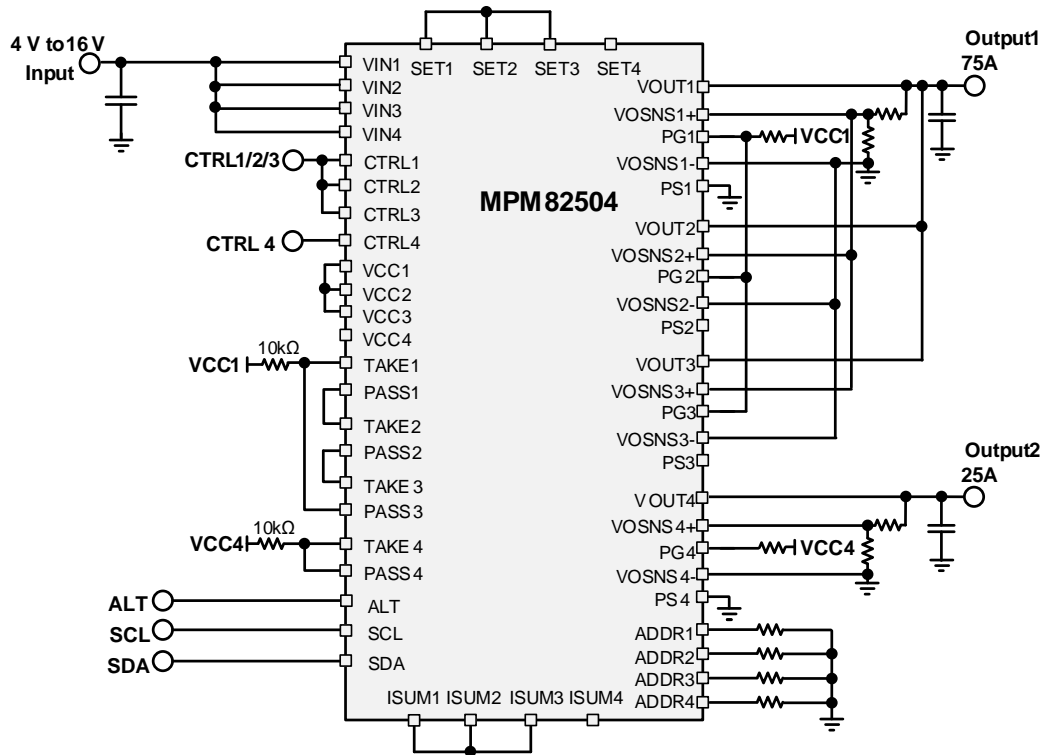# TYPICAL APPLICATION CIRCUITS *(continued)*



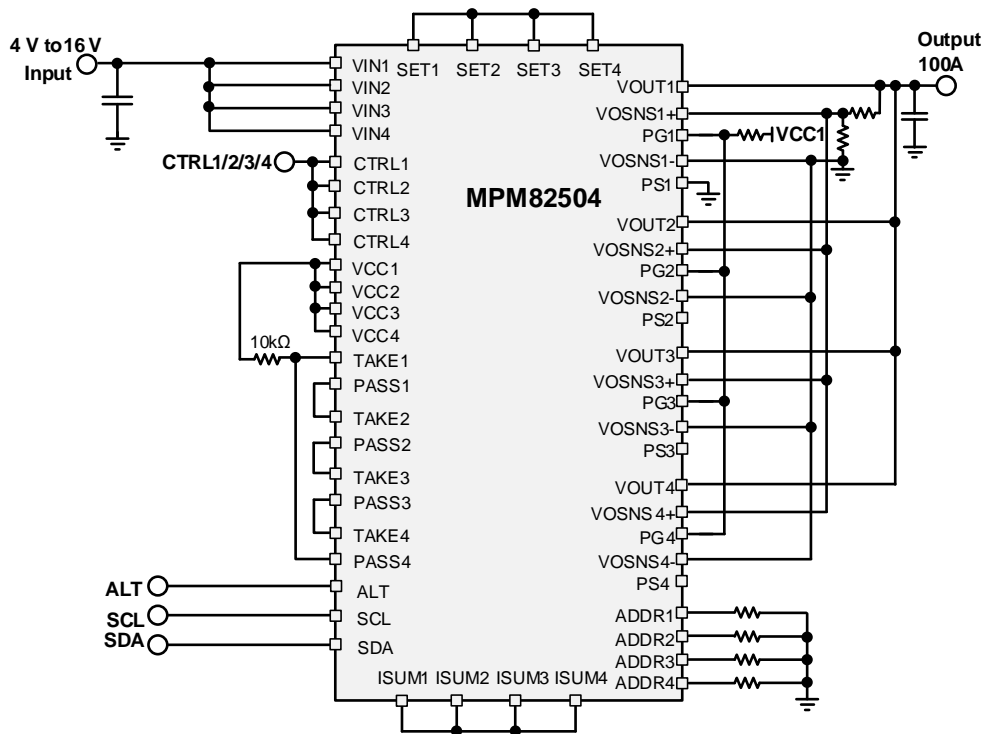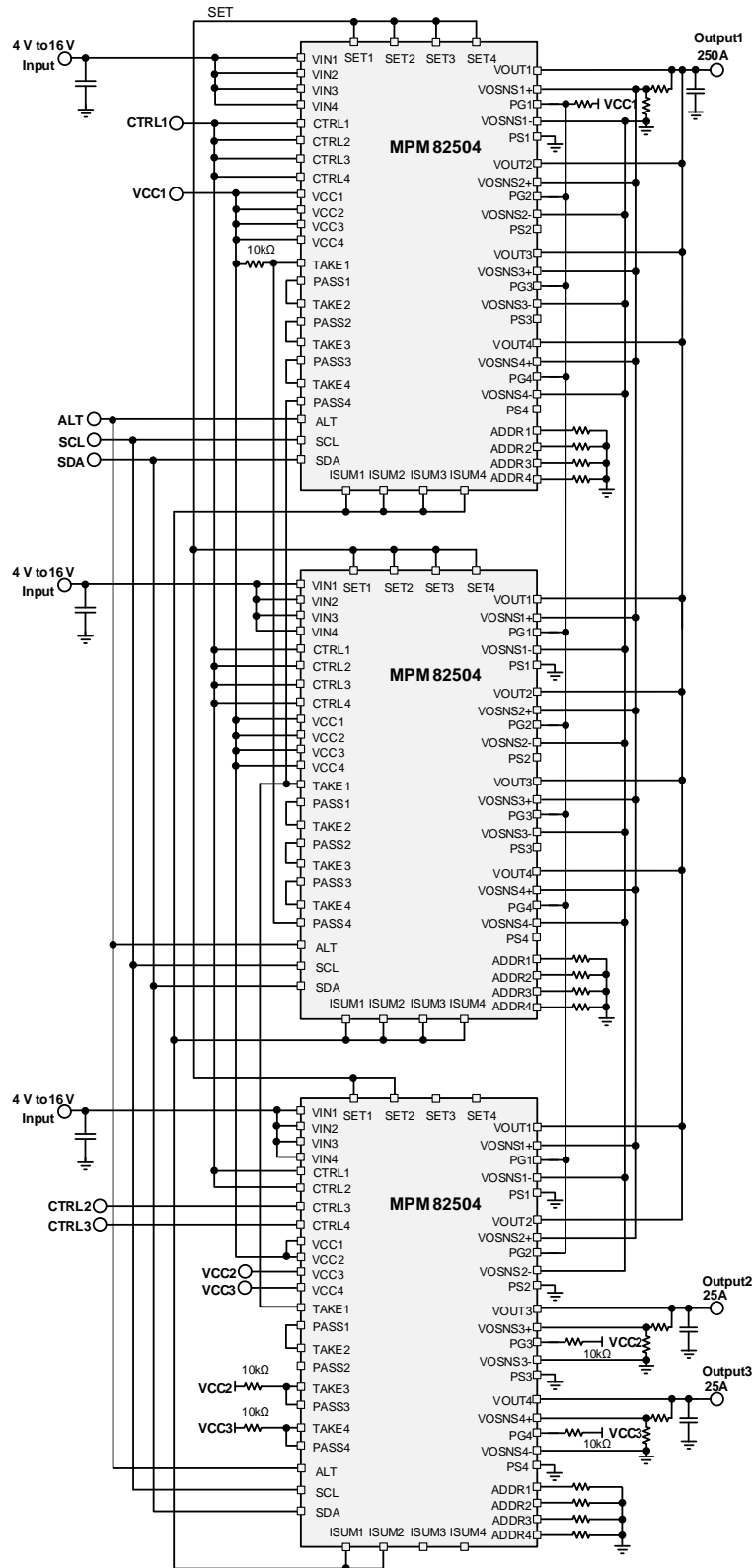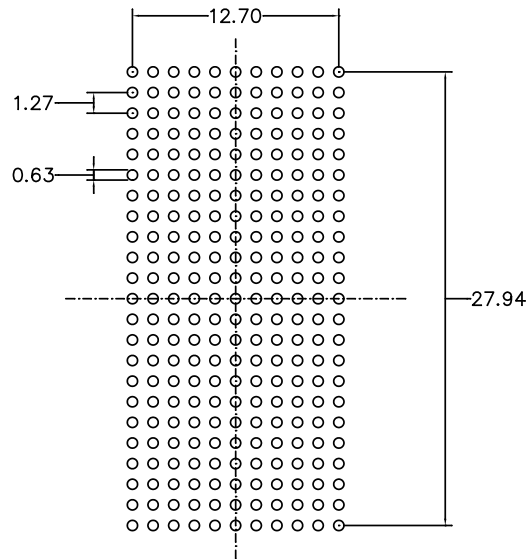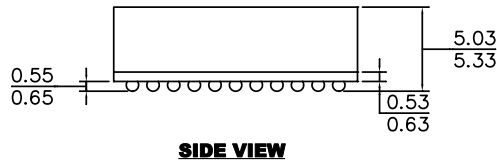**Figure 11: Typical Application Circuit (4V to 16V Input, 75A Output in Parallel Operation plus 25A Output)**



**Figure 12: Typical Application Circuit (4V to 16V Input, Single 100A Output in Parallel Operation)**
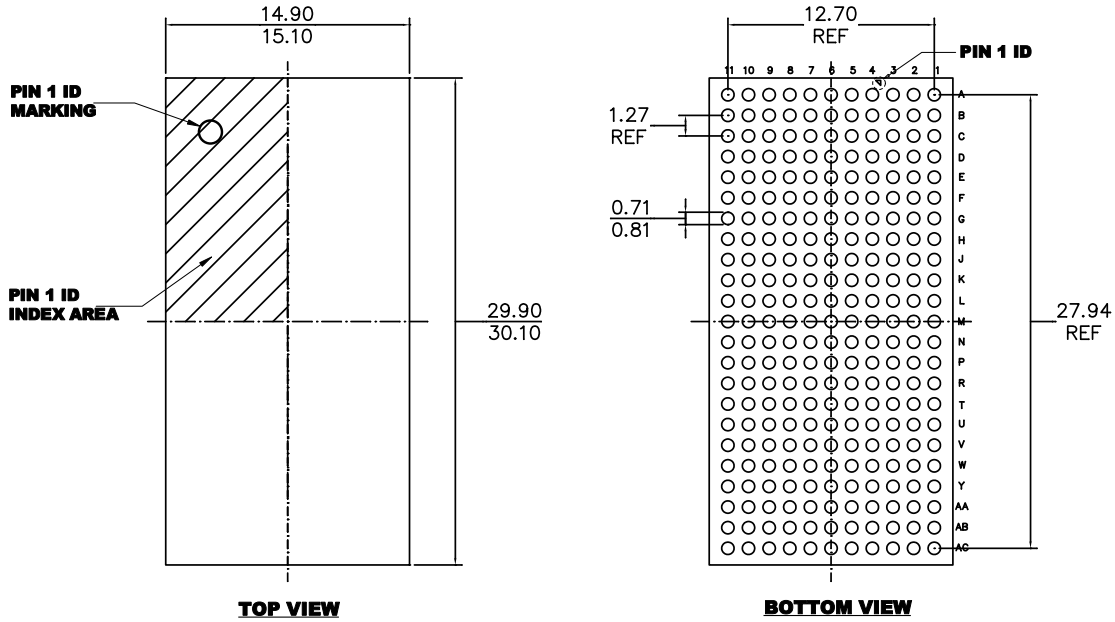
# TYPICAL APPLICATION CIRCUITS *(continued)*



**Figure 13: Typical Application Circuit (4V to 16V Input, Single 250A Output in Parallel Operation plus Dual 25A Output)**

# PACKAGE INFORMATION

## BGA-253L (15mmx30mmx5.18mm)

**TOP VIEW**

14.90
15.10

PIN 1 ID
MARKING

PIN 1 ID
INDEX AREA

29.90
30.10

**BOTTOM VIEW**

12.70
REF

PIN 1 ID

1.27
REF

0.71
0.81

27.94
REF

**SIDE VIEW**

5.03
5.33

0.55
0.65

0.53
0.63

**RECOMMENDED LAND PATTERN**

12.70

1.27

0.63

27.94

**NOTE:**

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-275A.
4) DRAWING IS NOT TO SCALE.

# CARRIER INFORMATION (X)

**All package in Tray**



Detail A
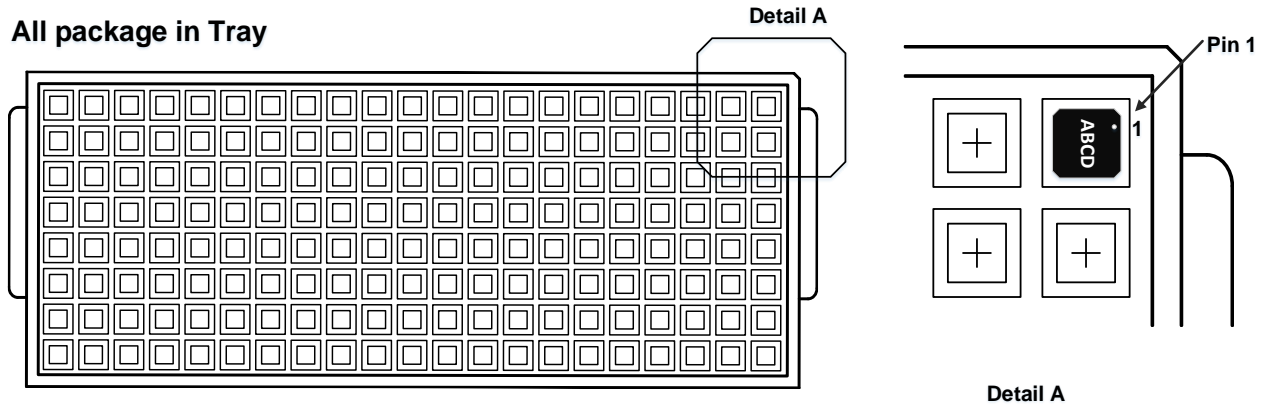
| Part Number | Package Description | Quantity/ Reel | Quantity/ Tray | Quantity/ Tube | Carrier Tape Width | Carrier Tape Pitch |
|---|---|---|---|---|---|---|
| MPM82504GBH–T | BGA-253L (15mmx30mmx5.18mm) | N/A | 48 | N/A | N/A | N/A |

**Note:**

This is a schematic diagram of Tray. Different packages correspond to different trays with different length, width, and height.

# REVISION HISTORY

| Revision # | Revision Date | Description | Pages Updated |
|---|---|---|---|
| 1.0 | 3/24/2021 | Initial Release | - |

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