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## Features

- 16-pin, 4x4 mm QFN Package
- Low Power Operation
- Class AB Operation
- Enable/Disable Control
- Capable of Driving Line Impedance Between 12 Ω to 100 Ω
- Operations to 86 MHz
- RoHS Compliant

## Applications

- Power Line Communications
- Home Networking
- HPNA
- G.HN

## Description

The Le87501 is a single channel line driver designed to work in Home Plug Alliance HPAV2 systems.

When enabled, the operating level can be set to Full, 90% or 80% power. The Le87501 delivers superior performance and can drive a line impedance of 100 Ω down to 12 Ω through a proper transformer.

In addition, the Le87501 features a Standby state which forces the driver into a long-term sleep mode.

**Ordering Information**

| | | |
|---|---|---|
| Le87501NQC | 16-pin QFN Green Pkg. | Tray |

*The green package is Halogen free and meets RoHS 2 Directive 2011/65/EU of the European Council to minimize the environmental impact of electrical equipment.*

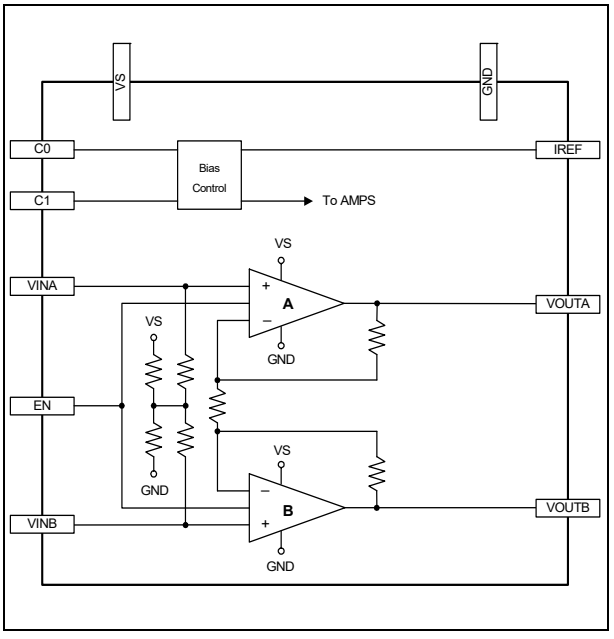



**Figure 1 - Block Diagram**

## Pin Diagram

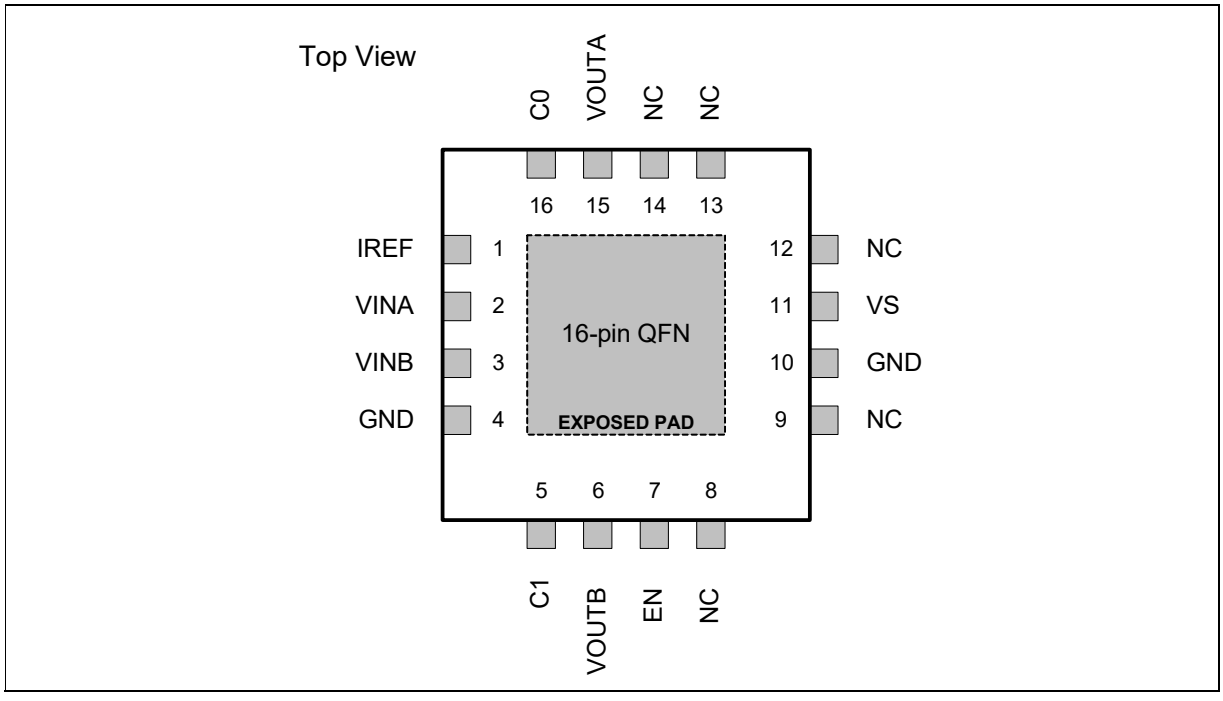



**Figure 2 - Pin Diagram**

Note 1: Pin 1 is marked for orientation.

Note 2: The device incorporates an exposed die pad on the underside of its package. The pad acts as a heat sink and must be connected to a copper plane through thermal vias for proper heat dissipation. It is electrically isolated and may be connected to GND.

## Pin Description

| Pin # | Pin Name | Type | Description |
|---|---|---|---|
| 1 | IREF | Input | Device Internal Reference Current. Connect a resistor to GND. |
| 2 | VINA | Input | Amplifier A input |
| 3 | VINB | Input | Amplifier B input |
| 4, 10 | GND | Ground | Low noise analog ground |
| 5, 16 | C1, C0 | Inputs | Control inputs, sets operation state when channel enabled |
| 6 | VOUTB | Output | Amplifier B output |
| 7 | EN | Input | Enable/Disable control |
| 8, 9, 12, 13, 14 | NC | | No connects, no internal connection |
| 11 | VS | Power | Power supply |
| 15 | VOUTA | Output | Amplifier A output |

**Table 1 - Pin Descriptions**

## Absolute Maximum Ratings

Stresses above the values listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

| | |
|---|---|
| Storage Temperature | $-65°C \le T_A \le +150°C$ |
| Operating Junction Temperature | $-40°C \le T_J \le +150°C$[1] |
| VS to GND | –0.3 V to +16.0 V |
| Driver inputs VINA/B | VS to GND |
| Control inputs C0/1, EN | –0.3 V to +4.0 V |
| Continuous Driver Output Current | 200 $mA_{RMS}$ |
| ESD Immunity (Human Body Model) | JESD22 Class 2 compliant |
| ESD Immunity (Charge Device Model) | JESD22 Class IV compliant |
| Note 1: Continuous operation above +145°C junction temperature may degrade device long term reliability. | |

**Table 2 - Absolute Maximum Ratings**

### Thermal Resistance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad be soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to larger internal copper planes.

### Package Assembly

The green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes.

Refer to IPC/JEDEC J-Std-020 for recommended peak soldering temperature and solder reflow temperature profile.

## Operating Ranges

Microsemi guarantees the performance of this device over the 0°C to +85°C temperature range by conducting electrical characterization and a single insertion production test coupled with periodic sampling. These procedures comply with the Telcordia GR-357-CORE Generic Requirements for Assuring the Reliability of Components Used in Telecommunications Equipment.

| | |
|---|---|
| Ambient temperature | 0°C to +85°C |
| VS with respect to GND | +10 to +15 V |

**Table 3 - Operation Ranges**

## Device Specifications

VS = +12 V. Device in Enable Full Power state using the Basic Test Circuit (Figure 3), unless otherwise specified.

**Typical Conditions:** $T_A$ = 25°C.

**Min/Max Parameters:** $T_A$ = 0°C to +85°C

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit | Notes |
|---|---|---|---|---|---|---|---|
| **Power** | | | | | | | |
| $I_{VS}$ | Quiescent Supply Current | VINA/B floating | | | | | |
| | | Enable Full Power State | 42 | 60 | 70 | mA | |
| | | Enable 90% Power State | 40 | 52 | 63 | mA | |
| | | Enable 80% Power State | 37 | 45 | 56 | mA | |
| | | Disable State | 0.6 | 1.0 | 1.2 | mA | |
| | | Standby State | 0.3 | 0.65 | 1.0 | mA | |
| **Control Input (C0/1, EN) Characteristics** | | | | | | | 1 |
| $V_{IH}$ | Input High Voltage | | 1.2 | | 3.6 | V | |
| $V_{IL}$ | Input Low Voltage | | -0.3 | | +0.6 | V | |
| $I_{IH}$ | Input High Current | | 0 | 75 | 100 | µA | |
| $I_{IL}$ | Input Low Current | | 0 | 10 | 15 | µA | |
| **Channel Input (VINA/B) Characteristics** | | | | | | | |
| $V_{IH}$ | Input Offset Voltage | | 0 | | 35 | mV | |
| $Z_I$ | Differential Input Impedance | VINA – VINB at 2 MHz | 12 | 15 | 18 | kΩ | 2 |
| **Channel Output (VOUTA/B) Characteristics** | | | | | | | |
| $V_O$ | Output Voltage | | 9.5 | | 12 | V | |
| $I_O$ | Output Current | RLoad = 10 Ω | | 600 | | mA | |
| $Z_O$ | Disabled Output Impedance | Differential | | 1400 | | Ω | |
| **Channel Dynamic Characteristics** | | | | | | | |
| | Voltage Gain | VOUT/VIN at 1 MHz | 6.0 | 6.5 | 7.0 | V/V | |
| | Bandwidth | -3 dB | | 170 | | MHz | |
| Noise | Input Referred Noise | Differential | | 8 | | nV/$\sqrt{Hz}$ | |
| MTPR | Multi Tone Power Ratio | PLoad = 40 mW | | | | | |
| | | 0.5 - 30 MHz | | -62 | | dBc | |
| | | 30 - 86 MHz | | -32 | | dBc | |
| | Enable Time | Between Disable and any Power-up state | | 500 | | ns | |
| | Disable Time | | | 500 | | ns | |
| TSD | Thermal Shutdown Temperature | | | 170 | | °C | |

Notes:
1. Internal 50 kΩ pull-down on all control inputs
2. Guaranteed by design and device characterization.

**Table 4 - Electrical Specifications**

## Test Circuit

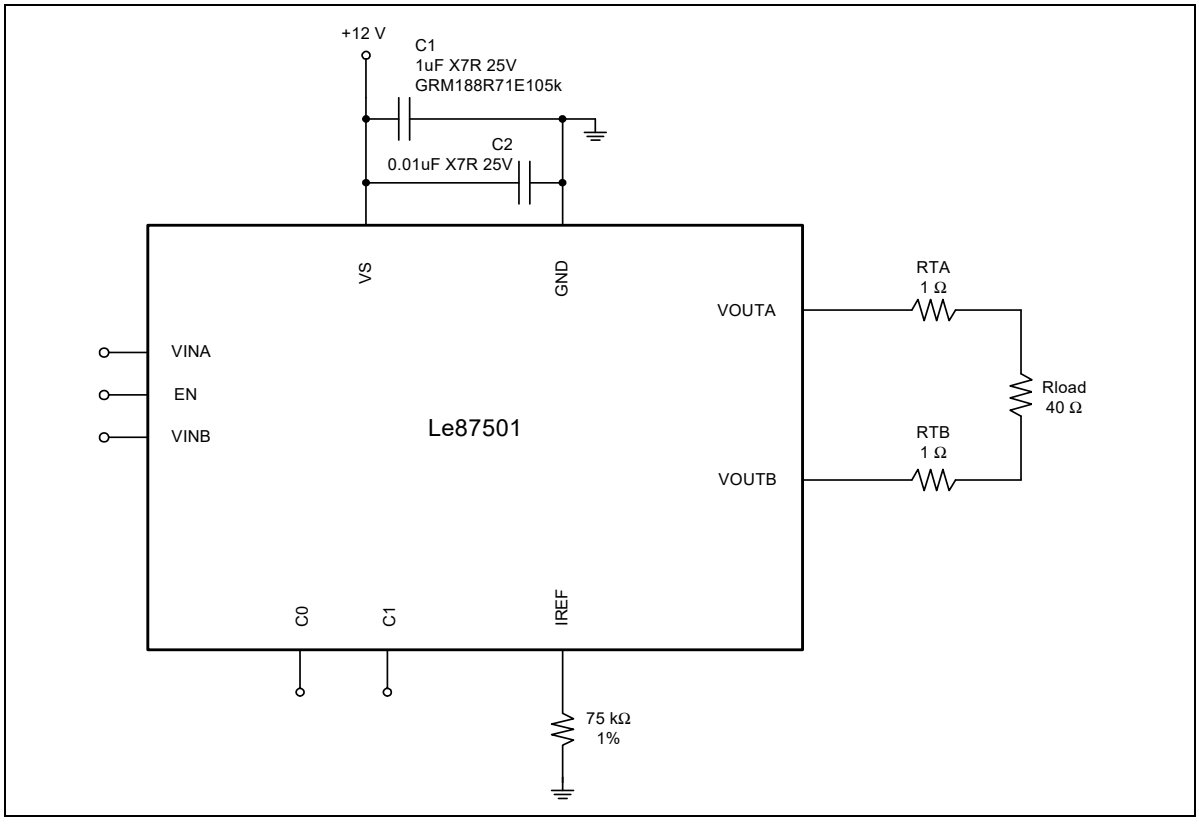



**Figure 3 - Basic Test Circuit**

## Operation States

Operation state control is depicted in Table 5.

For active operation, the driver will either be in Enable state (Power-up mode) or Disable state (Power-down mode). A Standby state (long-term Sleep mode) is also provided.

EN controls the driver's power mode as follows:

- EN = 0, channel A/B in Power-down mode; EN = 1, channel A/B in Power-up mode

C0 and C1 control state selection. A setting of C0 = C1 = 0 overrides EN and places the driver in Standby state.

Standby is the default state when power is initially supplied.

| EN | C1 | C0 | Device State | Mode |
|---|---|---|---|---|
| 1 | 1 | 1 | Enable Full Power | Power-up |
| 1 | 0 | 1 | Enable 90% Power | |
| 1 | 1 | 0 | Enable 80% Power | |
| X | 0 | 0 | Standby | Sleep |
| 0 | 1 | 1 | Disable | Power-down |
| 0 | 1 | 0 | | |
| 0 | 0 | 1 | | |

**Table 5 - Operation State Control**

X = Don't care.

## Typical Performance Characteristics

Some typical performance characteristics are shown in Figure 4, Figure 5 and Figure 6.

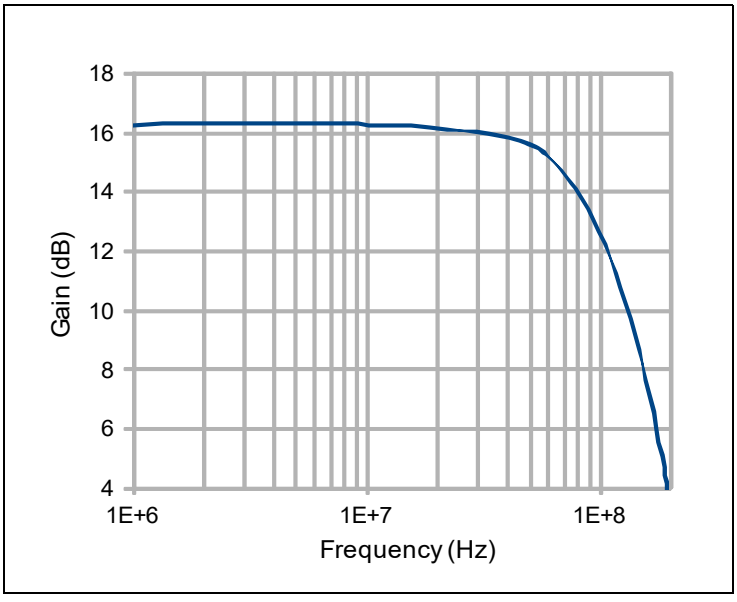



**Figure 4 - Differential Gain**

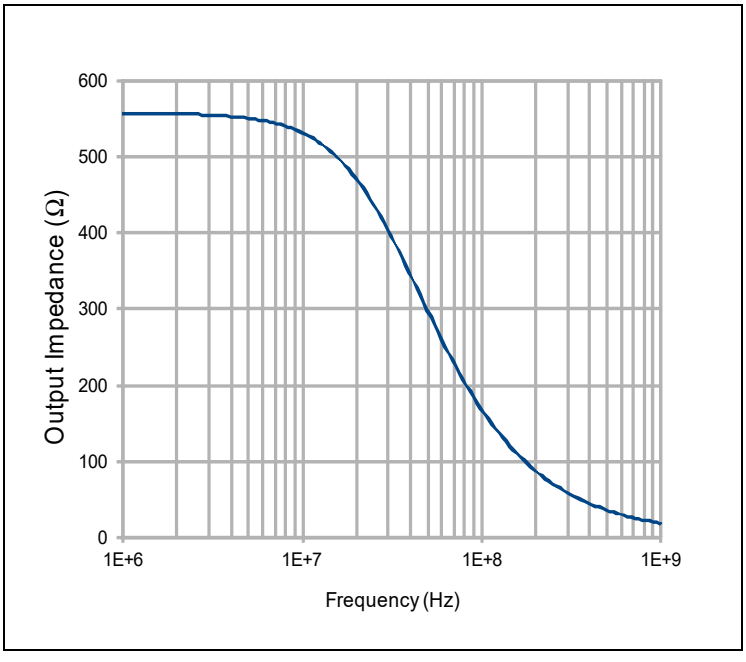



**Figure 5 - Disabled Output Impedance**

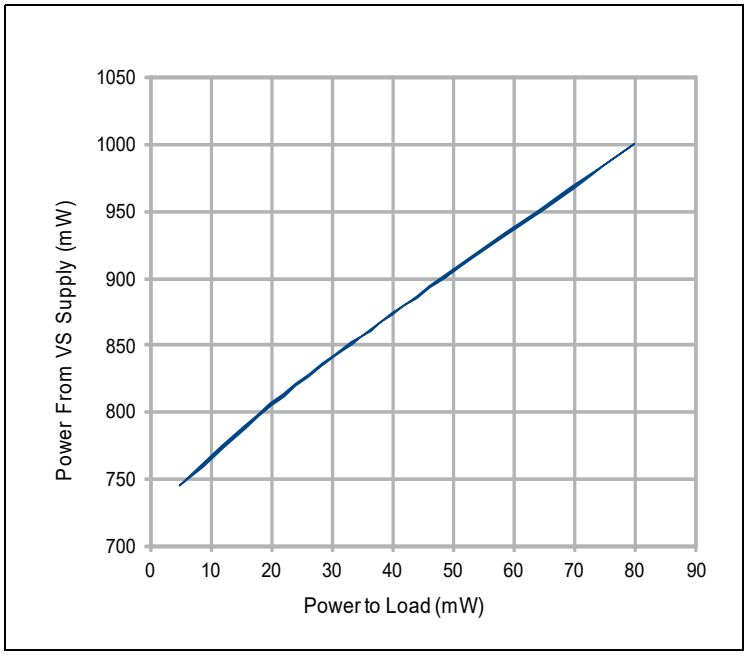



**Figure 6 - Supply Power Versus Load Power**

## Applications

The Le87501 integrates a high-power line driver amplifier designed for low distortion for signals up to 86 MHz. A typical application interface circuit is shown in Figure 7.

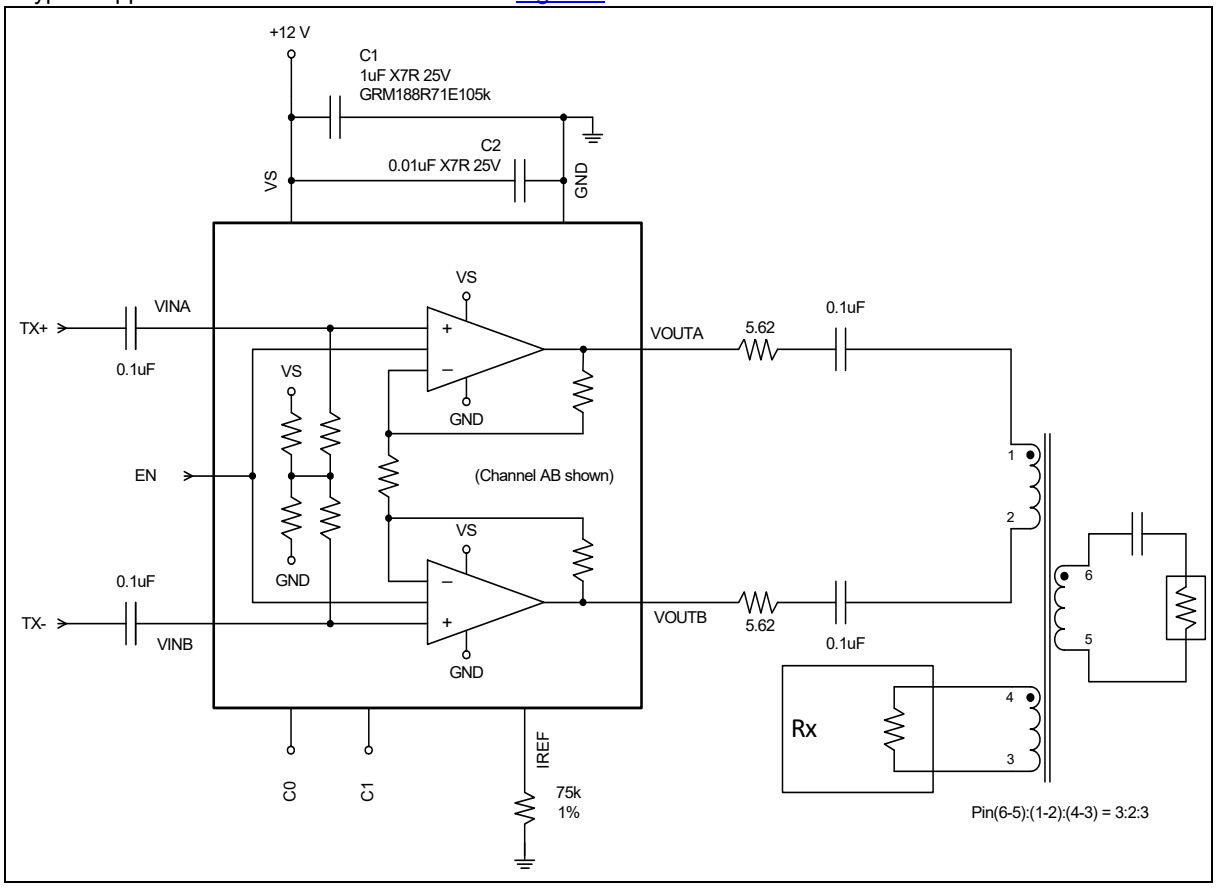



**Figure 7 - Typical Application Circuit**

The amplifiers have identical positive gain connections with common-mode rejection. Any DC input errors are duplicated and create common-mode rather than differential line errors.

### Input Considerations

The driving source impedance should be less than 100 nH to avoid any ringing or oscillation.

### Output Driving Considerations

The internal metallization is designed to drive 200 $mA_{RMS}$ sinusoidal current and there is no current limit mechanism. Driving lines without a series resistor is not recommended.

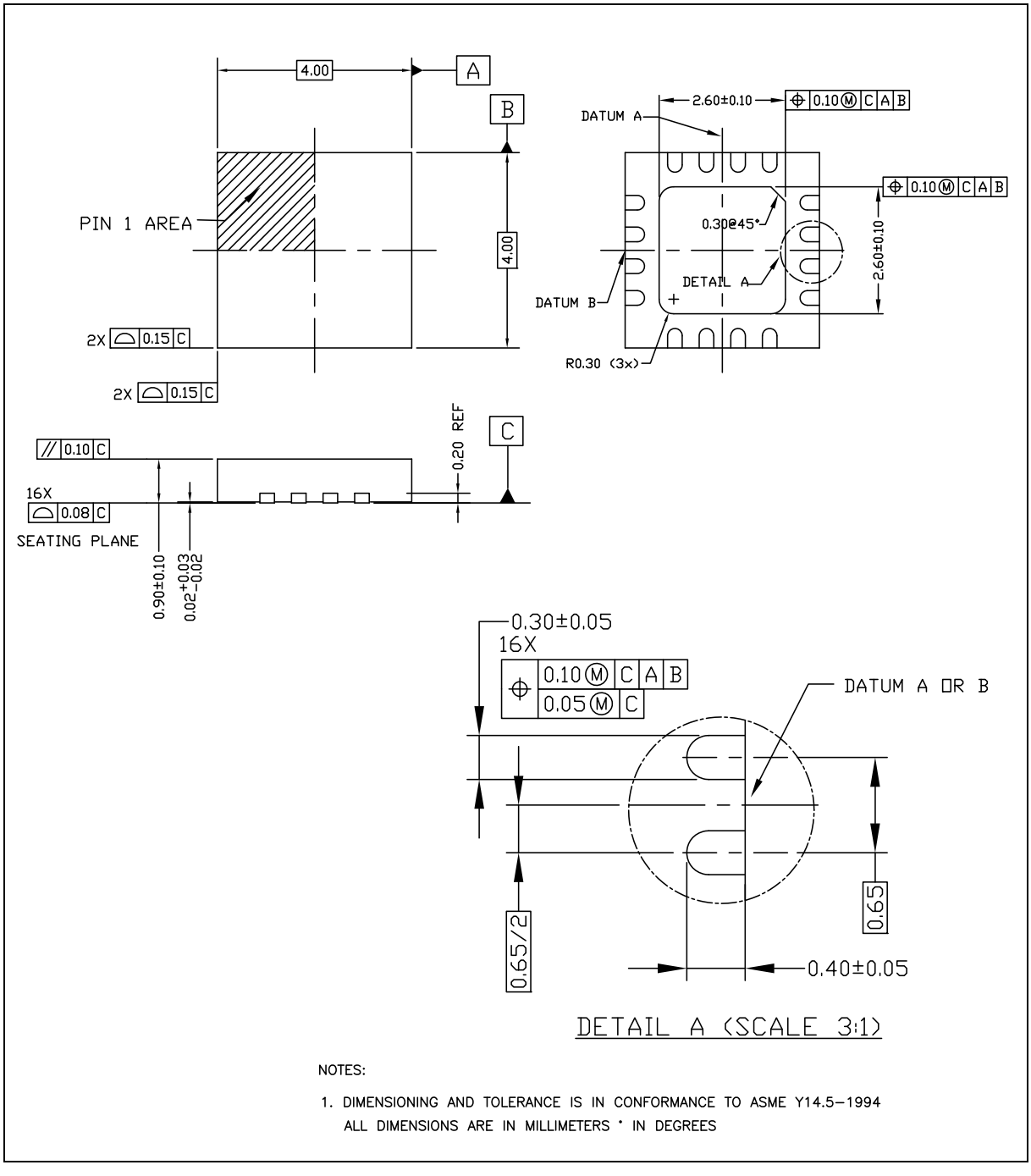
If a DC current path exists between the two outputs, a DC current can flow through the outputs. To avoid DC current flow, the most effective solution is to place DC blocking capacitors in series with the output as shown in Figure 7.

### Power Supplies and Component Placement

The power supply should be well bypassed with decoupling placed close to the Le87501.

## Physical Dimensions

### 16-Pin QFN




***Note:***

*Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.*

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