

Layerscape® LX2162A Communications Processor



The Layerscape LX2162A processor features 16 Arm®v8 Cortex®-A72 cores for server-level performance in a tiny 23 x 23 mm package. With twelve SerDes lanes supporting PCIe® Gen 3 and 4 x 25 Gigabit Ethernet and the low power of 16nm FinFET process technology, this processor is ideal for space-constrained high-performance boards.

OVERVIEW

The LX2162A processor squeezes the processing capability of the popular LX2160A device into a package that is nearly one quarter the size, making it suitable for small boards such as network interface cards, COM Express Type 7 modules, OCP3 mezzanine cards, and custom daughter cards. It retains LX2160A's 16 Cortex-A72 cores, 50 Gbit/s security engine and 88 Gbit/s data compression engine. It has 12 SerDes lanes at up to 25 Gbit/s, which can support four 25 Gbit Ethernet and x8 PCIe Gen3 simultaneously, among many other combinations.

FEATURES

- 16 64-bit Armv8 Cortex-A72 CPU cores, running up to 2.0 GHz
- 16 MB cache
- DDR4 72b including ECC, to 2900 MT/s, maximum capacity of 32 GB

- 2 MB packet caching buffer
- 12 SerDes lanes, operating up to 25 GHz
- Up to 12 Ethernet ports
- Supported Ethernet speeds include 1, 2.5, 10, 25, 40, and 50 Gbit/s
- 105 Gbit/s Layer 2 Ethernet switch
- Up to 12 PCle Gen3 lanes, supporting three ports, as wide as x8
- 50 Gbit/s security accelerator
- 88 Gbit/s data compression/decompression engine
- 4 x SATA3.0
- Secure boot and Arm TrustZone® technology
- 2 x SD / eMMC, 3 x SPI, one 8-bit SPI, 2 x DUART, 8 x I²C, 1 x USB3.0, 2 x CAN (FD optional)

TARGET APPLICATIONS

The LX2162A processor targets space-constrained boards. Designers can use it on a network interface card (NIC) as the control lane to a data path ASIC or FPGA. It also can be the main processor on a 2 x 25 Gbit Ethernet NIC. For industrial applications, designers can incorporate it into standard module form factors such as COM Express, mini-ITX and OCP 3.0.



RELATED SOFTWARE

- Linux® SDK for Layerscape Processors
- CodeWarrior® Development
 Software for Armv8 64-bit based
 Layerscape Series Processors

APPLICATION	EXAMPLES	RELEVANT FEATURES				
Data center offload	 2 x 25 Gbit/s NIC Control plane on FPGA-based NIC 	 8 x PCle® Gen 3 with SR-IOV Low power due to 16nm FinFET process technology Data-center friendly 25 Gbit Ethernet ports 				
Standard industrial module	COM Express Type 7Mini-ITXOCP 3.0 mezzanine card	 23 x 23 mm package Three PCle Gen3 controllers Flexible SerDes configs 				

LAYERSCAPE LX2162A BLOCK DIAGRAM

Arm® Cortex®-A72	A	72	A7	72	A72	A72	A72	2	A72	2		A72	
A72	A	72	A72		A72	A72	A72	A72		2		A72	
1MB L2	1ME	3 L2	1MB	3 L2	1MB L2	1MB L2	1MB I	L2	1MB	L2	11	MB L2	
Interconnect													
8 MB Platform Cache													
I/O MMU I/O MMU I/O MMU													
Secure Boot 2 MB Packet Express Buffer													
Arm® TrustZo	ne®									,	SATA3	SATA3	
Power Manage	ment	SEC - 50 G		WRIOP		x8 Gen3 PCle®	PCle		2	SA	SA		
SD/eMMC	:						en3 F	en3	9 6	2			
2 x DUAR1	Г			1/2 5/10/25/4		s bit Ethernet	8	x4 Gen3	200	t	SATA3	SATA3	
8 x I ² C		DCE -	· 88 G	1/2	.0/10/20/40/00 0	or 10/23/40/30 Gbit Ethernet		^		`		SA	
SPI, GPIO, J7	ΓAG												
USB3.0 + PH	HY	QB-N	Man	12 lanes @ up to 25 GHz									
2 x CAN FI)												

LAYERSCAPE LX2162A FAMILY MEMBERS

	LX2162A	LX2122A	LX2082A			
Cores	16	12	8			
L2 Cache	8 MB	6 MB	8 MB			
SerDes	12 lanes at up to 25 GHz					
PCle®	3 x Gen3, max width of x8					
DDR	DDR4, 2900 MT/s, 32 GB capacity					
Platform cache + PEB	10 MB					
Ethernet	105 Gbit/s L2 switch, supporting combinations of 12 ports of 1, 2.5, 10, 25, 40, and 50 Gbit Ethernet					
Security	50 Gbit/s					
Data Compression Engine	88 Gbit/s					
Package	23 x 23 mm, 1150 pins					

www.nxp.com/LX2162A

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