Le87290

Preliminary Datasheet

VDSL2 Dual Channel Line Driver

April 2019

Microsemi

a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 6.0

Revision 6.0 was published in April 2019. The following was a summary of changes made in this document.

- Added package thermal characteristic data in Table 2 Thermal Resistance Ratings (see page 8).
- Updated parameters in Table 9 Boost Characteristics (see page 10).

1.2 Revision 5.0

Revision 5.0 was published in February 2019. The following was a summary of changes made in this document.

- Added Product Overview and Ordering Information chapters. See Product Overview (see page 3) and Ordering Information (see page 19).

1.3 Revision 4.0

Moved from Advance to Preliminary.

1.4 Revision 3.0

The following was a summary of the changes in revision 3.0 of this document.

- Updated to the new template.
- Updated Boosting Waveforms diagram (Figure 3 (see page 6)).

1.5 Revision 2.0

Following was the list of changes that were made in this revision.

- All mentions of MIMO or SISO are removed from Features and Description (see page 3).
- Figure 4 (see page 12) Note 2: exposed pad is not electrically isolated. It must be connected to GND.
- Operational States description: deleted from "In the Disable Mode" to end of the section.
- Added the following to Table 8 (see page): Driver Outputs (VOUTA/B/C/D) (GND-4 V) to (VS+4 V) VBPI1/2 (VS-2 V) to (VS+7 V) VBNI1/2 (GND-7 V) to (GND+2 V) VBPIx-VBNIx < 26 V
- Added the following to Table 9 (see page 9): Logic Inputs with respect to GND -0.3 V to 3.3 V
- Changed default "Level 15" current to "Level 12" current in Device Specifications:
- Changed Supply Currents in Table 1 (see page): Transmission BSTEN = 0 Typ = 32 mA Transmission BSTEN = 1 Typ = 50 mA Disable Typ = 5 mA
- Changed Power During Transmission in Table 2 (see page):
  - VDSL30a add condition IQLevel = 12 Typ = 590 mW
  - VDSL17a add condition IQLevel = 7 Typ = 530 mW
  - VDSL8b add condition IQLevel = 3 Typ = 650 mW
  - ADSL2 add condition IQLevel = 0 Typ = 710 mW
- Changed Channel Dynamic Characteristics in Table 5 (see page):
  - Input Signal Peak: change max to 1.65 Vpkd
  - Input Signal Peak: condition delete "VOUT/VIN at 1 MHz"
  - Voltage Gain: change typical to 11.4 V/V

- Updated the following in Serial Interface Timing Parameters Table 11 (see page 14)
  - CLK Period: min 905 ns, delete typical
  - CLK Duty Cycle: min = 40 %, max = 60 %
  - DATA setup time: delete from table and from Fig 5
  - RESET hold time: add to table with min=400 ns
  - Add "RESET Release Time" min=200 ns (time from RESET low to first CLK low)
- Table 8 (see page) Quiescent Current Level Selection Change text to Level 0 ~ 18 mA, Level 15 ~ 36 mA, difference between levels ~ 1.2 mA
- Applications: added statement that protector capacitance must be < 110 pF

1.6 Revision 1.0

Revision 1.0 is the first publication of this document.

2 Product Overview

Le87290 is a 2-channel differential line driver supporting ADSL2+ and VDSL2 profiles up to 35b. The device operates from a +12 V supply with an independent Class-H boosting for each channel. Each channel can be enabled independently.

Le87290 can drive a line impedance of 100 Ω through a proper transformer and delivers superior performance with power efficiency.

Le87290 supports numerous operational states through a low pin-count serial interface. The Le87290 device block diagram is shown in Figure 1 (see page 4).

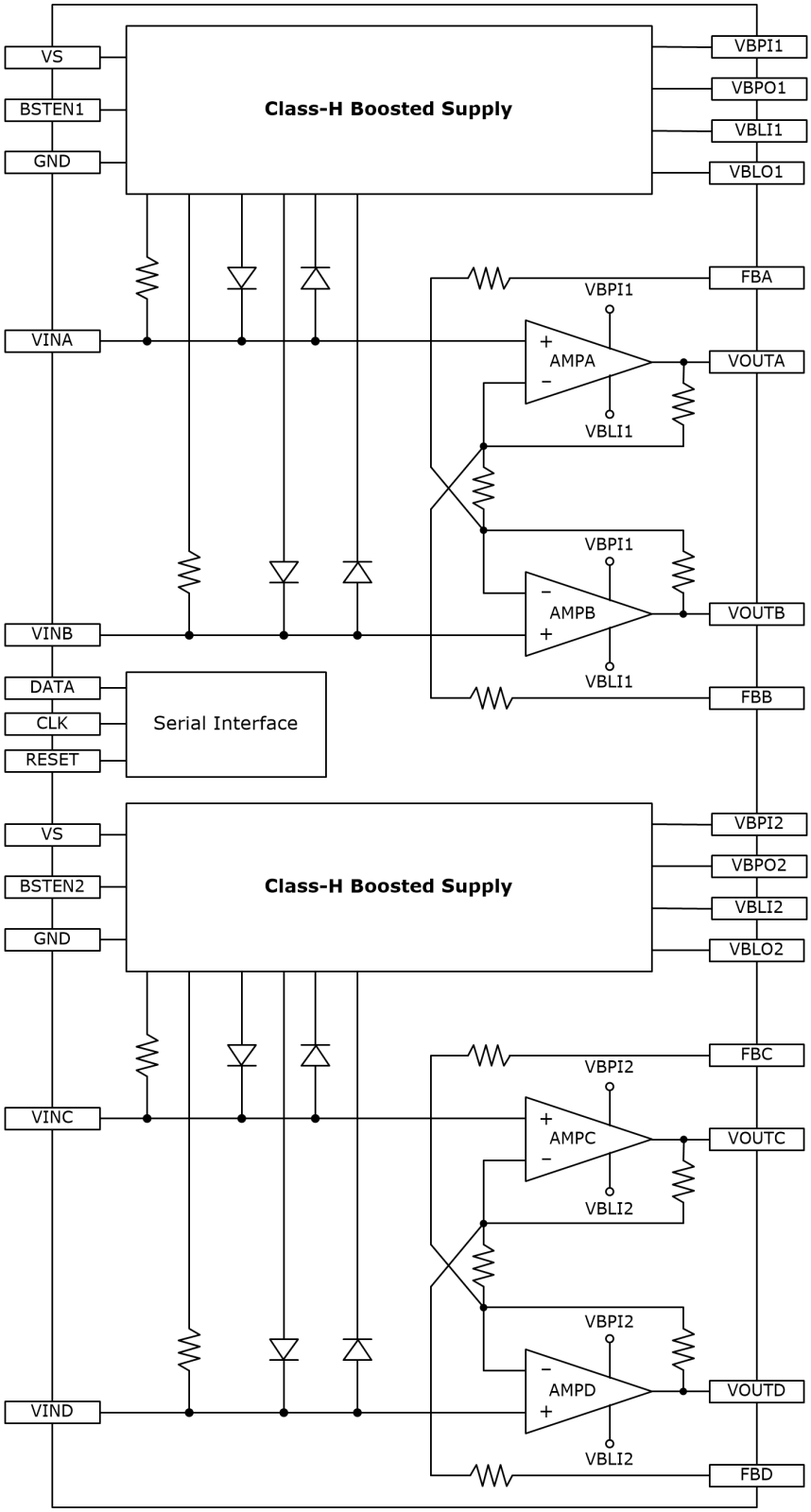
2.1 Features

- VDSL2 Line Drive Capability
  - 35b Profile, 14.5 dBm Line Driver
  - 17a Profile, 18.0 dBm Line Driver
  - 8b Profile, 19.8 dBm Line Driver
- Dual-channel Architecture
- Class-H Operation
- Independent Channel State Control
- Serial Control Interface
- 32-pin, 5mm x 5mm QFN Package
- Low-power Operation
- Capable of Driving 100 Ω Line Impedance
- +12 V Operation

2.2 Applications

- VDSL2 Line Driver
- ADSL2+ Line Driver

Figure 1 • Block Diagram



3 Functional Descriptions

The following sections describe the functionalities of the Le87290 device.

3.1 Operational States

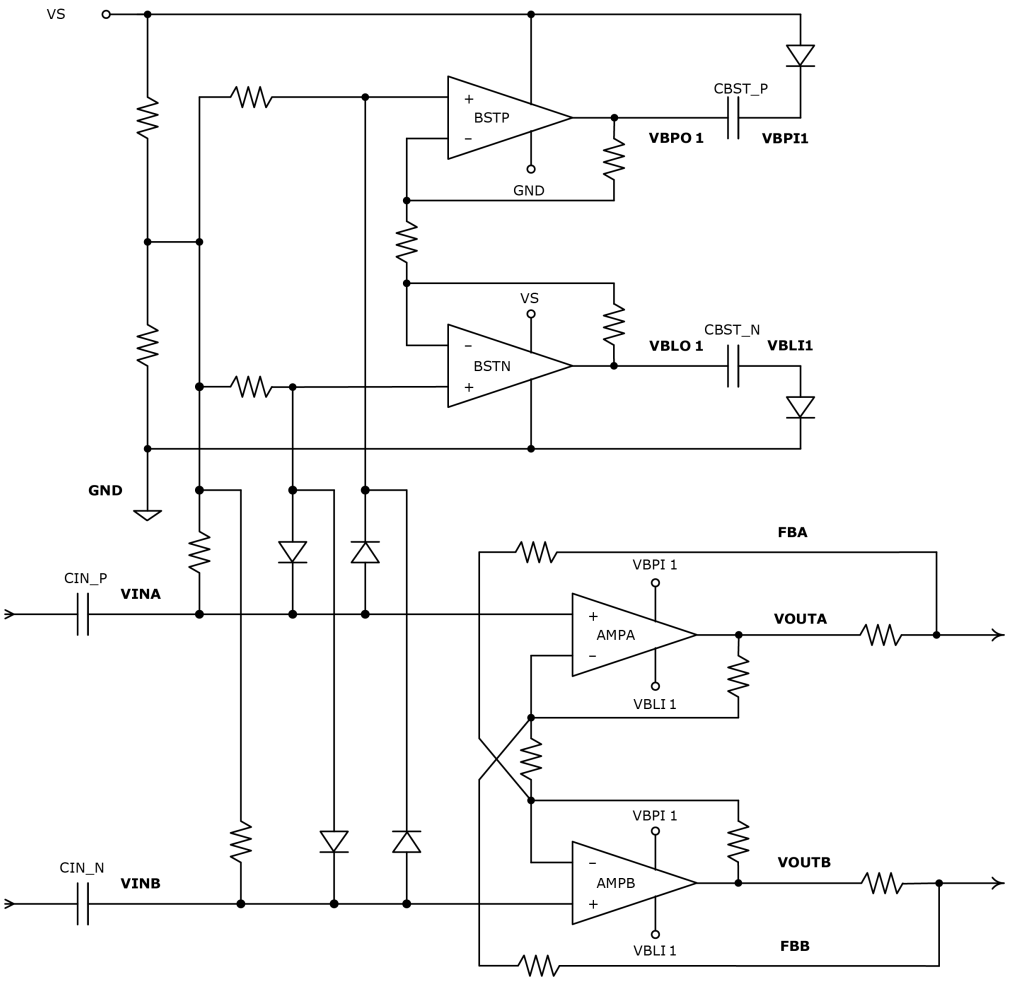
The Le87290 device has Disable and Enable modes and has 16 Quiescent Current Transmission states. See the Power Mode (see page 16) section for a complete listing of all the states and modes of operation.

3.2 Class-H Boosted Supply

The Le87290 device operates and drives signals using a low-voltage supply (VS). It includes circuitry that stores voltage on external boost capacitors. When boosting is operational, the output of the drive amplifiers is increased, thereby avoiding saturation and any associated distortion.

The following figure illustrates the boosting circuitry for one channel, and the device pin nodes are highlighted in bold. The four capacitors shown are discrete external components. For stability, it is important to minimize the inductance in series with the boost capacitors. The capacitors should be located close to the Le87290 device to minimize the trace length.

Figure 2 • Class-H Boosted Supply Operation - Channel AB Shown



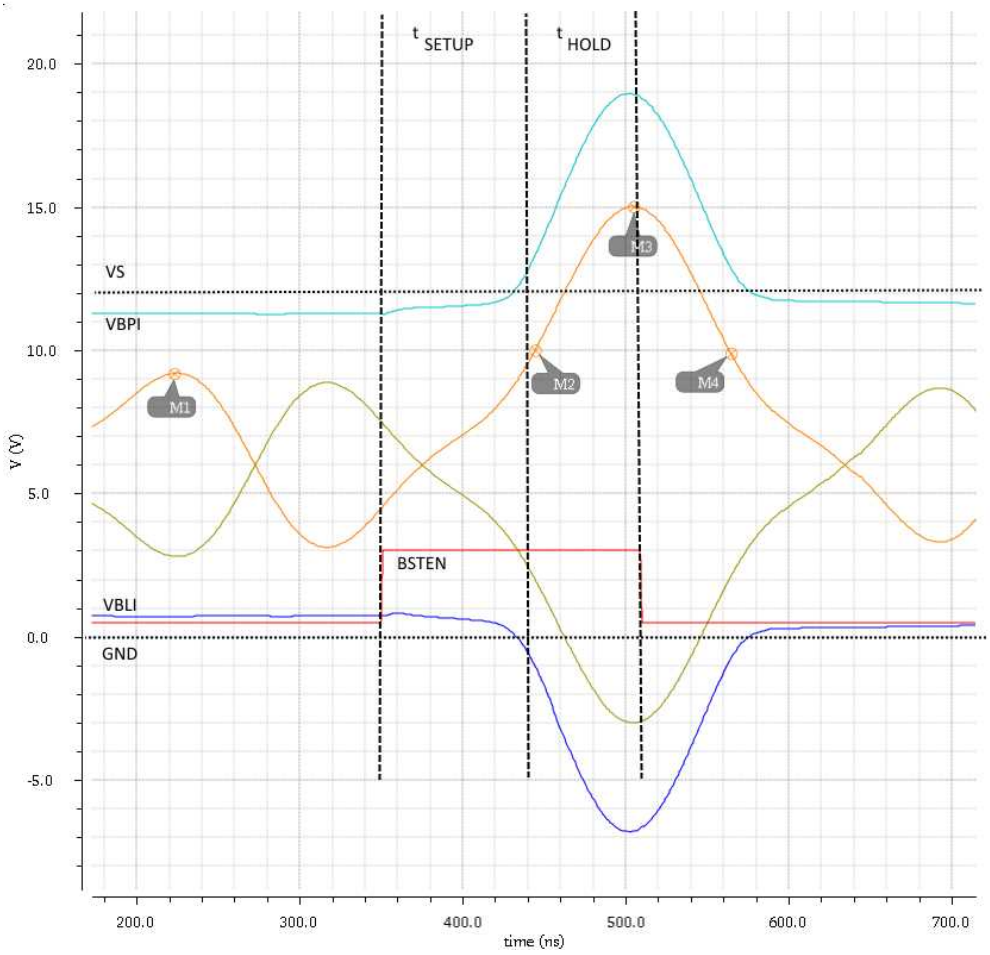
The line driver operates from a +12 V supply. For an increased range of output signal, the device generates a Class-H boosted supply at nodes VBPI/VBLI.

Boosting amplifier (combined BSTN and BSTP in the diagram) is enabled by BSTEN control input (not shown).

The preceding figure shows the function of one boost amplifier with one line driver channel. Channel 2 has a second, independent boost amplifier with an independent BSTEN control input.

The following figure shows an example of waveforms during boost operation. Nodes VBPI1 and VBLI1 effectively supply rails for the drive amplifiers (combined AMPA and AMPB). VBPI1/VBLI1 are offset from the VS/GND rails by approximately 1 V. There is an additional overhead offset between VBPI1 /VBLI1 and VOUTA/B, also approximately 1 V. Point M1 in the following figure marks the largest possible output signal without boosting (VMAX), approximately 8 VPKD.

Figure 3 • Boosting Waveforms



When the line driver output exceeds VMAX, the boost circuit must be enabled to avoid clipping. Point M2 in the preceding figure marks VOUT > VMAX. BSTEN is asserted with some setup time (tSETUP) before M2. BSTEN powers up the boost amplifier and lowers the internal boost detection threshold. An internal comparator holds the boost amplifier engaged until the line driver output drops. The timing of BSTEN does not control the timing or threshold of boosting the VBPI and VBLI signals. BSTEN must remain active for a time after VOUT > VMAX (tHOLD) to ensure that the internal comparator has activated. The preceding figure shows a valid BSTEN control signal.

VINA/B inputs to the drive amplifier are also inputs to the boost amplifier. The boost amplifier does not respond until |VINA/B| exceeds a boosting threshold voltage (VBTH). This is represented in Figure 2 (see page 5) by a set of rectifying diodes, but the actual VBTH value is different than that of a diode voltage drop. VBTH is fixed and is not externally adjustable. The gain of the boost amplifier is set independently of the drive amplifier gain and is not externally adjustable.

At point M3 in the preceding figure, VOUTA/B reaches the maximum required 18.5 VPKD. As shown, VBPI/VBLI reaches a maximum 21 VPKD.

3.2.1 Operation Without Boosting

If boosting is not used in an application, the external boost capacitors can be removed. Pin VBPI1 can be tied to VS, and pin VBLI1 can be tied to GND. Likewise, for Channel 2, pin VBPI2 can be tied to VS, and pin VBLI2 can be tied to GND. In this way, the drive amplifiers gain 2 more volts of operating ranges.

3.2.2 Boost Enable

Each boost circuit has a dedicated Boost control pin (BSTEN1 or BSTEN2). BSTEN is a 2-level input as defined in Table 3 (see page 9). There is a pull-down resistor on the BSTEN pins.

When BSTENx = 1, the boost amplifiers are fully biased and functional (if bit 5 is programmed high, see Table 13 (see page 16)).

When BSTENx = 0, the boost amplifiers are not functional.

4 Electrical Specifications

The following sections describe the electrical specifications of the Le87290 device.

4.1 Absolute Maximum Ratings

Stresses above the values listed under Absolute Maximum Ratings can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

Table 1 • Absolute Maximum Ratings

Parameter	Ranges
Storage Temperature	–65 °C ≤ T_A ≤ +150 °C
Operating Junction Temperature	–40 °C ≤ T_J ≤ +150 °C[1]
VS to GND	–0.3 V to +16 V
Driver inputs (VINA/B/C/D)	VS to GND
Driver outputs (VOUTA/B/C/D)	GND –4 V to VS +4 V
VBPI1/2	VS –2 V to VS +7 V
VBLI1/2	GND –7 V to GND +2 V
VBPIx - VBLIx	< 26 V
Logic inputs with respect to GND	–0.3 V to +4 V
ESD Immunity (Human Body Model)	JESD22 Class 2 compliant
ESD Immunity (Charge Device Model)	JESD22 Class IV compliant

1. Continuous operation above 145 °C junction temperature may degrade long-term reliability of the device.

4.1.1 Thermal Resistance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad is soldered to an equally sized exposed copper surface, which, in turn, conducts heat through multiple vias to larger internal copper planes.

Table 2 • Thermal Resistance Ratings

Parameter	Value
Maximum device power dissipation, continuous , T_A = 85 °C, P_D	2.35 W
Junction to ambient thermal resistance [1], Θ_{JA}	27.7 °C/W
Junction to board thermal resistance, Θ_{JB}	9.9° C/W
Junction to case top, Θ_{JC}	14.0° C/W
Junction to case bottom (exposed pad) thermal resistance, $\Theta_{JP\ (BOTTOM)}$	2.4° C/W
Junction-to-top characterization parameter, Ψ_{JT}	0.1 ° C/W

1. No air flow.

4.1.2 Package Assembly

The green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes.

See IPC/JEDEC J-Std-020for recommended peak soldering temperature and solder reflow temperature profile.

4.2 Operating Ranges

Microsemi guarantees the performance of this device over the industrial (−40 °C to 85 °C) temperature range by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with the Telcordia GR-357-CORE Generic Requirements for Assuring the Reliability of Components Used in Telecommunications Equipment.

Table 3 • Operating Ranges

Parameter	Min.	Max.	Units
Ambient temperature	−40	+85	°C
VS with respect to GND		12, ±5%	V
Logic inputs with respect to GND	−0.3	+3.3	V

4.3 Device Specifications

VS = +12 V.

Channels enabled with Level 12 Quiescent current state using the Application Circuit (Figure 6 (see page 17)) unless otherwise specified.

Typical Conditions: T_A = +25°C

Min/Max Parameters: T_A = –40 °C to +85 °C

4.3.1 Supply Currents

Table 4 • Supply Currents

Parameter	Condition	Min.	Typ.	Max.	Unit
I_{VS} (per channel)	Quiescent, VINA/B/C/D floating				
Transmission Power States	BSTEN = 0		32		mA
	BSTEN = 1		50		mA
Disable Mode (full chip)				6	mA

4.3.2 Power During Transmission

Table 5 • Power During Transmission

Parameter	Condition	Min.	Typ.	Max.	Unit
Device Power (per channel)	Rline = 100 Ω				
Enable VDSL30a Power State	Quiescent current Level 12		590		mW
Enable VDSL17a Power State	Quiescent current Level 7		530		mW
Enable VDSL8b Power State	Quiescent current Level 3		650		mW
Enable ADSL2 Power State	Quiescent current Level 0		710		mW

4.3.3 Control Inputs (DATA, CLK, RESET, and BSTEN1/2) Characteristics

Table 6 • Control Inputs (DATA, CLK, RESET, BSTEN1/2) Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}		2.0			V
V_{IL}				0.8	V

4.3.4 Channel Outputs (VOUTA/B and VOUTC/D) Characteristics

Table 7 • Channel Outputs (VOUTA/B, VOUTC/D) Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Output Voltage	Differential, Boosting[1], BSTEN1/2 = 1	18.5			V_{PKD}
	Differential, Not Boosting, BSTEN1/2 = 0		8		V_{PKD}
Output Current		250			mA

1. Guaranteed by design and device characterization.

4.3.5 Channel Dynamic Characteristics

Table 8 • Channel Dynamic Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Input Signal Peak[1]	Differential			1.39	V_{PKD}
Voltage Gain	(FBA-FBB)/(VINA-VINB) at 1 MHz		11.4[2]		V/V
Gain Flatness[1]	30 MHz	–1.5		1.0	dB
Bandwidth[1]	–3 dB	40			MHz
Output Noise[1]	Differential			300	nV/√Hz

1. Guaranteed by design and device characterization.
2. Gain to VOUTA-VOUTB is 13.55. See Figure 6 (see page 17) for signal name definition.

4.3.6 Boost Characteristics

Table 9 • Boost Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Boost Setup Time (t_{SETUP})[1]		20			ns
Boost Hold Time (t_{HOLD})[1]		35[2]			ns
Boost Threshold Voltage			260		mV_{PK}

1. Guaranteed by design and device characterization.
2. If input signal is greater than the Boost Threshold Voltage for less than 35 ns, then BSTEN can drop as soon as input signal falls below Boost Threshold Voltage.

4.3.7 Thermal Shutdown

Table 10 • Thermal Shutdown

Parameter	Condition	Min.	Typ.	Max.	Unit
Thermal Shutdown Temperature[1]			170		°C

1. Guaranteed by design and device characterization.

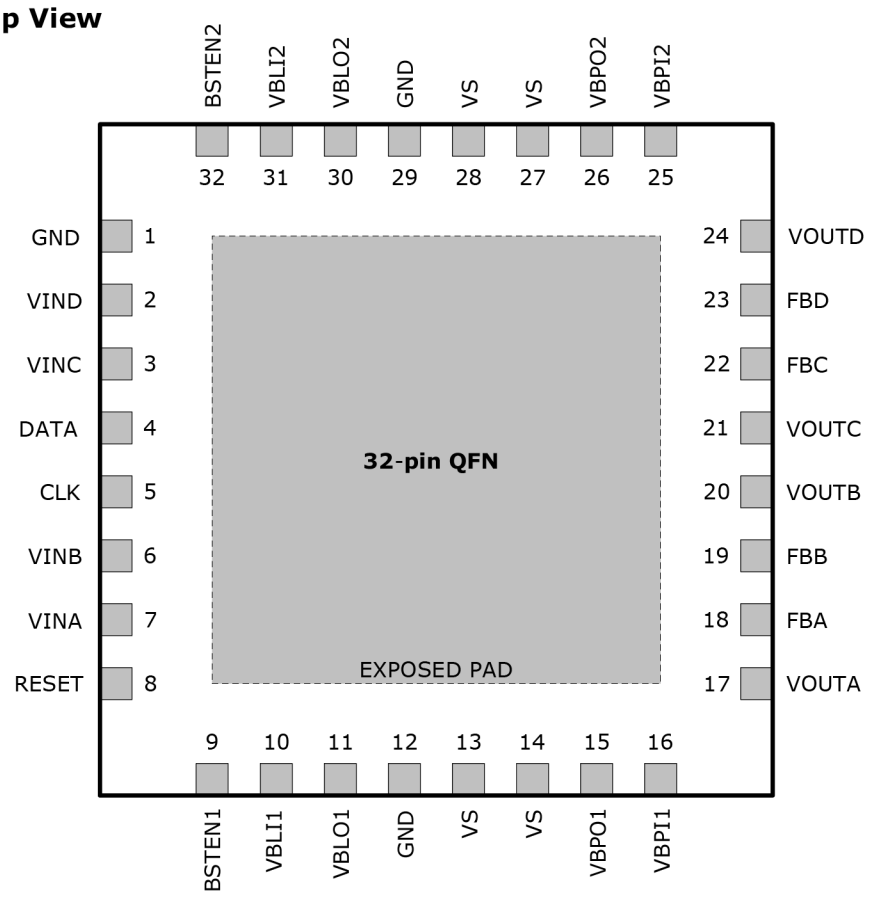
5 Pin Description

The Le87290 device has 32 pins, which are described in this section.

5.1 Pin Diagram

The following illustration is a representation of the Le87290 device, as seen from the top view.

Figure 4 • Le87290 Pin Diagram



Notes:

- Pin 1 is marked for orientation.
- The device incorporates an exposed die pad on the underside of its package. The pad acts as a heat sink and a ground connection, the exposed pad must be connected to a copper ground plane through thermal vias for proper heat dissipation.

5.2 Pin Description

The following table shows the functional pin descriptions for the Le87290 device.

Table 11 • Le87290 Pin Description

Pin Name	Pin #	Type	Description
GND	1, 12, 29, Exposed Pad	Ground	Low noise analog ground
VIND	2	Input	Amplifier D input
VINC	3	Input	Amplifier C input
DATA	4	Input	Control data input
CLK	5	Input	Clock for data control
VINB	6	Input	Amplifier B input
VINA	7	Input	Amplifier A input
RESET	8	Input	Resets the device (active high)
BSTEN1	9	Input	Boost control for amplifiers A and B
VBLI1	10	Input	Connects to ground through an internal diode
VBLO1	11	Output	Connect a capacitor to VBLI1
VS	13, 14, 27, 28	Power	+12 V power supply
VBPO1	15	Output	Connect a capacitor to VBPI1
VBPI1	16	Input	Connects to VS through an internal diode
VOUTA	17	Output	Amplifier A output
FBA	18	Input	Feedback node for A line driver
FBB	19	Input	Feedback node for B line driver
VOUTB	20	Output	Amplifier B output
VOUTC	21	Output	Amplifier C output
FBC	22	Input	Feedback node for C-line driver
FBD	23	Input	Feedback node for D line driver
VOUTD	24	Output	Amplifier D output
VBPI2	25	Input	Connects to VS through an internal diode
VBPO2	26	Output	Connect a capacitor to VBPI2
VBLO2	30	Output	Connect a capacitor to VBLI2
VBLI2	31	Power	Connects to ground through an internal diode
BSTEN2	32	Input	Boost control for amplifiers C and D

6 Serial Control Interface

The Le87290 device is controlled by five logic input signals - CLK, DATA, RESET, BSTEN1, and BSTEN2. All logic input pins have a pull-down resistor to force logic low when not externally driven.

CLK and DATA signals implement a serial interface for line driver state control. Each line driver channel is controlled independently. The driver amplifier bias current can be adjusted across 16 levels.

The boost amplifiers and driver amplifiers are separately enabled or disabled. Each boost amplifier has a dedicated BSTEN control pin. To operate the boost amplifier, it must first be enabled in an appropriate state through the serial interface. When in an enabled state, the boost amplifier has a small amount of bias current applied, but not enough to allow full operation of the boosting amplifier. The operational bias current is applied to the boost amplifier when BSTENx is a logic high.

RESET is an active high reset signal which operates independently and asynchronously to the CLK/DATA interface. RESET is generally applied at power-up and when CLK is inactive. When RESET is valid, all control bits on both channels are immediately cleared to low, forcing the disabled state on both channels. RESET also clears all bits in the serial interface input shift register. An equivalent reset function can be achieved by writing 12 high DATA bits as the data word (an invalid data word).

6.1 Serial Interface Timing

Figure 5 (see page 15) shows the timing of a clock and a data word on the serial interface.

Data setup occurs on clock transitions from high to low; this is illustrated in Figure 5 (see page 15) with the dotted lines. Data is latched on clock transitions from low to high.

Timing constraints on the CLK/DATA interface and on applying RESET are detailed in the following table.

Table 12 • Serial Interface Timing Parameters

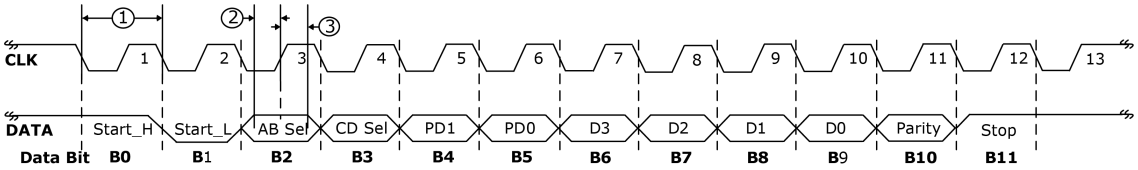
Timing Diagram #	Parameter	Condition	Min.	Typ.	Max.	Unit
1	CLK Period	Applies when writing data words	905			ns
	CLK Duty Cycle	Applies when writing data words	40	50	60	%
2	DATA Setup Time		200			ns
3	DATA Hold Time		200			ns
	RESET Hold Time		400			ns
	RESET Release Time	Time from RESET low (release) to first CLK bit low	200			ns

6.2 Clock and Data Word Format

The following figure shows the format of one data word. Each word consists of 12 data bits (labeled B0 to B11). The device requires 13 complete CLK cycles to read all 12 bits on DATA, as shown in the following figure.

After the data word is complete, both CLK and DATA must return to a logic high state until the next data word is sent. The next data word can occur anytime after the 13th CLK cycle.

Figure 5 • Data Word Format and Timing



6.3 Data Word Definitions

Data word bit definitions are described in the following table. The data bits consist of start, stop and parity bits, channel selection bits, bits to select the power mode, and bits to select the quiescent current.

Table 13 • Data Bit Description

Bit(s)	Description
B0	Start Bit = High.
B1	Start Bit = Low.
B2	Channel Select AB. When high, B4:B9 is loaded into Channel 1 (AB).
B3	Channel Select CD. When high, B4:B9 is loaded into Channel 2 (CD).
B4:B5	Power Mode Select, see Table 13 (see page 16).
B6:B9	Quiescent Current Select, see Table 14 (see page 16).
B10	Parity Bit. For valid data word, set so that B2:B10 always has odd parity.
B11	Stop Bit = High.

A data word will be deemed invalid and not acted upon if bits B0, B1, B10, and B11 are not as described in the preceding table .

7 Power Mode

Power mode bits are defined in the following table.

When the line driver is in the disabled mode, there is no bias current to the amplifiers and the line driver outputs are in a high impedance state.

In order to enable Class-H Boosted Supply operation, both bit B5 and the BSTENx control must be high. Boost operation can be toggled on and off for a given channel with the BSTENx control if bit B5 has been programmed high. Likewise, boost operation can be toggled on and off for a given channel using the B5 bit if BSTENx is tied or programmed high.

Table 14 • Power Mode Selection

PD1 (B4)	PD0 (B5)	Line Driver Mode	Class-H Boosted Supply Mode
0	0	Disabled	Disabled
0	1	Disabled	Enabled (when BSTENx = 1)
1	0	Enabled, Current set by D0:D3	Disabled
1	1	Enabled, Current set by D0:D3	Enabled (when BSTENx = 1)

7.1 Quiescent Current

Quiescent current bits are defined in the following table.

Level 0 has the lowest quiescent current, Level 15 has the highest quiescent current. There is a trade-off between quiescent current and bandwidth. States with higher quiescent currents are used for transmission of higher frequencies.

Table 15 • Quiescent Current Level Selection

Level	I_{VSq} (mA)	D3 (B6)	D2 (B7)	D1 (B8)	D0 (B9)	Application
0	16.0	0	0	0	0	ADSL2+
1	17.2	0	0	0	1	
2	18.4	0	0	1	0	
3	19.6	0	0	1	1	VDSL8b
4	20.8	0	1	0	0	
5	22.0	0	1	0	1	
6	23.2	0	1	1	0	
7	24.4	0	1	1	1	VDSL17a
8	25.6	1	0	0	0	
9	26.8	1	0	0	1	
10	28.0	1	0	1	0	
11	29.2	1	0	1	1	
12	30.4	1	1	0	0	VDSL30a
13	31.6	1	1	0	1	
14	32.8	1	1	1	0	
15	34.0	1	1	1	1	

Note: I_{VSq} quiescent current values are per channel when both channels are operational. Values are approximate.

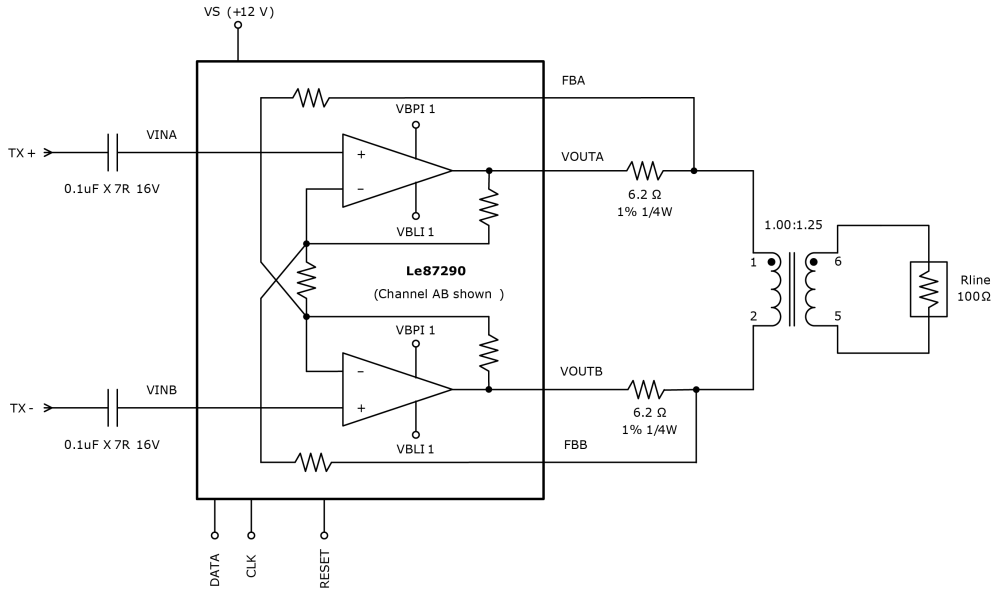
8 Application Information

The Le87290 integrates two sets of high-power line driver amplifiers with Class-H boost operation.

A typical application interface circuit (for one channel without boosting) is shown in the following figure. Output protection is required (but not shown).

The amplifiers have identical positive gain connections with common-mode rejection. Any DC input errors are duplicated and create common-mode rather than differential line errors.

Figure 6 • Typical Application Circuit – Channel A/B Shown



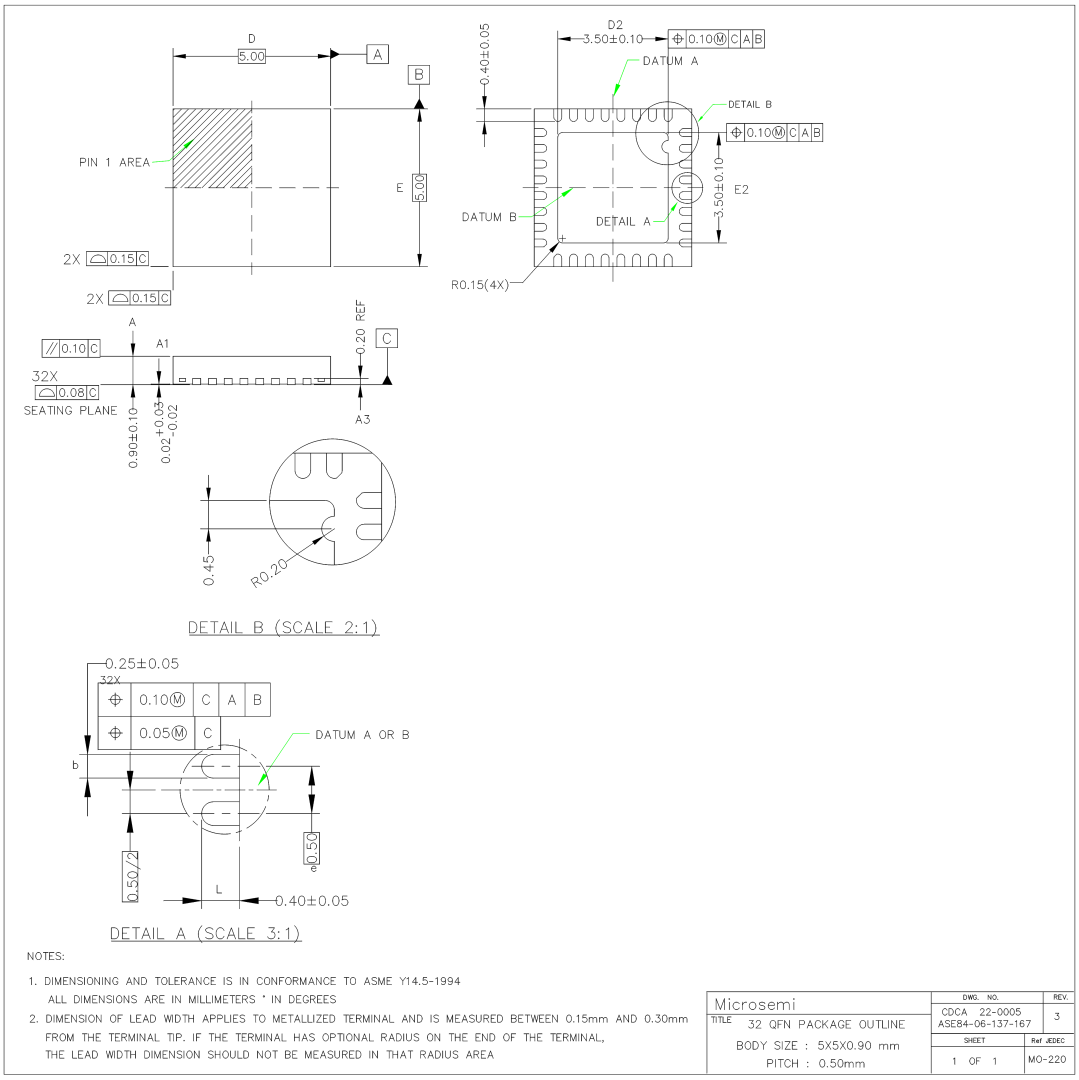
8.1 Protection

Protection circuitry placed across the Le87290 device side of the output transformer must exhibit a capacitance of less than 110 pF.

9 Package Specification

The following figure shows the physical dimensions of the Le87290 device.

Figure 7 • 32-pin_QFN



Note: Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

10 Ordering Information

The following section describes the ordering information of the Le87290 device.

Table 16 • Ordering Information

Part Number	Package	Packaging Type
Le87290YQC	32-pin QFN Green Pkg.	Tray
Le87290YQCT	32-pin QFN Green Pkg.	Tape and Reel

Note: The green package is Halogen-free and meets RoHS 2 Directive 2011/65/EU of the European Council to minimize the environmental impact of electrical equipment.

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