



## LAN91C96

# Non-PCI Single-Chip Full Duplex Ethernet Controller with Magic Packet

Data Brief

## Product Features

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- Non-PCI Single-Chip Ethernet Controller
- A Subset of Motorola 68000 Bus Interface Support
- Fully Supports Full Duplex Switched Ethernet
- Supports Enhanced Transmit Queue Management
- 6K Bytes of On-Chip RAM
- Supports IEEE 802.3 (ANSI 8802-3) Ethernet Standards
- Automatic Detection of TX/RX Polarity Reversal
- Enhanced Power Management Features
- Supports "Magic Packet" Power Management Technology
- Hardware Memory Management Unit
- Optional Configuration via Serial EEPROM Interface (Jumperless)
- Supports single +5V or +3.3V (for Revisions E and Later) VCC Designs
- Supports Mixed Voltage External PHY Designs
- Low Power CMOS Design
- 100 Pin QFP and TQFP (1.0 mm body Thickness) Lead-Free RoHS Compliant Packages
- Pin Compatible with the LAN91C92 and LAN91C94

### Bus Interface

- Direct Interface to Local Bus, PCMCIA, and 68000 Buses with No Wait States
- Flexible Bus Interface
- 16 Bit Data and Control Paths
- Fast Access Time
- Pipelined Data Path
- Handles Block Word Transfers for any Alignment
- High Performance Chained ("Back-to-Back") Transmit and Receive

- Pin Compatible with the LAN91C92 (in Local Bus Mode) and the LAN91C94 in Both Local Bus and PCMCIA Modes
- Dynamic Memory Allocation Between Transmit and Receive
- Flat Memory Structure for Low CPU Overhead
- Buffered Architecture, Insensitive to Bus Latencies (No Overruns/Underruns)
- Supports Boot PROM for Diskless Local Bus Applications

### Network Interface

- Integrated 10BASE-T Transceiver Functions:
  - Driver and Receiver
  - Link Integrity Test
  - Receive Polarity Detection and Correction
- Integrated AUI Interface
- 10 Mb/s Manchester Encoding/Decoding and Clock Recovery
- Automatic Retransmission, Bad Packet Rejection, and Transmit Padding
- External and Internal Loopback Modes
- Four Direct Driven LEDs for Status/ Diagnostics

### Software Drivers

- LAN9000 Drivers for Major Network Operating Systems Utilizing Local Bus or PCMCIA Interface
- Software Drivers Compatible with the LAN91C92, LAN91C94, LAN91C100FD (100 Mb/s), and LAN91C110 (100 Mb/s) Controllers in Local Bus Mode
- Software Drivers Utilize Full Capability of 32 Bit Microprocessor

**ORDER NUMBERS:**

LAN91C96-MS for 100 pin, QFP Lead-Free RoHS Compliant package

LAN91C96-MU for 100 pin, TQFP Lead-Free RoHS Compliant package



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## General Description

The LAN91C96 is a VLSI Ethernet Controller that combines Local Bus, PCMCIA, and Motorola 68000 bus interfaces in one chip. LAN91C96 integrates all MAC and physical layer functions, as well as the packet RAM, needed to implement a high performance 10BASE-T (twisted pair) node. For 10BASE5 (thick coax), 10BASE2 (thin coax), and 10BASE-F (fiber) implementations, the LAN91C96 interfaces to external transceivers via the provided AUI port. Only one additional IC is required for most applications. The LAN91C96 comes with Full Duplex Switched Ethernet (FDSWE) support allowing the controller to provide much higher throughput. 6K bytes of RAM is provided to support enhanced throughput and compensate for any increased system service latencies. The controller implements multiple advanced power-down modes including Magic Packet to conserve power and operate more efficiently. The LAN91C96 can directly interface with the Local Bus, PCMCIA, and 68000 buses and deliver no-wait-state operation. For Local Bus and PCMCIA interfaces, the LAN91C96 occupies 16 I/O locations and no memory space except for PCMCIA attribute memory space. The same I/O space is used for both LOCAL BUS and PCMCIA operations. Its shared memory is sequentially accessed with 40ns access times to any of its registers, including its packet memory. DMA services are not used by the LAN91C96, virtually de-coupling network traffic from local or system bus utilization. For packet memory management, the LAN91C96 integrates a unique hardware Memory Management Unit (MMU) with enhanced performance and decreased software overhead when compared to ring buffer and linked list architectures. The LAN91C96 is portable to different CPU and bus platforms due to its flexible bus interface, flat memory structure (no pointers), and its loosely coupled buffered architecture (not sensitive to latency).

The LAN91C96 is available in 100-pin QFP and TQFP (1.0 mm body thickness) packages. The low profile TQFP is ideal for mobile applications such as PC Card LAN adapters. The LAN91C96 operates with a single power supply voltage of 5.0V. Revisions E and later will also operate using a single 3.3V power supply.

# Block Diagram

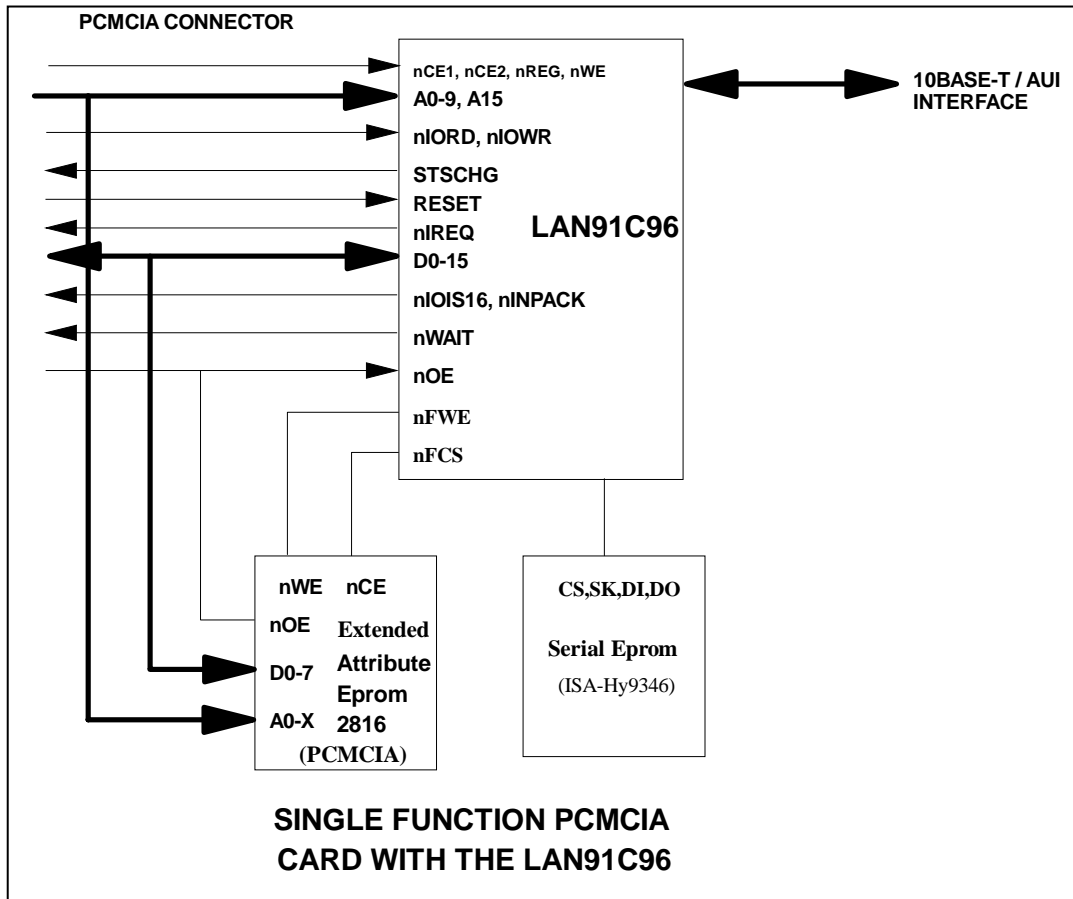


Figure 1 - LAN91C96 System Block Diagram

# Package Outlines

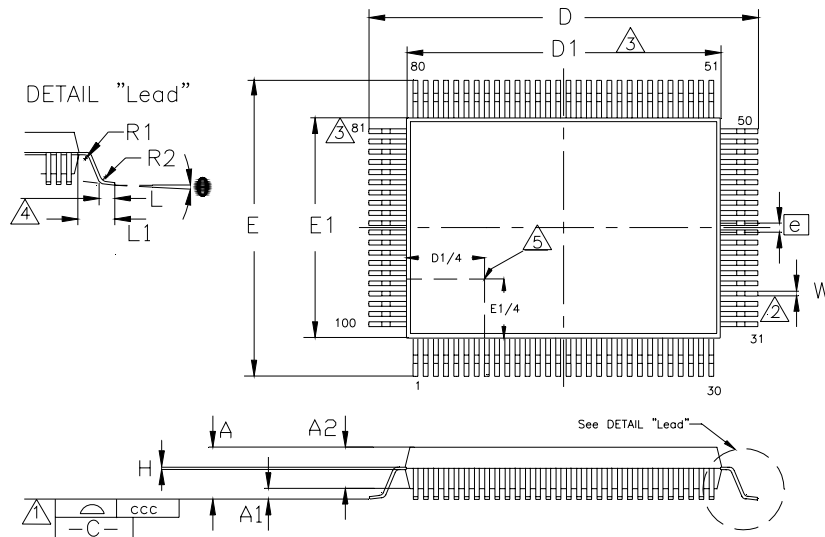
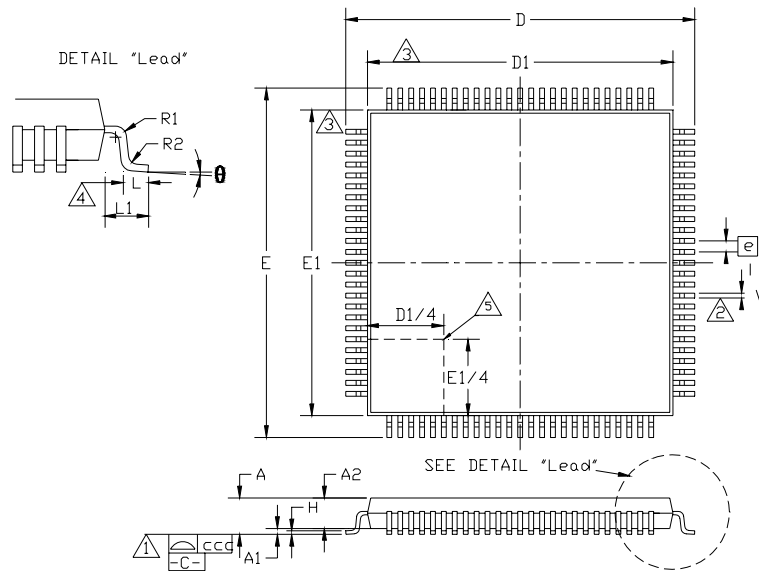


Figure 2 - 100 Pin QFP Package

	MIN	NOMINAL	MAX	REMARKS
<b>A</b>	~	~	3.4	Overall Package Height
<b>A1</b>	0.05	~	0.5	Standoff
<b>A2</b>	2.55	~	3.05	Body Thickness
<b>D</b>	23.65	~	24.15	X Span
<b>D1</b>	19.90	~	20.10	X body Size
<b>E</b>	17.65	~	18.15	Y Span
<b>E1</b>	13.90	~	14.10	Y body Size
<b>H</b>	0.11	~	0.23	Lead Frame Thickness
<b>L</b>	0.73	0.88	1.03	Lead Foot Length
<b>L1</b>	~	1.95	~	Lead Length
<b>e</b>	0.65 Basic			Lead Pitch
<b>θ</b>	0°	~	7°	Lead Foot Angle
<b>W</b>	0.20	~	0.40	Lead Width
<b>R1</b>	0.10	~	0.25	Lead Shoulder Radius
<b>R2</b>	0.15	~	0.40	Lead Foot Radius
<b>ccc</b>	~	~	0.10	Coplanarity

**Notes:**

- <sup>1</sup> Controlling Unit: millimeter.
- <sup>2</sup> Tolerance on the true position of the leads is ± 0.065 mm maximum
- <sup>3</sup> Package body dimensions D1 and E1 do not include the mold protrusion. Maximum mold protrusion is 0.25 mm.
- <sup>4</sup> Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
- <sup>5</sup> Details of pin 1 identifier are optional but must be located within the zone indicated.


**Figure 3 - 100 Pin TQFP Package**

	MIN	NOMINAL	MAX	REMARKS
<b>A</b>	~	~	1.20	Overall Package Height
<b>A1</b>	0.05	~	0.15	Standoff
<b>A2</b>	0.95	~	1.05	Body Thickness
<b>D</b>	15.80	~	16.20	X Span
<b>D1</b>	13.90	~	14.10	X body Size
<b>E</b>	15.80	~	16.20	Y Span
<b>E1</b>	13.90	~	14.10	Y body Size
<b>H</b>	0.09	~	0.20	Lead Frame Thickness
<b>L</b>	0.45	0.60	0.75	Lead Foot Length
<b>L1</b>	~	1.00	~	Lead Length
<b>e</b>	0.50 Basic			Lead Pitch
<b>θ</b>	0°	~	7°	Lead Foot Angle
<b>W</b>	0.17	0.22	0.27	Lead Width
<b>R1</b>	0.08	~	~	Lead Shoulder Radius
<b>R2</b>	0.08	~	0.20	Lead Foot Radius
<b>ccc</b>	~	~	0.08	Coplanarity

**Notes:**

- <sup>1</sup> Controlling Unit: millimeter.
- <sup>2</sup> Tolerance on the true position of the leads is  $\pm 0.04$  mm maximum.
- <sup>3</sup> Package body dimensions D1 and E1 do not include the mold protrusion.  
Maximum mold protrusion is 0.25 mm.
- <sup>4</sup> Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
- <sup>5</sup> Details of pin 1 identifier are optional but must be located within the zone indicated.

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