KSZ9893RNX

3-Port Gigabit Ethernet Switch with RGMII/MII/RMII Interface

Highlights

- Non-blocking wire-speed Ethernet switching fabric
- Full-featured forwarding and filtering control, including Access Control List (ACL) filtering
- Full VLAN and QoS support
- Two ports with integrated 10/100/1000BASE-T PHYs
- One port with 10/100/1000 Ethernet MAC and configurable RGMII/MII/RMII interface
- IEEE 802.1X port-based authentication support
- EtherGreen™ power management features, including low power standby and IEEE 802.3az
- Flexible management interface options: SPI, I^2C, MIIM, and in-band management via any port
- Commercial/Industrial temperature range support
- 64-pin VQFN (8 x 8mm) lead-free package

Target Applications

- Stand-alone 10/100/1000Mbps Ethernet switches
- VoIP infrastructure switches
- Broadband gateways/firewalls
- Wi-Fi access points
- Integrated DSL/cable modems
- Security/surveillance systems
- Industrial control/automation switches
- Networked measurement and control systems

Features

- Switch Management Capabilities
  - 10/100/1000Mbps Ethernet switch basic functions: frame buffer management, address look-up table, queue management, MIB counters
  - Non-blocking store-and-forward switch fabric assures fast packet delivery by utilizing 4096 entry forwarding table with 128kByte frame buffer
  - Jumbo packet support up to 9000 bytes
  - Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port
  - MIB counters for fully-compliant statistics gathering 34 counters per port
  - Tail tagging mode (one byte added before FCS) support at host port to inform the processor which ingress port receives the packet and its priority
  - Loopback modes for remote failure diagnostics
  - Rapid spanning tree protocol (RSTP) support for topology management and ring/linear recovery
  - Multiple spanning tree protocol (MSTP) support
- Two Integrated PHY Ports
  - 1000BASE-T/100BASE-TX/10BASE-T IEEE 802.3
  - Fast Link-up option significantly reduces link-up time
  - Auto-negotiation and Auto-MDI/MDI-X support
  - Energy-Efficient Ethernet (EEE) support with low-power idle mode and clock stoppage
  - On-chip termination resistors and internal biasing for differential pairs to reduce power
  - LinkMD® cable diagnostic capabilities for determining cable opens, shorts, and length
- One Configurable External MAC Port
  - Reduced Gigabit Media Independent Interface (RGMII) v2.0
  - Reduced Media Independent Interface (RMII) v1.2 with 50MHz reference clock input/output option
  - Media Independent Interface (MII) in PHY/MAC mode
- Advanced Switch Capabilities
  - IEEE 802.1Q VLAN support for 128 active VLAN groups and the full range of 4096 VLAN IDs
  - IEEE 802.1p/Q tag insertion/removal on per port basis
  - VLAN ID tag/untag options on per port or VLAN basis
  - IEEE 802.3x full-duplex flow control and half-duplex back pressure collision control
  - IEEE 802.1X (Port-Based Network Access Control)
  - IGMP v1/v2/v3 snooping for multicast packet filtering
  - IPv6 multicast listener discovery (MLD) snooping
  - IPv4/IPv6 QoS support, QoS/CoS packet prioritization
  - 802.1p QoS packet classification with 4 priority queues
  - Programmable rate limiting at ingress/egress ports
  - Broadcast storm protection
  - Four priority queues with dynamic packet mapping for IEEE 802.1p, IPv4 DIFFSERV, IPv6 Traffic Class
  - MAC filtering function to filter or forward unknown unicast, multicast and VLAN packets
  - Self-address filtering for implementing ring topologies
- Comprehensive Configuration Registers Access
  - High-speed 4-wire SPI (up to 50MHz), I^2C interfaces provide access to all internal registers
  - MII Management (MIIM, MDC/MDIO 2-wire) Interface provides access to all PHY registers
  - In-band management via any of the three ports
  - I/O pin strapping facility to set certain register bits from I/O pins at reset time
  - On-the-fly configurable control registers
- Power Management
  - IEEE 802.3az Energy Efficient Ethernet (EEE)
  - Energy detect power-down mode on cable disconnect
  - Dynamic clock tree control
  - Unused ports can be individually powered down
  - Full-chip software power-down
  - Wake-on-LAN (WoL) standby power mode

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1.0 INTRODUCTION

1.1 General Description

The KSZ9893RNX is a highly-integrated, IEEE 802.3 compliant networking device that incorporates a layer-2+ managed Gigabit Ethernet switch, two 10BASE-T/100BASE-TX/1000BASE-T physical layer transceivers (PHYs) and associated MAC units, and one MAC port with a configurable RGMII/MII/RMII interface for direct connection to a host processor/controller, another Ethernet switch, or an Ethernet PHY transceiver.

The KSZ9893RNX is built upon industry-leading Ethernet technology, with features designed to offload host processing and streamline the overall design:

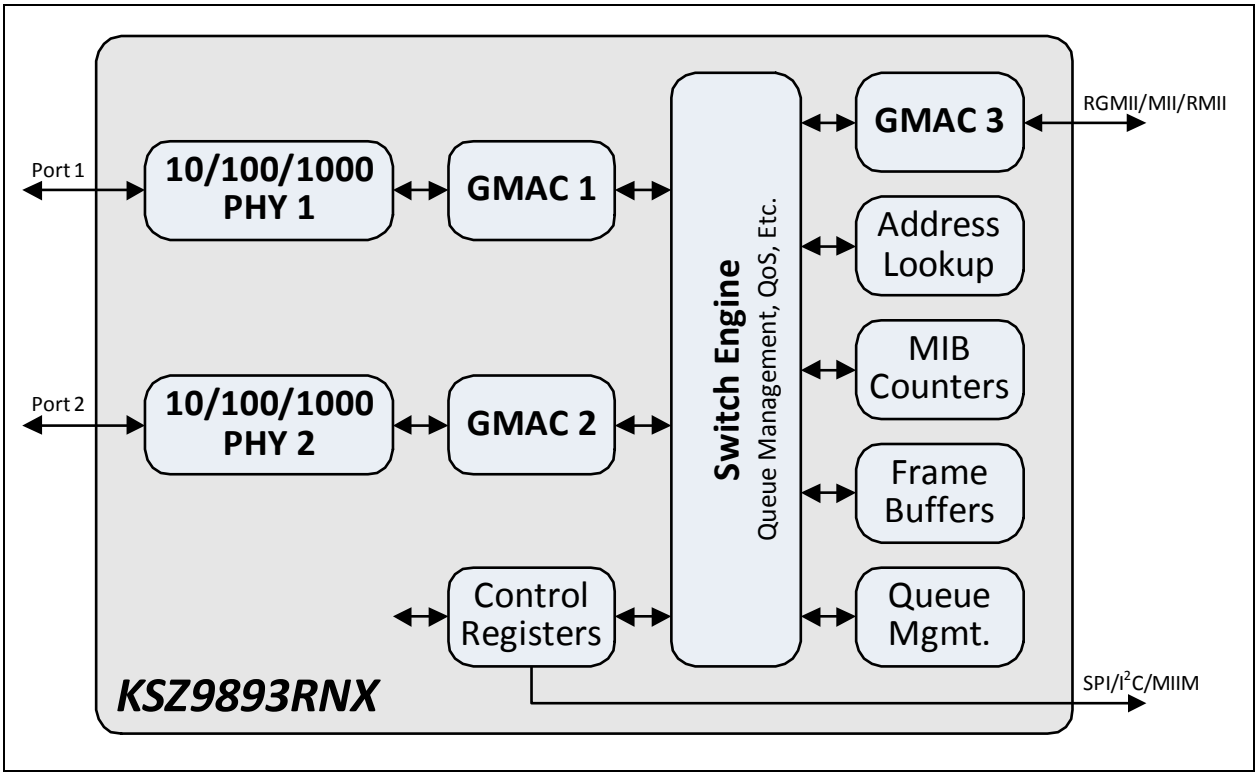
- Non-blocking wire-speed Ethernet switch fabric
- Full-featured forwarding and filtering control, including port-based Access Control List (ACL) filtering
- Full VLAN and QoS support
- Traffic prioritization with per-port ingress/egress queues and by traffic classification
- Spanning Tree support for RSTP and MSTP
- IEEE 802.1X port-based authentication support

A host processor can access all KSZ9893RNX registers for control over all PHY, MAC, and switch functions. Full register access is available via the integrated SPI or I^2C interfaces, and by in-band management via any one of the data ports. PHY register access is provided by a MIIM interface. Flexible digital I/O voltage allows the MAC port to interface directly with a 1.8/2.5/3.3V host processor/controller/FPGA.

Additionally, a robust assortment of power-management features including IEEE 802.3az Energy-Efficient Ethernet (EEE) for power savings with idle link, and Wake-on-LAN (WoL) for low power standby operation, have been designed to satisfy energy-efficient system requirements.

The KSZ9893RNX is available in commercial (0°C to +70°C) and industrial (-40°C to +85°C) temperature ranges. An internal block diagram of the KSZ9893RNX is shown in Figure 1-1.

FIGURE 1-1: INTERNAL BLOCK DIAGRAM



2.0 PACKAGE INFORMATION

2.1 Package Drawings

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

FIGURE 2-1: PACKAGE (DRAWING)

64-Lead Very Thin Plastic Quad Flat, No Lead Package (JXX) - 8x8 mm Body [VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

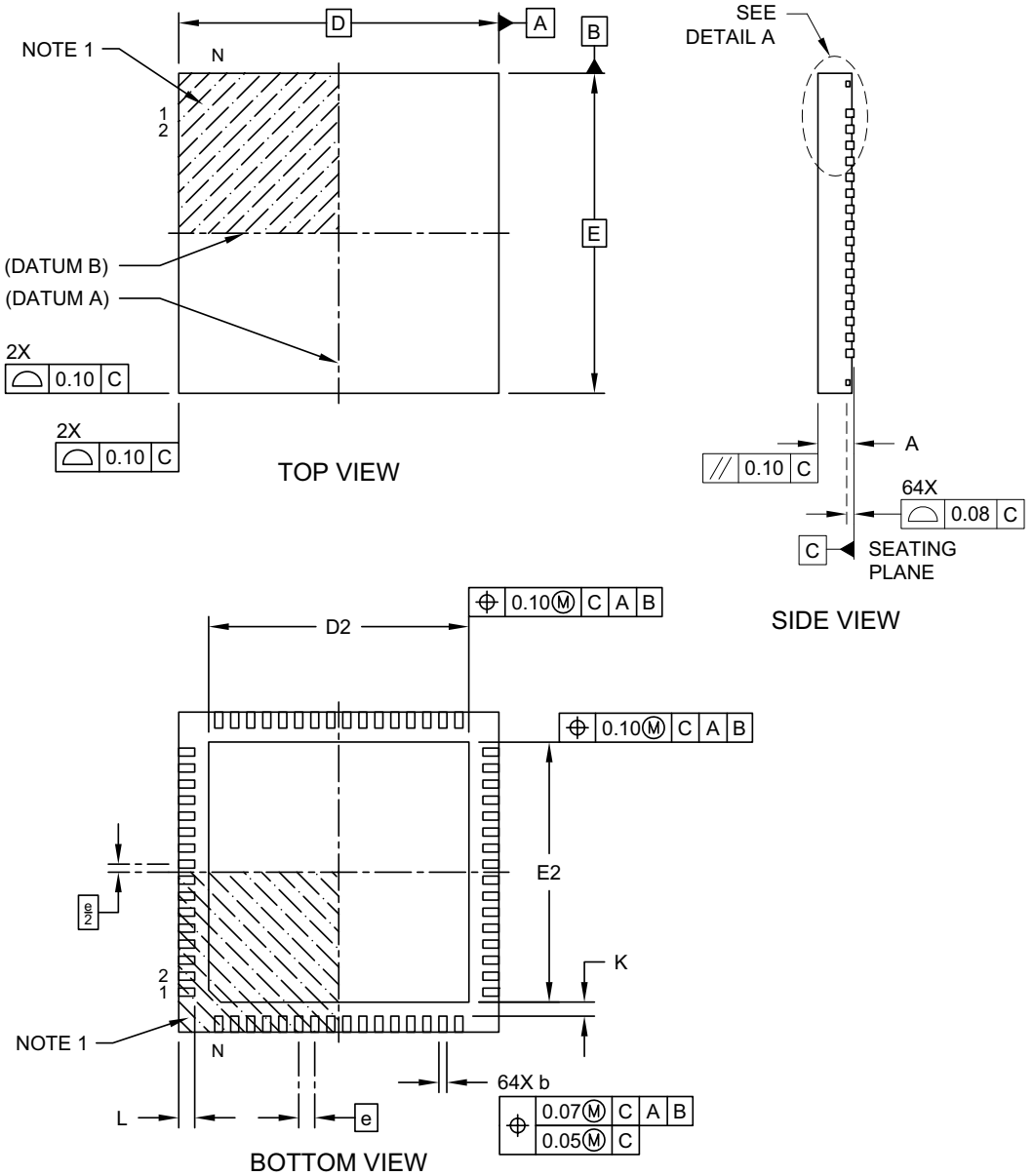


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FIGURE 2-2: PACKAGE (DIMENSIONS)

64-Lead Very Thin Plastic Quad Flat, No Lead Package (JXX) - 8x8 mm Body [VQFN]

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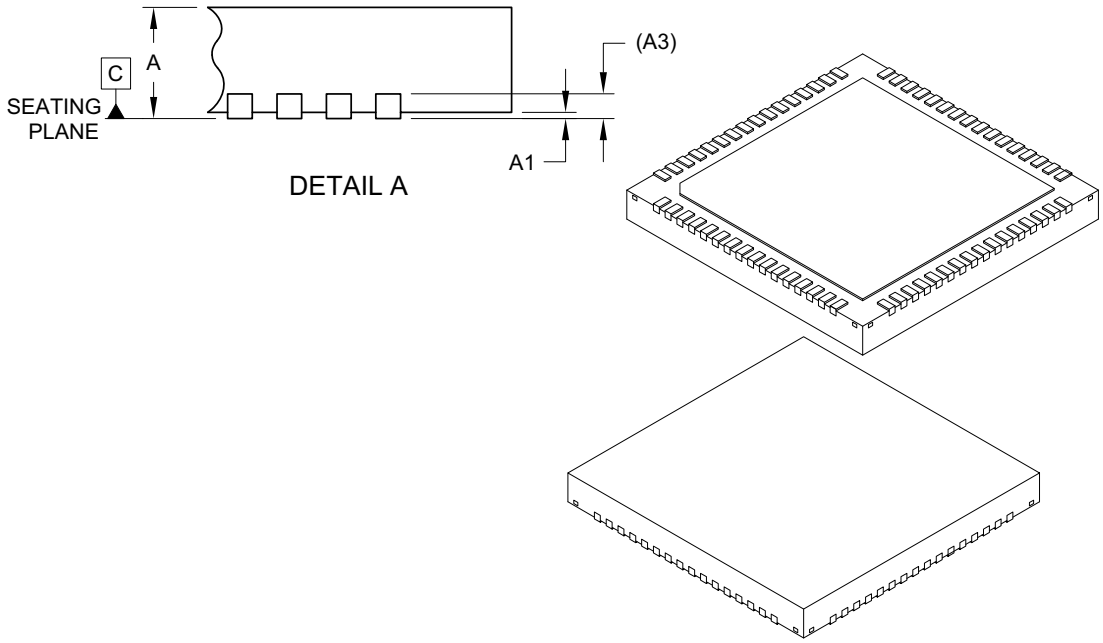

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		64	
Pitch	e		0.40 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.40	6.50	6.60
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.40	6.50	6.60
Terminal Width	b	0.15	0.20	0.25
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.25	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-437A Sheet 2 of 2

FIGURE 2-3: PACKAGE (LAND PATTERN)

64-Lead Very Thin Plastic Quad Flat, No Lead Package (JXX) - 8x8 mm Body [VQFN]

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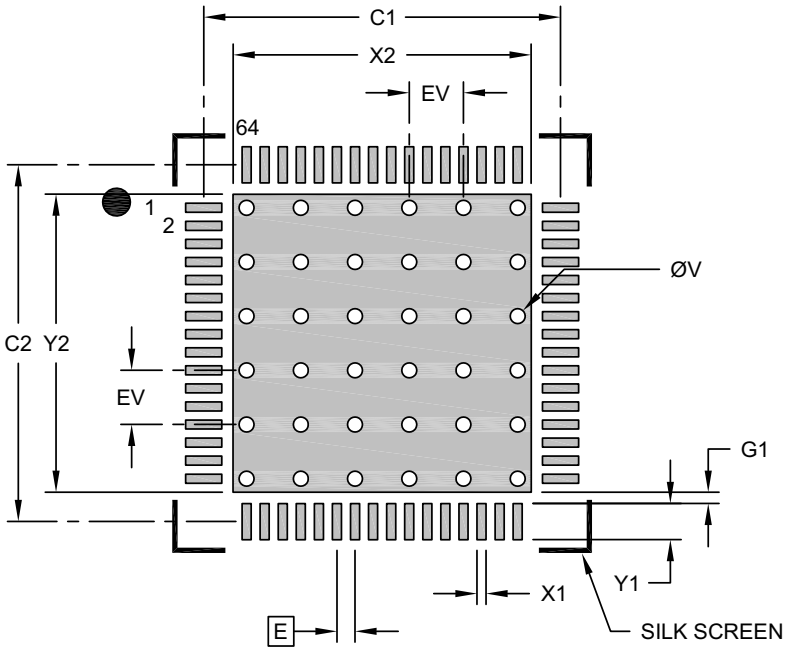

RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			6.60
Optional Center Pad Length	Y2			6.60
Contact Pad Spacing	C1		7.90	
Contact Pad Spacing	C2		7.90	
Contact Pad Width (X64)	X1			0.20
Contact Pad Length (X64)	Y1			0.80
Contact Pad to Center Pad (X64)	G1	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2437A

APPENDIX A: PRODUCT BRIEF REVISION HISTORY

TABLE A-1: REVISION HISTORY

Revision	Section/Figure/Entry	Correction
DS00002318A (12-16-16)	Initial Document Release	

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PART NO.	XX	X	[XX](1)
Device	Package	Temp. Range	Tape & Reel Option

Device:	KSZ9893R = 3-Port Switch with 1 RGMII/MII/RMII Interface	
Package:	NX	= 64-pin VQFN
Temperature Range:	C	= 0°C to +70°C (Commercial)
	I	= -40°C to +85°C (Industrial)
Tape and Reel Option:	Blank	= Standard packaging (tray)
	-TR	= Tape and Reel (Note 1)

Examples:

a) KSZ9893RNXC
64-pin VQFN package,
Commercial temperature,
Standard packaging

b) KSZ9893RNXI-TR
64-pin VQFN package,
Industrial temperature,
Tape and reel

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