# 32-Channel Serial to Parallel Converter With High Voltage Push-Pull Outputs

## Features

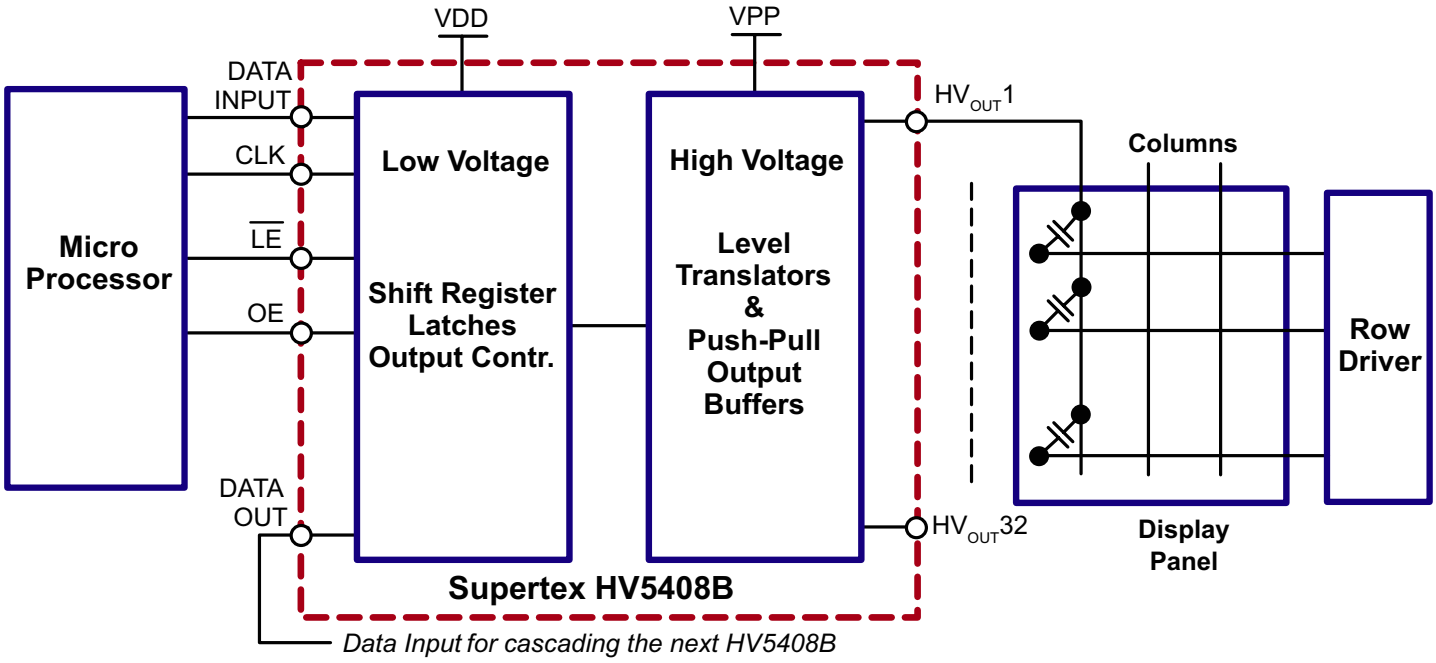
- Processed with HVCMOS® technology
- Low power level shifting
- SOURCE/SINK current minimum 20mA
- Shift register speed 8.0MHz
- Latched data outputs
- CMOS compatible inputs
- Forward and reverse shifting options
- Diode to VPP allows efficient power recovery

## General Description

The HV5408B is a low voltage serial to high voltage parallel converter with push-pull outputs. This device has been designed for use as a driver for AC-electroluminescent displays. It can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities, such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

The HV5408B consists of a 32-bit shift register, 32 latches, and control logic to enable outputs. Q1 is connected to the first stage of the shift register through the Output Enable logic. Data is shifted through the shift register on the low to high transition of the clock. When viewed from the top of the package, the HV5408B shifts in the counter-clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (32). Operation of the shift register is not affected by the $\overline{LE}$ (latch enable) or the OE (output enable) inputs. Transfer of data from the shift register to the latch occurs when the $\overline{LE}$ input is high. The data in the latch is retained when $\overline{LE}$ is low.

## Typical Application Circuit



## Ordering Information

| Device | Package Options | | |
|---|---|---|---|
| | **44-Lead Quad Cerpac**<br>*.650x.650in body*<br>*.190in height (max)*<br>*.050in pitch* | **44-Lead PQFP**<br>*10.00x10.00mm body*<br>*2.35mm height (max)*<br>*0.80mm pitch* | **44-Lead PLCC**<br>*.653x.653in body*<br>*.180in height (max)*<br>*.050in pitch* |
| HV5408B | HV5408DJ-B* | HV5408PG-B-G | HV5408PJ-B-G |

*-G indicates package is RoHS compliant ('Green').*
** Hi-Rel process flow available.*

## Absolute Maximum Ratings

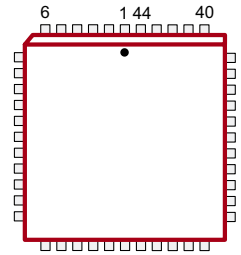
| Parameter | Value |
|---|---|
| Supply voltage, $V_{DD}$ | -0.5V to +16V |
| Supply voltage, $V_{PP}$ | -0.5V to +90V |
| Logic input levels | -0.5V to $V_{DD}$ +0.5V |
| Ground current[1] | 1.5A |
| Continuous total power dissipation[2]<br>Plastic<br>Ceramic | <br>1200mW<br>1500mW |
| Operating temperature range<br>Plastic<br>Ceramic | <br>-40°C to +85°C<br>-55°C to +125°C |
| Storage temperature range | -65°C to +150°C |

*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.*

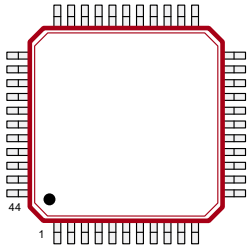
***Notes:***

1. *Duty cycle is limited by the total power dissipated in the package.*
2. *For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic and at 15mW/°C for ceramic.*

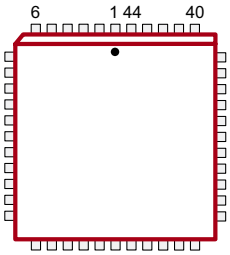
## Pin Configurations




**44-Lead Quad Cerpac (DJ)**
***(top view)***

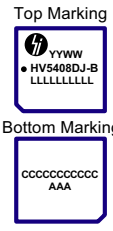



**44-Lead PQFP (PG)**
***(top view)***



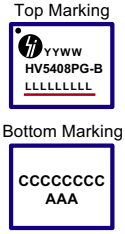

**44-Lead PLCC (PJ)**
***(top view)***

## Product Marking




YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
**May be part of top marking*

**44-Lead Quad Cerpac (DJ)**




YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
_____ = "Green" Packaging
**May be part of top marking*

**44-Lead PQFP (PG)**


YY = Year Sealed
WW = Week Sealed
L = Lot Number
A = Assembler ID
C = Country of Origin*
_____ = "Green" Packaging
**May be part of top marking*

**44-Lead PLCC (PJ)**

*Packages may or may not include the following marks: Si or*

## Recommended Operating Conditions *(over -40°C to 85°C for plastic and -55°C to 125°C for ceramic)*

| Sym | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ | Logic voltage supply | 10.8 | 13.2 | V |
| $V_{PP}$ | High voltage supply | 8.0 | 80 | V |
| $V_{IH}$ | Input high voltage | $V_{DD}$ - 2.0 | $V_{DD}$ | V |
| $V_{IL}$ | Input low voltage | 0 | 2.0 | V |
| $f_{CLK}$ | Clock frequency | 0 | 8.0 | MHz |

## Power-Up Sequence

***Power-up sequence should be the following:***

1. *Connect ground*
2. *Apply $V_{DD}$*
3. *Set all inputs (Data, CLK, $\overline{LE}$, etc.) to a known state*
4. *Apply $V_{PP}$*
5. *The $V_{PP}$ should not fall below $V_{DD}$ or float during operation.*

***Power-down sequence should be the reverse of the above.***

## Electrical Characteristics *($V_{PP}$ = 60V, $V_{DD}$ = 12V, $T_A$ = 25°C)*

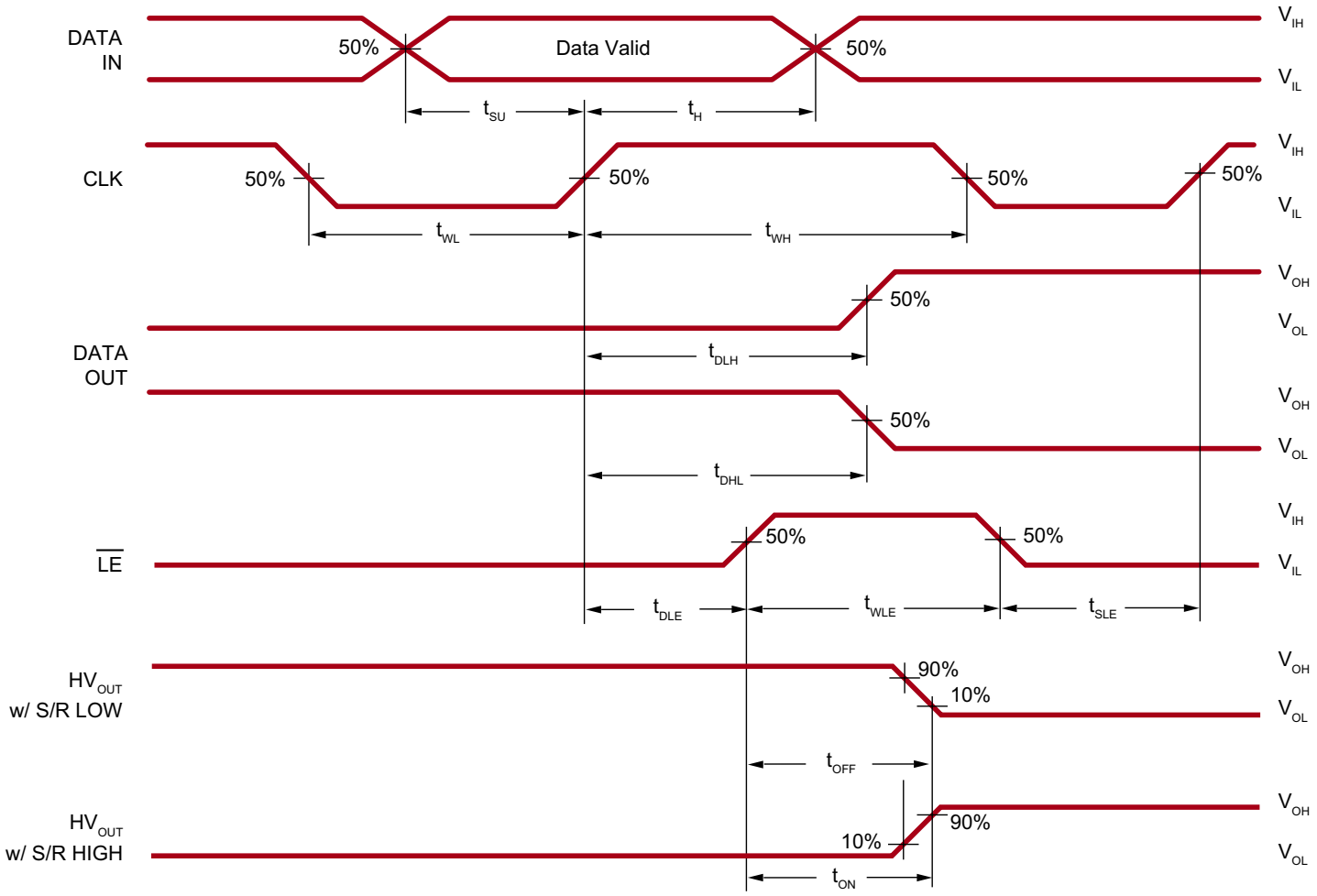
### DC Characteristics

| Sym | Parameter | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $I_{PP}$ | $V_{PP}$ supply current | - | 0.5 | mA | $HV_{OUTPUTS}$ high to low |
| $I_{DDQ}$ | $I_{DD}$ supply current (quiescent) | - | 100 | µA | All inputs = $V_{DD}$ or GND |
| $I_{DD}$ | $I_{DD}$ supply current (operating) | - | 15 | mA | $V_{DD}$ = $V_{DD}$ max, $f_{CLK}$ = 8.0MHz |
| $V_{OH}$ (data) | Shift register output voltage | 10.5 | - | V | $I_O$ = -100µA |
| $V_{OL}$ (data) | Shift register output voltage | - | 1.0 | V | $I_O$ = 100µA |
| $I_{IH}$ | Current leakage, any input | - | 1.0 | µA | $V_{IN}$ = $V_{DD}$ |
| $I_{IL}$ | Current leakage, any input | - | -1.0 | µA | $V_{IN}$ = 0 |
| $V_{OC}$ | HV output clamp diode voltage | - | -1.5 | V | $I_{OL}$ = -100mA |
| $V_{OH}$ | HV output when sourcing | 52 | - | V | $I_{OH}$ = -20mA, -40 to 85°C |
| $V_{OL}$ | HV output when sinking | - | 8.0 | V | $I_{OL}$ = 20mA, -40 to 85°C |
| $V_{OH}$ | HV output when sourcing | 52 | - | V | $I_{OH}$ = -15mA, -55 to 125°C |
| $V_{OL}$ | HV output when sinking | - | 8.0 | V | $I_{OL}$ = 15mA, -55 to 125°C |

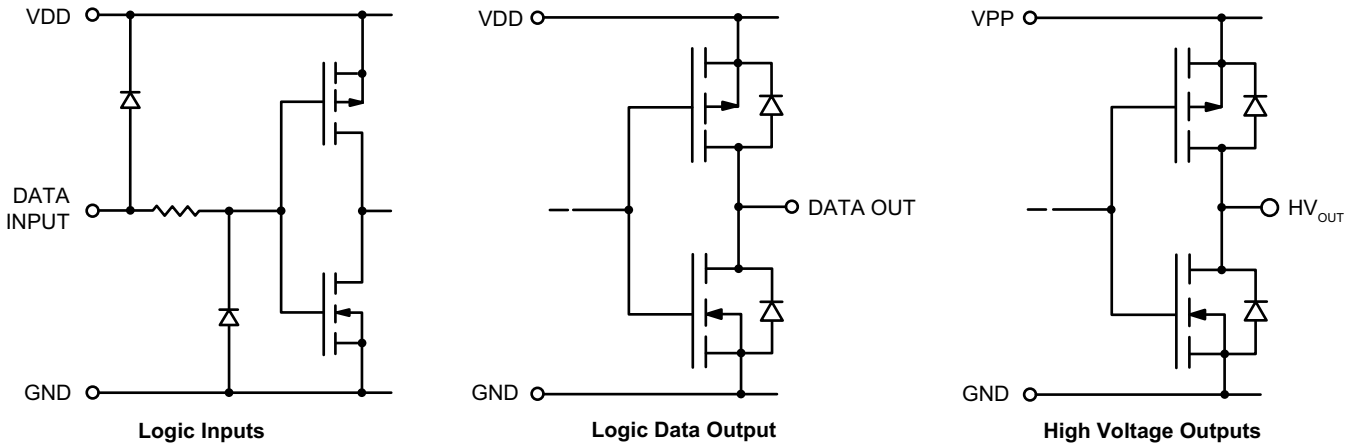
## AC Characteristics

| Sym | Parameter | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $f_{CLK}$ | Clock frequency | - | 8.0 | MHz | --- |
| $t_{WL}$ or $t_{WH}$ | Clock width, HIGH or LOW | 62 | - | ns | --- |
| $t_{SU}$ | Setup time before CLK rises | 25 | - | ns | --- |
| $t_{H}$ | Hold time after CLK rises | 10 | - | ns | --- |
| $t_{DLH}$ (data) | Data output delay after L to H CLK | - | 110 | ns | $C_L$ = 15pF |
| $t_{DHL}$ (data) | Data output delay after H to L CLK | - | 110 | ns | $C_L$ = 15pF |
| $t_{DLE}$ | $\overline{LE}$ delay after L to H CLK | 50 | - | ns | --- |
| $t_{WLE}$ | Width of $\overline{LE}$ pulse | 50 | - | ns | --- |
| $t_{SLE}$ | $\overline{LE}$ setup time before L to H CLK | 50 | - | ns | --- |
| $t_{ON}$ | Delay from $\overline{LE}$ to $HV_{OUT}$, L to H | - | 500 | ns | --- |
| $t_{OFF}$ | Delay from $\overline{LE}$ to $HV_{OUT}$, H to L | - | 500 | ns | --- |

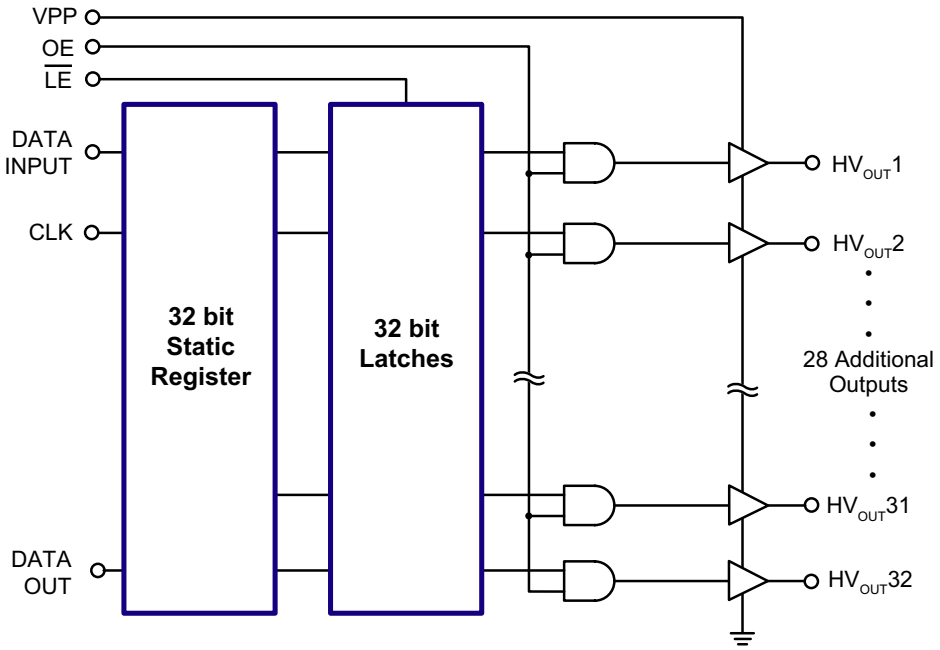
## Switching Waveforms



## Input and Output Equivalent Circuits




## Functional Block Diagram




## Function Tables

| DATA INPUT | CLK* | DATA OUT |
|---|---|---|
| H | ↑ | H |
| L | ↑ | L |
| X | No ↑ | No change |

***Note:***

** ↑ = LOW - to - HIGH transition*

*H = High*
*L = Low*
*X = Don't Care*

| DATA INPUT | $\overline{LE}$ | OE | HV OUT |
|---|---|---|---|
| X | X | L | All HV$_{OUT}$ = LOW |
| X | L | H | Previous latched data |
| H | H | H | H |
| L | H | H | L |

## 44-Lead PQFP Pin Assignment (PG)

| Pin | Function | Description |
|---|---|---|
| 1 | $HV_{OUT}11$ | High voltage outputs.<br><br>High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to GND, or to $V_{PP}$ rail levels. |
| 2 | $HV_{OUT}12$ | |
| 3 | $HV_{OUT}13$ | |
| 4 | $HV_{OUT}14$ | |
| 5 | $HV_{OUT}15$ | |
| 6 | $HV_{OUT}16$ | |
| 7 | $HV_{OUT}17$ | |
| 8 | $HV_{OUT}18$ | |
| 9 | $HV_{OUT}19$ | |
| 10 | $HV_{OUT}20$ | |
| 11 | $HV_{OUT}21$ | |
| 12 | $HV_{OUT}22$ | |
| 13 | $HV_{OUT}23$ | |
| 14 | $HV_{OUT}24$ | |
| 15 | $HV_{OUT}25$ | |
| 16 | $HV_{OUT}26$ | |
| 17 | $HV_{OUT}27$ | |
| 18 | $HV_{OUT}28$ | |
| 19 | $HV_{OUT}29$ | |
| 20 | $HV_{OUT}30$ | |
| 21 | $HV_{OUT}31$ | |
| 22 | $HV_{OUT}32$ | |
| 23 | DATA OUT | Serial data output.<br><br>Data output for cascading to the data input of the next device. |
| 24 | N/C | No connect. |
| 25 | | |
| 26 | | |
| 27 | CLK | Data shift register clock<br><br>Input are shifted into the shift register on the positive edge of the clock. |
| 28 | GND | Logic and high voltage ground. |
| 29 | VPP | High voltage power rail. |
| 30 | VDD | Low voltage logic power rail. |

## 44-Lead PQFP Pin Assignment (PG)

| Pin | Function | Description |
|---|---|---|
| 31 | $\overline{LE}$ | Latch enable input.<br><br>When $\overline{LE}$ is HIGH, shift register data is transferred into a data latch. When $\overline{LE}$ is LOW, data is latched, and new data can be clocked into the shift register. |
| 32 | DATA IN | Serial data input.<br><br>Data needs to be present before each rising edge of the clock. |
| 33 | OE | Output enable input.<br><br>When OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched. |
| 34 | N/C | No connect. |
| 35 | $HV_{OUT}1$ | High voltage outputs.<br><br>High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to GND, or to $V_{PP}$ rail levels. |
| 36 | $HV_{OUT}2$ | |
| 37 | $HV_{OUT}3$ | |
| 38 | $HV_{OUT}4$ | |
| 39 | $HV_{OUT}5$ | |
| 40 | $HV_{OUT}6$ | |
| 41 | $HV_{OUT}7$ | |
| 42 | $HV_{OUT}8$ | |
| 43 | $HV_{OUT}9$ | |
| 44 | $HV_{OUT}10$ | |

## 44-Lead Quad Cerpac/PLCC Pin Assignment (DJ/PJ)

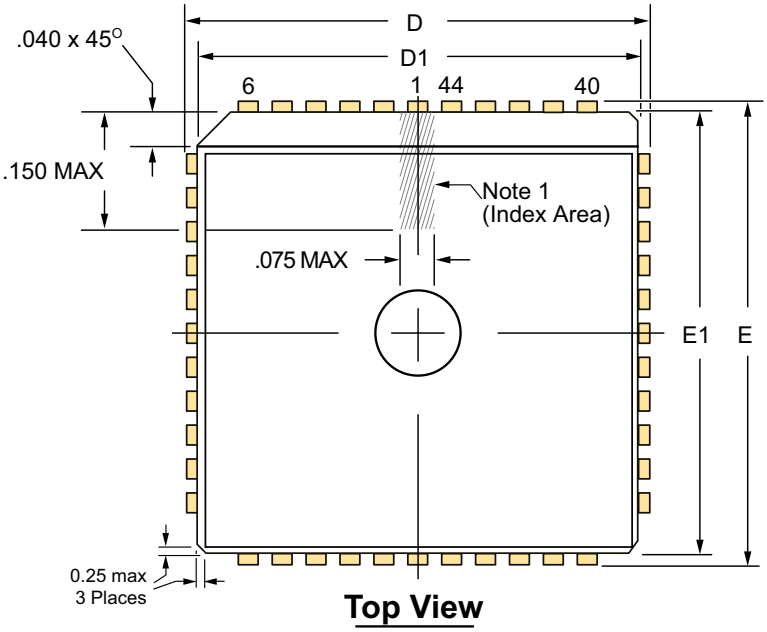
| Pin | Function | Description |
|---|---|---|
| 1 | $HV_{OUT}16$ | High voltage outputs.<br><br>High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to GND, or to $V_{PP}$ rail levels. |
| 2 | $HV_{OUT}17$ | |
| 3 | $HV_{OUT}18$ | |
| 4 | $HV_{OUT}19$ | |
| 5 | $HV_{OUT}20$ | |
| 6 | $HV_{OUT}21$ | |
| 7 | $HV_{OUT}22$ | |
| 8 | $HV_{OUT}23$ | |
| 9 | $HV_{OUT}24$ | |
| 10 | $HV_{OUT}25$ | |
| 11 | $HV_{OUT}26$ | |
| 12 | $HV_{OUT}27$ | |
| 13 | $HV_{OUT}28$ | |
| 14 | $HV_{OUT}29$ | |
| 15 | $HV_{OUT}30$ | |
| 16 | $HV_{OUT}31$ | |
| 17 | $HV_{OUT}32$ | |
| 18 | DATA OUT | Serial data output.<br><br>Data output for cascading to the data input of the next device. |
| 19 | N/C | No connect. |
| 20 | | |
| 21 | | |
| 22 | CLK | Data shift register clock<br><br>Input are shifted into the shift register on the positive edge of the clock. |
| 23 | GND | Logic and high voltage ground. |
| 24 | VPP | High voltage power rail. |
| 25 | VDD | Low voltage logic power rail. |
| 26 | $\overline{LE}$ | Latch enable input.<br><br>When $\overline{LE}$ is HIGH, shift register data is transferred into a data latch. When $\overline{LE}$ is LOW, data is latched, and new data can be clocked into the shift register. |
| 27 | DATA IN | Serial data input.<br><br>Data needs to be present before each rising edge of the clock. |

## 44-Lead Quad Cerpac/PLCC Pin Assignment (DJ/PJ)

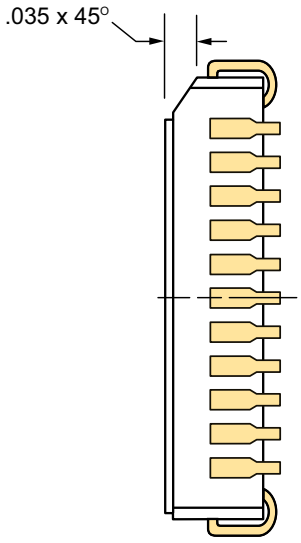
| Pin | Function | Description |
|---|---|---|
| 28 | OE | Output enable input.<br><br>When OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched. |
| 29 | N/C | No connect. |
| 30 | $HV_{OUT}1$ | High voltage outputs.<br><br>High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to GND, or to $V_{PP}$ rail levels. |
| 31 | $HV_{OUT}2$ | |
| 32 | $HV_{OUT}3$ | |
| 33 | $HV_{OUT}4$ | |
| 34 | $HV_{OUT}5$ | |
| 35 | $HV_{OUT}6$ | |
| 36 | $HV_{OUT}7$ | |
| 37 | $HV_{OUT}8$ | |
| 38 | $HV_{OUT}9$ | |
| 39 | $HV_{OUT}10$ | |
| 40 | $HV_{OUT}11$ | |
| 41 | $HV_{OUT}12$ | |
| 42 | $HV_{OUT}13$ | |
| 43 | $HV_{OUT}14$ | |
| 44 | $HV_{OUT}15$ | |

# 44-Lead Quad Cerpac Package Outline (DJ)

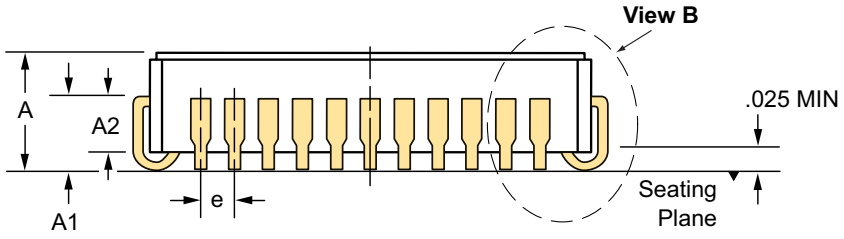
***.650x.650in body, .190in height (max), .050in pitch***



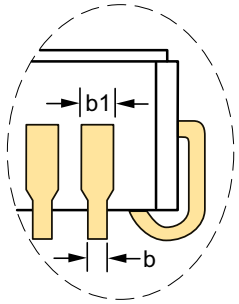

**Top View**




**Vertical Side View**




**Horizontal Side View**




**View B**

***Note:***

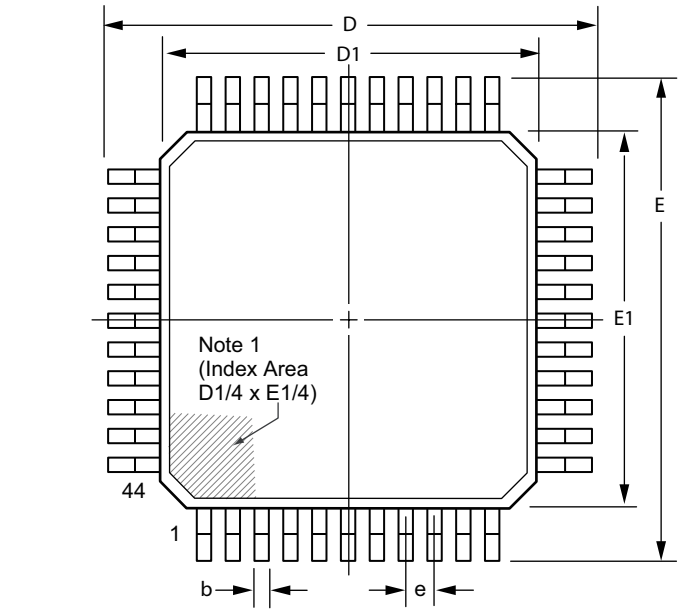
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

| Symbol | | A | A1 | A2 | b | b1 | D | D1 | E | E1 | e |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (inches) | MIN | .155 | .090 | .060 REF | .017 | .026 | .685 | .630 | .685 | .630 | .050 BSC |
| | NOM | .172 | .100 | | .019 | .029 | .690 | .650 | .690 | .650 | |
| | MAX | .190 | .120 | | .021 | .032 | .695 | .665 | .695 | .665 | |

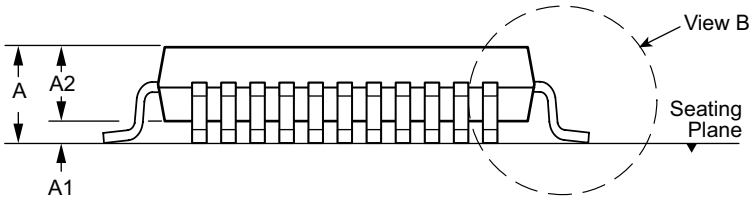
*JEDEC Registration MO-087, Variation AB, Issue B, August, 1991.*
***Drawings not to scale.***
***Supertex Doc. #:*** *DSPD-44CERPACDJ, Version D090808.*

# 44-Lead PQFP Package Outline (PG)

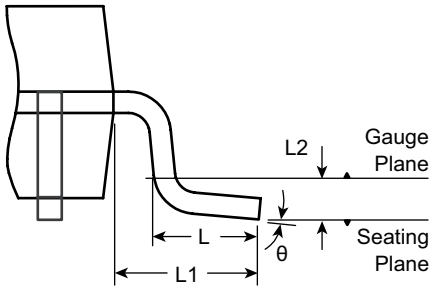
***10.00x10.00mm body, 2.35mm height (max), 0.80mm pitch***




**Top View**




**Side View**




**View B**

***Note:***

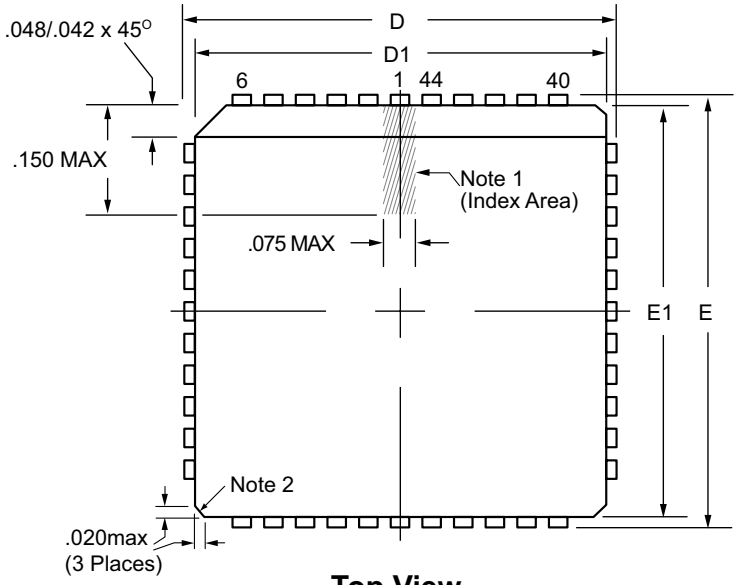
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

| Symbol | | A | A1 | A2 | b | D | D1 | E | E1 | e | L | L1 | L2 | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (mm) | MIN | 1.95* | 0.00 | 1.95 | 0.30 | 13.65* | 9.80* | 13.65* | 9.80* | 0.80 BSC | 0.73 | 1.95 REF | 0.25 BSC | 0° |
| | NOM | - | - | 2.00 | - | 13.90 | 10.00 | 13.90 | 10.00 | | 0.88 | | | 3.5° |
| | MAX | 2.35 | 0.25 | 2.10 | 0.45 | 14.15* | 10.20* | 14.15* | 10.20* | | 1.03 | | | 7° |

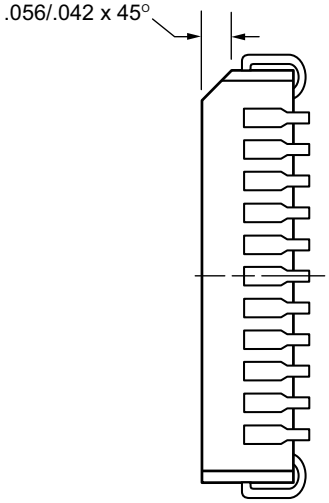
*JEDEC Registration MO-112, Variation AA-2, Issue B, Sep.1995.*
** This dimension is not specified in the JEDEC drawing.*
***Drawings not to scale.***
***Supertex** Doc. #: DSPD-44PQFPPG, Version C041309.*

# 44-Lead PLCC Package Outline (PJ)

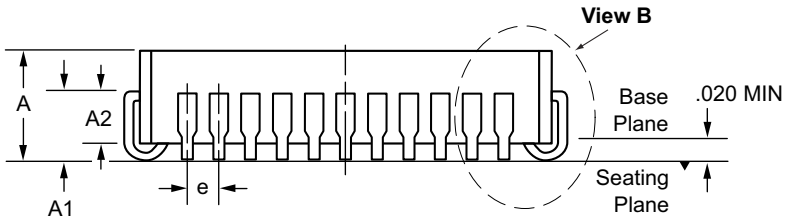
## *.653x.653in body, .180in height (max), .050in pitch*



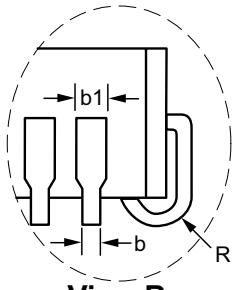

**Top View**




**Vertical Side View**




**Horizontal Side View**




**View B**

***Notes:***

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Actual shape of this feature may vary.*

| Symbol | | A | A1 | A2 | b | b1 | D | D1 | E | E1 | e | R |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Dimension (inches) | MIN | .165 | .090 | .062 | .013 | .026 | .685 | .650 | .685 | .650 | .050 BSC | .025 |
| | NOM | .172 | .105 | - | - | - | .690 | .653 | .690 | .653 | | .035 |
| | MAX | .180 | .120 | .083 | .021 | .036† | .695 | .656 | .695 | .656 | | .045 |

*JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.*
*† This dimension differs from the JEDEC drawing.*
***Drawings not to scale.***
***Supertex Doc. #:*** *DSPD-44PLCCPJ, Version F031111.*

*(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)*

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