

- ESD performance
 - HBM: 1 kV
 - MM: 200 V
 - CDM: 1 kV

Applications

- Automotive
- Industrial
- Computer
- Consumer

Features

- Medium-speed operation
 $t_{PD} = 30 \text{ ns}$ (typ.) at 10 V
- Standardized symmetrical output characteristics
- Quiescent current specified up to 20 V
- 5 V, 10 V, and 15 V parametric ratings
- Input leakage current $I_I = 100 \text{ nA}$ (max.) at $V_{DD} = 18 \text{ V}$ and $T_A = 25 \text{ }^\circ\text{C}$
- 100 % tested for quiescent current

Description

The HCF4069U is a monolithic integrated circuit fabricated in metal oxide semiconductor technology available in the SO14 package. The HCF4069U consists of six COS/MOS inverter circuits. This device is intended for all general purpose inverter applications where the medium power TTL-drive and logic level conversion capabilities of circuits such as HCF4049 hex inverter/buffers are not required.

Table 1. Device summary table

Order code	Temperature range	Package	Packing	Marking
HCF4069UM013TR	-55 ° C to +125 ° C	SO14	Tape and reel	HCF4069U
HCF4069YUM013TR (1)	-40 ° C to +125 ° C	SO14 (automotive grade) ⁽¹⁾		HCF4069Y

1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.

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1 Pin information

Figure 1. Pin connections (top view)

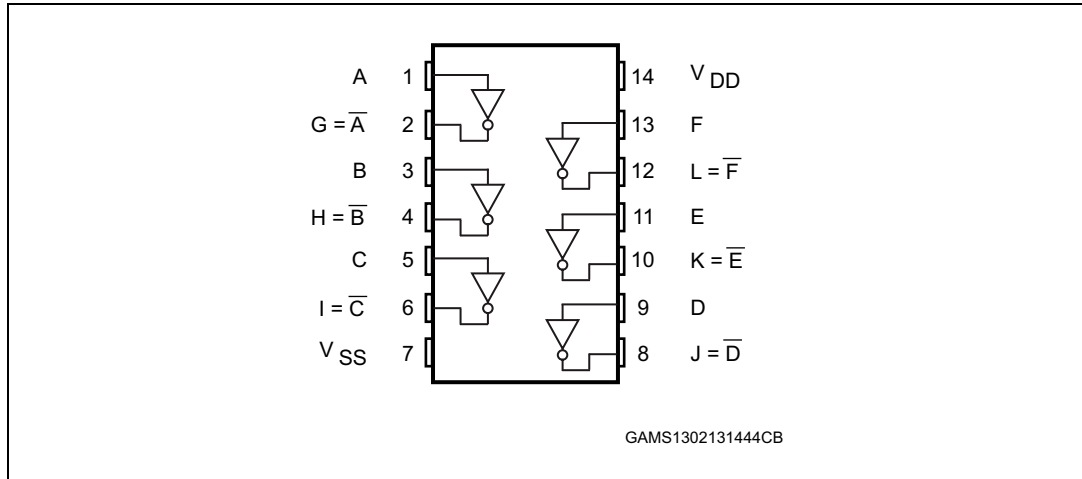


Table 2. Pin description

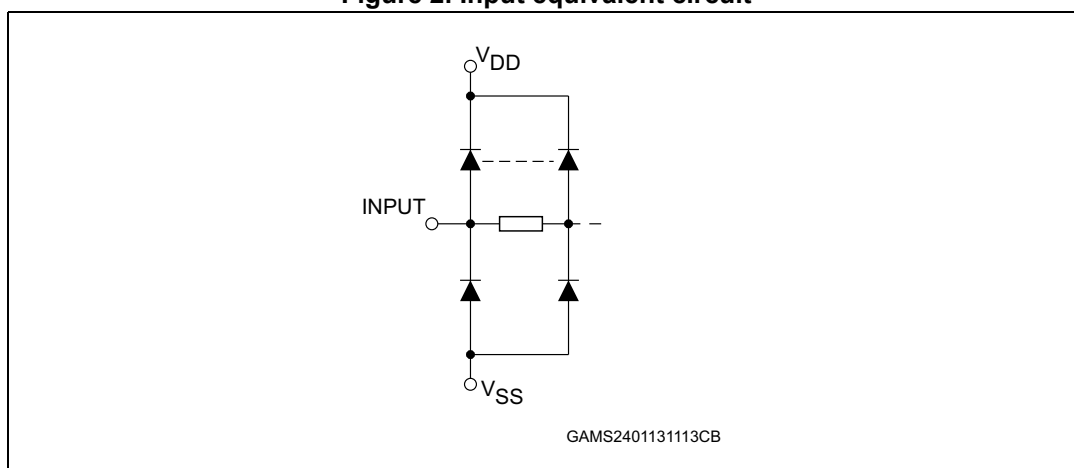
Pin no	Symbol	Name and function
1, 3, 5, 9, 11, 13	A, B, C, D, E, F	Data inputs
2, 4, 6, 8, 10, 12	G, H, I, J, K, L	Data outputs
7	V _{SS}	Negative supply voltage
14	V _{DD}	Positive supply voltage

2 Functional description

Table 3. Truth table

Inputs	Outputs
A, B, C, D, E, F	G, H, I, J, K, L
L	H
H	L

Figure 2. Input equivalent circuit



3 Electrical characteristics

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltage values are referred to V_{SS} pin voltage.

Table 4. Absolute maximum ratings (AMR)

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	-0.5 to +22	V
V_I	DC input voltage	-0.5 to $V_{DD} + 0.5$	
I_I	DC input current	± 10	mA
P_D	Power dissipation per package	200	mW
	Power dissipation per output transistor	100	
T_{op}	Operating temperature	-55 to +125	°C
T_{stg}	Storage temperature	-65 to +150	

Table 5. Recommended operating conditions

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	3 to 20	V
V_I	Input voltage	0 to V_{DD}	
T_{op}	Operating temperature	-55 to 125	°C

Table 6. DC specifications⁽¹⁾

Sym.	Parameter	Test condition				Value						Unit	
		V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _A = 25 °C			-40 to 85 °C		-55 to 125 °C		
						Min.	Typ.	Max.	Min.	Max.	Min.		Max.
I _L	Quiescent current	0/5			5			0.25		7.5		7.5	μA
		0/10			10		0.01	0.5		15		15	
		0/15			15			1		30		30	
		0/20			20		0.02	5		150		150	
V _{OH}	High level output voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10			10	9.95			9.95		9.95		
		0/15			15	14.95			14.95		14.95		
V _{OL}	Low level output voltage	5/0		<1	5		0.05			0.05		0.05	
		10/0			10								
		15/0			15								
V _{IH}	High level input voltage		0.5/4.5	<1	5	4			4		4		
			1/9		10	8			8		8		
			1.5/13.5		15	12.5			12.5		12.5		
V _{IL}	Low level input voltage		4.5/0.5	<1	5			1		1		1	
			9/1		10			2		2		2	
			13.5/1.5		15			2.5		2.5		2.5	
I _{OH}	Output drive current	0/5	2.5	<1	5	-1.36	-3.2		-1.15		-1.1		
			4.6			-0.44	-1		-0.36		-0.36		
		0/10	9.5		10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5		15	-3.0	-6.8		-2.4		-2.4		
I _{OL}	Output sink current	0/5	0.4	<1	5	0.44	1		0.36		0.36	mA	
		0/10	0.5		10	1.1	2.6		0.9		0.9		
		0/15	1.5		15	3.0	6.8		2.4		2.4		
I _I	Input leakage current	0/18	Any input	18		±10 ⁻⁵	±0.1		±1		±1	μA	
C _I	Input capacitance		Any input			5	7.5					pF	

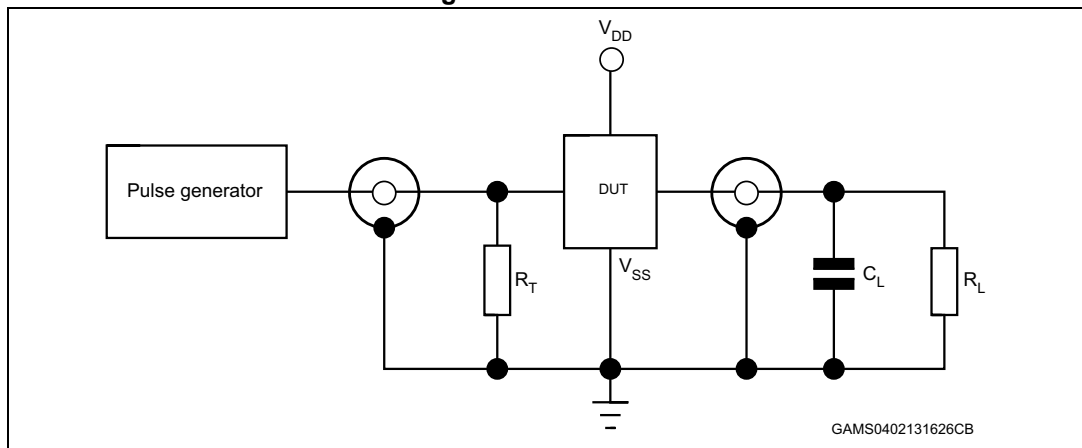
1. The noise margin for both level "1" and "0" is: 1 V min. with V_{DD} = 5 V, 2 V min. with V_{DD} = 10 V, and 2.5 V min. with V_{DD} = 15 V.

Table 7. Dynamic electrical characteristics
 ($T_{amb} = 25\text{ }^{\circ}\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$, $t_r = t_f = 20\text{ ns}$)

Symbol	Parameter	Test condition	Value ⁽¹⁾		Unit
			V_{DD} (V)	Typ.	
t_{PLH} , t_{PHL}	Propagation delay time	5	55	110	ns
		10	30	60	
		15	25	50	
t_{TLH} , t_{THL}	Output transition time	5	100	200	
		10	50	100	
		15	40	80	

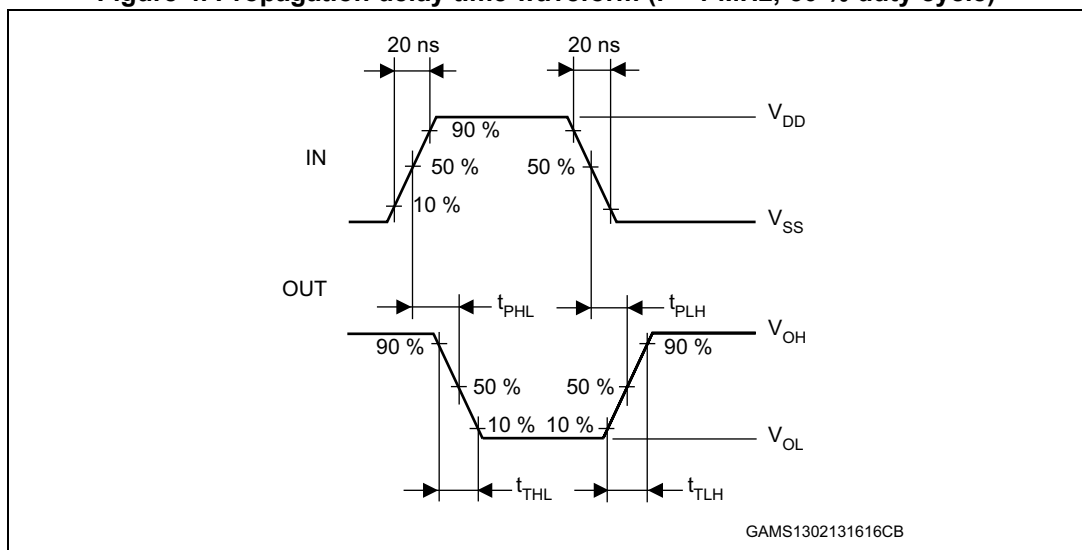
1. The typical temperature coefficient for all V_{DD} values is 0.3 %/°C.

Figure 3. Test circuit



1. Legend: $C_L = 50\text{ pF}$ or equivalent (includes jig and probe capacitance), $R_L = 200\text{ k}\Omega$, $R_T = Z_{OUT}$ of pulse generator (typically $50\text{ }\Omega$)

Figure 4. Propagation delay time waveform (f = 1 MHz; 50 % duty cycle)



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 SO14 package information

Figure 5. SO14 package mechanical drawing

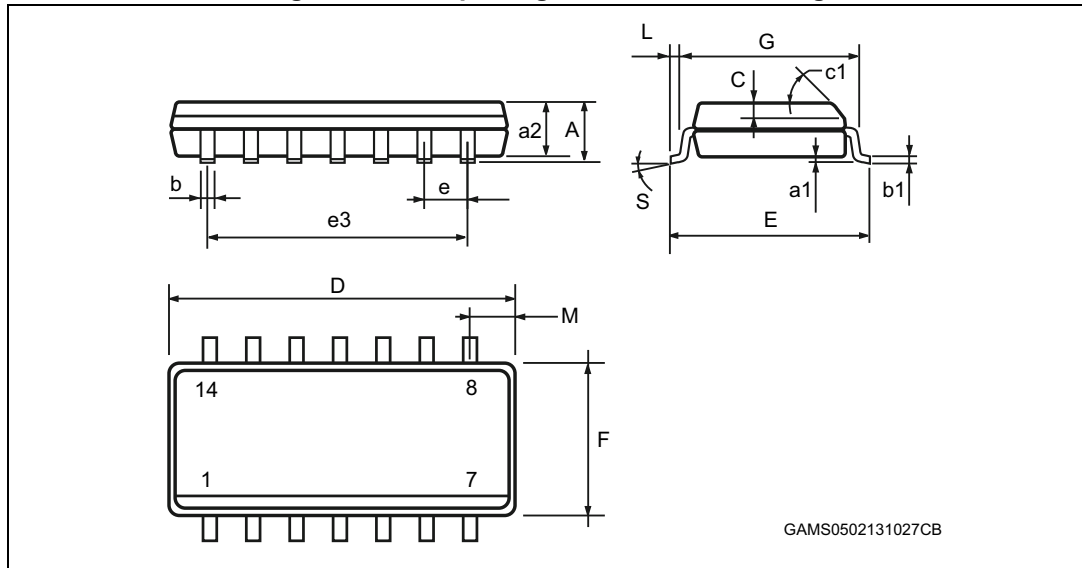


Table 8. SO14 package mechanical data

Ref	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1		45 °			45 °	
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S			8 °			8 °

5 Ordering information

Table 9. Order codes

Order code	Temp. range	Package	Packing	Marking
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1. Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
18-Feb-2013	4	Document template and layout updated Removed "B" from part number. Updated package names (PDIP-14 and SO14 instead of DIP-14 and SOP-14). Added Applications . Added Device summary table . Added Section 5: Ordering information .
22-Mar-2013	5	Updated Table 1: Device summary table and Table 9: Order codes .
10-Jan-2014	6	Removed PDIP-14 package Added ESD data to Features Table 1: Device summary table : updated footnote 1. Table 9: Order codes : updated footnote 1.

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