Six-Phase, Synchronous Bidirectional Buck or Boost Controller

FEATURES

- **Unique Architecture Allows Dynamic Regulation of Input Voltage, Output Voltage or Current**
- **Operates with External Gate Drivers and MOSFETs**
- **V_{HIGH} Voltages Up to 100V; V_{LOW} Voltages Up to 60V**
- **Synchronous Rectification: Up to 98% Efficiency**
- **ADI-Proprietary Advanced Current Mode Control**
- **±1% Voltage Regulation Accuracy Overtemperature**
- **Accurate, Programmable Inductor Current Monitoring and Bidirectional Regulation**
- **SPI Compliant Serial Interface**
  - **Operation Status and Fault Report**
  - **Programmable V_{HIGH}, V_{LOW} Margining**
- Phase-Lockable Frequency: 60kHz to 750kHz
- Optional Spread Spectrum Modulation
- Multiphase/Multi-ICs Operation Up to 24 Phases
- Selectable CCM/DCM/Burst Mode Operation
- Thermally Enhanced 64-Lead LQFP Package
- AEC-Q100 Qualification in Progress

APPLICATIONS

- Automotive 48V/12V Dual Battery Systems
- Backup Power Systems

DESCRIPTION

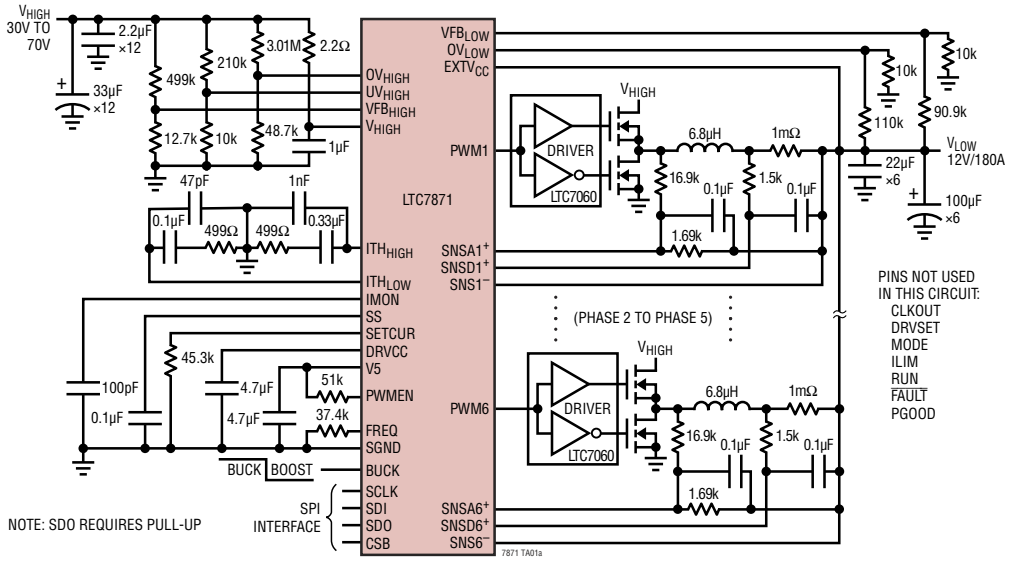
The LTC®7871 is a high performance bidirectional buck or boost switching regulator controller that operates in either buck or boost mode on demand. It regulates in buck mode from V_{HIGH}-to-V_{LOW} and boost mode from V_{LOW}-to-V_{HIGH} depending on a control signal, making it ideal for 48V/12V automotive dual battery systems. An accurate current programming loop regulates the maximum current that can be delivered in either direction. The LTC7871 allows both batteries to supply energy to the load simultaneously by driving energy from either battery to the other.

Its proprietary constant frequency current mode architecture enhances the signal-to-noise ratio enabling low noise operation and provides excellent current matching between phases. Additional features include an SPI-compliant serial interface, discontinuous or continuous mode of operation, OV/UV monitors, independent loop compensation for buck and boost operation, accurate inductor current monitoring and overcurrent protection.

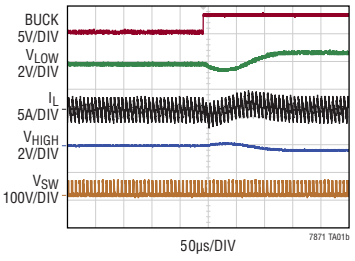
The LTC7871 is available in a 64 pin 10mm × 10mm LWE package.

TYPICAL APPLICATION

High Voltage Bidirectional Controller with Programming and Monitoring Functions



Boost-to-Buck Transition



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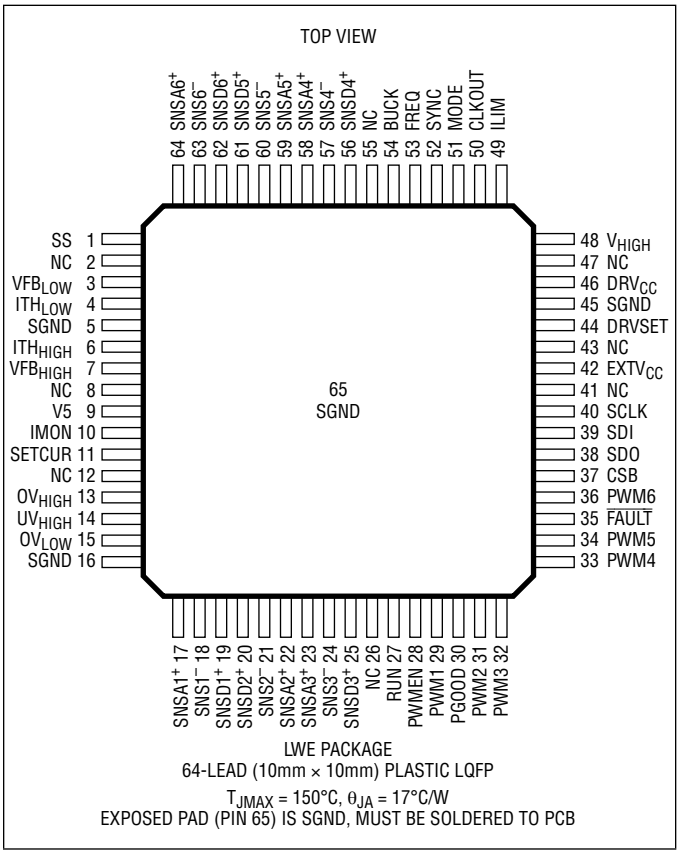
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{HIGH} ..... –0.3V to 100V
Current Sense Voltages
(SNSD+, SNSA+, SNS– Phase 1 to 6) ... –0.3V to 60V
(SNSA+ – SNS–) ..... –0.3V to 0.3V
(SNSD+ – SNS–) ..... –0.3V to 0.3V
$EXTV_{CC}$ ..... –0.3V to 60V
DRV_{CC} ..... –0.3V to 11V
RUN, OV_{HIGH}, UV_{HIGH}, OV_{LOW} ..... –0.3V to 6V
V5 ..... –0.3V to 6V
SCLK, SDI, SDO, CSB..... –0.3V to 6V
PWM1, PWM2, PWM3
PWM4, PWM5, PWM6, PWMEN..... –0.3V to V5
ITH_{HIGH}, ITH_{LOW}, VFB_{HIGH}, VFB_{LOW}..... –0.3V to V5
$\overline{FAULT}$, SETCUR, DRVSET, PGOOD..... –0.3V to V5
IMON, ILIM, SS, BUCK, MODE..... –0.3V to V5
FREQ, SYNC, CLKOUT..... –0.3V to V5
Operating Junction Temperature Range
(Notes 2, 3)..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
$DRV_{CC}/EXTV_{CC}$ Peak Current
(Guarantee by Design) 150mA

PIN CONFIGURATION



LWE PACKAGE
64-LEAD (10mm × 10mm) PLASTIC LQFP
T_{JMAX} = 150°C, θ_{JA} = 17°C/W
EXPOSED PAD (PIN 65) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING*	PACKAGE DESCRIPTION*	TEMPERATURE RANGE
LTC7871ELWE#PBF	LTC7871	64-Lead (10mm × 10mm) Plastic LQFP	–40°C to 125°C
LTC7871ILWE#PBF	LTC7871	64-Lead (10mm × 10mm) Plastic LQFP	–40°C to 125°C
LTC7871JLWE#PBF	LTC7871	64-Lead (10mm × 10mm) Plastic LQFP	–40°C to 150°C
LTC7871HLWE#PBF	LTC7871	64-Lead (10mm × 10mm) Plastic LQFP	–40°C to 150°C
AUTOMOTIVE PRODUCTS**			
LTC7871ELWE#WPBF	LTC7871	64-Lead (10mm × 10mm) Plastic LQFP	–40°C to 125°C
LTC7871ILWE#WPBF	LTC7871	64-Lead (10mm × 10mm) Plastic LQFP	–40°C to 125°C
LTC7871JLWE#WPBF	LTC7871	64-Lead (10mm × 10mm) Plastic LQFP	–40°C to 150°C
LTC7871HLWE#WPBF	LTC7871	64-Lead (10mm × 10mm) Plastic LQFP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

This product is available in 160-piece trays.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{HIGH} = 48V, V_{RUN} = 5V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops							
V_{HIGH}	V_{HIGH} Supply Voltage Range			6		100	V
V_{LOW}	V_{LOW} Supply Voltage Range	V_{HIGH} > 6V		1.2		60	V
	V_{LOW} Regulated Feedback Voltage	(Note 4); ITH_{LOW} Voltage = 1.5V	●	1.188	1.200	1.212	V
	V_{HIGH} Regulated Feedback Voltage	(Note 4); ITH_{HIGH} Voltage = 0.5V	●	1.188	1.200	1.212	V
	V_{LOW} EA Feedback Current	(Note 4)			–10	–40	nA
	V_{HIGH} EA Feedback Current	(Note 4)			–10	–40	nA
	Reference Voltage Line Regulation	(Note 4); V_{HIGH} = 7V to 80V			0.02	0.2	%
	V_{HIGH}/V_{LOW} Voltage Load Regulation	Measured in Servo Loop, ΔITH Voltage = 1.0V to 1.5V Measured in Servo Loop, ΔITH Voltage = 1.0V to 0.5V			0.01 –0.01	0.2 –0.2	% %
g_{m-buck}	Buck Mode Transconductance Amplifier g_{m-buck}	(Note 4) ITH_{LOW} = 1.5V, Sink/Source 5µA			2		mmho
$g_{m-boost}$	Boost Mode Transconductance Amplifier $g_{m-boost}$	(Note 4) ITH_{HIGH} = 0.5V, Sink/Source 5µA			1		mmho
I_Q	V_{HIGH} DC Supply Current Shutdown Mode, V_{HIGH} Supply Current Shutdown Mode, V_{LOW} Supply Current	(Note 5) V_{RUN} = 0V; V_{HIGH} = 48V V_{RUN} = 0V; V_{LOW} = 12V			10 30 20	16	mA µA µA
UVLO	DRV_{CC} Undervoltage Lockout Threshold	DRV_{CC} Ramping Down, V_{DRVSET} = V_{V5} DRV_{CC} Ramping Down, V_{DRVSET} = Float DRV_{CC} Ramping Down, V_{DRVSET} = 0V		6.9 4.8 3.9	7.2 5.0 4.1	7.5 5.2 4.3	V V V
	DRV_{CC} Undervoltage Hysteresis	V_{DRVSET} = Float, V_{V5} V_{DRVSET} = 0V			0.8 0.5		V V
	V5 Undervoltage Lockout Threshold	V5 Ramping Down, V_{DRVSET} = Float, V_{V5} V5 Ramping Down, V_{DRVSET} = 0V		4.2 3.9	4.4 4.1	4.6 4.3	V V
	V5 Undervoltage Hysteresis	V_{DRVSET} = Float, V_{V5} V_{DRVSET} = 0V			0.2 0.5		V V
	RUN Pin On Threshold	V_{RUN} Rising		1.1	1.22	1.35	V
	RUN Pin On Hysteresis				80		mV
	RUN Pin Source Current	V_{RUN} < 1.1V	●	0.6	2		µA
	RUN Pin Hysteresis Current	V_{RUN} > 1.3V	●	2	6		µA
I_{SS}	Soft-Start Charging Current	V_{SS} = 1.2V		0.8	1.0	1.2	µA
	BUCK Pin Input Threshold	V_{BUCK} Rising V_{BUCK} Falling			2.2 1.7		V V
	BUCK Pin Pull-Up Resistance	BUCK Pin to V5			200		kΩ
	Maximum Duty Cycle	Buck Mode Boost Mode		96	98 92		% %
Current Monitoring and Regulation Functions							
I_{SNSA+}	$SNSA^+$ Pins Input Current				±0.05	±1	µA
I_{SNSD+}	$SNSD^+$ Pins Input Current				±0.05	±1	µA
I_{SNS-}	SNS^- Pins Input Current				1		mA
	ILIM Pin Input Resistance				100		kΩ
I_{SETCUR}	SETCUR Pin Sourcing Current	MFR_IDAC_SETCUR = 0x00	●	15.0	16.0	17.0	µA
	IMON Current Proportional to V_{LOW} at Max Current	V_{ILIM} = Float, R_{SENSE} = 3mΩ				±10	%
	I_{MON} Zero Current Voltage			1.240	1.250	1.260	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{HIGH} = 48V, V_{RUN} = 5V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Current Sense Pin Voltage ($V_{SNSD}^+ - V_{SNS}^-$) to IMON Gain	V_{ILIM} = 0V, 1/4 V_{V5} V_{ILIM} = Float, 3/4 V_{V5}, V_{V5}			40 20		V/V V/V
	Total DC Sense Signal Gain	DCR Configuration			5		V/V
	Total DC Sense Signal Gain	R_{SENSE} Configuration			4		V/V
$V_{SENSE(MAX)}$ (DCR Configuration)	Maximum Current Sense Threshold (Buck and Boost Mode)	V_{ILIM} = 0V V_{ILIM} = 1/4 V_{V5} V_{ILIM} = Float V_{ILIM} = 3/4 V_{V5} V_{ILIM} = V_{V5}	● ● ● ● ●	6.5 17.0 27.0 36.0 44.0	10.0 20.0 30.0 40.0 50.0	13.5 23.0 33.0 44.0 56.0	mV mV mV mV mV
$V_{SENSE(MAX)}$ (R_{SENSE} Configuration)	Maximum Current Sense Threshold (Buck and Boost Mode)	V_{ILIM} = 0V V_{ILIM} = 1/4 V_{V5} V_{ILIM} = Float V_{ILIM} = 3/4 V_{V5} V_{ILIM} = V_{V5}	● ● ● ● ●	8.1 21.2 33.7 45.0 55.0	12.5 25.0 37.5 50.0 62.5	16.9 28.8 41.3 55.0 70.0	mV mV mV mV mV
V_{OCFT}	Overcurrent Fault Threshold, $V_{SNSD}^+ - V_{SNS}^-$	V_{ILIM} = 0V V_{ILIM} = 1/4 V_{V5} V_{ILIM} = Float V_{ILIM} = 3/4 V_{V5} V_{ILIM} = V_{V5}	● ● ● ● ●	31.0 43.0 54.0 65.0 76.0	37.5 50.0 62.5 75.0 87.5	44.0 57.0 71.0 85.0 99.0	mV mV mV mV mV
V_{NOCFT}	Negative Overcurrent Fault Threshold, $V_{SNSD}^+ - V_{SNS}^-$	V_{ILIM} = 0V V_{ILIM} = 1/4 V_{V5} V_{ILIM} = Float V_{ILIM} = 3/4 V_{V5} V_{ILIM} = V_{V5}	● ● ● ● ●	–45.0 –58.0 –72.0 –86.0 –100.0	–37.5 –50.0 –62.5 –75.0 –87.5	–30.0 –42.0 –53.0 –64.0 –75.0	mV mV mV mV mV
	Overcurrent Fault Threshold Hysteresis, $\lvert V_{SNSD}^+ - V_{SNS}^-\rvert$	V_{ILIM} = 0V V_{ILIM} = 1/4 V_{V5}, Float, 3/4 V_{V5}, V_{V5}			25 31		mV mV
DRV_{CC} and V5 Linear Regulators							
V_{DRVCC}	DRV_{CC} Regulation Voltage	12V < V_{EXTVCC} < 60V, V_{DRVSET} = V_{V5} 12V < V_{EXTVCC} < 60V, V_{DRVSET} = Float 12V < V_{EXTVCC} < 60V, V_{DRVSET} = 0V		9.5 7.6 4.8	10 8 5	10.5 8.4 5.2	V V V
	DRV_{CC} Load Regulation	I_{DRVCC} = 0mA to 100mA, V_{EXTVCC} = 14V			1.6	3.0	%
	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive, V_{DRVSET} = V_{V5} $EXTV_{CC}$ Ramping Positive, V_{DRVSET} = Float $EXTV_{CC}$ Ramping Positive, V_{DRVSET} = 0V			10.7 8.5 6.9		V V V
	$EXTV_{CC}$ Hysteresis				12		%
V5	V5 Regulation Voltage	6V < V_{DRVCC} < 10V		4.8	5.0	5.2	V
	V5 Load Regulation	I_{V5} = 0mA to 20mA			0.5	1	%
Current DACs (IDAC)							
	V_{HIGH}/V_{LOW} IDAC Accuracy	MFR_IDAC_$V_{LOW/HIGH}$ = 0x40 or 0x7F		–1		1	%
	V_{HIGH}/V_{LOW} IDAC Program Range			–64		63	µA
	SETCUR IDAC Program Range			0		31	µA
LSB	V_{HIGH}/V_{LOW} IDAC LSB SETCUR IDAC LSB				1 1		µA µA
Oscillator and Phase-Locked Loop							
I_{FREQ}	FREQ Pin Output Current		●	19	20	21	µA
	Nominal Frequency	V_{SYNC} = 0V, R_{FREQ} = 51.1k		230	250	270	kHz
f_{LOW}	Low Fixed Frequency	V_{SYNC} = 0V, R_{FREQ} = 27.4k		55	70	85	kHz
f_{HIGH}	High Fixed Frequency	V_{SYNC} = 0V, R_{FREQ} = 105k		640	710	780	kHz

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Synchronizable Frequency	SYNC = External Clock	●	60		750	kHz
	Spread Spectrum Frequency Modulation Range	V_{SYNC} = 5V, R_{FREQ} = 51.1k, MFR_SSFM = 0x00		–12		12	%
$\theta_2 - \theta_1$	Phase 2 Relative to Phase 1				180		Deg
$\theta_3 - \theta_1$	Phase 3 Relative to Phase 1				60		Deg
$\theta_4 - \theta_1$	Phase 4 Relative to Phase 1				240		Deg
$\theta_5 - \theta_1$	Phase 5 Relative to Phase 1				120		Deg
$\theta_6 - \theta_1$	Phase 6 Relative to Phase 1				300		Deg
$\theta_{CLKOUT} - \theta_1$	CLKOUT Phase to Phase 1				30		Deg
	Clock Output High Voltage	I_{LOAD} = 0.5mA		V5 – 0.2	V5		V
	Clock Output Low Voltage	I_{LOAD} = –0.5mA				0.2	V
	SYNC Pin Input Threshold	SYNC Pin Rising SYNC Pin Falling		2		 1.1	V V
	SYNC Pin Input Resistance				100		kΩ
Power Good and $\overline{FAULT}$							
	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
	PGOOD Trip Level, VFB_{HIGH}/VFB_{LOW} With Respect to the Regulated Voltage	VFB_{HIGH}/VFB_{LOW} Ramping Negative VFB_{HIGH}/VFB_{LOW} Ramping Positive			–10 10		% %
	PGOOD Delay	PGOOD Pin High to Low			40		µs
	$\overline{FAULT}$ Voltage Low	I_{FAULT} = 2mA			0.1	0.3	V
	$\overline{FAULT}$ Voltage Leakage Current	V_{FAULT} = 5V				±1	µA
	$\overline{FAULT}$ Delay	$\overline{FAULT}$ Pin High to Low			120		µs
	V_{LOW} OV Comparator Threshold			1.15	1.2	1.25	V
	V_{LOW} OV Comparator Hysteresis	V_{OVLOW} > 1.2V			5		µA
	V_{HIGH} OV Comparator Threshold			1.15	1.2	1.25	V
	V_{HIGH} OV Comparator Hysteresis	V_{OVHIGH} > 1.2V			5		µA
	V_{HIGH} UV Comparator Threshold			1.15	1.2	1.25	V
	V_{HIGH} UV Comparator Hysteresis	V_{UVHIGH} < 1.2V			5		µA
PWM Outputs							
	PWM Output High Voltage	I_{LOAD} = 0.5mA	●	V5 – 0.5			V
	PWM Output Low Voltage	I_{LOAD} = –0.5mA	●			0.5	V
	PWM Output Current in Hi-Z State					±5	µA
DIGITAL I/O: CSB, SCLK, SDI, SDO							
V_{IL}	Digital Input Low Voltage	Pins CSB, SCLK, SDI				0.5	V
V_{IH}	Digital Input High Voltage	Pins CSB, SCLK, SDI		1.8			V
V_{OL}	Digital Output Voltage Low	Pin SDO, Sinking 1mA				0.3	V
R_{CSB}	CSB Pin Pull-Up Resistor				300		kΩ
R_{SCLK}	SCLK Pin Pull-Down Resistor				300		kΩ
R_{SDI}	SDI Pin Pull-Down Resistor				300		kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{HIGH} = 48V, V_{RUN} = 5V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SPI Interface Timing Characteristics (Refer to Timing Diagram in Figure 9 and 10)							
t_{CKH}	SCLK High Time			45			ns
t_{CSS}	CSB Setup Time			40			ns
t_{CSH}	CSB High Time			60			ns
t_{CS}	SDI to SCLK Setup Time			40			ns
t_{CH}	SDI to SCLK Hold Time			20			ns
t_{DO}	SCLK to SDO Time			90			ns
$t_{C\%}$	SCLK Duty Cycle			45	50	55	%
$f_{SCLK(MAX)}$	Maximum SCLK Frequency			5			MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7871 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7871E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7871I is guaranteed over the –40°C to 125°C operating junction temperature range. The LTC7871J is guaranteed over the –40°C to 150°C operating junction temperature range. The LTC7871H is guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperature degrades operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

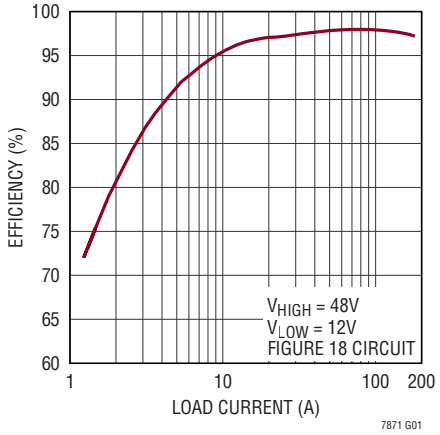
$$T_J = T_A + (P_D \bullet 17°C/W)$$

Note 4: The LTC7871 is tested in a feedback loop that servos $V_{ITHHIGH}$ and V_{ITHLOW} to a specified voltage and measures the resultant VFB_{HIGH}, VFB_{LOW}, respectively.

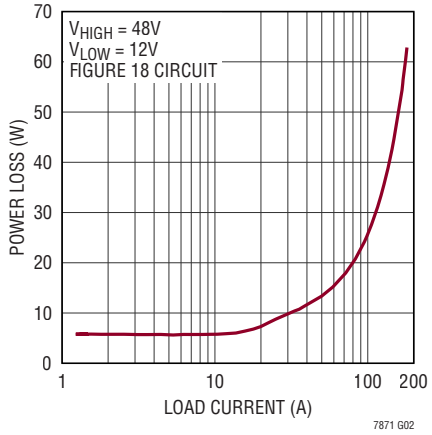
Note 5: Dynamic supply current may be higher due to the loading current at DRV_{CC} linear regulator.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

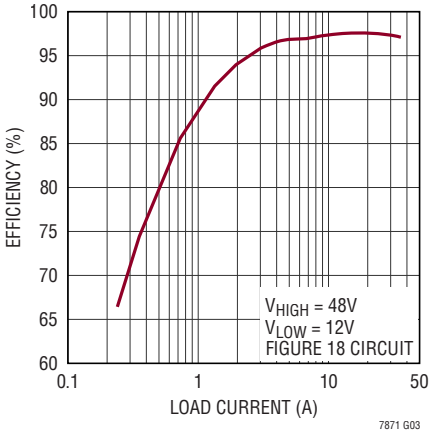
Efficiency Buck Mode



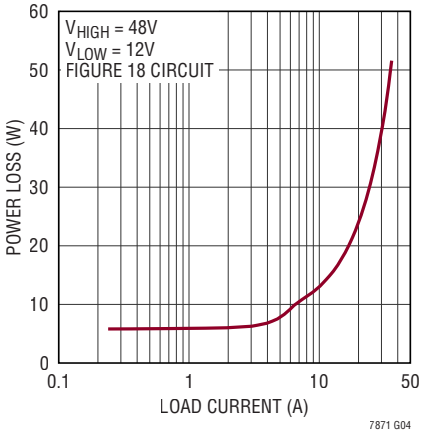
Power Loss Buck Mode



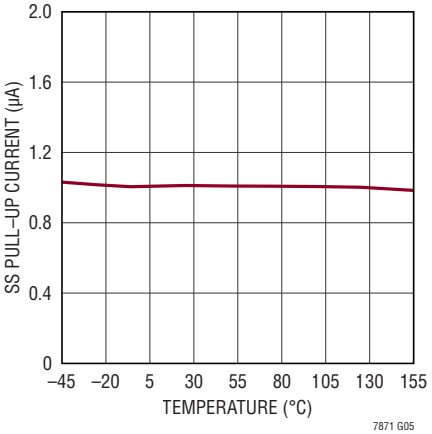
Efficiency Boost Mode



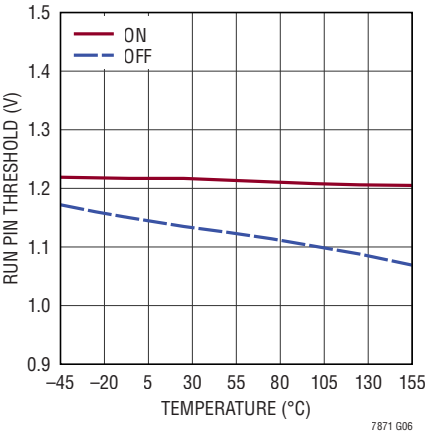
Power Loss Boost Mode



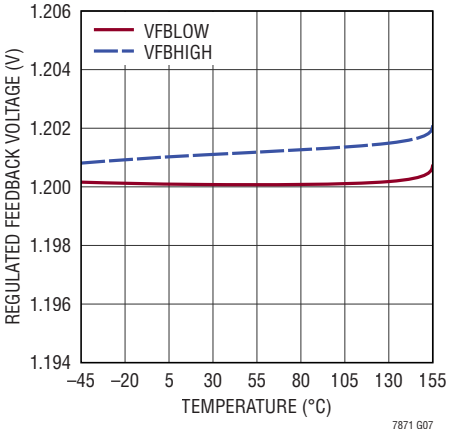
SS Pin Pull-Up Current vs Temperature



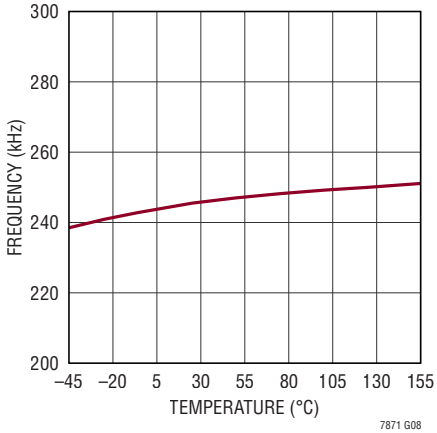
RUN Pin Threshold vs Temperature



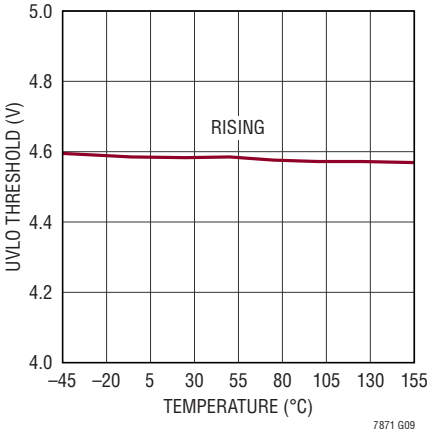
Regulated Feedback Voltage vs Temperature



Oscillator Frequency vs Temperature



Undervoltage Lockout Threshold (V5) vs Temperature



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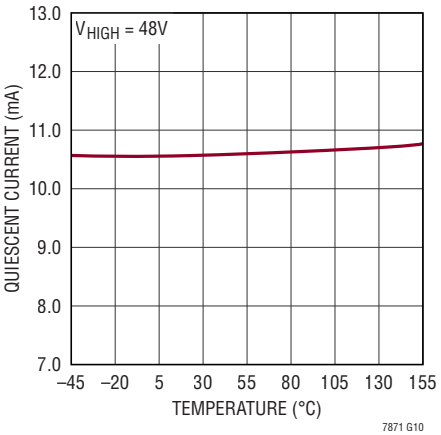
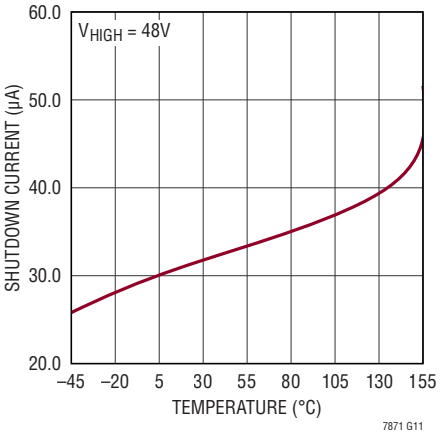
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

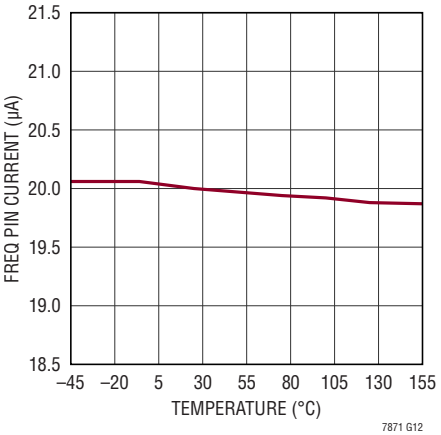
Quiescent Current vs Temperature



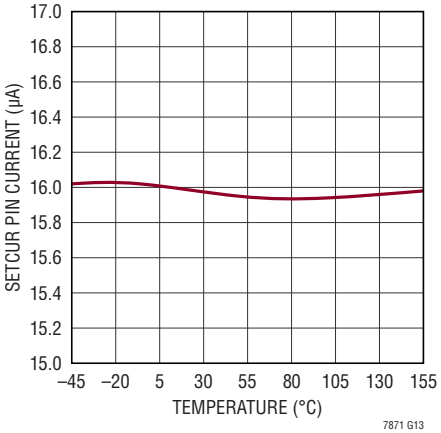
Shutdown Current vs Temperature



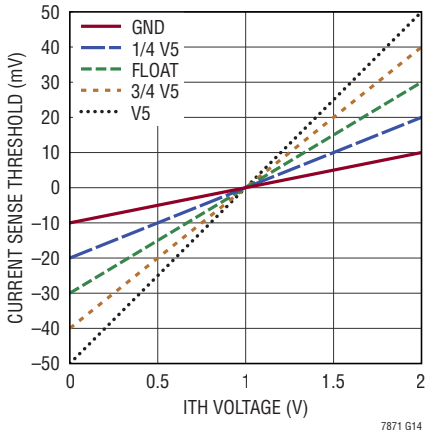
FREQ Pin Source Current vs Temperature



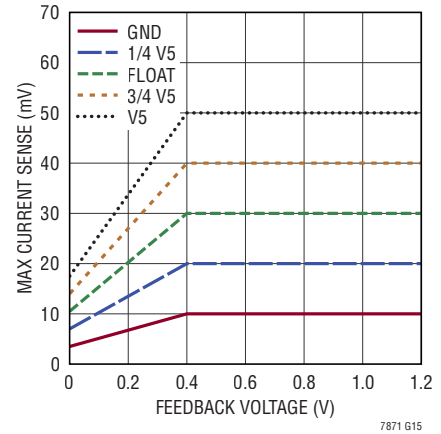
SETCUR Pin Source Current vs Temperature



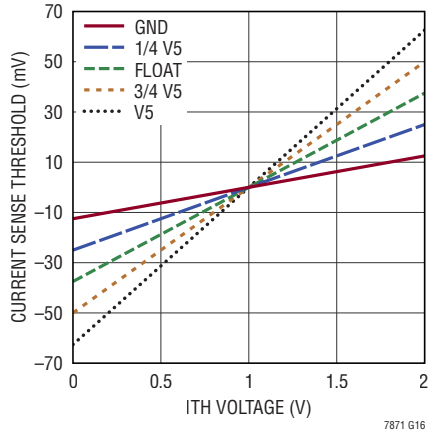
Current Sense Threshold vs ITH Voltage (DCR)



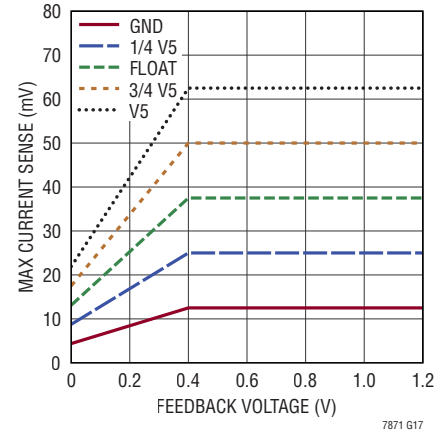
Maximum Current Sense Threshold vs Feedback Voltage—BUCK (DCR)



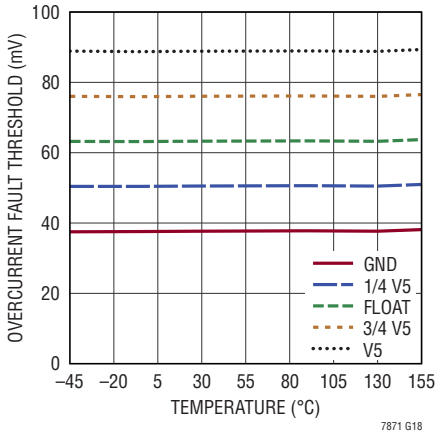
Current Sense Threshold vs ITH Voltage—(R_{SENSE})



Maximum Current Sense Threshold vs Feedback Voltage—BUCK (R_{SENSE})



Overcurrent Fault Threshold vs Temperature



PIN FUNCTIONS

RUN (Pin 27): Enable Control Input. A voltage above 1.22V turns on the IC. There is a 2µA pull-up current on this pin. Once the RUN pin rises above the 1.22V threshold, the pull-up current increases to 6µA.

VFB_{HIGH} (Pin 7): V_{HIGH} Voltage Sensing Error Amplifier Noninverting Input.

VFB_{LOW} (Pin 3): V_{LOW} Voltage Sensing Error Amplifier Inverting Input.

ITH_{HIGH}/ITH_{LOW} (Pins 6 and 4): Current Control Threshold and Error Amplifier Compensation Point. The current comparator's threshold varies with the ITH control voltage.

SS (Pin 1): Soft-Start Input. The voltage ramp rate at this pin sets the voltage ramp rate of the regulated voltage. A capacitor to ground accomplishes soft-start. This pin has a 1µA pull-up current.

MODE (Pin 51): Mode Set Pin. Tying this pin to SGND enables forced continuous mode in buck or boost modes. Floating this pin results in burst mode in buck mode and discontinuous mode in boost mode. Tying this pin to V5 enables discontinuous mode in buck or boost modes. The input impedance of this pin is 90kΩ.

SYNC (Pin 52): Switching Frequency Synchronization or Spread Spectrum Set Pin. Applying an external clock between 60kHz to 750kHz to this pin causes the switching frequency to synchronize to the clock signal. If SYNC is low, a resistor from the FREQ pin to SGND sets the switching frequency. Tying this pin to V5 allows switching frequency spread spectrum. This pin has a 100kΩ internal resistor to ground.

FREQ (Pin 53): Frequency Set Pin. A resistor between this pin and SGND sets the switching frequency. This pin sources 20µA current.

DRVSET (Pin 44): The voltage setting on this pin programs the DRV_{CC} output voltage. There are two internal resistors, 200kΩ and 160kΩ, connecting this pin to the V5 and SGND, respectively.

CLKOUT (Pin 50): Clock Output Pin. Use this pin to synchronize multiple LTC7871 ICs. Signal swing is from V5 to ground.

V5 (Pin 9): Internal 5V Regulator Output. The control circuits are powered from this voltage. Bypass this pin to SGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor.

DRV_{CC} (Pin 46): Gate Driver Current Supply LDO Output. The voltage on this pin can be set to 5V, 8V, or 10V by the DRVSET pin. Bypass this pin to ground plane with a minimum of 4.7µF low ESR tantalum or ceramic capacitor.

$EXTV_{CC}$ (Pin 42): External Power Input to an Internal LDO Connected to DRV_{CC}. This LDO supplies DRV_{CC} power, bypassing the internal LDO powered from V_{HIGH}, whenever $EXTV_{CC}$ is higher than its switchover threshold. Do not exceed 60V on this pin.

ILIM (Pin 49): Current Comparator Sense Voltage Limit Selection Pin. The input impedance of this pin is 100kΩ.

$SNSD1^+$/$SNSD2^+$/$SNSD3^+$/$SNSD4^+$/$SNSD5^+$/$SNSD6^+$ (Pins 19, 20, 25, 56, 61, and 62): DC Positive Current Sense Comparator Inputs. These inputs amplify the DC portion of the current signal to the IC's current comparators and current sense amplifiers.

$SNS1^-$/$SNS2^-$/$SNS3^-$/$SNS4^-$/$SNS5^-$/$SNS6^-$ (Pins 18, 21, 24, 57, 60, and 63): Negative Current Sense Comparator Inputs. The negative input of the current comparator is normally connected to the V_{LOW}.

$SNSA1^+$/$SNSA2^+$/$SNSA3^+$/$SNSA4^+$/$SNSA5^+$/$SNSA6^+$ (Pins 17, 22, 23, 58, 59, and 64): AC Positive Current Sense Comparator Inputs. These inputs amplify the AC portion of the current signal to the IC's current comparator.

V_{HIGH} (Pin 48): Main V_{HIGH} Supply. Bypass this pin to ground with a capacitor (0.1µF to 1µF).

$\overline{FAULT}$ (Pin 35): Fault Indicator Output. Open-drain output that pulls to ground during a fault condition.

PGOOD (Pin 30): Power Good Indictor Output for the Regulated V_{HIGH}/V_{LOW}. Open drain logic out that is pulled to ground when the regulated V_{HIGH}/V_{LOW} exceeds ±10% regulation window, after the internal 40µS power bad mask timer expires.

PIN FUNCTIONS

UV_{HIGH} (Pin 14): V_{HIGH} Undervoltage Threshold Set Pin. A resistor divider from V_{HIGH} is needed to set this threshold. When the voltage on this pin falls below the 1.2V trip point, a 5µA current is sunk in to the pin to provide externally adjustable hysteresis.

OV_{HIGH} (Pin 13): V_{HIGH} Overvoltage Threshold Set Pin. A resistor divider from V_{HIGH} is needed to set this threshold. When the voltage on this pin rises past the 1.2V trip point, a 5µA current is sourced out of the pin to provide externally adjustable hysteresis.

OV_{LOW} (Pin 15): V_{LOW} Overvoltage Threshold Set Pin. A resistor divider from V_{LOW} is needed to set this threshold. When the voltage on this pin rises past the 1.2V trip point, a 5µA current is sourced out of the pin to provide externally adjustable hysteresis.

BUCK (Pin 54): The voltage on this pin determines if the IC is regulating the V_{LOW} or V_{HIGH} voltage/current. Float or tie this pin to V5 for buck mode operation. Ground this pin for boost mode operation.

IMON (Pin 10): Current Monitor Pin. The voltage on this pin is directly proportional to the average inductor currents of all 6 channels. 1.25V on this pin indicates zero average inductor current per phase.

SETCUR (Pin 11): This pin sets the maximum average inductor current in buck or boost mode. This pin sources 16µA current and it is programmable by the SPI interface.

PWM1, PWM2, PWM3, PWM4, PWM5, PWM6 (Pins 29, 31, 32, 33, 34, and 36): (Top) Gate Signal Output. This signal goes to the PWM or top gate input of the external gate driver or integrated driver MOSFET. This is a three-state compatible output.

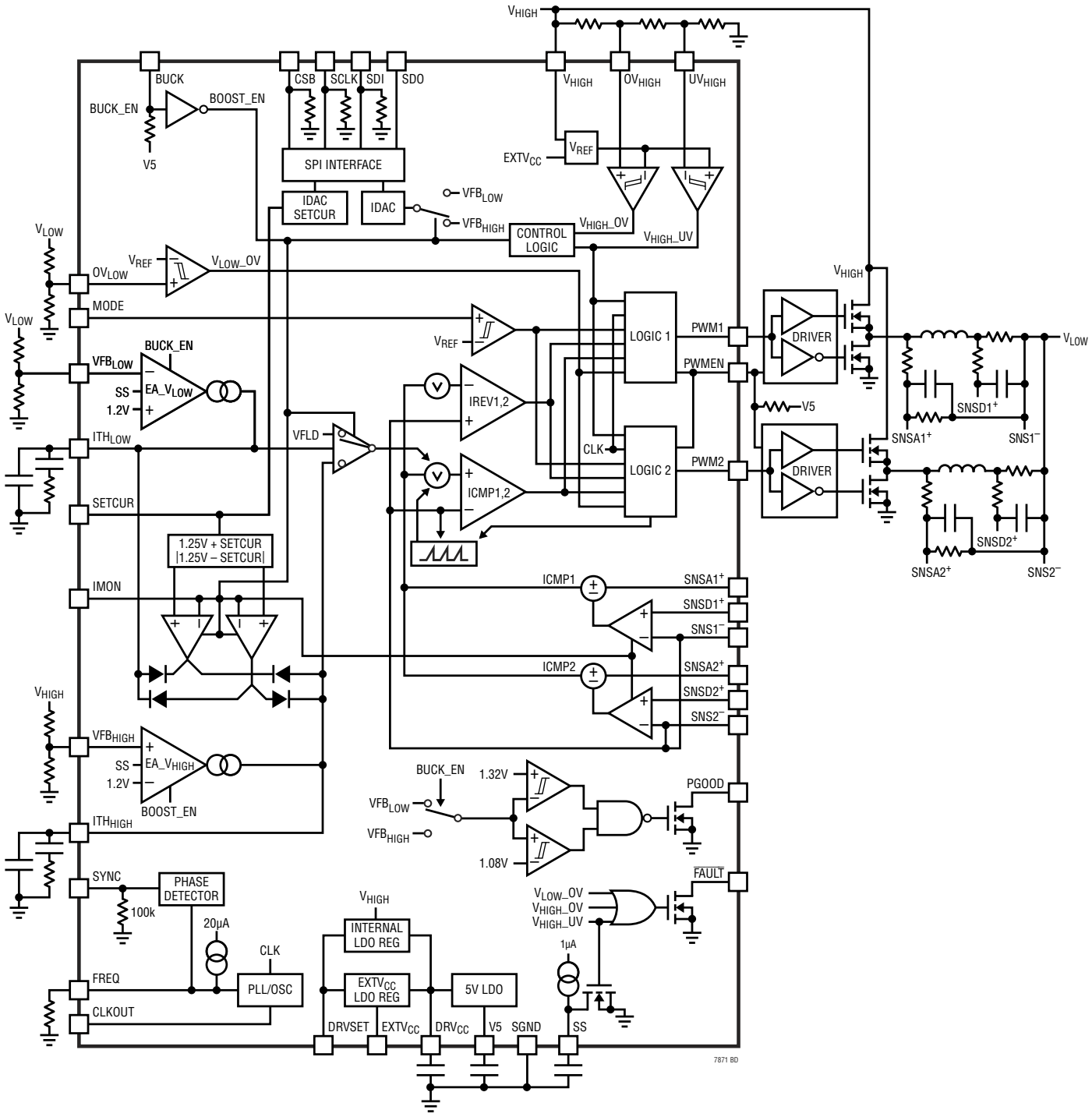
PWMEN (Pin 28): Enable Pin for External Gate Drivers. Open drain logic that is pulled to ground when the LTC7871 shut downs the external gate drivers. When this pin is low, all the PWM pin outputs are high impedance.

CSB, SDO, SDI, SCLK (Pins 37, 38, 39 and 40): 4-Wire Serial Peripheral Interface (SPI). Active low chip select (CSB), serial clock (SCLK) and serial data in (SDI) are digital Inputs. Serial data out (SDO) is an open-drain NMOS output pin. SDO requires an external pull-up resistor. Refer to the Serial Port section for more details.

NC (Pins 2, 8, 12, 26, 41, 43, 47, and 55): No Connect Pins.

SGND (Pins 5, 16, 45 and Exposed Pad): Ground. Must be soldered to PCB ground for rated thermal performance. Connect this pin closely to negative terminal of V_{HIGH}, DRV_{CC}, V5 bypass capacitors. All small signal components and compensation components should connect here.

BLOCK DIAGRAM Functional Diagram Shows Two Channels Only.



OPERATION

Main Control Loop

The LTC7871 is a bidirectional, constant-frequency, current mode buck or boost switching regulator controller with six channels operating equally out of phase. The LTC7871 is capable of delivering power from V_{HIGH} to V_{LOW} as well as from V_{LOW} back to V_{HIGH}. When power is delivered from V_{HIGH} to V_{LOW}, the LTC7871 operates as a peak-current mode constant-frequency buck regulator; and when power delivery is reversed, it operates as a valley current mode constant-frequency boost regulator. Four control loops, two for current and two for voltage, allow control of voltage or bidirectional current on either V_{HIGH} or V_{LOW}. The LTC7871 uses an ADI proprietary current sensing, current mode architecture. During normal buck mode operation, the top MOSFET is turned on every cycle when the oscillator sets the RS latch, and turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The error amplifier receives the feedback signal and compares it to the internal 1.2V reference. When the load current increases, it causes a slight change in the feedback pin voltage relative to the 1.2V reference, which in turn causes the ITH voltage to change until the inductor's average current equals the new load current. After the top MOSFET has turned off, the bottom synchronous MOSFET is turned on until the beginning of the next cycle.

In either buck or boost mode, the two current control loops always monitor the maximum average inductor current. When it increases above the thresholds, the current loops will take over the ITH pin control from the voltage loop. As a result, the maximum average inductor current is limited.

The main control loop is shut down by pulling the RUN pin low. Releasing the RUN pin allows an internal 2µA current source to pull it up. When the RUN pin reaches 1.22V, the IC is powered up and the pull-up current increases to 6µA. When the RUN pin is low, all functions are kept in a controlled shutdown state.

Current Sensing with Low DCR or R_{SENSE}

The LTC7871 employs a unique architecture to enhance the signal-to-noise ratio with low current sense offsets. This enables it to operate with a small current sense signal from a very low value inductor DCR to improve power efficiency, and reduce jitter due to switching noise which could corrupt the signal. Each channel has two positive current sense pins, $SNSD^+$ and $SNSA^+$, which share the negative current sense pin SNS^-. These sense pins acquire signals and process them internally to provide the response equivalent to a DCR sense signal that has a 14dB (5 times) signal-to-noise ratio. Accordingly, the current limit threshold is still a function of the inductor peak-current and its DCR value and can be accurately set from 10mV to 50mV in 10mV steps with the ILIM pin.

$DRV_{CC}/EXTV_{CC}$/V5 Power

Power for the external top and bottom MOSFET drivers is derived from the DRV_{CC} pin. The DRV_{CC} voltage can be set to 5V, 8V, or 10V using the DRVSET pin. When the $EXTV_{CC}$ pin is left open or tied to a voltage less than the switchover voltage programmed by the DRVSET pin, an internal linear regulator supplies DRV_{CC} power from V_{HIGH}. When $EXTV_{CC}$ is taken above the switchover voltage, the internal regulator between V_{HIGH} and DRV_{CC} is turned off, and a second internal regulator is turned on between $EXTV_{CC}$ and DRV_{CC}. Each top MOSFET driver is biased from a floating bootstrap capacitor, which normally recharges during each off cycle through an external diode when the top MOSFET turns off. If the input voltage, V_{HIGH}, decreases to a voltage close to V_{LOW}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one-twelfth of the clock period plus 160ns every fifth cycle to allow the bootstrap capacitor to recharge.

Most of the internal circuitry is powered from the V5 rail that is generated by an internal linear regulator from DRV_{CC}. The V5 pin needs to be bypassed with a minimum 4.7µF external capacitor to SGND. This pin provides a 5V output that can supply up to 20mA of current. See the Applications Information section for more details.

OPERATION

Soft-Start (Buck Mode)

By default, the start-up of the V_{LOW} voltage is normally controlled by an internal soft-start ramp. The internal soft-start ramp represents a noninverting input to the error amplifier. The VFB_{LOW} pin is regulated to the lowest of the error amplifier's three noninverting inputs (the internal soft-start ramp, the SS pin or the internal 1.2V reference). As the ramp voltage rises from 0V to 1.2V over approximately 1ms, the V_{LOW} voltage rises smoothly from its prebiased value to its final set value. Certain applications can require the start-up of the converter into a non-zero load voltage, where residual charge is stored on the V_{LOW} capacitor at the onset of converter switching. In order to prevent the V_{LOW} from discharging under these conditions, the top and bottom MOSFETs are disabled until soft-start is greater than VFB_{LOW}.

Soft-Start (Boost Mode)

The same internal soft-start capacitor and external soft-start capacitor are also active if the controller starts with boost mode of operation. The error amplifier for boost mode also tries to regulate to the lowest reference during start-up. However, the topology of the boost converter limits the effectiveness of this soft-start mechanism until the boost output voltage reaches its input voltage level. Therefore, it is recommended that the controller starts in buck mode of operation.

Shutdown and Start-Up (RUN and SS Pins)

The LTC7871 can be shut down using the RUN pin. Pulling the RUN pin below 1.22V shuts down the main control loop for the controller and most internal circuits, including the DRV_{CC} and V5 regulators. Releasing the RUN pin allows an internal 2µA current to pull up the pin and enable the controller. Alternatively, the RUN pin may be externally pulled up or driven directly by logic. Be careful not to exceed the absolute maximum rating of 6V on this pin. The start-up of the controller's V_{LOW} voltage is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 1.2V internal reference, the LTC7871 regulates the VFB_{LOW} voltage to the SS pin voltage instead of the 1.2V reference. This allows the SS pin to be used to program a soft-start by connecting an external capacitor from the SS pin to SGND. An internal 1µA pull-up current charges this capacitor, creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 1.2V (and beyond), the V_{LOW} voltage rises smoothly from zero to its final value. When the RUN pin is pulled low to disable the controller, or when V5 drops below its undervoltage lockout threshold, the SS pin is pulled low by an internal MOSFET. When in undervoltage lockout, the controller is disabled and the external MOSFETs are held off. External circuitry can be added to discharge the soft-start capacitor during fault conditions to ensure a soft-start when the faults are cleared.

Frequency Selection, Spread Spectrum, and Phase-Locked Loop (FREQ and SYNC Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

If the SYNC pin is tied to SGND, the FREQ pin can be used to program the controller's operating frequency from 67kHz to 725kHz. There is a precision 20µA current flowing out of the FREQ pin so that the user can program the controller's switching frequency with a single resistor to SGND. A curve is provided later in the Applications Information section showing the relationship between the voltage on the FREQ pin and switching frequency (Figure 7).

Switching regulators can be particularly troublesome for applications when electromagnetic interface (EMI) is a concern. To improve EMI, the LTC7871 can operate in spread spectrum mode, which is enabled by tying the SYNC pin to V5. This feature varies the switching frequency at low frequency rate (switching frequency/512, by default) with a triangular frequency modulation of ±12%. For example, if the LTC7871's frequency is programmed to switch at 200kHz, enabling spread spectrum will modulate the frequency between 176kHz and 224kHz at a 0.4kHz rate. These spread spectrum parameters are programmed by the MFR_SSFM register.

OPERATION

A phase-locked loop (PLL) is available on the LTC7871 to synchronize the internal oscillator to an external clock source that is connected to the SYNC pin. The PLL loop filter network is integrated inside the LTC7871. The phase locked loop is capable of locking to any frequency within the range of 60kHz to 750kHz. The frequency setting resistor should always be present to set the controller's initial switching frequency before locking to the external clock. The controller operates in the user selected mode when it is synchronized.

Undervoltage Lockout

The LTC7871 has two functions that help protect the controller in case of undervoltage conditions. Two precision UVLO comparators constantly monitor the V5 and DRV_{CC} voltages to ensure that adequate voltages are present. The switching action is stopped when V5 or DRV_{CC} is below the undervoltage lockout threshold. To prevent oscillation when there is a disturbance on the V5 or DRV_{CC}, the UVLO comparators have precision hysteresis.

Another way to detect an undervoltage condition is to monitor the V_{HIGH} supply. Because the RUN pin has a precision turn-on reference of 1.22V, one can use a resistor divider to V_{HIGH} to turn on the IC when V_{HIGH} is high enough. An extra 4µA of current flows out of the RUN pin once the RUN pin voltage passes 1.22V. The RUN comparator itself has about 80mV of hysteresis. Additional hysteresis for the RUN comparator can be programmed by adjusting the values of the resistive divider. For accurate V_{HIGH} undervoltage detection, V_{HIGH} needs to be higher than 5V.

Fault Flag ($\overline{FAULT}$, OV_{HIGH}, OV_{LOW} and UV_{HIGH} Pins)

The $\overline{FAULT}$ pin is connected to the open-drain of an internal N-channel MOSFET. It can be pulled high with an external resistor connected to a voltage up to 6V, such as V5 or an external bias voltage. The $\overline{FAULT}$ pin is pulled low when at least one of the following conditions is met:

a. The RUN pin is below its turn on threshold.

b. When V5 or DRV_{CC} is below its UVLO threshold.

c. Any of the three OV/UV comparators has been tripped.

d. During a startup sequence until the SS pin charges up past 1.2V.

e. When any channel is in overcurrent fault status.

f. When the IC is over temperature.

The OV_{LOW} and OV_{HIGH} thresholds are set using an external resistor divider off V_{LOW} and V_{HIGH}, respectively. When the voltage at the pin exceeds the comparator threshold of 1.2V, a 5µA hysteresis current is sourced out of the respective pin and the $\overline{FAULT}$ signal goes low after a 120µs delay. The UV_{HIGH} threshold is also set using an external resistor divider off V_{HIGH}. When the voltage at the pin falls below the comparator threshold of 1.2V, a 5µA hysteresis current is sunk into the UV_{HIGH} pin and the $\overline{FAULT}$ signal goes low after a 120µs delay. The amount of hysteresis can be adjusted by changing the total impedance of the resistor divider, while the resistor ratio sets the UV/OV trip point.

Besides flagging the $\overline{FAULT}$ pin, the UV/OV comparators also affect the operation of the controller, as shown in Table 1. When the OV_{LOW} comparator crosses its 1.2V threshold:

a. In buck mode, the controller stops switching.

b. In boost mode, the controller continues to switch.

c. ITH and SS are unaffected in both buck and boost modes. Whenever a fault is detected, discharge the SS pin as needed externally.

When the OV_{HIGH} comparator crosses its 1st threshold of 1.2V:

a. The controller stops switching in both buck and boost modes.

b. ITH and SS are unaffected in both buck and boost modes. Whenever a fault is detected, discharge the SS pin as needed externally.

When the OV_{HIGH} comparator crosses its 2nd threshold of 2.4V:

a. The controller stops switching in both buck and boost modes.

OPERATION

b. Both ITH and IMON pins are driven into high impedance. This feature allows the users to isolate one LTC7871 from a multiphase system in case a fault is detected on one particular IC.

c. The SS pin is unaffected.

When the UV_{HIGH} comparator crosses its 1.2V threshold:

a. In buck mode, the controller stops switching after a 120µs delay, and the SS pin pulls to SGND.

b. In boost mode, the controller continues to switch. The SS pin is unaffected.

c. ITH is unaffected in both buck and boost modes.

Table 1. OV/UV Faults

$\overline{FAULT}$	MODE	SWITCHING	ITH PINS	IMON	SS
OV_{LOW} 1.2V Threshold	Buck	Stops	No Effect	No Effect	No Effect
	Boost	Continues	No Effect	No Effect	No Effect
OV_{HIGH} 1.2V Threshold	Buck	Stops	No Effect	No Effect	No Effect
	Boost	Stops	No Effect	No Effect	No Effect
OV_{HIGH} 2.4V Threshold	Buck	Stops	Hi-Z	Hi-Z	No Effect
	Boost	Stops	Hi-Z	Hi-Z	No Effect
UV_{HIGH} 1.2V Threshold	Buck	Stops	No Effect	No Effect	Pulls to SGND
	Boost	Continues	No Effect	No Effect	No Effect

Current Monitoring and Regulation (IMON, SETCUR Pins)

The inductor current can be sensed using either its DCR or a R_{SENSE} resistor. The current monitoring pin, IMON, outputs a voltage that is proportional to the average inductor current of the six channels sensed by the LTC7871. The operational range of IMON is 0.4V to 2.5V. When the average inductor current is zero, the IMON pin voltage rests at 1.25V. As the inductor current increases in buck mode, the IMON voltage proportionally increases; As the inductor current increases in boost mode, the IMON voltage proportionally decreases. Use the following equation to calculate the voltages on IMON:

$$V_{IMON} = V_{ZERO} + \frac{K \bullet I_{L(ALL)} \bullet R_{SENSE}}{6};\ \text{Buck Mode}$$

$$V_{IMON} = V_{ZERO} - \frac{K \bullet I_{L(ALL)} \bullet R_{SENSE}}{6};\ \text{Boost Mode}$$

where:

V_{ZERO} is the IMON voltage when average output current is zero; V_{ZERO} = 1.25V typically

K = 40 if the ILIM voltage is 0V or 1/4 V_{V5}

K = 20 if the ILIM voltage is float, 3/4 V_{V5} or V_{V5}

$I_{L(ALL)}$ is the total average inductor current including all six channels

R_{SENSE} is the current sensing resistor value.

An external voltage can be applied to the SETCUR pin to regulate the maximum average inductor current. The SETCUR pin voltage should be set as:

$$V_{SETCUR} = \frac{K \bullet I_{L(MAX)} \bullet R_{SENSE}}{6}$$

where:

$I_{L(MAX)}$ is the maximum total average inductor current including all six channels

The SETCURP and SETCURN are internally generated voltages based on the SETCUR pin:

SETCURP = 1.25V + V_{SETCUR}

SETCURN = |1.25V – V_{SETCUR}|

SETCURP, SETCURN, and IMON are the three inputs to the current regulation loop error amplifier with SETCURP and SETCURN acting as the reference. When the IMON pin voltage approaches SETCURP or SETCURN, the ITH pin control is taken over by the current loop error amplifier from the voltage loop error amplifier.

In either buck or boost mode, both the maximum positive average current and the maximum negative average current are regulated. There is a 16µA current flowing out of the SETCUR pin so that a single resistor to SGND can set both the positive average current loop and negative average current loop. The sourcing current from the SETCUR pin is programmable through the SPI interface. For battery charging applications, SETCUR can be programmed dynamically on-the-fly to set the charging currents to the batteries in either buck or boost mode. SETCUR can be used at start-up to limit the in-rush current in both buck mode and boost mode.

OPERATION

To defeat the average current programming operation, tie the SETCUR pin to V5 or voltage higher than 1.25V.

Buck and Boost Modes (BUCK Pin)

The LTC7871 can be dynamically and seamlessly switched from buck mode to boost mode and vice versa via the BUCK pin. Tie this pin to V5 to select buck mode and to ground to select boost mode operation. This pin has an internal pull up resistor that defaults to buck mode if left floating. There are two separate error amplifiers for V_{HIGH} or V_{LOW} regulation. Having two error amplifiers allows fine tuning of the loop compensation for the buck and boost modes independently to optimize transient response. When buck mode is selected, the corresponding error amplifier is enabled, and ITH_{LOW} voltage controls the peak inductor current. The other error amplifier is disabled and ITH_{HIGH} is parked at its zero current level. In boost mode, ITH_{HIGH} is enabled while ITH_{LOW} is parked at its zero current level. During a buck to boost or a boost to buck transition, the internal soft-start is reset. Resetting soft-start and parking the ITH pin at the zero current level ensures a smooth transition to the newly selected mode. Refer to Table 2 for a summary.

To further minimize any transients, SETCUR can be programmed to zero current level before switching between boost and buck modes.

Table 2. ITH PIN Parking Conditions

Pin	Mode	When Parked	Comments
ITH_{HIGH}	Buck	Normal Operation	OV_{HIGH} 2.4V Threshold Overrides Park
	Boost	Prebiased Turn-on	OV_{HIGH} 2.4V Threshold Overrides Park
ITH_{LOW}	Buck	Prebiased Turn-on	OV_{HIGH} 2.4V Threshold and OV_{LOW} Override Park
	Boost	Normal Operation	OV_{HIGH} 2.4V Threshold Overrides Park

Power Good (PGOOD Pin)

When the regulated VFB_{LOW}/VFB_{HIGH} voltage is not within ±10% of the 1.2V reference voltage, the PGOOD pin is pulled low. The PGOOD pin is also pulled low when the RUN pin is below 1.2V or when the LTC7871 is in the soft-start or UVLO. The PGOOD pin will flag power good immediately when the regulated VFB_{LOW}/VFB_{HIGH} voltage is within ±10% of the reference window. However, there is an internal 40µs power bad mask when regulated VFB_{LOW}/VFB_{HIGH} voltage goes out of the ±10% window. The PGOOD pin is allowed to be pulled up by an external resistor to sources of up to 6V.

Programmable V_{HIGH}, V_{LOW} Margining

As shown in the Figure 1, the LTC7871 has a SPI controlled 7-bit D/A converter current source. Through the SPI interface, the LTC7871 receives a 7-bit DAC code and converts this value to a bidirectional analog output current. The current is connected to the VFB_{LOW} pin in buck mode or the VFB_{HIGH} pin in boost mode. By connecting the DAC current to the feedback node of a voltage regulator, in buck mode, V_{LOW} voltage is programmed with the equation:

$$V_{LOW} = 1.2V \bullet (1 + R_B/R_A) - I_{DAC} \bullet R_B$$

In boost mode, V_{HIGH} voltage is programmed with the equation:

$$V_{HIGH} = 1.2V \bullet (1 + R_D/R_C) - I_{DAC} \bullet R_D$$

There are two different registers for V_{LOW} and V_{HIGH} programming, MFR_IDAC_VLOW and MFR_IDAC_VHIGH. The current DAC selects the register value based on the buck or boost mode. The current DAC's LSB is 1µA. The MSB determines the current direction. When MSB is 0, IDAC is sourcing current (reducing V_{LOW} or V_{HIGH}), which is positive current flowing out of the feedback pin. When MSB is 1, IDAC is sinking current (increasing V_{LOW} or V_{HIGH}), which is negative current flowing into the feedback pin.

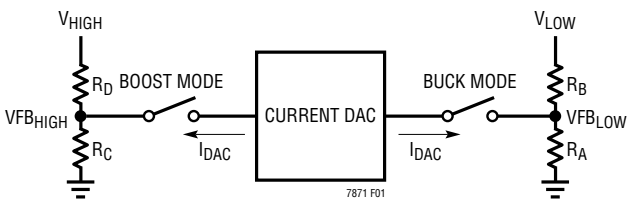


Figure 1. Current DAC for V_{LOW}/V_{HIGH} Programming

OPERATION

Buck Mode Light Load Current Operation (DCM/CCM/ Burst Mode Operation)

In buck mode, the LTC7871 can be enabled to enter discontinuous conduction mode (DCM), forced continuous conduction mode (CCM), or Burst Mode operation. To select forced continuous operation, tie the MODE pin to SGND. To select discontinuous conduction mode of operation, tie the MODE pin to V5. To select Burst Mode operation, float the MODE pin.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH_{LOW} pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in DCM operation. However, continuous mode has the advantages of lower output ripple and less interference with audio circuitry.

When the LTC7871 is enabled for Burst Mode operation, the peak current in the inductor is set to approximately one-third of the maximum sense voltage even though the voltage on the ITH_{LOW} pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier, EA, will decrease the voltage on the ITH_{LOW} pin. When the ITH_{LOW} voltage drops below 1.1V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator. When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (I_{REV}) turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous conduction mode.

When the MODE pin is connected to V5, the LTC7871 operates in discontinuous conduction mode at light loads. At very light loads, the current comparator, I_{CMP}, may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping-pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Boost Mode Light Load Current Operation (DCM/CCM)

In boost mode, the LTC7871 can be enabled to enter constant-frequency discontinuous conduction mode or forced continuous conduction mode. To select forced continuous operation, tie the MODE pin to SGND. To select discontinuous conduction mode of operation, tie the MODE pin to V5 or float it. In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The inductor current valley is determined by the voltage on the ITH_{HIGH} pin, just as in normal operation. In this mode, the efficiency at light loads is lower. However, continuous mode has the advantage of lower output ripple.

When the MODE pin is connected to V5 or floated, the LTC7871 operates in discontinuous conduction mode at light loads. At very light loads, the current comparator, I_{CMP}, may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping-pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference. It provides higher low current efficiency than forced continuous mode.

The LTC7871 operation mode is summarized in Table 3.

Table 3. Operation Mode

MODE Pin	Buck Operation Mode	Boost Operation Mode
0V	CCM	CCM
Float	Burst Mode Operation	DCM
V_{V5}	DCM	DCM

OPERATION

Overcurrent Fault Monitor (OCFT and NOCFT)

Besides the peak/valley current comparator and the maximum average current regulation loops, the LTC7871 has an additional overcurrent fault comparator to monitor the voltage difference between the SNSD+ and SNS– pins. If one channel's ($V_{SNSD}^+ – V_{SNS}^–$) is larger than overcurrent fault threshold (OCFT) or less than the negative overcurrent threshold (NOCFT) as shown in the Table 4, all six channels stop switching and all PWM pins are Hi-Z. The OCFT and NOCFT status can be obtained through the SPI interface by the MFR_OC_FAULT and MFR_NOC_FAULT registers.

Table 4. OCFT and NOCFT Threshold ($V_{SNSD}^+ – V_{SNS}^–$)

ILIM Pin Voltage	OCFT Threshold	NOCFT Threshold	Hysteresis
0V	37.5mV	–37.5mV	25mV
1/4 V_{V5}	50mV	–50mV	31mV
Float	62.5mV	–62.5mV	31mV
3/4 V_{V5}	75mV	–75mV	31mV
V_{V5}	87.5mV	–87.5mV	31mV

PWM and PWMEN Pins

The PWM pins are three-state compatible outputs, designed to drive power stages such as power blocks, DrMOS, and drivers with MOSFETs, none of which represents a heavy capacitive load. An external resistor divider may be used to set the PWM voltage to mid-rail while the PWM is in the high impedance state.

The PWMEN pin is an open-drain output pin. It should be pulled up by an external resistor to V5 when the controller starts switching. During any fault status, the LTC7871 pulls down the PWMEN pin to disable the external MOSFET driver.

The LTC7871's PWMEN pin is used to communicate the controller's status with the external MOSFET drivers or other LTC7871s. When the LTC7871 releases the PWMEN pin but finds it is still pulled down externally, the LTC7871 will keep all the PWM pins in Hi-Z status.

Multiphase Operation

For output loads that demand high current, multiple LTC7871s can be daisy chained to run out of phase to provide more output current without increasing input and output voltage ripple. The SYNC pin allows the LTC7871 to synchronize to the CLKOUT signal of another LTC7871. The CLKOUT signal can be connected to the SYNC pin of the following LTC7871 stage to line up both the frequency and the phase of the entire system. When paralleling multiple ICs, please be aware of the input impedance of pins connected to the same node.

Thermal Shutdown

The LTC7871 has a temperature sensor integrated on the IC, to sense the die temperature. When the die temperature exceeds 180°C, all switching actions stop, and all PWM pins become Hi-Z, thus turning off all external MOSFETs. At the same time, all the channels are disconnected from the IMON pins, and the SS and ITH_{HIGH}/ITH_{LOW} pins continue to function normally, so as not to interfere with other LTC7871 chips that may reference the common pins. When the temperature drops 15°C below the trip threshold, normal operation resumes.

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The Typical Application on the first page of this data sheet is a basic LTC7871 application circuit. In general, external component selection is driven by the load requirements, and begins with the DCR or R_{SENSE} and inductor value. Next, power MOSFETs are selected. Finally, V_{HIGH} and V_{LOW} capacitors are selected.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant frequency architectures by preventing subharmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, this results in a reduction of maximum inductor peak current for duty cycles > 40%. However, the LTC7871 uses a scheme that counteracts this compensating ramp, which allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

Current Limit Programming

The ILIM pin is a 5-level logic input which sets the maximum current limit of the controller. Table 5 shows the five ILIM settings. Please note that these settings represent the peak inductor current setting. Because of the inductor ripple current, the average output current is lower than the peak current. Setting ILIM using a resistor divider from V5 to SGND will allow the maximum current sense threshold setting to not change when the 5V LDO is in dropout at start-up. Please note that the ILIM pin has an internal 200k pull down resistor to SGND and a 200k pull up resistor to V5.

Table 5. ILIM Settings

	Maximum Current Sense Threshold	
ILIM Pin Voltage	DCR Sensing	R_{SENSE}
0V	10mV	12.5mV
1/4 V_{V5}	20mV	25mV
Float	30mV	37.5mV
3/4 V_{V5}	40mV	50mV
V_{V5}	50mV	62.5mV

SNSD+, SNSA+ and SNS– Pins

The SNSA+ and SNS– pins are the inputs to the current comparators, while the SNSD+ and SNS– pins are the input of an internal DC amplifier. The operating input voltage range is 0V to 60V for all three sense pins. All the positive sense pins that are connected to the current comparator or the amplifier are high impedance with input bias currents of less than 1µA. The SNS– pin is not a high impedance pin. For V_{LOW} voltages greater than V5, the current comparators derive their bias currents directly from the SNS– pins. The SNS– pins should be connected directly to V_{LOW}. Care must be taken not to float these pins during normal operation. Filter components, especially capacitors, must be placed close to the LTC7871, and the sense lines should run close together to a Kelvin connection underneath the current sense element (Figure 2). Because the LTC7871 is designed to be used with a very low value sensing element to sense inductor current, without proper care, the parasitic resistance, capacitance and inductance will degrade the current sense signal integrity, making the programmed current limit unpredictable. As shown in Figure 3, resistor R1 is placed close to the output inductor and capacitors C1 and C2 are close to the IC pins to prevent noise coupling to the sense signal.

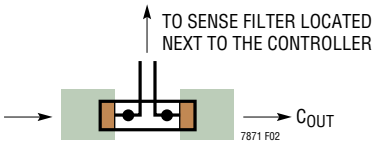

Figure 2. Sense Lines Placement with Sense Resistor

Inductor DCR Sensing

The LTC7871 is specifically designed for high load current applications requiring the highest possible efficiency; it is capable of sensing the signal of an inductor DCR in the milliohm range (Figure 3). The DCR is the DC winding resistance of the inductor's copper, which is often several mΩ for high current inductors. In high current applications, the conduction loss of a high DCR or a sense resistor will cause a significant reduction in power efficiency. The SNSA+ pin connects to the filter that has a R1 • C1 time constant one-fifth of the L/DCR of the inductor. The SNSD+ pin is connected to the second filter with the time

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constant matched to L/DCR of the inductor. For a specific output requirement, choose the inductor with the DCR that satisfies the maximum desired sense voltage, and uses the relationship of the sense pin filters to output inductor characteristics as depicted below.

$$DCR = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

$$\frac{L}{DCR} = 5 \bullet R1 \bullet C1 = R2 \bullet C2$$

where:

$V_{SENSE(MAX)}$ is the maximum sense voltage for a given ILIM threshold

ΔI_L is the Inductor ripple current

L and DCR are the output inductor characteristics

R1 • C1 is the filter time constant of the $SNSA^+$ pin

R2 • C2 is the filter time constant of the $SNSD^+$ pin

To ensure that the load current will be delivered over the full operating temperature range, the temperature coefficient of DCR resistance, approximately 0.4%/°C, should be taken into account.

Typically, C1 and C2 are selected in the range of 0.047µF to 0.47µF. If C1 and C2 are chosen to be 0.1µF, and an inductor of 10µH with 2mΩ DCR is selected, R1 and R2 will be 10k and 49.9k, respectively. The bias current at $SNSD^+$ and $SNSA^+$ is less than 1µA, and it introduces a small error to the sense signal.

There will be some power loss in R1 that relates to the duty cycle, and will be the most in continuous mode at the maximum V_{HIGH} voltage:

$$P_{LOSS}(R) = \frac{\left(V_{HIGH(MAX)} - V_{LOW}\right) \bullet V_{LOW}}{R}$$

Ensure that R1 has a power rating higher than this value. Care has to be taken for voltage coefficients of these resistors at high V_{HIGH} voltages. Multiple resistors can be used in series to minimize this effect. However, DCR sensing eliminates the conduction loss of a sense resistor; it also provides better efficiency at heavy loads. To maintain a good signal-to-noise ratio for the current sense signal, use a minimum of 10mV between $SNSA^+$ and SNS^- pins or the equivalent of 2mV ripple on the current sense signal for duty cycles less than 40%. The actual ripple voltage across $SNSA^+$ and SNS^- pins will be determined by the following equation:

$$\Delta V_{SENSE} = \frac{V_{LOW}}{V_{HIGH}} \bullet \frac{V_{HIGH} - V_{LOW}}{R1 \bullet C1 \bullet f_{OSC}}$$

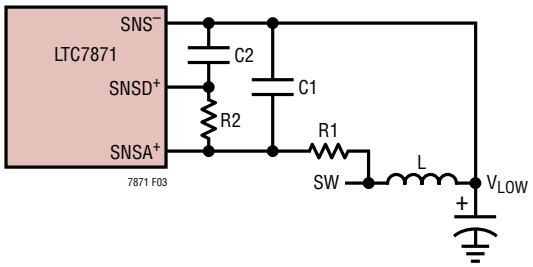

Figure 3. Inductor DCR Sensing

Sensing Using an R_{SENSE} Resistor

The LTC7871 can be used with an external R_{SENSE} resistor to sense current accurately. The external components required to accomplish this are shown in Figure 4. The $SNSD^+$ pin senses directly across the R_S resistor through R3 and C3 network. The R1, R2, and C1 network provide the current signal path to the $SNSA^+$ pin. Internally the signals from the AC and DC paths are combined for accurate current sensing and low jitter performance. Resistor R2 is used to divide down the DC component of the signal seen by $SNSA^+$ due to the DCR of the inductor. As a rule of thumb, R2 needs to be 10 times smaller than R1 so the DCR value can be safely ignored.

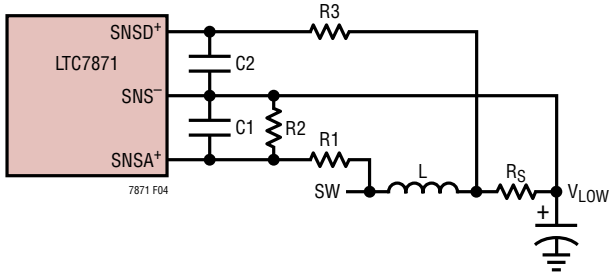

Figure 4. R_{SENSE} Resistor Sensing

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The R1 • C1 time constant should be selected such that:

$$\frac{L}{R_S} = 4 \bullet R1 \bullet C1 \text{ for } R1 = 10 \bullet R2$$

The R3 • C2 time constant should be selected such that:

$$R3 \bullet C2 = \frac{R1 \bullet R2}{R1 + R2} \bullet C1$$

If a 6.8µH inductor and a 1mΩ sense resistor are selected and C1 and C2 are chosen to be 0.1µF, then the values for R1, R2 and R3 will be 16.9k, 1.69k and 1.5k, respectively when the nearest standard value is chosen.

Pre-Biased Output Start-Up

There may be situations that require the power supply to start up with a prebias on the V_{LOW} output capacitors. In this case, it is desirable to start up without discharging that output prebias. The LTC7871 can safely power up into a prebiased output without discharging it.

The LTC7871 accomplishes this by disabling both the top and bottom MOSFETs until the SS pin voltage and the internal soft-start voltage are above the VFB_{LOW} pin voltage. When VFB_{LOW} is higher than SS or the internal soft-start voltage, the error amp output is parked at its zero current level. Disabling both top and bottom MOSFETs prevents the prebiased output voltage from being discharged. When SS and the internal soft-start both cross 1.32V or VFB_{LOW}, whichever is lower, both top and bottom MOSFETs are enabled.

Overcurrent Fault Protection

In the buck mode, when the output of the power supply is loaded beyond its preset current limit, the regulated output voltage will collapse depending on the load. The V_{LOW} rail may be shorted to ground through a very low impedance path or it may be a resistive short, in which case the output will collapse partially, until the load current equals the preset current limit. The controller will continue to source current into the short. The amount of current sourced depends on the ILIM pin setting and the VFB_{LOW} voltage as shown in the Current Foldback graph in the Typical Performance Characteristics section.

Upon removal of the short, V_{LOW} soft starts using the internal soft-start, thus reducing output overshoot. In the absence of this feature, the output capacitors would have been charged at current limit, and in applications with minimal output capacitance this may have resulted in output overshoot. Current limit foldback is not disabled during an overcurrent recovery. The load must drop below the folded back current limit threshold in order to restart from a hard short.

In both buck and boost modes of operation, forcing a voltage on the SETCUR pin regulates the average current. Zero average inductor current can be obtained by forcing 0V on SETCUR.

The LTC7871 has additional overcurrent fault comparators to monitor the current of each channel. If there is any catastrophic failure in the system which causes one or more channel's inductor current to be higher than the overcurrent fault threshold, all the channels will be shut down and both the PWMEN and the $\overline{FAULT}$ pins will be pulled down to SGND.

Another way to protect against overcurrent is to monitor the IMON pin voltage. If the IMON voltage indicates excessive current, an external circuit can be used to shut down the system.

Inductor Value Calculation

Given the desired input and output voltages, the inductor value and operating frequency, f_{OSC}, directly determine the inductor's peak-to-peak ripple current:

$$I_{RIPPLE} = \frac{V_{LOW}}{V_{HIGH}} \left(\frac{V_{HIGH} - V_{LOW}}{f_{OSC} \bullet L} \right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor.

A reasonable starting point is to choose a ripple current that is about 40% of the maximum inductor current. Note that the largest ripple current occurs at the highest V_{HIGH} voltage. To guarantee that ripple current does not exceed

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a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{HIGH} - V_{LOW}}{f_{OSC} \bullet I_{RIPPLE}} \bullet \frac{V_{LOW}}{V_{HIGH}}$$

Inductor Core Selection

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET and Schottky Diode (Optional) Selection

At least two external power MOSFETs need to be selected: One N-channel MOSFET for the top switch and one or more N-channel MOSFET(s) for the bottom switch. The number, type and on-resistance of all MOSFETs selected take into account the voltage step-down ratio as well as the actual position (top or bottom) in which the MOSFET will be used. A much smaller and much lower input capacitance MOSFET should be used for the top MOSFET in applications that have an V_{LOW} that is less than one-third of V_{HIGH}. In applications where $V_{HIGH} >> V_{LOW}$, the top MOSFETs’ on-resistance is normally less important for overall efficiency than its input capacitance at operating frequencies above 300kHz. MOSFET manufacturers have designed special purpose devices that provide reasonably low on-resistance with significantly reduced input capacitance for the top switch application in switching regulators.

The peak-to-peak MOSFET gate drive levels are set by the internal DRV_{CC} regulator voltage. Pay close attention to the BV_{DSS} specification for the MOSFETs as well. Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, input capacitance, input voltage and maximum output current. MOSFET input capacitance is a combination of several components but can be taken from the typical gate charge curve included on most data sheets (Figure 5). The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time.

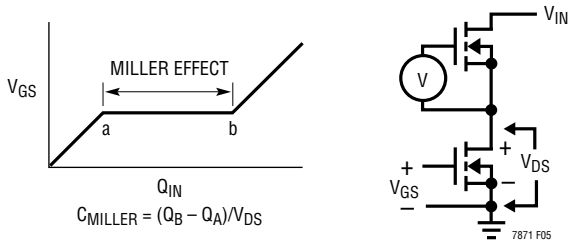

Figure 5. Gate Charge Characteristic

The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltages by multiplying the ratio of the application V_{DS} to the curve specified V_{DS} values. A way to estimate the C_{MILLER} term is to take the change in gate charge from points a and b on a manufacturer’s data sheet and divide by the stated V_{DS} voltage specified. C_{MILLER} is the most important selection criteria for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. C_{RSS} and C_{OS} are specified sometimes but definitions of these parameters are not included. When

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the controller is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Top Switch Duty Cycle} = \frac{V_{LOW}}{V_{HIGH}}$$

$$\text{Bottom Switch Duty Cycle} = \left(\frac{V_{HIGH} - V_{LOW}}{V_{HIGH}}\right)$$

The power dissipation for the top and bottom MOSFETs at maximum output current are given by:

$$P_{TOP} = \frac{V_{LOW}}{V_{HIGH}}\left(I_{MAX}\right)^2(1+\delta)R_{DS(ON)} +$$

$$(V_{HIGH})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet$$

$$\left[\frac{1}{DRV_{CC} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right]\bullet f$$

$$P_{BOT} = \frac{V_{HIGH} - V_{LOW}}{V_{HIGH}}\left(I_{MAX}\right)^2(1+\delta)R_{DS(ON)}$$

I_{MAX} = Maximum Inductor Current.

where δ is the temperature dependency of $R_{DS(ON)}$, R_{DR} is the effective top driver resistance; V_{HIGH} is the drain potential and the change in drain potential in the particular application. $V_{TH(MIN)}$ is the data sheet specified typical gate threshold voltage specified in the power MOSFET data sheet at the specified drain current. C_{MILLER} is the calculated capacitance using the gate charge curve from the MOSFET data sheet and the technique described above.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which peak at the highest input voltage. The bottom MOSFET losses are greatest at high V_{HIGH} voltage when the top switch duty factor is low or during a V_{LOW} short-circuit when the bottom switch is on close to 100% of the period.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

An optional Schottky diode across the bottom MOSFET conducts during the dead time between the conduction of the two large power MOSFETs in buck mode. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead time and requiring a reverse-recovery period which could cost as much as several percent in efficiency. A 2A to 8A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition loss due to their larger junction capacitance.

C_{HIGH} and MOSFETs Selection (on V_{HIGH} and V_{LOW})

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{LOW})/(V_{HIGH})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. In the following discussion, it is assumed that C_{IN} is C_{HIGH}, C_{OUT} is C_{LOW}, V_{IN} is V_{HIGH}, and V_{OUT} is V_{LOW}. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[\left(V_{OUT}\right)\left(V_{IN} - V_{OUT}\right)\right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of use.

This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

Ceramic capacitors are becoming very popular for small designs but several cautions should be observed. X7R, X5R and Y5V are examples of a few of the ceramic materials used as the dielectric layer, and these different dielectrics have very different effect on the capacitance value due to the voltage and temperature conditions applied. Physically, if the capacitance value changes due to applied voltage change, there is a concomitant piezo effect which results

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in radiating sound! A load that draws varying current at an audible rate may cause an attendant varying input voltage on a ceramic capacitor, resulting in an audible signal. A secondary issue relates to the energy flowing back into a ceramic capacitor whose capacitance value is being reduced by the increasing charge. The voltage can increase at a considerably higher rate than the constant current being supplied because the capacitance value is decreasing as the voltage is increasing! Nevertheless, ceramic capacitors, when properly selected and used, can provide the lowest overall loss due to their extremely low ESR.

A small (0.1µF to 1µF) capacitor, C_{IN}, placed close to the LTC7871 between the V_{IN} pin and ground, bypasses switching noise to ground. A 2.2Ω to 10Ω resistor, placed between C_{IN} and V_{HIGH} pins decouples the V_{HIGH} pin from switching noise.

The selection of C_{OUT} at V_{OUT} is driven by the required effective series resistance (ESR). Typically once the ESR requirement is satisfied the capacitance is adequate for filtering. The steady-state output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_{RIPPLE}\left(ESR + \frac{1}{8fC_{OUT}}\right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_{RIPPLE} = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_{RIPPLE} increases with input voltage (V_{HIGH}). The output ripple will be less than 50mV at maximum V_{IN} with ΔI_{RIPPLE} = 0.4 $I_{OUT(MAX)}$ assuming:

C_{OUT} required ESR < N • R_{SENSE}

and

$$C_{OUT} > \frac{1}{(8f)(R_{SENSE})}$$

The emergence of very low ESR capacitors in small, surface mount packages makes very small physical implementations possible. The ability to externally compensate the switching regulator loop using the ITH pin allows a much wider selection of output capacitor types. The impedance characteristic of each capacitor type is significantly different from that of an ideal capacitor and therefore requires accurate modeling or bench evaluation during design. Manufacturers such as Nichicon, Nippon Chemi-Con and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitors available from Sanyo and the Panasonic SP surface mount types have a good (ESR)(size) product.

Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P–P)}$ requirement. Ceramic capacitors from AVX, Taiyo Yuden, Murata and TDK offer high capacitance value and very low ESR, especially applicable for low output voltage applications.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent choices are the AVX TPS, AVX TPSV, the KEMET T510 series of surface mount tantalums or the Panasonic SP series of surface mount special polymer capacitors available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo POSCAP, Sanyo OS-CON, Nichicon PL series and Sprague 595D series. Consult the manufacturers for other specific recommendations.

C_{HIGH} Capacitor Selection for Boost Operation

Contributions of ESR (equivalent series resistance), ESL (equivalent series inductance) and the bulk capacitance must be considered when choosing the correct combination of output capacitors for a boost converter application.

The choice of component(s) begins with the maximum acceptable ripple voltage (expressed as a percentage of the output voltage), and how this ripple should be divided between the ESR step and the charging/discharging ΔV. For the purpose of simplicity we will choose 2% for the maximum output ripple, to be divided equally between the ESR step and the charging/discharging ΔV. This percentage

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ripple will change, depending on the requirements of the application, and the equations provided below can easily be modified.

One of the key benefits of multiphase operation is a reduction in the peak current supplied to the output capacitor by the boost diodes. As a result, the ESR requirement of the capacitor is relaxed. For a 1% contribution to the total ripple voltage, the ESR of the output capacitor can be determined using the following equation:

$$ESR_{COUT} > \frac{0.01 \bullet V_{OUT}}{I_{D(PEAK)}}$$

where:

$$I_{D(PEAK)} = \frac{1}{n} \bullet \left(1 + \frac{\chi}{2}\right) \bullet \frac{I_{O(MAX)}}{1 - D_{MAX}}$$

The factor n represents the number of phases and the factor χ represents the percentage inductor ripple current.

For the bulk capacitance, which we assume contributes 1% to the total output ripple, the minimum required capacitance is approximately:

$$C_{OUT} \geq \frac{I_{O(MAX)}}{0.01 \bullet n \bullet V_{OUT} \bullet f}$$

For many designs it will be necessary to use one type of capacitor to obtain the required ESR, and another type to satisfy the bulk capacitance. For example, using a low ESR ceramic capacitor can minimize the ESR step, while an electrolytic capacitor can be used to supply the required bulk C.

The voltage rating of the output capacitor must be greater than the maximum output voltage, with sufficient derating to account for the maximum capacitor temperature.

Because the ripple current in the output capacitor is a square wave, the ripple current requirements for this capacitor depend on the duty cycle, the number of phases and the maximum output current. In order to choose a ripple current rating for the output capacitor, first establish the duty cycle range, based on the output voltage and range of input voltage.

The output ripple current is divided between the various capacitors connected in parallel at the output voltage. Although ceramic capacitors are generally known for low ESR (especially X5R and X7R), these capacitors suffer from a relatively high voltage coefficient. Therefore, it is not safe to assume that the entire ripple current flows in the ceramic capacitor. Aluminum electrolytic capacitors are generally chosen because of their high bulk capacitance, but they have a relatively high ESR. As a result, some amount of ripple current will flow in this capacitor. If the ripple current flowing into a capacitor exceeds its RMS rating, the capacitor will heat up, reducing its effective capacitance and adversely affecting its reliability. After the output capacitor configuration has been determined using the equations provided, measure the individual capacitor case temperatures in order to verify good thermal performance.

Setting Output Voltage

The LTC7871 output voltage is set by two external feedback resistive dividers carefully placed across V_{HIGH} to ground and V_{LOW} to ground, as shown in Figure 6. The regulated output voltage is determined by:

$$V_{LOW} = 1.2V \bullet \left(1 + \frac{R_B}{R_A}\right) \text{ and } V_{HIGH} = 1.2V \bullet \left(1 + \frac{R_D}{R_C}\right)$$

To improve the frequency response, a feed forward capacitor, C_{FF1}/C_{FF2}, may be used. Great care should be taken to route the feedback line away from noise sources, such as the inductor or the SW line.

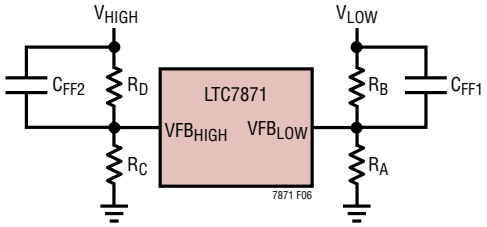

Figure 6. Setting Output Voltage

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External Soft-Start

The LTC7871 has the ability to soft-start by itself using the internal soft-start or at a slower rate with an external capacitor on the SS pin. The controller is in the shutdown state if its RUN pin voltage is below 1.14V and its SS pin is actively pulled to ground in this shutdown state. If the RUN pin voltage is above 1.22V, the controller powers up. Once V5 and DRV_{CC} pass the UVLO thresholds and power on reset delay expires, a soft-start current of 1µA then starts to charge the SS soft-start capacitor. Note that soft-start is achieved not by limiting the maximum V_{LOW} output current of the controller but by controlling the output ramp voltage according to the ramp rate on the SS pin. Current foldback is disabled during this phase. The soft-start range is defined to be the voltage range from 0V to 1.2V on the SS pin. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = 1.2 \bullet \frac{C_{SS}}{1\mu A}$$

The Internal LDOs

The LTC7871 features three internal PMOS LDOs. Two provide power to DRV_{CC} from either the V_{HIGH} or V_{LOW} supply, and the third provides the V5 rail from DRV_{CC}. DRV_{CC} powers the external top and bottom gate drive circuits, and V5 powers the LTC7871's internal circuitry.

There are two DRV_{CC} LDOs—one that converts DRV_{CC} from V_{HIGH} (LDO1) and another that converts DRV_{CC} from V_{LOW} (LDO2), thus allowing the part to start up with just one of the two rails present! Only one of those LDOs is active at any given time. If V_{LOW} is higher than the $EXTV_{CC}$ switchover threshold, LDO2 is active; if it is below the switchover threshold, LDO1 is active. The DRV_{CC} pin regulation voltage is determined by the state of the DRVSET pin. The DRVSET pin uses a 3-level logic. When DRVSET is either grounded, floated or tied to V5, the typical value for the DRV_{CC} voltage will be 5V, 8V and 10V, respectively. Please note that the DRVSET pin has an internal 160kΩ pull down resistor to SGND and a 200kΩ pull up resistor to V5.

The V5 LDO regulates the voltage at the V5 pin to 5V when DRV_{CC} is at least 6V. The LDO can supply a peak current of 20mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the V5 and SGND pins is highly recommended.

Fault Conditions: Current Limit and Current Foldback

In buck mode, the LTC7871 includes current foldback to help limit power dissipation when the V_{LOW} is shorted to ground. If the V_{LOW} falls below 33% of its nominal output level, then the maximum sense voltage is progressively lowered from its maximum programmed value to one-third of the maximum value. Foldback current limiting is disabled during soft-start. Under short-circuit conditions with very low duty cycles, the LTC7871 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short circuit ripple current is determined by the minimum on-time $t_{ON(MIN)}$ of the LTC7871, the V_{HIGH} voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \bullet \frac{V_{HIGH}}{L}$$

The resulting short circuit current is:

$$I_{SC} = \left(\frac{1/3\, V_{SENSE(MAX)}}{R_{SENSE}} - \frac{1}{2} \Delta I_{L(SC)} \right)$$

After a short, make sure that the load current takes the folded back current limit into account.

Phase-Locked Loop and Frequency Synchronization

The LTC7871 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the turn-on of the top MOSFET to be locked to the rising edge of an external clock signal applied to the SYNC pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the internal filter network. There is a precision 20µA current

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flowing out of the FREQ pin. This allows the user to use a single resistor to SGND to set the switching frequency when no external clock is applied to the SYNC pin. The internal switch between the FREQ pin and the integrated PLL filter network is on, allowing the filter network to be pre-charged at the same voltage as of the FREQ pin. The relationship between the voltage on the FREQ pin and operating frequency is shown in Figure 7 and specified in the Electrical Characteristics table. If an external clock is detected on the SYNC pin, the internal switch mentioned above turns off and isolates the influence of the FREQ pin. Note that the LTC7871 can only be synchronized to an external clock whose frequency is within range of the LTC7871's internal VCO. A simplified block diagram is shown in Figure 8.

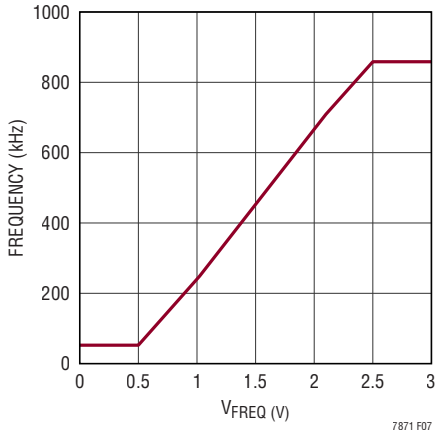

Figure 7. Relationship Between Oscillator Frequency and Voltage at the FREQ Pin

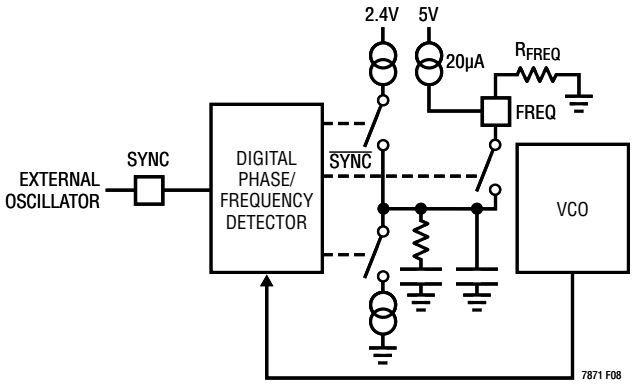

Figure 8. Phase-Locked Loop Block Diagram

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the filter network. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the filter network. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the filter network is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor holds the voltage.

Typically, the external clock (on the SYNC pin) input high threshold is 2V, while the input low threshold is 1.1V. The LTC7871 switching frequency is determined by:

$$\text{Frequency} = V_{FREQ} \bullet 414\text{kHz/V} - 163.5\text{kHz}$$

where, $V_{FREQ} = I_{FREQ}$ (from spec table) $\bullet R_{FREQ}$

Or,

$$\text{Frequency} = R_{FREQ} \bullet 8.28\text{kHz/k}\Omega - 163.5\text{kHz}$$

This assumes a perfect 20µA I_{FREQ}.

Shared Pin Connections in Multichip Applications

When multiple LTC7871 ICs are used together in high current applications, the customer may or may not connect certain pins together, balancing better communication between the ICs versus avoiding a single point failure.

The CLKOUT pin allows multiple LTC7871s to be daisy chained together. The clock output signal on the CLKOUT pin can be used to synchronize additional ICs in a multiphase power supply solution feeding a single high current output, or even several outputs from the same input supply.

The SS and PWMEN pins should be tied together to enable every LTC7871 IC to start up together. Not connecting them together may result in some phases sourcing a lot of current and others sinking current.

The IMON pins may or may not be tied together, depending on whether the customer wants to monitor the average current per IC or the total average current in the application.

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The ILIM, SETCUR, FREQ, MODE, BUCK, and DRVSET pins may or may not be tied together based on convenience. When tying these pins together, please be aware of the pull-up/down currents/resistors on these pins! Any external resistor or resistor divider network must take those into account. For example, each FREQ pin sources 20µA. When two LTC7871 ICs have their FREQ pins tied together, that is 40µA.

The OV_{LOW}, OV_{HIGH} and UV_{HIGH} pins of multiple LTC7871s must be tied together. This enables the entire system to react to an OV/UV condition appropriately. The resistor divider used on these pins must be scaled based on the number of LTC7871s paralleled, as these pins have 5µA hysteresis currents that turn on and off.

The ITH_{LOW} and ITH_{HIGH} pins of multiple LTC7871s should be tied together. Tying the ITH_{LOW} pins together and the ITH_{HIGH} pins together gives the best current sharing between phases. Each error amplifier's compensation network must be placed local to the specific IC to minimize jitter and stability issues.

The RUN pins must be tied together – this is very critical for boost mode operation. In boost mode, when multiple LTC7871 have their RUN pins connected together, care must be taken to ensure that the logic signal on the RUN pin is a clean fast rising/falling signal so all ICs are enabled at the same instant. If a resistor divider is used on the RUN pin, then the part must be started up in buck mode. Using a resistor divider on the RUN pin off V_{HIGH}, set for a start-up voltage higher than the UV_{HIGH} set point, allows the part to soft start cleanly after a UV_{HIGH} fault is cleared.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC7871 is capable of turning on the top MOSFET. It is determined by internal timing delays, power stage timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{LOW}}{V_{HIGH}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage and current will continue to be regulated, but the voltage ripple and current ripple will increase. The minimum on-time for the LTC7871 is approximately 150ns, with good PCB layout, minimum 30% inductor current ripple and at least 2mV ripple on the current sense signal or equivalent 10mV between $SNSA^+$ and SNS^- pins.

The minimum on-time can be affected by PCB switching noise in the voltage and current loop. As the peak sense voltage decreases, the minimum on-time gradually increases. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC7871 circuits: 1) IC V_{HIGH} current, 2) MOSFET driver current, 3) I^2R losses, 4) top MOSFET transition losses.

1. The V_{HIGH} current is the DC supply current given in the Electrical Characteristics table. V_{HIGH} current typically results in a small (<0.1%) loss.
2. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge d_Q moves from the driver supply to ground. The resulting d_Q/d_t is a current

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out of the driver supply that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the top and bottom MOSFETs.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFETs, inductor and current sense resistor. In continuous mode, the average output current flows through L and R_{SENSE}, but is chopped between the top MOSFET and the bottom MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain I^2R losses. For example, if each $R_{DS(ON)} = 10m\Omega$, $R_L = 10m\Omega$, $R_{SENSE} = 5m\Omega$, then the total resistance is $25m\Omega$. This results in losses ranging from 0.6% to 3% as the output current increases from 3A to 15A for a 12V output in buck mode.

   Efficiency varies as the inverse square of V_{LOW} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the top MOSFET(s), and become significant only when operating at high V_{HIGH} voltages (typically 15V or greater). Transition losses can be estimated from:

   $$\text{Transition Loss} = (1.7)\, V_{HIGH}^2 \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f$$

   $I_{O(MAX)}$ = Maximum Load on V_{LOW}

Other hidden losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{HIGH} has adequate charge storage and very low ESR at the switching frequency. Other losses including Schottky conduction losses during dead time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{LOW} shifts by an amount equal to $\Delta I_{LOAD} \bullet$ ESR, where ESR is the effective series resistance of C_{OUT} at V_{LOW}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{LOW} to its steady-state value. During this recovery time V_{LOW} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the ITH pin not only allows optimization of control loop behavior but also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in the Typical Application circuit will provide an adequate starting point for most applications. The ITH series RC-CC filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing RC and the

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bandwidth of the loop will be increased by decreasing CC. If RC is increased by the same factor that CC is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{LOW}, causing a rapid drop in V_{LOW}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

SERIAL PORT

The SPI-compatible serial port provides control and monitoring functionality.

Communication Sequence

The serial bus is comprised of CSB, SCLK, SDI and SDO. Data transfers to the part are accomplished by the serial bus master device first taking CSB low to enable the LTC7871's port. Input data applied on SDI is clocked on the rising edge of SCLK, with all transfers MSB first. The communication burst is terminated by the serial bus master returning CSB high. See Figure 9 for details.

Data is read from the part during a communication burst using SDO. Readback may be multidrop (more than one LTC7871 connected in parallel on the serial bus), as SDO is high impedance (Hi-Z) when CSB = 1, or when data is not being read from the part. If the LTC7871 is not used in a multidrop configuration, or if the serial port master is not capable of setting the SDO line level between read sequences, it is recommended to attach a resistor between SDO and V5 to ensure the line returns to V5 during Hi-Z states. The resistor value should be large enough to ensure that the SDO output current does not exceed 10mA. See Figure 10 for details.

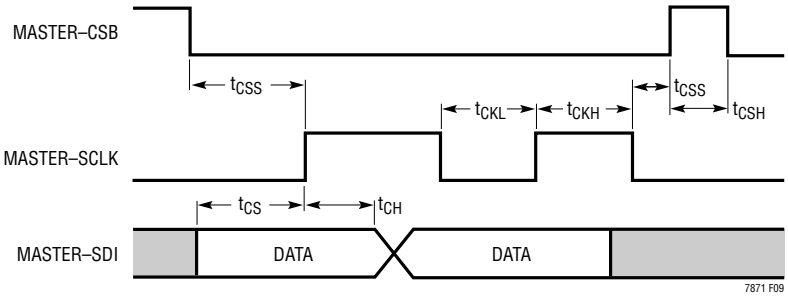

Figure 9. Serial Port Write Timing Diagram

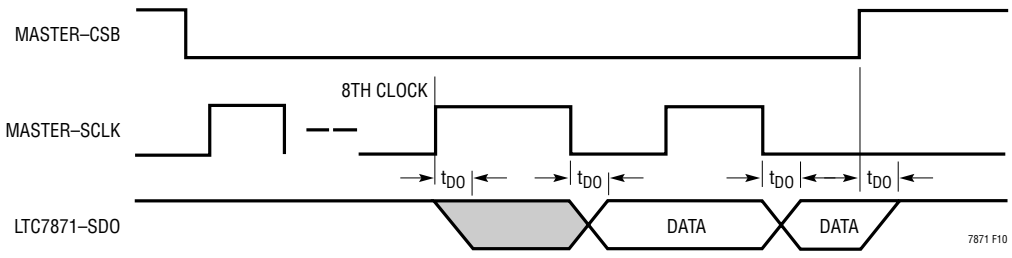

Figure 10. Serial Port Read Timing Diagram

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Single Byte Transfers

The serial port is arranged as a simple memory map, with status and control available in 5 read/write and 6 read only byte-wide registers. All data bursts are comprised of at least three bytes. The 7 most significant bits (MSB) of the first byte are the register address, with an LSB of 1 indicating a read from the part, and LSB of 0 indicating a write to the part. The second byte, is data from/to the specified register address. The third byte, is the PEC (packet error code) byte. See Figure 11 for an example of a detailed write sequence, and Figure 12 for a read sequence. All bytes shift with MSB first.

Figure 13 shows an example of two write communication bursts. The first byte of the first burst sent from the

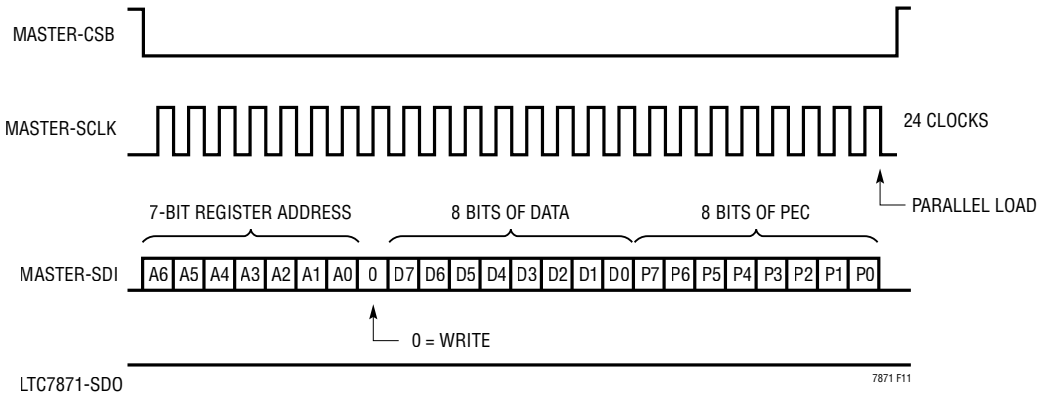

Figure 11. Serial Port Write Sequence

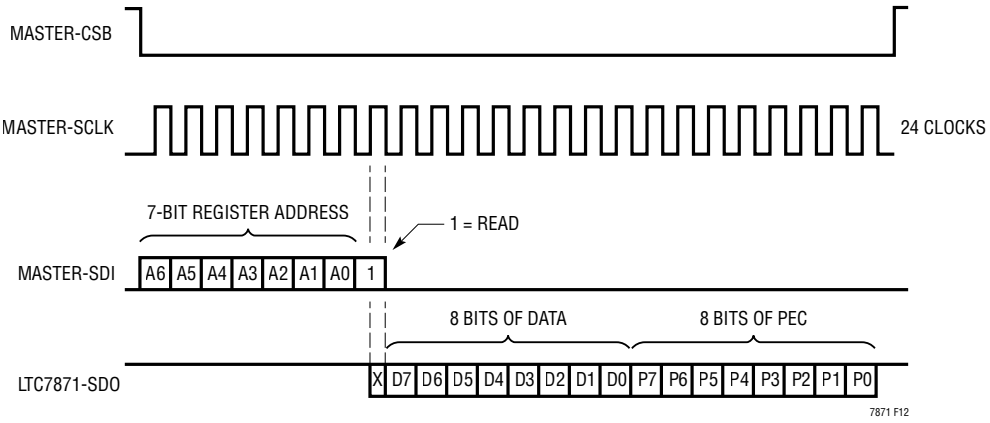

Figure 12. Serial Port Read Sequence

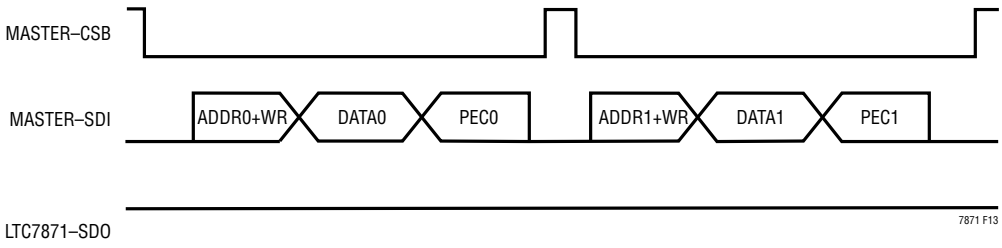

Figure 13. Two Write Communication Bursts

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serial bus master on SDI contains the destination register address (ADDR0) and a following 0 indicating a write. The next byte is the DATA0 intended for the register at address ADDR0. The third byte is the PEC0. CSB is then taken high to terminate the transfer. The first byte of the second burst contains the destination register address (ADDR1) and a following 0 indicating a write. The next byte on SDI is the DATA1 intended for the register at address ADDR1. The third byte is the PEC1. CSB is then taken high to terminate the transfer. Note that the written data is transferred to the internal register at the falling edge of the 24th clock cycle (parallel load) in each burst after the PEC is checked as valid.

PEC Byte

The PEC byte a cyclic redundancy check (CRC) value calculated for all the bits in a register group in the order they are passed, using the initial PEC value of 01000001 (0x41) and the following characteristic polynomial:

$$x^8 + x^2 + x + 1$$

To calculate the 8-bit PEC value, a simple procedure can be established:

1. Initialize the PEC to 0100 0001.
2. For each bit DIN coming into the register group, set IN0 = DIN XOR PEC[7], then IN1=PEC[0] XOR IN0, IN2 = PEC[1] XOR IN0.
3. Update the 8-bit PEC as PEC[7] = PEC[6], PEC[6] = PEC[5],……PEC[3] = PEC[2], PEC[2] = IN2, PEC[1] = IN1, PEC[0] = IN0.
4. Go back to step 2 until all data are shifted. The 8-bit result is the final PEC byte.

An example to calculate the PEC is listed in Table 6 and Figure 14. The PEC of the 1 byte data 0x01 is computed as 0xC7 after the last bit of the byte clocked in.

For the serial port write sequence, the master calculates the PEC byte for the address byte and data byte it sends out. The master latches the PEC byte it calculates at the 15th clock falling edge and attaches the calculated PEC byte following the data byte it shifts out. The LTC7871 also calculates PEC byte for the address byte and data byte it receives. The LTC7871 latches the PEC byte it calculates at the 16th clock rising edge and compares it with the PEC byte following the data byte. The data is regarded as valid only if the PEC bytes match.

For the serial port read sequence, the LTC7871 calculates PEC byte for the received address byte and data byte it sends out. The LTC7871 latches the PEC byte at the 15th clock falling edge and attaches the calculated PEC byte following the data byte it shifts out. The master calculates PEC byte for the address byte it sends and data byte it receives. The master latches the PEC byte at the 16th clock rising edge and compares it with the PEC byte following the data byte it receivers. The data is regarded as valid only if the PEC bytes match.

Table 6. Procedure to Calculate PEC Byte

CLOCK CYCLE	DIN	IN0	IN1	IN2	PEC[7]	PEC[6]	PEC[5]	PEC[4]	PEC[3]	PEC[2]	PEC[1]	PEC[0]
0	0	0	1	0	0	1	0	0	0	0	0	1
1	0	1	1	0	1	0	0	0	0	0	1	0
2	0	0	1	1	0	0	0	0	0	0	1	1
3	0	0	0	1	0	0	0	0	0	1	1	0
4	0	0	0	0	0	0	0	0	1	1	0	0
5	0	0	0	0	0	0	0	1	1	0	0	0
6	0	0	0	0	0	0	1	1	0	0	0	0
7	1	1	1	1	0	1	1	0	0	0	0	0
8					1	1	0	0	0	1	1	1

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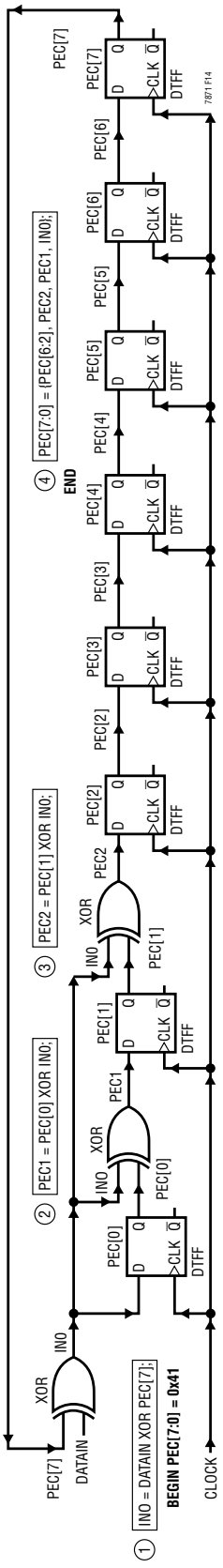

Figure 14. 8-Bit PEC Computation Circuit

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Multidrop Configuration

Several LTC7871s may share the serial bus. In this multidrop configuration, SCLK, SDI, and SDO are common between all parts. The serial bus master must use a separate CSB for each LTC7871 and ensure that only one device has CSB asserted at any time during the serial port read sequence. It is recommended to attach a high value resistor to SDO to ensure the line returns to a known level during Hi-Z states.

Serial Port Register Definition

Table 7. Register Summary

Register NAME	Register Address (7 bits)	Description	TYPE	DEFAULT VALUE
MFR_FAULT	0x01	One byte summary of the unit's fault condition.	R	
MFR_OC_FAULT	0x02	One byte summary of the unit's overcurrent fault condition.	R	
MFR_NOC_FAULT	0x03	One byte summary of the unit's negative overcurrent fault condition.	R	
MFR_STATUS	0x04	One byte summary of the unit's operation status.	R	
MFR_CONFIG1	0x05	One byte summary of the unit's configuration	R	
MFR_CONFIG2	0x06	One byte summary of the unit's configuration	R	
MFR_CHIP_CTRL	0x07	[3] = Communication Fault, [1] = Sticky Bit, [0] = Write Protection	R/W	0x00
MFR_IDAC_VLOW	0x08	Adjust the IDAC_VLOW to program V_{LOW} voltage.	R/W	0x00
MFR_IDAC_VHIGH	0x09	Adjust the IDAC_VHIGH to program V_{HIGH} voltage.	R/W	0x00
MFR_IDAC_SETCUR	0x0A	Adjust the IDAC_SETCUR to program SETCUR pin's sourcing current.	R/W	0x00
MFR_SSFM	0x0B	Adjust the spread spectrum frequency modulation parameters.	R/W	0x00
RESERVED	0x0C 0x0D 0x0E 0x0F			

SERIAL PORT REGISTER DETAILS

MFR_FAULT

The MFR_FAULT returns a one-byte summary of the most critical faults.

MFR_FAULT Register Contents:

BIT	NAME	VALUE	MEANING
7			Reserved
6	VLOW_OV	1	The OV_{LOW} pin is higher than 1.2V threshold.
5	VHIGH_OV	1	The OV_{HIGH} pin is higher than 1.2V threshold.
4	VHIGH_UV	1	The UV_{HIGH} pin is less than 1.2V threshold.
3	DRVCC_UV	1	The DRV_{CC} pin is undervoltage.
2	V5_UV	1	The V5 pin is undervoltage.
1	VREF_BAD	1	The internal reference self-check fails.
0	OVER_TEMP	1	An over temperature fault has occurred.

APPLICATIONS INFORMATION

MFR_OC_FAULT

The MFR_OC_FAULT returns a one-byte summary of overcurrent fault condition. When the voltage difference between $SNSD^+$ and SNS^- pins is larger than the overcurrent fault threshold programmed by the ILIM pin, the corresponding register bit will become 1.

MFR_OC_FAULT Register Contents:

BIT	NAME	VALUE	MEANING
7:6			Reserved
5	OC_FAULT_6	1	Channel 6 overcurrent fault has occurred.
4	OC_FAULT_5	1	Channel 5 overcurrent fault has occurred.
3	OC_FAULT_4	1	Channel 4 overcurrent fault has occurred.
2	OC_FAULT_3	1	Channel 3 overcurrent fault has occurred.
1	OC_FAULT_2	1	Channel 2 overcurrent fault has occurred.
0	OC_FAULT_1	1	Channel 1 overcurrent fault has occurred.

MFR_NOC_FAULT

The MFR_NOC_FAULT returns a one-byte summary of negative overcurrent fault condition. When the voltage difference between $SNSD^+$ and SNS^- pins is less than the negative overcurrent fault threshold programmed by the ILIM pin, the corresponding register bit will become 1.

MFR_NOC_FAULT Register Contents:

BIT	NAME	VALUE	MEANING
7:6			Reserved
5	NOC_FAULT_6	1	Channel 6 negative overcurrent fault has occurred.
4	NOC_FAULT_5	1	Channel 5 negative overcurrent fault has occurred.
3	NOC_FAULT_4	1	Channel 4 negative overcurrent fault has occurred.
2	NOC_FAULT_3	1	Channel 3 negative overcurrent fault has occurred.
1	NOC_FAULT_2	1	Channel 2 negative overcurrent fault has occurred.
0	NOC_FAULT_1	1	Channel 1 negative overcurrent fault has occurred.

APPLICATIONS INFORMATION

MFR_STATUS

The MFR_STATUS returns a one-byte summary of the operation status. The content of the MFR_STATUS register is read only.

MFR_STATUS Register Contents:

BIT	NAME	VALUE	MEANING
7:3			Reserved
2	SS_DONE	1	The soft-start is finished.
1	MAX_CURRENT	1	The maximum current programmed by the ILIM pin is reached.
0	PGOOD	1	The regulated V_{LOW}/V_{HIGH} is within ±10% regulation windows.

MFR_CONFIG1

The MFR_CONFIG1 returns a one-byte summary of the configuration of the controller programmed by the pins. The content of the MFR_CONFIG1 register is read only.

MFR_CONFIG1 Register Contents:

BIT	NAME	VALUE	MEANING
7:6			Reserved
5	SERCUR_WARNING	1	The SETCUR pin is programmed to be above 1.25V.
4:3	DRVCC_SET[1:0]	00 01 10	The DRV_{CC} is programmed to 5V. The DRV_{CC} is programmed to 8V. The DRV_{CC} is programmed to 10V.
2:0	ILIM_SET[2:0]	000 001 010 011 100	The maximum current sense threshold is programmed to 10mV. The maximum current sense threshold is programmed to 20mV. The maximum current sense threshold is programmed to 30mV. The maximum current sense threshold is programmed to 40mV. The maximum current sense threshold is programmed to 50mV.

APPLICATIONS INFORMATION

MFR_CONFIG2

The MFR_CONFIG2 returns a one-byte summary of the configuration of the controller programmed by the pins. The content of the MFR_CONFIG2 register is read only.

MFR_CONFIG2 Register Contents:

BIT	NAME	VALUE	MEANING
7:5			Reserved
4	BURST	1	The controller is in burst mode operation.
3	DCM	1	The controller is in DCM.
2	HIZ	1	The controller is in Hi-Z mode.
1	SPRD	1	The controller is in spread spectrum mode.
0	BUCK_BOOST	0 1	The controller is in boost mode. The controller is in buck mode.

MFR_CHIP_CTRL

The MFR_CHIP_CTRL is for general chip control.

MFR_CHIP_CTRL Message Contents:

BIT	NAME	VALUE	MEANING
7:3			Reserved
2	CML	1	A communication fault related to PEC during writing registers has occurred. Write 1 to this bit will clear the CML.
1	RESET	1	Sticky bit, reset all R/W registers.
0	WP	0 1	Write allowed for all three IDAC registers, and MFR_SSFM register. Write inhibited for all three IDAC registers, and MFR_SSFM register.

APPLICATIONS INFORMATION

MFR_IDAC_VLOW

The MFR_IDAC_VLOW stores the current DAC value to program the V_{LOW} voltage by injecting the current DAC output to the VFB_{LOW} pin. It is formatted as a 7-bit two's complement value. Setting BIT[6] = 0 means sourcing current from the VFB_{LOW} pin; and BIT[6] = 1 means sinking current. The detail is listed in Table 8. The DAC current is only injected to the VFB_{LOW} pin in buck mode. Sinking current will cause V_{LOW} to rise. The default value for this register is 0x00. Writes to this register are inhibited when the WP, BIT[0] in MFR_CHIP_CTRL, is set high.

MFR_IDAC_VLOW Message Contents:

BIT	VALUE	MEANING
7		Reserved
6	0 1	0µA –64µA
5	0 1	0µA 32µA
4	0 1	0µA 16µA
3	0 1	0µA 8µA
2	0 1	0µA 4µA
1	0 1	0µA 2µA
0	0 1	0µA 1µA

MFR_IDAC_VHIGH

The MFR_IDAC_VHIGH stores the current DAC value to program the V_{HIGH} voltage by injecting the current DAC output to the VFB_{HIGH} pin. It is formatted as a 7-bit two's complement value. Setting BIT[6] = 0 means sourcing current from the VFB_{HIGH} pin; and BIT[6] = 1 means sinking current. The detail is listed in Table 8. The DAC current is only injected to the VFB_{HIGH} pin in boost mode. Sinking current will cause V_{HIGH} to rise in boost mode. The default value for this register is 0x00. Writes to this register are inhibited when the WP, BIT[0] in MFR_CHIP_CTRL, is set high.

MFR_IDAC_VHIGH Message Contents:

BIT	VALUE	MEANING
7		Reserved
6	0 1	0µA –64µA
5	0 1	0µA 32µA
4	0 1	0µA 16µA
3	0 1	0µA 8µA
2	0 1	0µA 4µA
1	0 1	0µA 2µA
0	0 1	0µA 1µA

APPLICATIONS INFORMATION

MFR_IDAC_SETCUR

The MFR_IDAC_SETCUR stores the current DAC value to program the sourcing current of the SETCUR pin. It is formatted as a 5-bit two's complement value. The default value for this register is 0x00 and the SETCUR pin originally sources 16µA. This register can program the SETCUR pin sourcing current from 0 to 31µA as shown in the Table 9. Writes to this register are inhibited when the WP, BIT[0] in MFR_CHIP_CTRL, is set high.

MFR_IDAC_SETCUR Message Contents:

BIT	VALUE	MEANING
7:5		RESERVED
4	0 1	16µA 0µA
3	0 1	0µA 8µA
2	0 1	0µA 4µA
1	0 1	0µA 2µA
0	0 1	0µA 1µA

MFR_SSFM

The MFR_SSFM is for spread spectrum frequency modulation control. The default value for this register is 0x00. Writes to this register are inhibited when the WP, BIT[0] in MFR_CHIP_CTRL, is set high.

MFR_SSFM Message Contents:

BIT	NAME	VALUE	MEANING
7:5			Reserved
4:3	Frequency Spread Range	00	±12%
		01	±15%
		10	±10%
		11	±8%
2:0	Modulation Signal Frequency	000	Controller Switching Frequency/512
		001	Controller Switching Frequency/1024
		010	Controller Switching Frequency/2048
		011	Controller Switching Frequency/4096
		100	Controller Switching Frequency/256
		101	Controller Switching Frequency/128
		110	Controller Switching Frequency/64
		111	Controller Switching Frequency/512

APPLICATIONS INFORMATION

Table 8. VFB_{LOW}/VFB_{HIGH} PIN Current and Corresponding DAC Codes

MFR_IDAC_V_{LOW}/MFR_IDAC_V_{HIGH}							
[6]	[5]	[4]	[3]	[2]	[1]	[0]	$I_{VFBLOW/VFBHIGH}$ (µA)
1	0	0	0	0	0	0	–64
1	0	0	0	0	0	1	–63
1	0	0	0	0	1	0	–62
1	0	0	0	0	1	1	–61
1	0	0	0	1	0	0	–60
1	0	0	0	1	0	1	–59
1	0	0	0	1	1	0	–58
1	0	0	0	1	1	1	–57
1	0	0	1	0	0	0	–56
1	0	0	1	0	0	1	–55
1	0	0	1	0	1	0	–54
1	0	0	1	0	1	1	–53
1	0	0	1	1	0	0	–52
1	0	0	1	1	0	1	–51
1	0	0	1	1	1	0	–50
1	0	0	1	1	1	1	–49
1	0	1	0	0	0	0	–48
1	0	1	0	0	0	1	–47
1	0	1	0	0	1	0	–46
1	0	1	0	0	1	1	–45
1	0	1	0	1	0	0	–44
1	0	1	0	1	0	1	–43
1	0	1	0	1	1	0	–42
1	0	1	0	1	1	1	–41
1	0	1	1	0	0	0	–40
1	0	1	1	0	0	1	–39
1	0	1	1	0	1	0	–38
1	0	1	1	0	1	1	–37
1	0	1	1	1	0	0	–36
1	0	1	1	1	0	1	–35
1	0	1	1	1	1	0	–34
1	0	1	1	1	1	1	–33

Table 8. VFB_{LOW}/VFB_{HIGH} PIN Current and Corresponding DAC Codes

MFR_IDAC_V_{LOW}/MFR_IDAC_V_{HIGH}							
[6]	[5]	[4]	[3]	[2]	[1]	[0]	$I_{VFBLOW/VFBHIGH}$ (µA)
1	1	0	0	0	0	0	–32
1	1	0	0	0	0	1	–31
1	1	0	0	0	1	0	–30
1	1	0	0	0	1	1	–29
1	1	0	0	1	0	0	–28
1	1	0	0	1	0	1	–27
1	1	0	0	1	1	0	–26
1	1	0	0	1	1	1	–25
1	1	0	1	0	0	0	–24
1	1	0	1	0	0	1	–23
1	1	0	1	0	1	0	–22
1	1	0	1	0	1	1	–21
1	1	0	1	1	0	0	–20
1	1	0	1	1	0	1	–19
1	1	0	1	1	1	0	–18
1	1	0	1	1	1	1	–17
1	1	1	0	0	0	0	–16
1	1	1	0	0	0	1	–15
1	1	1	0	0	1	0	–14
1	1	1	0	0	1	1	–13
1	1	1	0	1	0	0	–12
1	1	1	0	1	0	1	–11
1	1	1	0	1	1	0	–10
1	1	1	0	1	1	1	–9
1	1	1	1	0	0	0	–8
1	1	1	1	0	0	1	–7
1	1	1	1	0	1	0	–6
1	1	1	1	0	1	1	–5
1	1	1	1	1	0	0	–4
1	1	1	1	1	0	1	–3
1	1	1	1	1	1	0	–2
1	1	1	1	1	1	1	–1

APPLICATIONS INFORMATION

Table 8. VFB_{LOW}/VFB_{HIGH} PIN Current and Corresponding DAC Codes

MFR_IDAC_V_{LOW}/MFR_IDAC_V_{HIGH}							
[6]	[5]	[4]	[3]	[2]	[1]	[0]	$I_{VFBLOW/VFBHIGH}$ (µA)
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
0	0	0	0	0	1	0	2
0	0	0	0	0	1	1	3
0	0	0	0	1	0	0	4
0	0	0	0	1	0	1	5
0	0	0	0	1	1	0	6
0	0	0	0	1	1	1	7
0	0	0	1	0	0	0	8
0	0	0	1	0	0	1	9
0	0	0	1	0	1	0	10
0	0	0	1	0	1	1	11
0	0	0	1	1	0	0	12
0	0	0	1	1	0	1	13
0	0	0	1	1	1	0	14
0	0	0	1	1	1	1	15
0	0	1	0	0	0	0	16
0	0	1	0	0	0	1	17
0	0	1	0	0	1	0	18
0	0	1	0	0	1	1	19
0	0	1	0	1	0	0	20
0	0	1	0	1	0	1	21
0	0	1	0	1	1	0	22
0	0	1	0	1	1	1	23
0	0	1	1	0	0	0	24
0	0	1	1	0	0	1	25
0	0	1	1	0	1	0	26
0	0	1	1	0	1	1	27
0	0	1	1	1	0	0	28
0	0	1	1	1	0	1	29
0	0	1	1	1	1	0	30
0	0	1	1	1	1	1	31

Table 8. VFB_{LOW}/VFB_{HIGH} PIN Current and Corresponding DAC Codes

MFR_IDAC_V_{LOW}/MFR_IDAC_V_{HIGH}							
[6]	[5]	[4]	[3]	[2]	[1]	[0]	$I_{VFBLOW/VFBHIGH}$ (µA)
0	1	0	0	0	0	0	32
0	1	0	0	0	0	1	33
0	1	0	0	0	1	0	34
0	1	0	0	0	1	1	35
0	1	0	0	1	0	0	36
0	1	0	0	1	0	1	37
0	1	0	0	1	1	0	38
0	1	0	0	1	1	1	39
0	1	0	1	0	0	0	40
0	1	0	1	0	0	1	41
0	1	0	1	0	1	0	42
0	1	0	1	0	1	1	43
0	1	0	1	1	0	0	44
0	1	0	1	1	0	1	45
0	1	0	1	1	1	0	46
0	1	0	1	1	1	1	47
0	1	1	0	0	0	0	48
0	1	1	0	0	0	1	49
0	1	1	0	0	1	0	50
0	1	1	0	0	1	1	51
0	1	1	0	1	0	0	52
0	1	1	0	1	0	1	53
0	1	1	0	1	1	0	54
0	1	1	0	1	1	1	55
0	1	1	1	0	0	0	56
0	1	1	1	0	0	1	57
0	1	1	1	0	1	0	58
0	1	1	1	0	1	1	59
0	1	1	1	1	0	0	60
0	1	1	1	1	0	1	61
0	1	1	1	1	1	0	62
0	1	1	1	1	1	1	63

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Table 9. SETCUR Pin Current and Corresponding DAC Codes

MFR_IDAC_SETCUR[4:0]					
[4]	[3]	[2]	[1]	[0]	I_{SETCUR} (µA)
1	0	0	0	0	0
1	0	0	0	1	1
1	0	0	1	0	2
1	0	0	1	1	3
1	0	1	0	0	4
1	0	1	0	1	5
1	0	1	1	0	6
1	0	1	1	1	7
1	1	0	0	0	8
1	1	0	0	1	9
1	1	0	1	0	10
1	1	0	1	1	11
1	1	1	0	0	12
1	1	1	0	1	13
1	1	1	1	0	14
1	1	1	1	1	15

Table 9. SETCUR Pin Current and Corresponding DAC Codes

MFR_IDAC_SETCUR[4:0]					
[4]	[3]	[2]	[1]	[0]	I_{SETCUR} (µA)
0	0	0	0	0	16
0	0	0	0	1	17
0	0	0	1	0	18
0	0	0	1	1	19
0	0	1	0	0	20
0	0	1	0	1	21
0	0	1	1	0	22
0	0	1	1	1	23
0	1	0	0	0	24
0	1	0	0	1	25
0	1	0	1	0	26
0	1	0	1	1	27
0	1	1	0	0	28
0	1	1	0	1	29
0	1	1	1	0	30
0	1	1	1	1	31

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PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 15. Check the following in the PC layout:

1. The DRV_{CC} bypass capacitor should be placed immediately adjacent to the IC between the DRV_{CC} pin and the GND plane. A 1µF ceramic capacitor of the X7R or X5R type is small enough to fit very close to the IC. An additional 4.7µF to 10µF of ceramic, tantalum or other very low ESR capacitance is recommended in order to keep the internal IC supply quiet.
2. The V5 bypass capacitor should be placed immediately adjacent to the IC between the V5 and the SGND pins. A 4.7µF to 10µF capacitor of ceramic, tantalum or other very low ESR capacitance is recommended.
3. Place the feedback divider between the + and – terminals of C_{LOW}/C_{HIGH}. Route VFB_{LOW}/VFB_{HIGH} with minimum PC trace spacing from the IC to the feedback dividers.
4. Are the $SNSA^+$, $SNSD^+$ and SNS^- printed circuit traces routed together with minimum PC trace spacing? The filter capacitors between $SNSA^+$, $SNSD^+$ and SNS^- should be as close as possible to the pins of the IC.
5. Do the (+) plates of C_{HIGH} decoupling cap connect to the drain of the topside MOSFET as closely as possible? This capacitor provides the pulsed current to the MOSFET.
6. Keep the switching nodes away from sensitive small-signal nodes ($SNSD^+$, $SNSA^+$, SNS^-, V_{FB}). Ideally the switch nodes printed circuit traces should be routed away and separated from the IC and especially the quiet side of the IC. Separate the high dV/dt traces from sensitive small-signal nodes with ground traces or ground planes.
7. Use a low impedance source such as a logic gate to drive the SYNC pin and keep the PCB trace as short as possible.
8. The ceramic capacitors between each ITH pin and signal ground should be placed as close as possible to the IC. Figure 15 illustrates all branch currents in a switching regulator. It becomes very clear after studying the current waveforms why it is critical to keep the high switching current paths to a small physical size. High electric and magnetic fields will radiate from these loops just as radio stations transmit signals. The C_{LOW} ground should return to the negative terminal of C_{HIGH} and not share a common ground path with any switched current paths. The left half of the circuit gives rise to the noise generated by a switching regulator. The ground terminations of the bottom MOSFET and Schottky diode should return to the bottom plate(s) of the V_{HIGH} capacitor(s) with a short isolated PC trace since very high switched currents are present. External OPTI-LOOP® compensation allows overcompensation for PC layouts which are not optimized, but this is not the recommended design procedure.

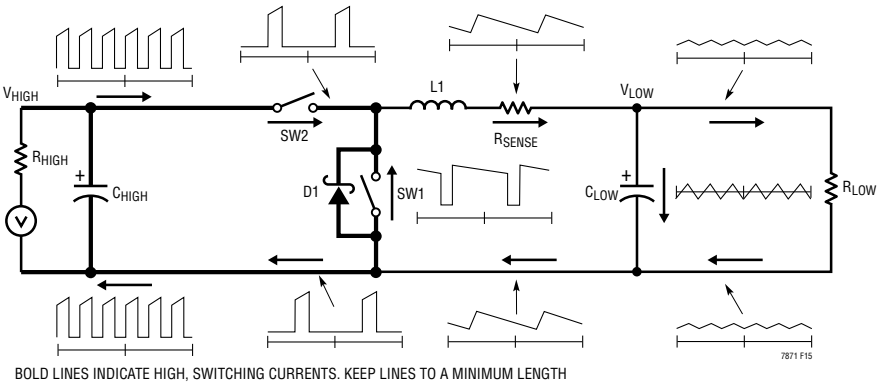

Figure 15. Branch Current Waveforms (Buck Mode Shown)

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Special Layout Consideration

Exceeding Absolute Max ratings on the $EXTV_{CC}$ pin can result in damage to the controller. As the $EXTV_{CC}$ pin is normally connected to V_{LOW}, it is recommended to put a Schottky diode with an appropriately high voltage rating between the V_{LOW} and the $EXTV_{CC}$ pins as shown in Figure 16(a). Choose the right Schottky diode with the forward voltage less than 0.5V at the maximum $EXTV_{CC}$ pin current.

Another method to protect on the $EXTV_{CC}$ pin is to use a Schottky diode to clamp the $EXTV_{CC}$ pin to reduce voltage spiking below ground. The Schottky diode should be placed close to the controller IC, with the cathode connected to the $EXTV_{CC}$ pin and the anode connected to ground as shown in the Figure 16(b). Choose a minimum 1Ω R_{FLTR} and keep the maximum voltage drop across the R_{FLTR} less than 0.5V.

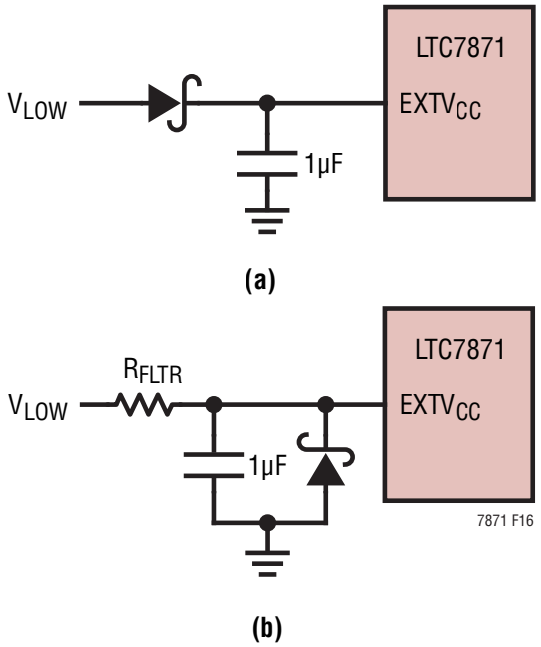

Figure 16. Methods to Protect the $EXTV_{CC}$ Pin

Design Example

As a design example for a six-phase single output high current regulator, assume V_{HIGH} = 48V (nominal), V_{HIGH} = 60V (maximum), V_{LOW} = 12V, $I_{VLOW(MAX)}$ = 180A (30A/phase), and f = 150kHz. The regulated output voltage is determined by:

$V_{LOW} = 1.2V \bullet (1 + R_B/R_A)$.

Using a 10k 1% resistor from the VFB_{LOW} node to ground, the top feedback resistor is (to the nearest 1% standard value) 90.9k. The frequency is set by selecting the R_{FREQ} to be 37.4kΩ. The inductance values are based on a 35% maximum ripple current assumption (10.5A for each phase). The highest value of ripple current occurs at the maximum V_{HIGH} voltage:

$$L = \frac{V_{LOW}}{f \bullet \Delta I_{L(MAX)}} \bullet \left(1 - \frac{V_{LOW}}{V_{HIGH(MAX)}}\right)$$

Each phase will require 6.1µH. The Sagami CVE2622C-6R8M, 6.8µH, 1.8mΩ DCR inductor is chosen. At the nominal V_{HIGH} voltage (48V), the ripple current will be:

$$\Delta I_{L(NOM)} = \frac{V_{LOW}}{f \bullet L} \bullet \left(1 - \frac{V_{LOW}}{V_{HIGH(NOM)}}\right)$$

Each phase will have 8.8A (29.3%) ripple. The peak inductor current will be the maximum DC value plus one-half the ripple current, or 34.4A. The minimum on-time occurs at the maximum V_{HIGH}, and should not be less than 150ns:

$$T_{ON(MIN)} = \frac{V_{LOW}}{V_{HIGH(MAX)} \bullet f} = \frac{12V}{60V \bullet 150kHz} = 1.33\mu s$$

With V_{ILIM} = 3/4 V_{V5}, the equivalent R_{SENSE} resistor value can be calculated by using the minimum value for the maximum current sense threshold (45mV):

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MIN)}}{\frac{I_{LOAD(MAX)}}{\#OF\ PHASES} + \frac{\Delta I_{L(NOM)}}{2}}$$

The equivalent required R_{SENSE} value is 1.31mΩ. Choose R_S = 1mΩ to allow some design margin. As shown in Figure 17, set R2 to be below 1/10th of the R1. Therefore, the DC component of the $SNSA^+$ filter is small enough to be omitted. R1 • C1 should have a bandwidth that is four times as high as the L/R_S.

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Typically, C1 is selected in the range of 0.047µF to 0.47µF. If C1 is chosen to be 0.1µF, R1 and R2 will be 16.9kΩ and 1.69kΩ respectively. The bias current at SNSD+ and SNSA+ is about 50nA, and it causes some small error to the current sense signal. If C2 is also chosen to be 0.1µF, R3 will be 1.5kΩ.

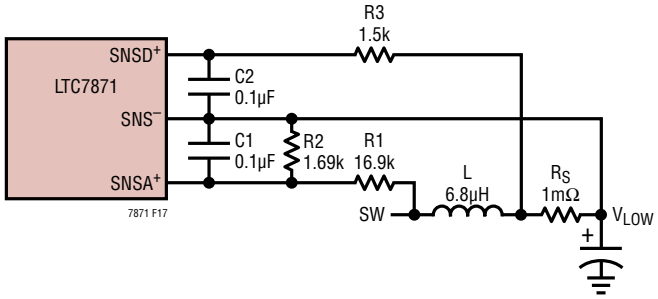


Figure 17. R_{SENSE} Resistor Sensing in Design Example

The power dissipation on the top MOSFET can be easily estimated. Set the gate drive voltage (DRV_{CC}) to be 10V. Choosing two Infineon BSC117N08NS5 MOSFETs results in:

$R_{DS(ON)}$ = 11.7mΩ (max),
V_{MILLER} = 5V, C_{MILLER} ≅ 19pF.

At typical V_{HIGH} voltage with T_J (estimated) = 75°C:

$$P_{MAIN} = \left\{ \begin{array}{l} \frac{12V}{48V} \bullet 15A^2 \\ \bullet \left[(1 + 0.005 \bullet (75°C - 25°C)) \bullet 11.7m\Omega \right] \\ +48V^2 \bullet \frac{15A}{2} \bullet 4\Omega \bullet 19pF \\ \bullet \left(\frac{1}{10-5} + \frac{1}{5} \right) \bullet 150k \end{array} \right\} \bullet 2$$

$$= \{823mW + 79mW\} \bullet 2$$

$$= 1804mW$$

Two Infineon BSC052N08NS5 MOSFETs, $R_{DS(ON)}$ = 5.2mΩ, C_{OSS} = 370pF are chosen for the bottom MOSFET. The resulting power loss is:

$$P_{SYNC} = \left\{ \begin{array}{l} \frac{48V - 12V}{48V} \bullet 15A^2 \\ \bullet \left[(1 + 0.005 \bullet (75°C - 25°C)) \bullet 5.2m\Omega \right] \end{array} \right\} \bullet 2$$

$$= \{1.1W\} \bullet 2$$

$$= 2.2W$$

C_{HIGH} is chosen for an equivalent RMS current rating of at least 20A. C_{LOW} is chosen with an equivalent ESR of 10mΩ for low output ripple. The V_{LOW} output ripple in continuous mode will be highest at the maximum V_{HIGH} voltage. The V_{LOW} output voltage ripple due to ESR is approximately:

$$V_{LOWRIPPLE} = R_{ESR} \bullet \Delta I_L = 0.01\Omega \bullet 8.8A = 88mV$$

Further reductions in V_{LOW} output voltage ripple can be made by placing ceramic capacitors across C_{LOW}.

If the output load is a battery, the voltage loop is first set for the desired output voltage and then the charge current can be regulated using the current regulation loop—via the SETCUR and IMON pins. Selecting a maximum charge current of 120A, the desired SETCUR pin voltage is calculated using:

$$V_{SETCUR} = \frac{K \bullet I_{L(MAX)} \bullet R_{SENSE}}{6}$$

$$= \frac{20 \bullet 120A \bullet 1m\Omega}{6}$$

$$= 400mV$$

The SETCUR pin can be driven by an ADC's output to 400mV for the best accuracy. If one is not available, the 16µA current sourced out of the SETCUR pin can be used to set the voltage with a resistor from SETCUR to ground, calculated using:

$$R_{SETCUR} = \frac{400mV}{16\mu A} = 25k$$

A 1% or more accurate 30.1k resistor can be chosen to allow some design margin. The 16µA current out of the SETCUR pin can be programmed by the SPI interface so the maximum charge current can be changed on-the-fly.

TYPICAL APPLICATIONS

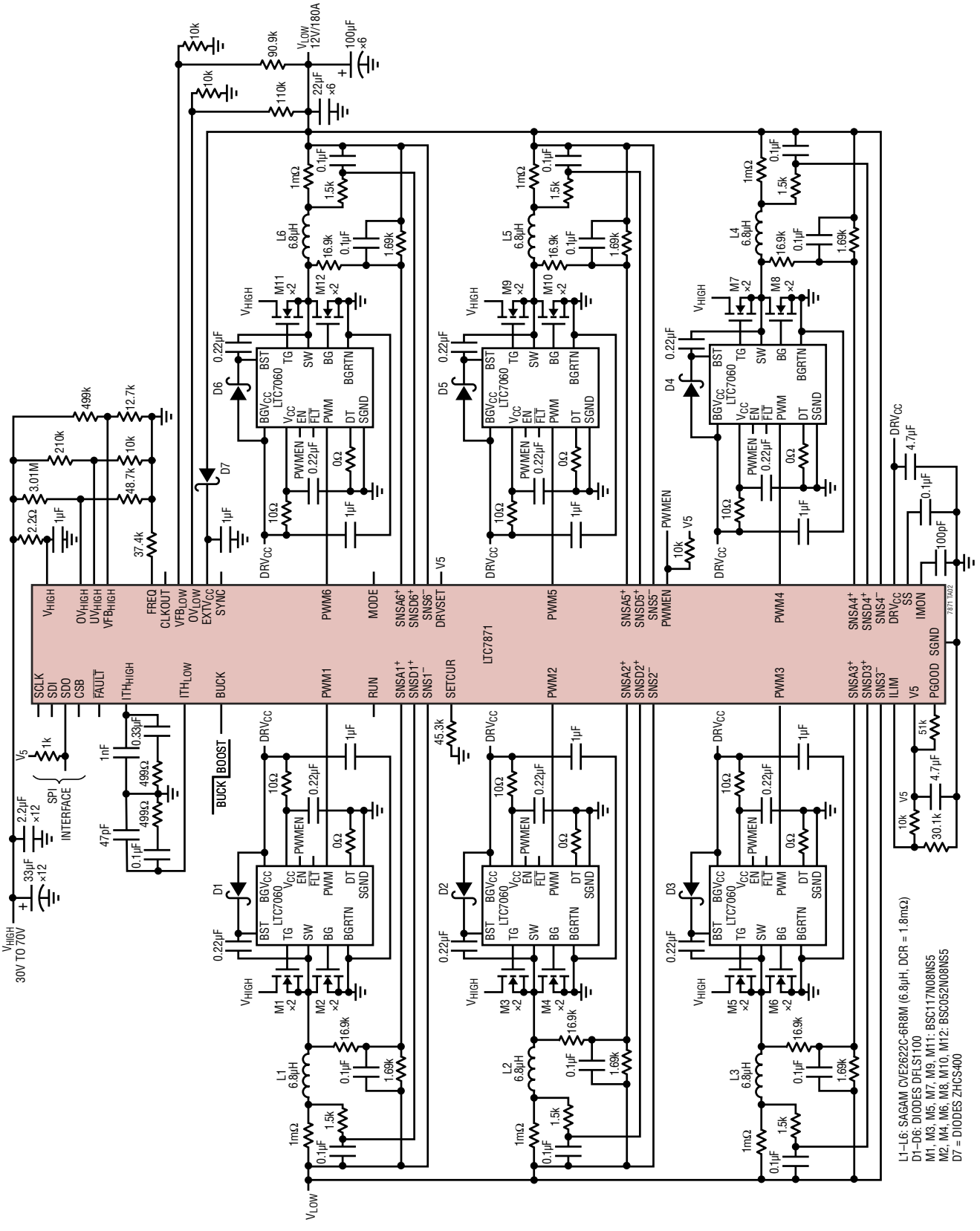
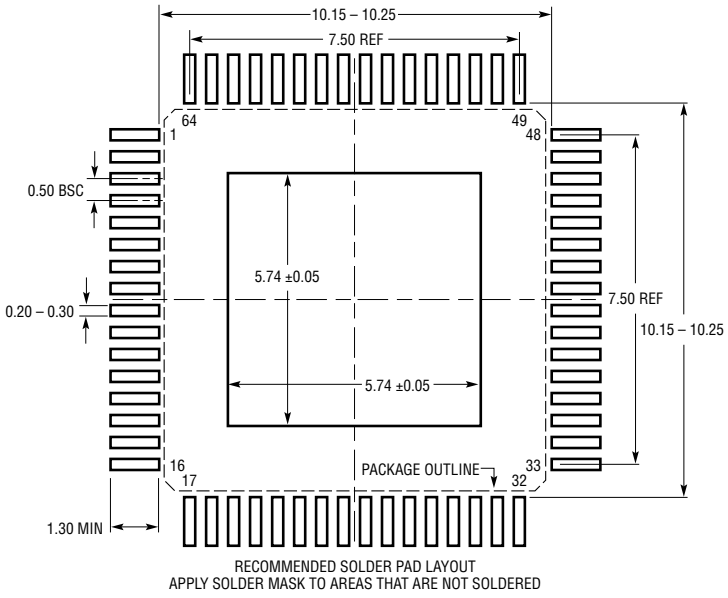
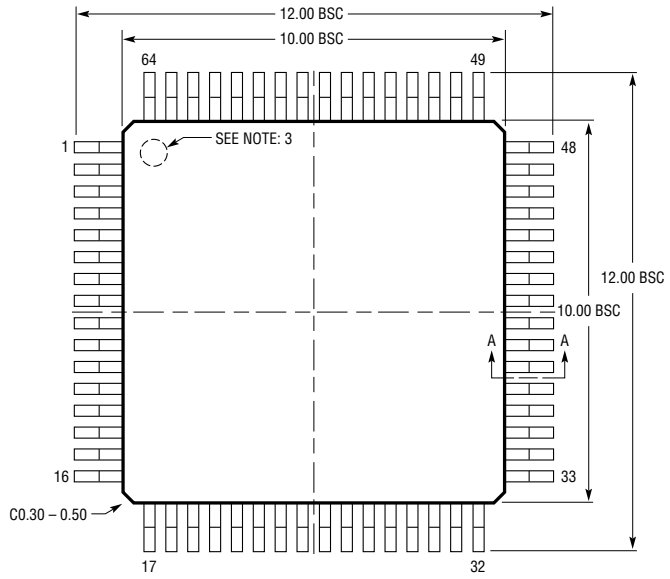


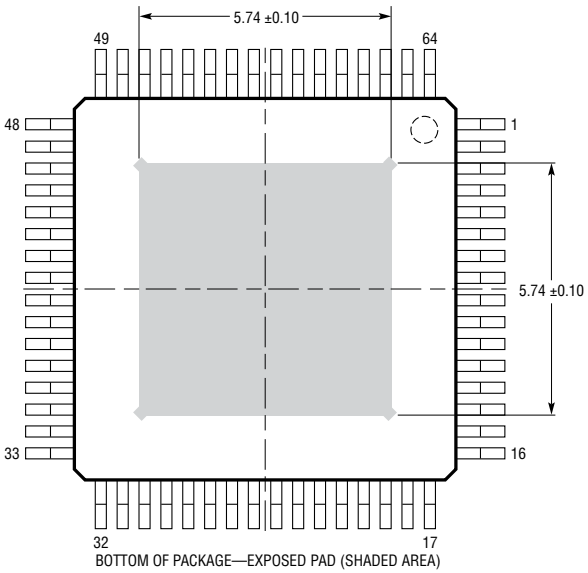
Figure 18. High Efficiency 6-Phase, 12V/180A Bidirectional Supply

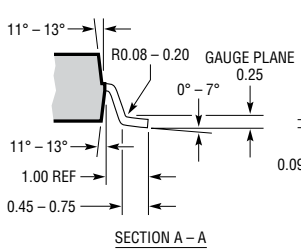
PACKAGE DESCRIPTION

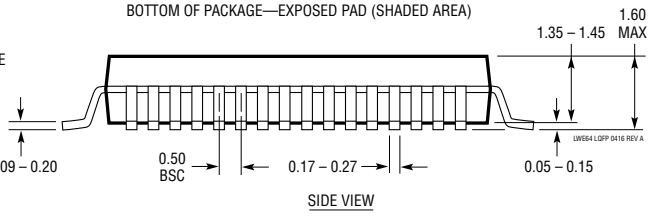
LWE Package
64-Lead Plastic Exposed Pad LQFP (10mm × 10mm)
(Reference LTC DWG #05-08-1982 Rev A)











NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.25mm (10 MILS) BETWEEN THE LEADS AND MAX 0.50mm (20 MILS) ON ANY SIDE OF THE EXPOSED PAD, MAX 0.77mm (30 MILS) AT CORNER OF EXPOSED PAD, IF PRESENT
3. PIN-1 INDENTIFIER IS A MOLDED INDENTATION, 0.50mm DIAMETER
4. DRAWING IS NOT TO SCALE

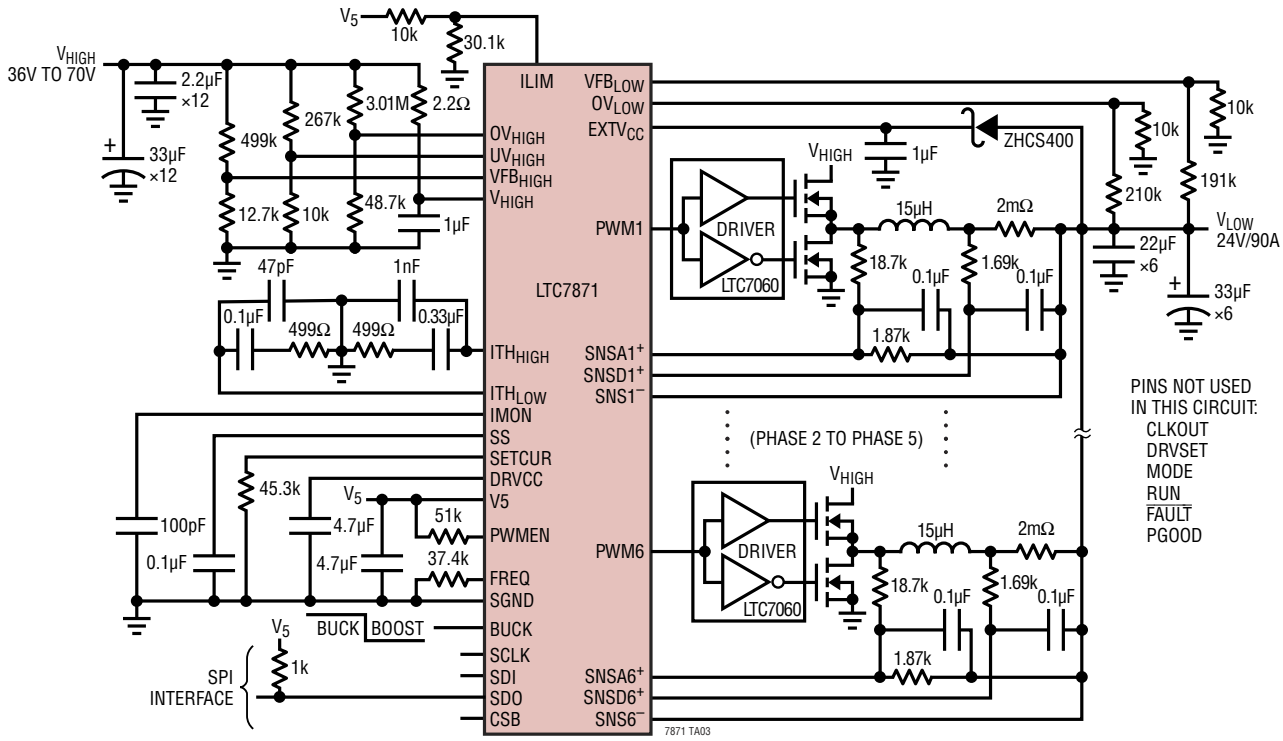
Rev. A

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	07/21	Add Guarantee by Design to DRV_{CC}/$EXTV_{CC}$ Peak Current in ABS MAX Rating section.	3
		Add UNITS for V5 UVLO and $EXTV_{CC}$ Switchover Voltage parameters.	4, 5
		SYNC (Pin 52): Update internal resistor value.	10
		Update EA_VLOW.	12
		Update P_{TOP} equation.	24
		Update the external clock (on the SYNC pin) input low threshold voltage.	28
		Update MFR_IDAC_VLOW and MFR_IDAC_VHIGH tables.	38
		Update inductor's name.	44, 46

TYPICAL APPLICATION

High Efficiency 6-Phase 24V/90A Bidirectional Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7060	100V Half Bridge Gate Driver with Floating Grounds and Programmable Dead-Time	Up to 100V Supply Voltage, 6V ≤ V_{CC} ≤ 14V, Adaptive Shoot-Through Protection, 2mm × 3mm LFCSP and 12-LEAD MSOP
LT8228	Bidirectional Buck or Boost Controller with Fault Protection	Up to 100V for V_{HIGH}, and V_{LOW}, Ideal for 48V/12V Automotive Battery Applications
LT8708/LT8708-1	80V Synchronous 4-Switch Buck-Boost DC/DC Controller with Flexible Bidirectional Capability	2.8V ≤ V_{IN} ≤ 80V, 1.3V ≤ V_{OUT} ≤ 80V, PLL Fixed Frequency 100kHz to 400kHz, 5mm × 8mm QFN-40
LTC3871	Bidirectional PolyPhase Synchronous Buck or Boost Controller	Up to 100V V_{HIGH}, Up to 30V V_{LOW}, PLL Fixed Frequency 60kHz to 460kHz, 48-Lead LQFP
LTC4449	High Speed Synchronous N-Channel MOSFET Driver	Up to 38V Supply Voltage, 4V ≤ V_{CC} ≤ 6.5V, Adaptive Shoot-Through Protection, 2mm × 3mm DFN-8
LTC3779	150V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost Controller	4.5V ≤ V_{IN} ≤ 150V, 1.2V ≤ V_{OUT} ≤ 150V, PLL Fixed Frequency 50kHz to 600kHz, FE38 TSSOP
LTC7813	60V Low I_Q Synchronous Boost+Buck Controller, Low EMI and Low Input/Output Ripple	4.5V (Down to 2.2V After Start-Up) ≤ V_{IN} ≤ 60V, Boost V_{OUT} Up to 60V, 0.8V ≤ Buck V_{OUT} ≤ 60V, I_Q = 29µA, 5mm × 5mm QFN-32 Package
LTC3899	60V, Triple Output, Buck/Buck/Boost Synchronous Controller with 29µA Burst Mode I_Q	4.5V (Down to 2.2V after Start-Up) ≤ V_{IN} ≤ 60V, V_{OUT} Up to 60V, Buck V_{OUT} Range: 0.8V to 60V, Boost V_{OUT} Up to 60V
LTM® 8056	58V_{IN}, Buck-Boost µModule Regulator, Adjustable Input and Output Current Limiting	5V ≤ V_{IN} ≤ 58V, 1.2V ≤ V_{OUT} ≤ 48V, 15mm × 15mm × 4.92mm BGA Package
LTC7103	105V, 2.3A, Low EMI Synchronous Step-Down Regulator	4.4V ≤ V_{IN} ≤ 105V, 1V ≤ V_{OUT} ≤ V_{IN}, I_Q = 2µA, Fixed Frequency 200kHz, 5mm × 6mm QFN Package

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