# 26V, 9A Low-$I_Q$ CC/CV Monolithic Buck-Boost Converter

## FEATURES

- **Input Voltage Range: 2.5V to 26V**
- **0.8V to 24V Output Voltage Range**
- **High Output Current**
  - **6.5A with $V_{OUT}$ = 5V, $V_{IN}$ > 6V**
  - **3A with $V_{OUT}$ = 5V, $V_{IN}$ = 3V**
  - **6.5A with $V_{OUT}$ = 12V, $V_{IN}$ > 14V**
  - **4 A with $V_{OUT}$ = 12V, $V_{IN}$ = 9V**
- **Ultralow Noise Buck-Boost Architecture**
- **Programmable Output Current Limit**
- Programmable Frequency Range: 400kHz to 2MHz
- Accurate Enable Comparator Threshold
- Burst Mode® Operation, No-Load $I_Q$ = 35µA
- Current Mode Control
- External Clock Synchronization
- Maximum Power Point Control
- 28-Lead 4mm × 5mm LQFN Package

## APPLICATIONS

- RF Power Supply
- USB Power Delivery
- System Backup Power Supply
- 1-Cell to 5-Cell Lithium Battery Powered Products
- Wide Input Range Power Supply
- Lead Acid to 12V Regulator

## DESCRIPTION

The LT®3120 is a high efficiency 26V monolithic buck-boost converter. Extensive feature integration and very low resistance internal power switches minimize the total solution footprint for even the most demanding applications. A proprietary 4-switch PWM architecture provides seamless low noise operation from input voltages above, equal to, or below the output voltage.

External frequency programming as well as synchronization using an internal PLL enable operation over a wide switching frequency range of 400kHz to 2MHz. The wide 2.5V to 26V input range is well suited for operation from unregulated power sources including battery stacks and backup capacitors. After start-up, operation is possible with input voltages as low as 500mV.

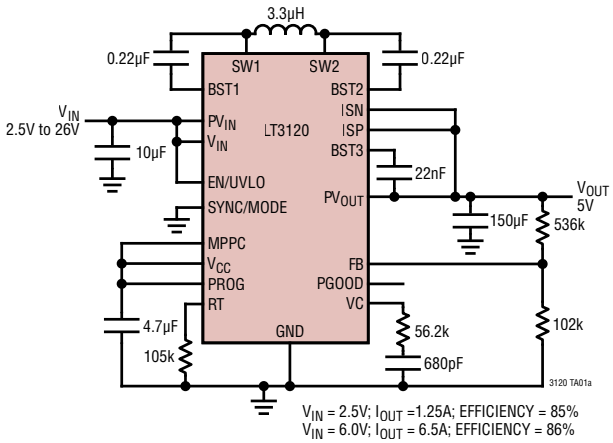
Other features include, output short-circuit protection, thermal overload protection, less than 3µA shutdown current, power good indicator, Burst Mode operation, and maximum power point control.

The LT3120 is offered in thermally enhanced 28-lead 4mm × 5mm LQFN package.

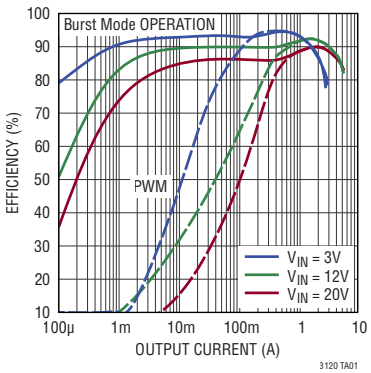


## TYPICAL APPLICATION

**Wide Input Range 750kHz 5V Regulator**




**Efficiency, $V_{OUT}$ = 5V, $f_{SW}$ = 750kHz**

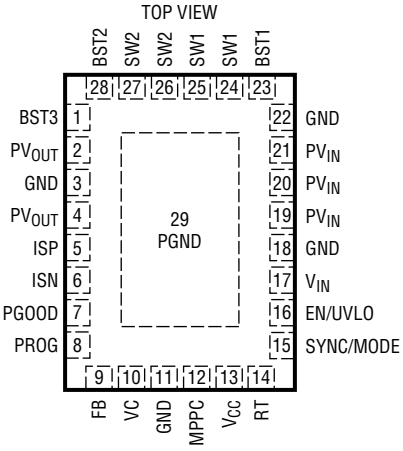


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{IN}$, $PV_{IN}$, $PV_{OUT}$, EN/UVLO, PGOOD ..... –0.3V to 27V
FB, VC, RT, SYNC/MODE, MPPC, $V_{CC}$ ..... –0.3V to 6V
BST1 ..... (SW1 – 0.3V) to (SW1 + 6V)
BST2 ..... (SW2 – 0.3V) to (SW2 + 6V)
BST3 ..... ($PV_{OUT}$ – 0.3V) to ($PV_{OUT}$ + 6V)
Operating Junction Temperature (Note 2)
LT3120J ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Maximum Reflow (Package Body) Temperature ... 260°C

## PIN CONFIGURATION




LQFN PACKAGE
28-LEAD (4mm × 5mm) LGA
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 20°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| PART NUMBER | PAD OR BALL FINISH | PART MARKING | | PACKAGE TYPE | MSL RATING | TEMPERATURE RANGE (SEE NOTE 2) |
|---|---|---|---|---|---|---|
| | | DEVICE | FINISH CODE | | | |
| LT3120JV#PBF | Au (RoHS) | 3120 | e4 | LQFN (Laminate Package with QFN Footprint) | 3 | –40°C to 150°C |

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = $PV_{IN}$ = 12V, $PV_{OUT}$ = 5V unless otherwise stated.**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Operating Voltage | <br>After Start-Up (Note 4) | ●<br> | 2.5<br>0.5 | | 26<br>26 | V<br>V |
| Output Operating Range | | ● | 0.8 | | 24 | V |
| $V_{CC}$ Undervoltage Lockout Threshold | $V_{CC}$ Rising<br>$V_{CC}$ Falling | ●<br>● | <br>2.2 | 2.35<br>2.25 | 2.4 | V<br>V |
| $V_{CC}$ Undervoltage Lockout Hysteresis | | | | 100 | | mV |
| Input Current in Shutdown | EN/UVLO = 0V | | | | 3 | µA |
| Input Current in Sleep | FB = 0.9V | | | 30 | | µA |
| Oscillator Frequency | $R_T$ = 76.8kΩ | ● | 900 | 1000 | 1100 | kHz |
| Oscillator Frequency Range | | ● | 400 | | 2000 | kHz |
| SYNC/MODE Frequency Range | | ● | 400 | | 2000 | kHz |
| SYNC/MODE Logic Threshold | | ● | 0.3 | 0.7 | 1.1 | V |
| SYNC/MODE Minimum Pulse Width | Minimum Low or High Duration | | 100 | | | ns |
| Soft-Start Duration | | | | 6 | | ms |
| Feedback Voltage | <br> | <br>● | 787<br>779 | 795<br>795 | 803<br>811 | V<br>V |
| FB Pin Input Current | | | | 1 | 50 | nA |
| Error Amplifier Transconductance | | | | 120 | | µs |
| EN/UVLO Pin Input Logic Threshold | | ● | 0.3 | 0.8 | 1.0 | V |
| EN/UVLO Pin Comparator Threshold | Rising<br>Rising, –40°C ≤ $T_J$ ≤ 125°C | ● | 1.169<br>1.169 | 1.205 | 1.258<br>1.241 | V<br>V |
| EN/UVLO Pin Hysteresis Current | | | | 250 | | nA |
| EN/UVLO Pin Hysteresis Voltage | | | | 90 | | mV |
| PROG Pin Current | $V_{ISP} – V_{ISN}$ = 25mV<br>$V_{ISP} – V_{ISN}$ = 10mV | | 47.5<br>18 | 50<br>20 | 52.5<br>22 | µA<br>µA |
| PROG Pin Threshold | | ● | 779 | 795 | 811 | V |
| MPPC Pin Threshold | | ● | 774 | 795 | 822 | V |
| PGOOD Threshold | Percent of FB Voltage Falling | ● | –9.5 | –8 | –6.5 | % |
| PGOOD Hysteresis | Percent of FB Voltage | | | 1.2 | | % |
| PGOOD Pull-Down Resistance | | | | 100 | 250 | Ω |
| PGOOD Leakage | $V_{PGOOD}$ = 24V | | | 1 | 40 | nA |
| Inductor Current Limit | Limit on Average (Not Peak) Inductor Current | ● | 8.25 | 9.5 | | A |
| Burst Mode Inductor Current Limit | Limit on Average (Not Peak) Inductor Current | | | 1 | | A |
| Maximum Duty Cycle | Percentage of Period SW2 is Low in Boost Mode, $R_T$ = 76.8kΩ (Note 4) | ● | 91 | 95 | | % |
| SW1, SW2 Minimum Low Time | (Note 4) | | | 70 | | ns |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = $PV_{IN}$ = 12V, $PV_{OUT}$ = 5V unless otherwise stated.**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| N-Channel Switch Resistance | Switch A ($PV_{IN}$ to SW1)<br>Switch B (SW1 to PGND)<br>Switch C (SW2 to PGND)<br>Switch D (SW2 to $PV_{OUT}$) | | | 25<br>23<br>23<br>25 | | mΩ<br>mΩ<br>mΩ<br>mΩ |
| N-Channel Switch Leakage | $PV_{IN}$ = $PV_{OUT}$ = 24V; SW1 = SW2 = 0V | | | 1 | 10 | µA |
| $V_{CC}$ Regulation Voltage | | ● | 3.6 | 3.73 | 3.86 | V |
| $V_{CC}$ Dropout Voltage | $I_{CC}$ = 50mA, $V_{IN}$ = 3.6V | | | 100 | | mV |
| $V_{CC}$ Current Limit | | | 100 | | | mA |
| $V_{CC}$ Reverse Current | $V_{CC}$ = 5V, $V_{IN}$ = 3V | | | 5 | | µA |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

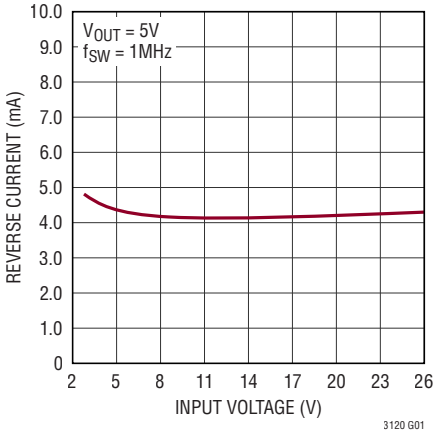
**Note 2:** The LT3120J is guaranteed to meet performance specifications over the –40°C to 150°C operating junction temperature ranges. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C.

**Note 3:** Minimum input voltage is governed by the $V_{CC}$ UVLO threshold. If $V_{CC}$ is maintained through external bootstrapping, the part will continue to operate until power transfer to the output is no longer possible.

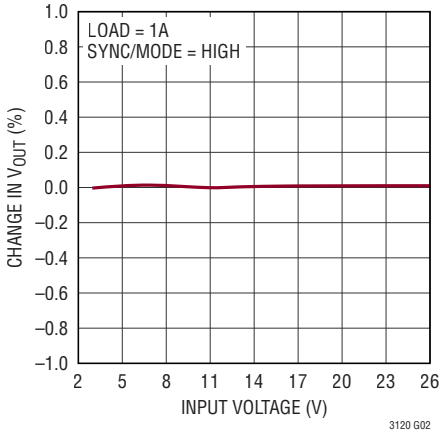
**Note 4:** Switch timing measurements are made in an open-loop test configuration. Timing in the application may vary somewhat from these values due to differences in the switch pin voltage during the non-overlap durations when switch pin voltage is influenced by the magnitude and direction of the inductor current.

# TYPICAL PERFORMANCE CHARACTERISTICS

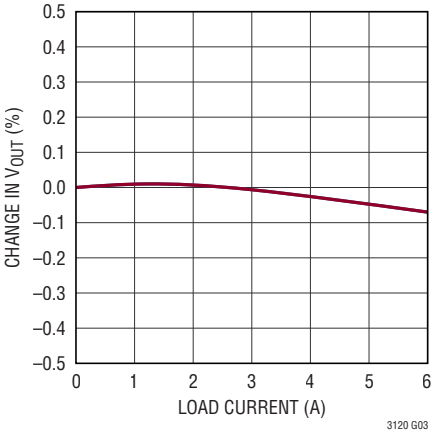
### Maximum Reverse Current During MPPC Control ($V_{MPPC}$ < 0.83)



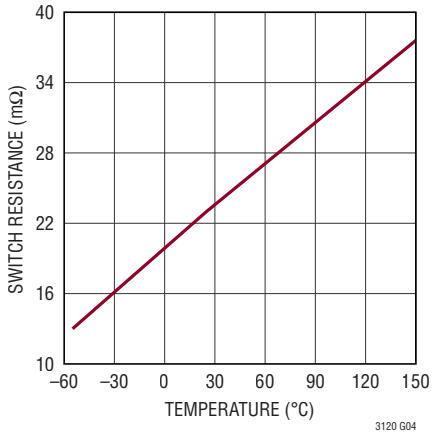

### Line Regulation



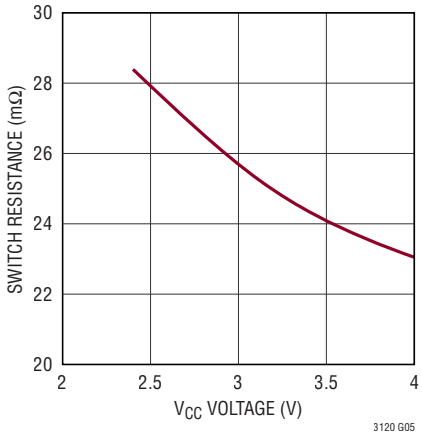

### Load Regulation



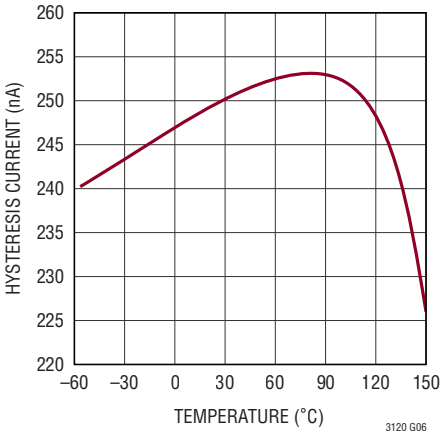

### Power Switch Resistance vs Temperature



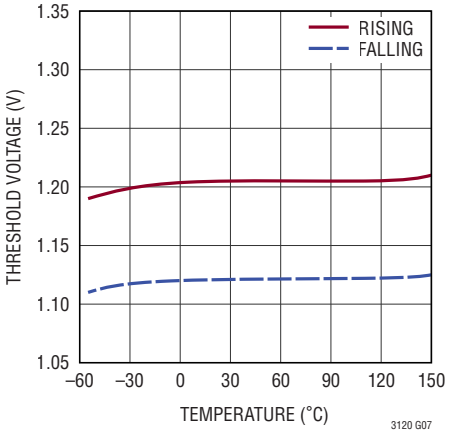

### Power Switch Resistance vs $V_{CC}$



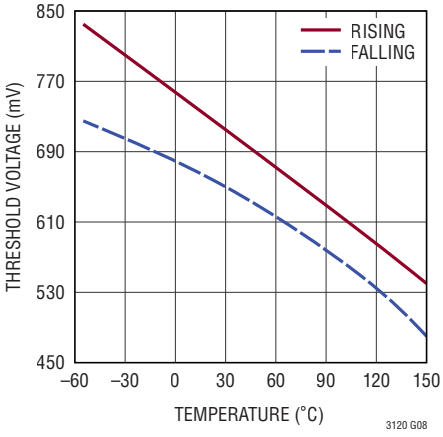

### EN/UVLO Pin Hysteresis Current vs Temperature



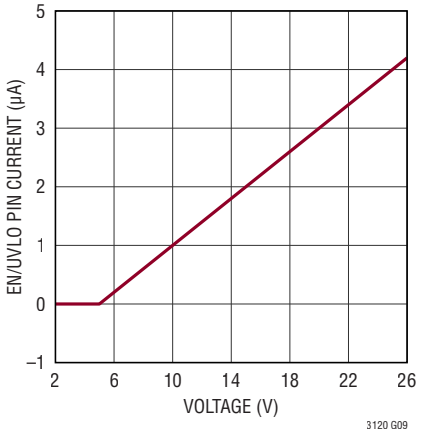

### EN/UVLO Pin Accurate Threshold vs Temperature




### EN/UVLO Pin Logic Thresholds vs Temperature

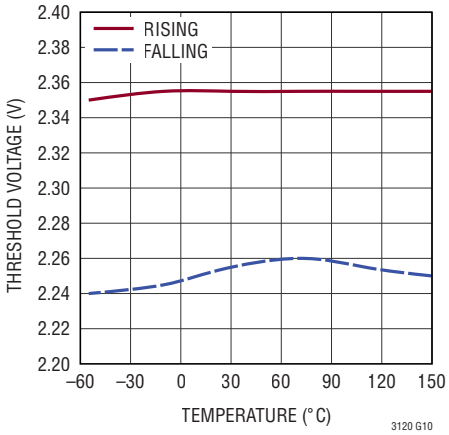



### EN/UVLO Pin Current vs EN/UVLO Pin Voltage

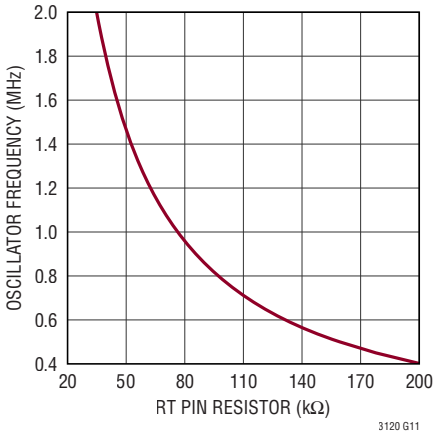


## TYPICAL PERFORMANCE CHARACTERISTICS

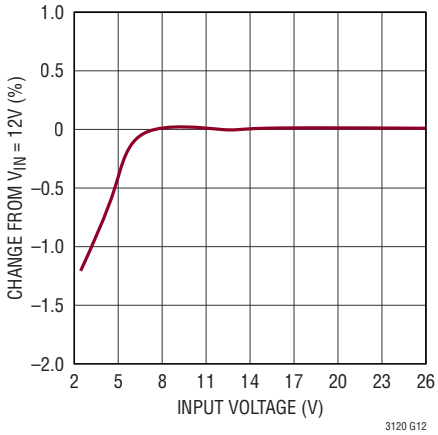
**$V_{CC}$ UVLO Threshold vs Temperature**



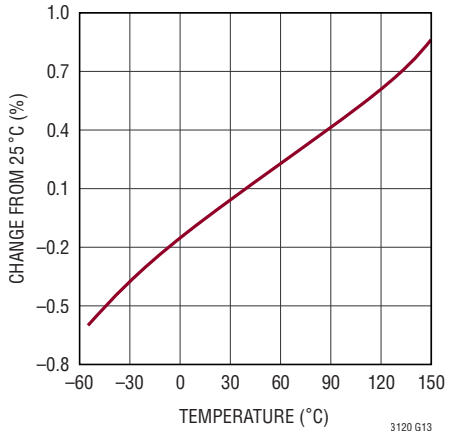

**Oscillator Frequency vs $R_T$**



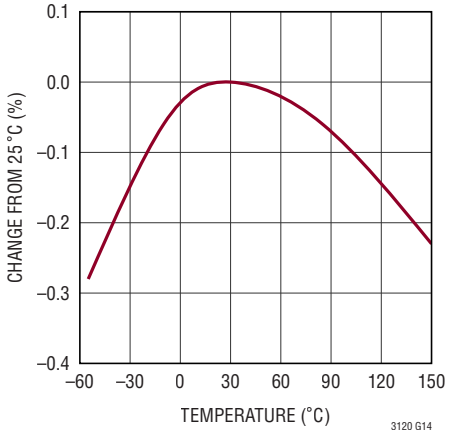

**Oscillator Frequency vs $V_{IN}$**



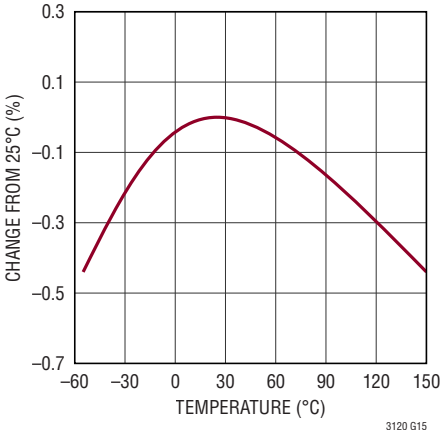

**Oscillator Frequency vs Temperature**



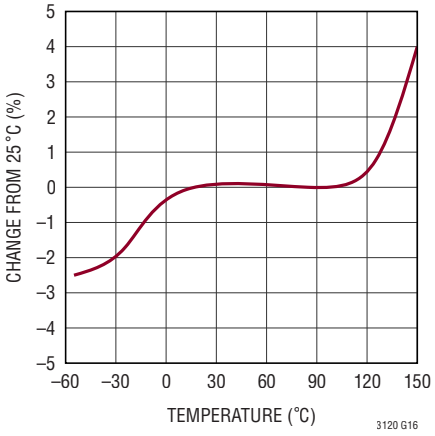

**FB Voltage vs Temperature**



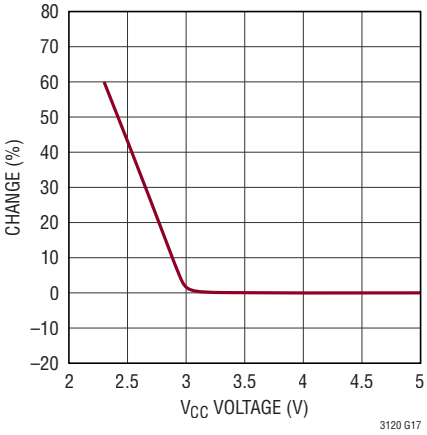

**PROG Pin Voltage vs Temperature**




**MPPC Pin Voltage vs Temperature**

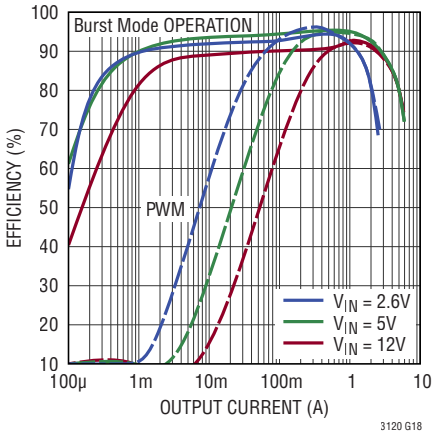



**SW1, SW2 Minimum Low Time vs $V_{CC}$**

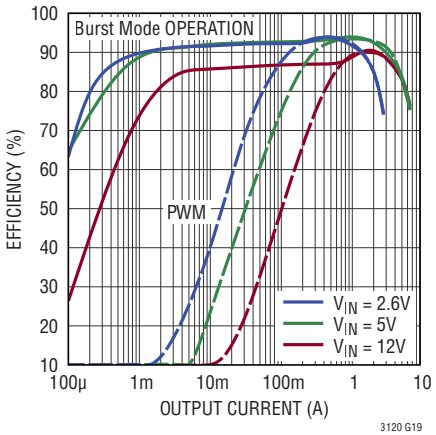


# TYPICAL PERFORMANCE CHARACTERISTICS

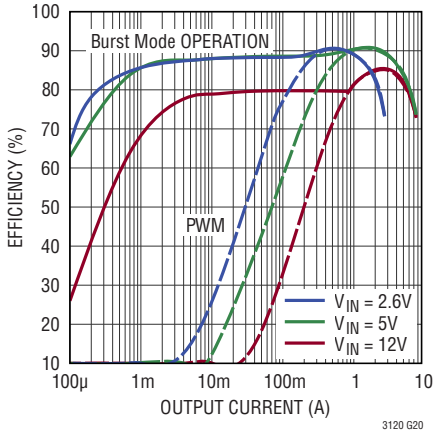
**Efficiency, $V_{OUT}$ = 3.3V, $f_{SW}$ = 500kHz**



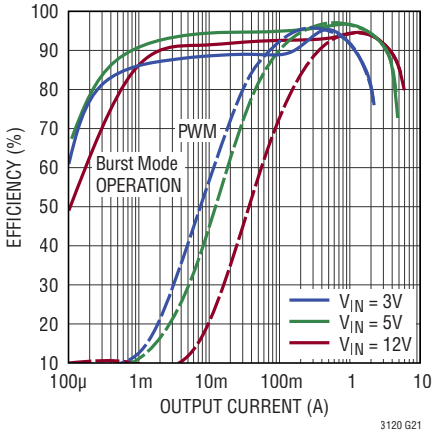

**Efficiency, $V_{OUT}$ = 3.3V, $f_{SW}$ = 1MHz**



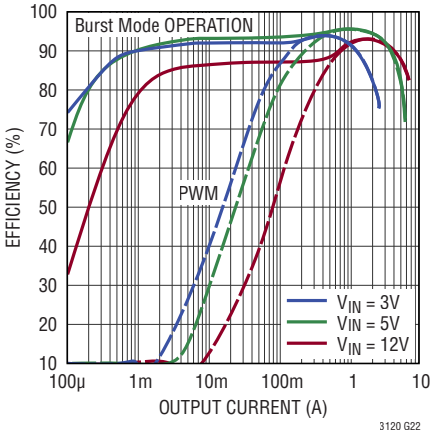

**Efficiency, $V_{OUT}$ = 3.3V, $f_{SW}$ = 2MHz**



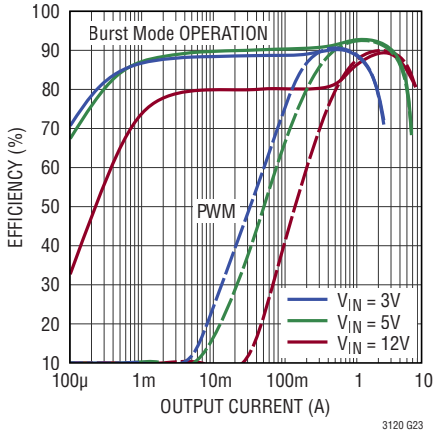

**Efficiency, $V_{OUT}$ = 5V, $f_{SW}$ = 500kHz**



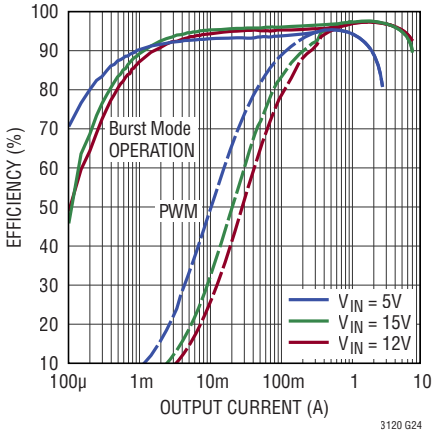

**Efficiency, $V_{OUT}$ = 5V, $f_{SW}$ = 1MHz**



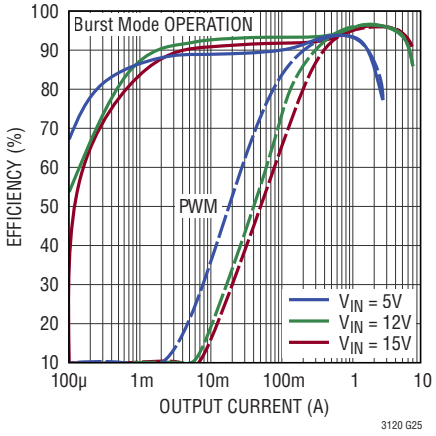

**Efficiency, $V_{OUT}$ = 5V, $f_{SW}$ = 2MHz**



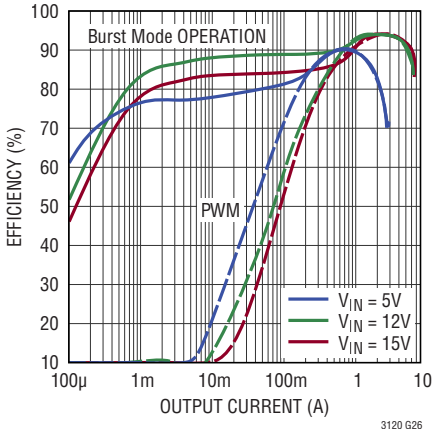

**Efficiency, $V_{OUT}$ = 12V, $f_{SW}$ = 500kHz**




**Efficiency, $V_{OUT}$ = 12V, $f_{SW}$ = 1MHz**

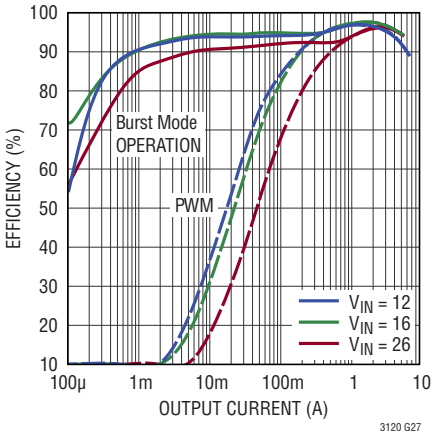



**Efficiency, $V_{OUT}$ = 12V, $f_{SW}$ = 2MHz**

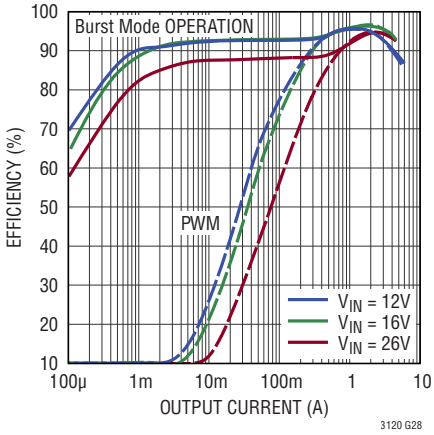


## TYPICAL PERFORMANCE CHARACTERISTICS

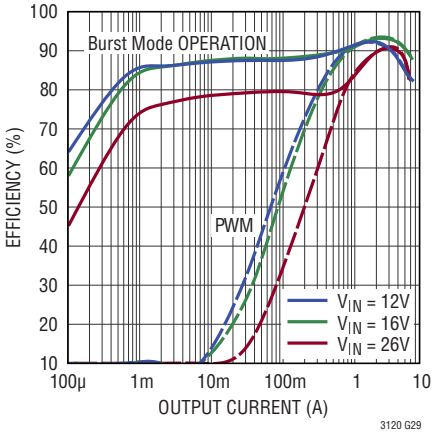
**Efficiency, $V_{OUT}$ = 15V, $f_{SW}$ = 500kHz**



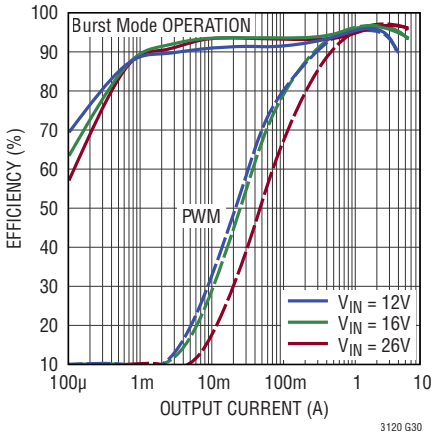

**Efficiency, $V_{OUT}$ = 15V, $f_{SW}$ = 1MHz**



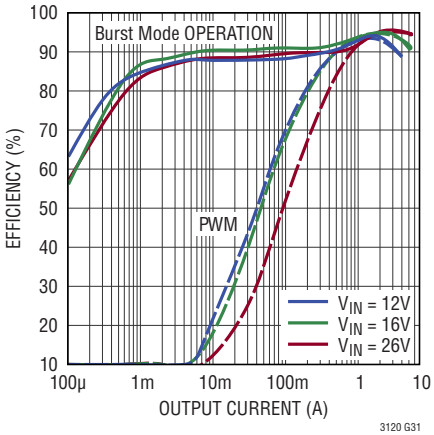

**Efficiency, $V_{OUT}$ = 15V, $f_{SW}$ = 2MHz**



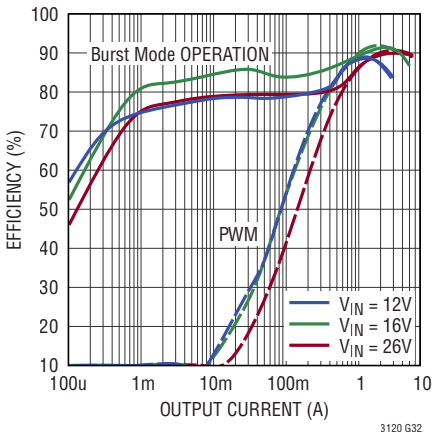

**Efficiency, $V_{OUT}$ = 20V, $f_{SW}$ = 500kHz**



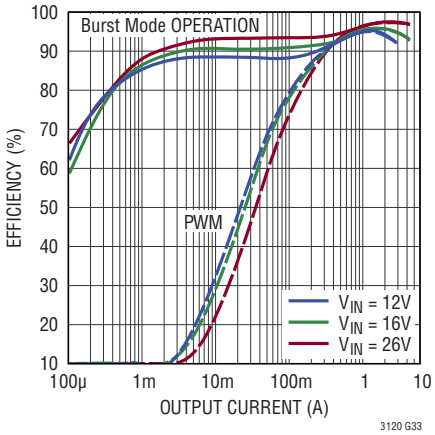

**Efficiency, $V_{OUT}$ = 20V, $f_{SW}$ = 1MHz**



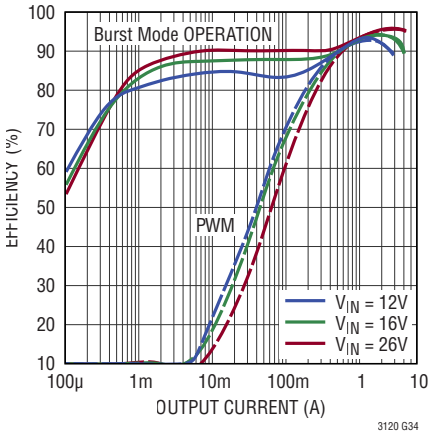

**Efficiency, $V_{OUT}$ = 20V, $f_{SW}$ = 2MHz**



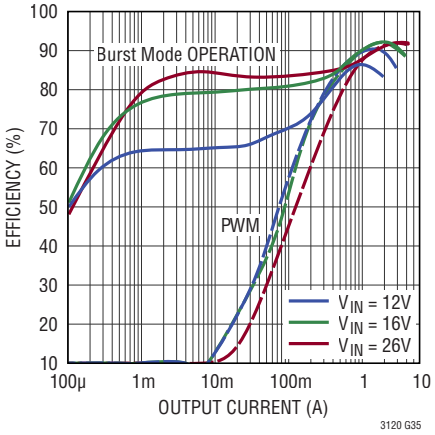

**Efficiency, $V_{OUT}$ = 24V, $f_{SW}$ = 500kHz**




**Efficiency, $V_{OUT}$ = 24V, $f_{SW}$ = 1MHz**

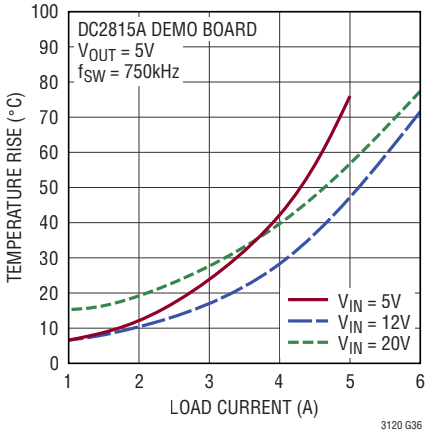



**Efficiency, $V_{OUT}$ = 24V, $f_{SW}$ = 2MHz**

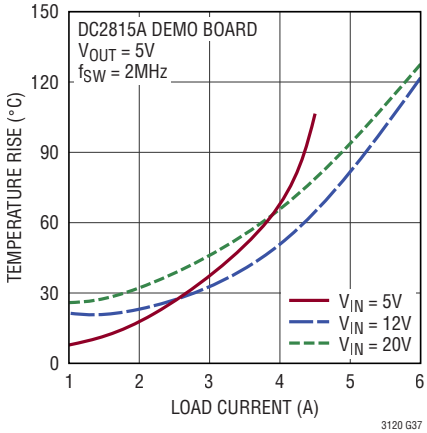


# TYPICAL PERFORMANCE CHARACTERISTICS

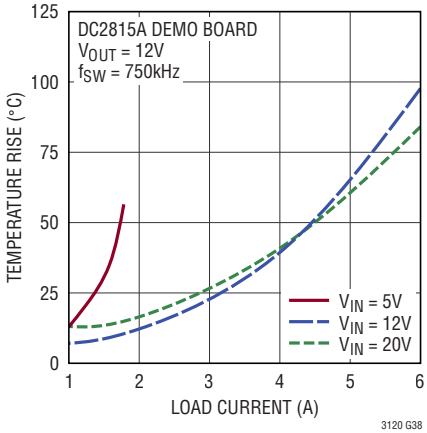
### Temperature Rise vs Load Current




### Temperature Rise vs Load Current




### Temperature Rise vs Load Current

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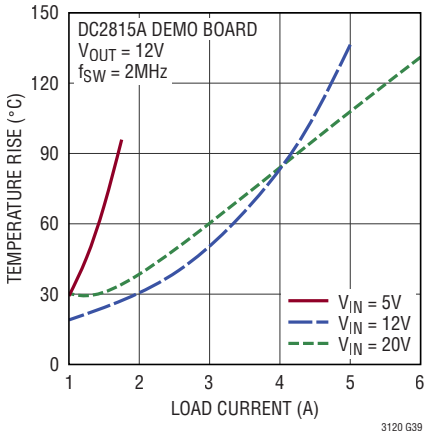
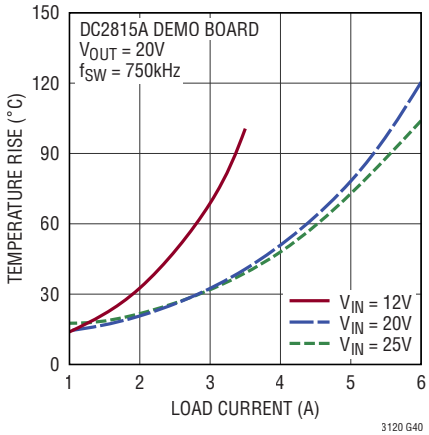
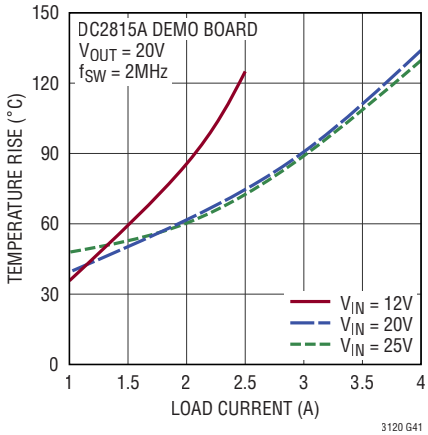


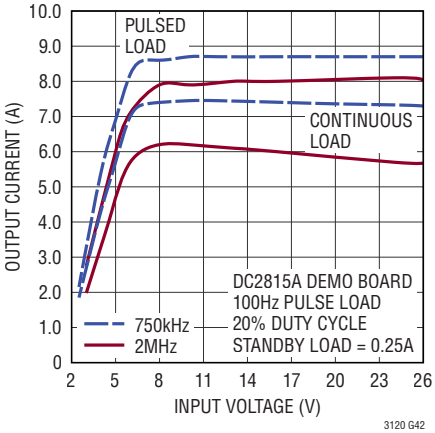

### Temperature Rise vs Load Current



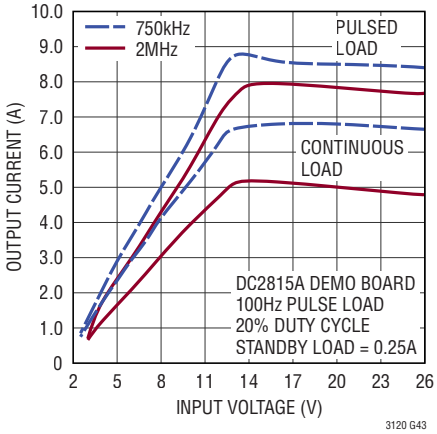

### Temperature Rise vs Load Current



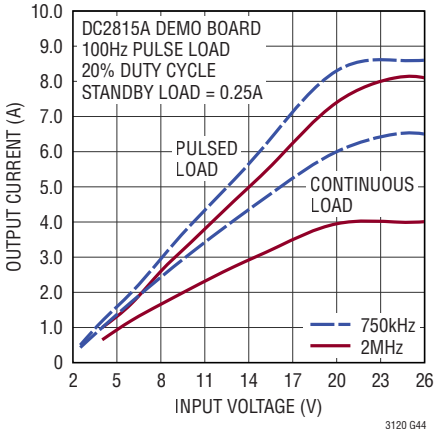

### Maximum Output Current, $V_{OUT}$ = 5V




### Maximum Output Current, $V_{OUT}$ = 12V

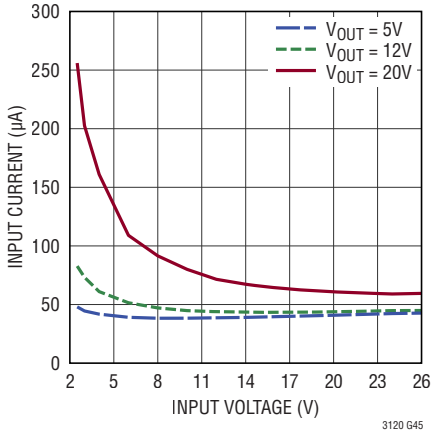



### Maximum Output Current, $V_{OUT}$ = 20V

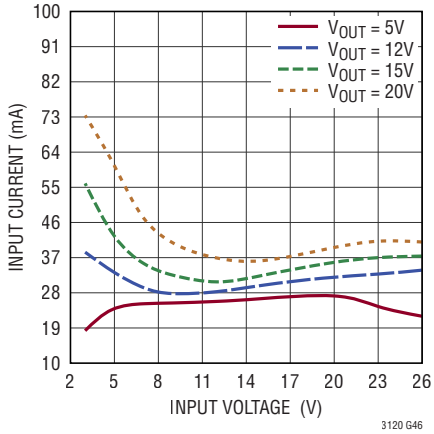


## TYPICAL PERFORMANCE CHARACTERISTICS

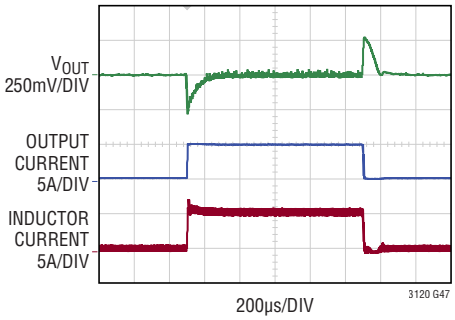
**Burst Mode Operation No-Load Input Current**



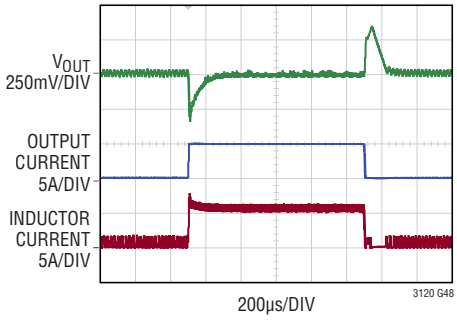

**PWM Mode No-Load Input Current**



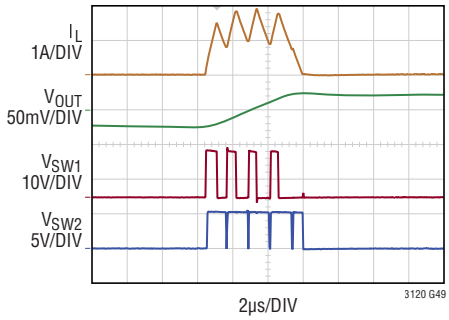

**PWM Mode Operation 0.5A to 5A Load Step, $V_{IN}$ = 12V, $V_{OUT}$ = 5V**



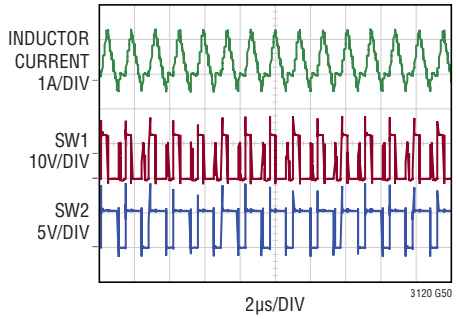

**Burst Mode Operation 0.5A to 5A Load Step, $V_{IN}$ = 12V, $V_{OUT}$ = 5V**




**Burst Mode Operation $V_{OUT}$ Ripple, $V_{OUT}$ = 5V**




**PWM Light Load Operation, $V_{OUT}$ = 5V**



## PIN FUNCTIONS

**BST3 (Pin 1):** Flying Capacitor Pin for Output Current Sense Amplifier. This pin must be connected to $PV_{OUT}$ through a 22nF capacitor.

**$PV_{OUT}$ (Pins 2, 4):** Output Voltage Power Connection. These pins are connected to switch D of the buck-boost converter. Connect a low ESR capacitor between these pins and GND using the lowest impedance path possible.

**GND (Pins 3, 11, 18, 22, Exposed Pad Pin 29):** Ground Connection. These pins should be connected to the board ground using the shortest and widest connections possible. High via density should be used under the exposed pad to maximize heat transfer away from the part.

**ISP (Pin 5):** Current Sense Positive Input. Connect this pin to the IC side of the output current sense resistor. If current sense is not being used, connect this pin to $PV_{OUT}$.

**ISN (Pin 6):** Current Sense Negative Input. Connect this pin to the $V_{OUT}$ side of the output current sense resistor. If current sense is not being used, connect this pin to $PV_{OUT}$.

**PGOOD (Pin 7):** Open Drain Output Indicator. When FB drops too far below its regulated voltage this output pulls to ground. Connect a pull-up resistor from this pin to a positive supply. Refer to the Operation section for more detail.

**PROG (Pin 8):** Output Average Current Limit Set Point. A resistor should be connected between this pin and GND to program the maximum average output current. The output current from this pin can also be used as an analog output current indicator. To disable this function, the pin should be connected to $V_{CC}$.

**FB (Pin 9):** Feedback Voltage Input. A resistive divider connected to this pin sets the output voltage for the buck-boost converter. The nominal FB voltage is 0.795V.

**VC (Pin 10):** Error Amplifier Output. A frequency compensation network must be connected between this pin and GND to stabilize the voltage control loop.

**MPPC (Pin 12):** Maximum Power Point Control Pin Setpoint. Connect this pin to a resistive divider from $V_{IN}$ to GND to set the input regulation voltage. When not being used, the MPPC pin should be tied to $V_{CC}$.

**$V_{CC}$ (Pin 13):** Internal Regulator Output Voltage. This pin is the output of the internal low voltage linear regulator used to supply the control circuitry. A 4.7µF capacitor should be connected between this pin and GND using the shortest trace possible. An additional external load of up to 10mA may be drawn from this output.

**RT (Pin 14):** Oscillator Frequency Programming Pin. Connect a resistor between this pin and GND to set the buck-boost converter switching frequency.

**SYNC/MODE (Pin 15):** Automatic Burst Mode Operation/PWM Mode Control Pin and Synchronization Input. Forcing this pin high causes the IC to operate in fixed frequency PWM mode at all loads using the internal oscillator at the frequency set by the RT Pin. Forcing this pin low, causes the IC to enable Burst Mode operation at light loads to maximize efficiency. Clocking this pin will cause the part to synchronize to the clock for frequencies higher than the frequency programmed by the RT Pin. When using this pin for synchronization, a minimum input pulse width of 100ns must be used.

**EN/UVLO (Pin 16):** Input to Enable and Disable the IC and Set Custom Input UVLO Threshold. The EN/UVLO pin can be driven by external logic signals to enable and disable the IC. In addition, the voltage on this pin can be set by a resistive divider connected to the input voltage to provide an accurate undervoltage lockout threshold. The IC is enabled if the EN/UVLO pin voltage exceeds 1.215V nominally.

**$V_{IN}$ (Pin 17):** Input Voltage Pin for Internal $V_{CC}$ Regulator.

**$PV_{IN}$ (Pins 19, 20, 21):** Input Voltage Power Connection. These pins are connected to switch A of the buck-boost converter. Connect a 10µF or larger capacitor between these pins and GND using the lowest impedance path possible.

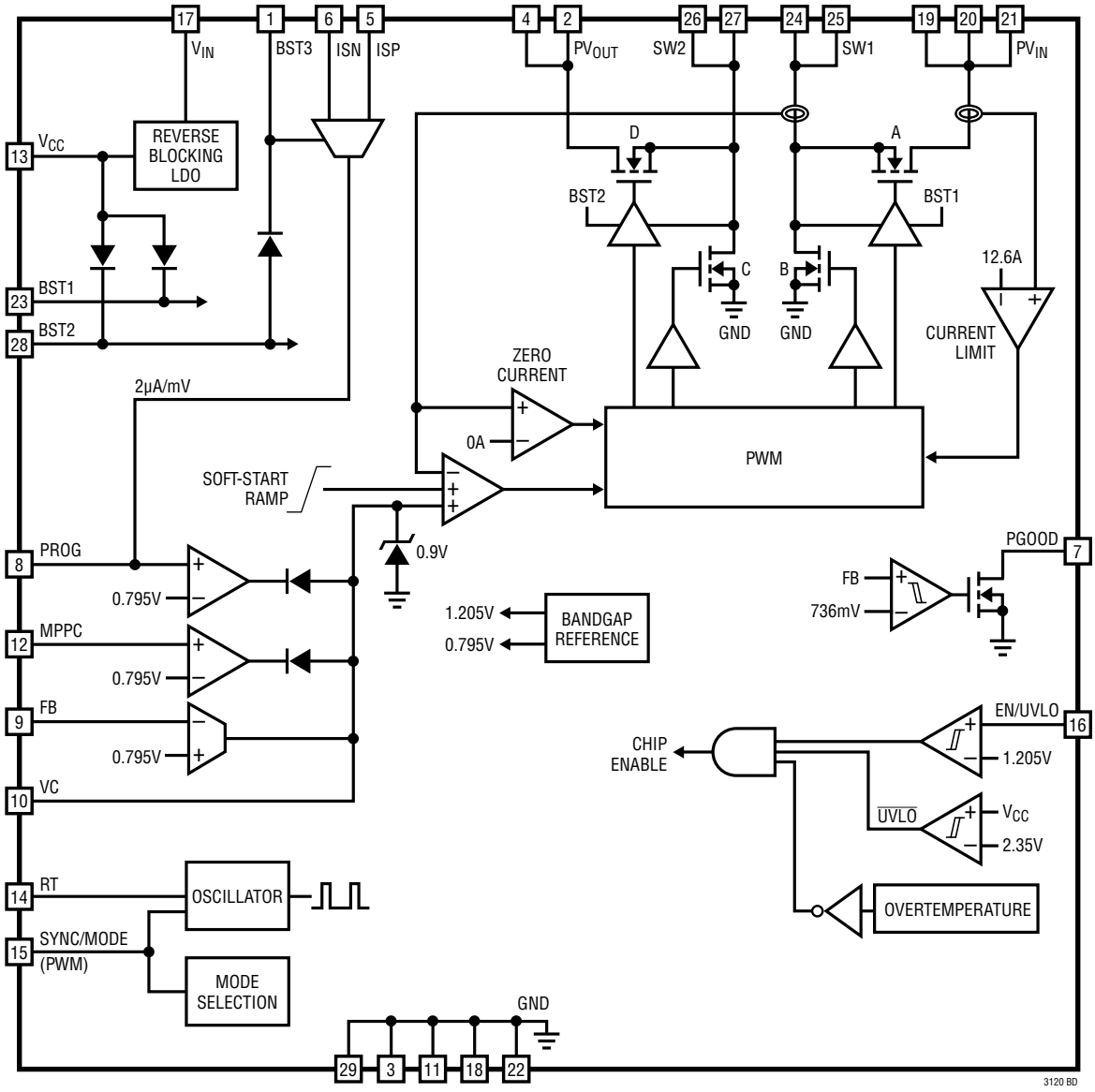
**BST1 (Pin 23):** Flying Capacitor Pin for SW1. This pin must be connected to SW1 through a 0.22µF capacitor. This pin is used to generate the gate drive rail for power switch A.

**SW1 (Pins 24, 25):** Buck-Boost Converter Power Switch Pin. These pins should be connected to one side of the buck-boost inductor.

**SW2 (Pins 26, 27):** Buck-Boost Converter Power Switch Pin. These pins should be connected to one side of the buck-boost inductor.

**BST2 (Pin 28):** Flying Capacitor Pin for SW2. This pin must be connected to SW2 through a 0.22µF capacitor. This pin is used to generate the gate drive rail for power switch D. The capacitance on this node should be 10 times greater than that used between BST3 and $PV_{OUT}$.

## BLOCK DIAGRAM



# OPERATION

## INTRODUCTION

The LT3120 is a monolithic buck-boost DC/DC converter that can operate over 2.5V to 26V input voltage and 0.8V to 24V output voltage range. Integrated low $R_{DS(ON)}$ N-channel DMOS power switches reduce solution complexity and maximize conversion efficiency. Internal high side power switch drivers require only two small external capacitors and further simplify application circuit design. The LT3120 incorporates many additional features to allow for maximum flexibility when designing application solutions, including an accurate EN/UVLO pin comparator, wide operating frequency range of 400kHz to 2MHz, external clock synchronization, power good indicator, and Maximum Power Point Control (MPPC) of the input voltage for operation from current limited sources such as photovoltaic arrays.

High side drive and sense circuitry allow for operation to 0V on the output while maintaining current control and synchronous switch operation. Operation to voltages below 2.5V on the input is also possible when bootstrapping the $V_{CC}$ pin from $V_{OUT}$, or other alternate sources, allowing for maximum extraction of energy from storage devices such as supercapacitors.

A proprietary ultralow noise PWM switching algorithm maintains output regulation with input voltages that are below, equal to, or above the output voltage. Transitions between buck and boost operating modes occur seamlessly without transients or subharmonic switching. The LT3120 has an internal oscillator that can be configured to operate over a wide range of frequencies. Using a single programming resistor, the operating frequency can be configured between 400kHz and 2MHz allowing for flexibility when optimizing for board area and efficiency. The internal oscillator can also be synchronized to an external clock applied to the SYNC/MODE pin in noise sensitive applications.

Burst Mode operation allows for high efficiency operation at light loads while automatically transitioning to PWM mode at heavier loads. At low output currents, Burst Mode operation is enabled, with a current of only 30µA (typical). In shutdown the total supply current is further reduced to 3µA (maximum).

## PWM MODE OPERATION

If the SYNC/MODE pin is held high, or the load current on the converter is high enough to command PWM mode operation with the SYNC/MODE pin held low, the LT3120 operates in a fixed frequency PWM mode. The operating frequency is defined by the resistance on the RT pin as described in the Applications Information section of this data sheet. PWM mode minimizes output voltage ripple and yields a low noise switching frequency spectrum. A proprietary switching algorithm provides seamless transitions between operating modes and eliminates discontinuities in the average inductor current, inductor ripple current and loop transfer function throughout all modes of operation. These advantages result in increased efficiency, improved loop stability and lower output voltage ripple in comparison to a traditional buck-boost converter. Figure 1 shows the topology of the LT3120 power stage which is comprised of four N-channel DMOS switches and their associated gate drivers.

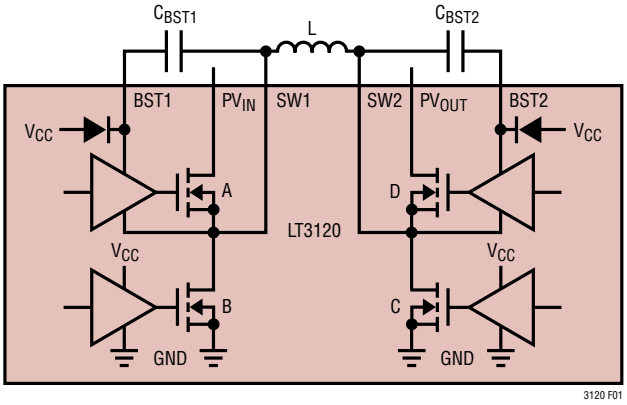



**Figure 1. Power Stage Schematic**

In PWM mode operation, both switch pins transition on every cycle independent of the input and output voltages. The internal average current control loop operates such that the pulse width modulator generates the appropriate switch duty cycle to maintain regulation of the output voltage.

### Oscillator and Phase-Locked Loop

The LT3120 operates from an internal oscillator with a switching frequency that is configured by a single external resistor between the RT pin and GND. For noise sensitive applications, an internal phase-locked loop allows the

## OPERATION

LT3120 to be synchronized to an external clock signal applied to the SYNC/MODE pin. The phase-locked loop is only able to increase the frequency of the internal oscillator to obtain synchronization. Therefore, the resistor $R_T$ must be chosen to program the internal oscillator to a lower frequency than the frequency of the clock applied to the SYNC/MODE pin. Sufficient margin must be included to account for the frequency variation of the external synchronization clock as well as the worst-case variation in frequency of the internal oscillator. In most cases setting the internal oscillator frequency 20% lower than the synchronization clock is sufficient. Whether operating from its internal oscillator or synchronized to an external clock signal, the LT3120 is able to operate with a switching frequency from 400kHz to 2MHz, providing the ability to trade-off small solution size and optimum power conversion efficiency.

### EN/UVLO Pin Comparator

In addition to serving as a logic-level input to enable the IC, the EN/UVLO pin features an accurate internal comparator allowing it to be used to set custom rising and falling input undervoltage lockout thresholds with the addition of an external resistor divider. When the EN/UVLO pin is driven above its logic threshold (typically 0.8V), the $V_{CC}$ regulator is enabled which provides power to the internal control circuitry of the IC and the accurate EN/UVLO pin comparator is enabled. If the EN/UVLO pin voltage is increased further so that it exceeds the EN/UVLO comparator threshold (1.205V nominal), the buck-boost converter will be enabled. If the EN/UVLO pin is brought below the EN/UVLO comparator threshold, the buck-boost converter will inhibit switching, but the $V_{CC}$ regulator and control circuitry will remain powered unless the EN/UVLO pin is brought below its logic threshold. Therefore, in order to place the part in shutdown and reduce the input current to its minimum level (3µA), it is necessary to ensure that the EN/UVLO pin is brought below the worst-case logic threshold (0.3V). The EN/UVLO pin is a high voltage input and can be connected directly to $V_{IN}$ to continuously enable the part when the input supply is present. If the EN/UVLO pin is forced above approximately 5V, it will sink a small current as given by Equation 1.

$$I_{EN/UVLO} = \frac{(V_{EN/UVLO} - 5V)}{5M\Omega} \quad (1)$$

With the addition of an external resistor divider as shown in Figure 2, the EN/UVLO pin can be used to establish a custom input undervoltage lockout threshold. The buck-boost converter is enabled when the EN/UVLO pin reaches 1.205V which allows the rising UVLO threshold to be set via the resistor divider ratio. Once the EN/UVLO pin reaches the threshold voltage, the comparator switches and the buck-boost converter is enabled. When the part is enabled an internal 0.25µA (typical) current source is enabled which sources current out of the EN/UVLO pin raising the EN/UVLO pin voltage away from the threshold.

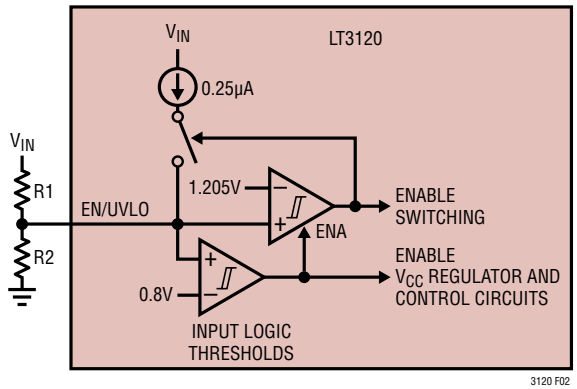



**Figure 2. Accurate EN/UVLO Pin Comparator**

In order to disable the part, $V_{IN}$ must be reduced sufficiently to overcome the hysteresis generated by this current as well as the 90mV hysteresis of the EN/UVLO comparator. As a result, the amount of hysteresis can be independently programmed without affecting the rising UVLO threshold by scaling the values of both resistors.

### $V_{CC}$ REGULATOR

An internal low dropout regulator generates the 3.73V (nominal) $V_{CC}$ rail from $V_{IN}$. The $V_{CC}$ rail powers the internal control circuitry and powers device gate drivers of the LT3120. In addition to powering the internal circuitry of the LT3120, the $V_{CC}$ regulator can also support an external load of 10mA. The $V_{CC}$ regulator is disabled when the EN/UVLO pin is below its logic threshold and enabled when the EN/UVLO pin is above its logic threshold. The $V_{CC}$ regulator includes current limit protection to safeguard against short-circuiting and overload conditions. For ap-

## OPERATION

plications where the output voltage is set to 5V, $V_{CC}$ can be driven from the output rail through a Schottky diode. Bootstrapping in this manner can provide a significant efficiency improvement, particularly at large voltage step-down ratios, and also allows operation down to lower input voltages. The maximum operating voltage for the $V_{CC}$ pin is 5.5V and care must be taken to ensure that this limit is not exceeded when driving $V_{CC}$ externally.

### Current Mode Control

The LT3120 utilizes an average current mode control scheme shown in Figure 3. Current mode control provides simplified loop compensation, rapid response to load transients and inherent line voltage rejection. The voltage on the VC pin defines the average inductor current level , and is adjusted by the error amplifiers to maintain regulation of the active control loop (FB or MPPC).

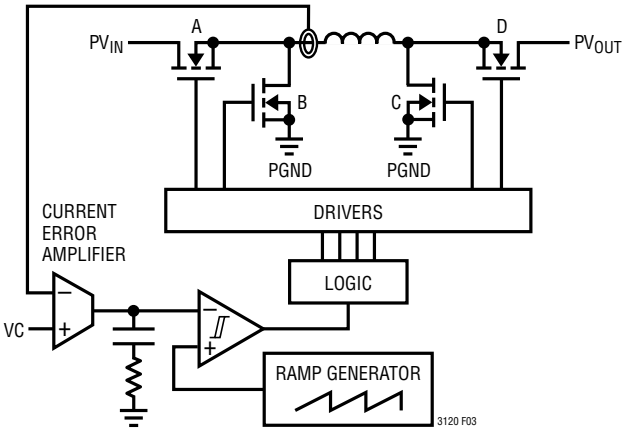



**Figure 3. Inner Average Current Loop Diagram**

The internal current mode control loop error amplifier compares the sensed average inductor current and the commanded average inductor current level to modulate the SW1 and SW2 pins on a cycle-by-cycle basis.

The average current mode control technique is similar to peak current mode control except that the average current amplifier, by virtue of its configuration as an integrator, controls average current instead of the peak current. This difference eliminates the peak-to-average current error of peak current mode control, while maintaining most of the advantages inherent to peak current mode control. Compensation of the inner current loop is accomplished by an internal compensation network that is optimized to provide high bandwidth and low regulation error under all operating conditions.

### ERROR AMPLIFIERS

Integrated into the LT3120 are three separate error amplifiers to control the input to the inner current mode control loop. These amplifiers monitor voltages at the FB , PROG, and MPPC pins. The outputs from these amplifiers are summed together and used as the commanded current level for the inner current mode control loop. To ensure stability, a compensation network must be connected between the output of the error amplifiers (VC pin) and GND. A Type II compensation network, as shown in Figure 4, is recommended for most applications since it provides the flexibility to optimize converter response while minimizing DC errors in the output voltage.

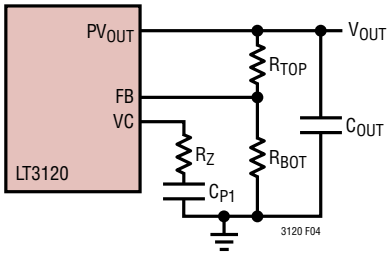



**Figure 4. FB and VC Pin Configuration**

While the FB error amplifier is the only amplifier with the ability to increase the commanded current level, all amplifiers can reduce the commanded current to maintain regulation for their associated control loop (see Block Diagram). At any given time, only one control loop is active while the other two are inactive. Priority is given to the PROG and MPPC control loops, which can override the voltage loop and reduce the commanded current level. When under control of the MPPC or PROG error amplifiers, the compensation network of the VC pin is ignored in favor of the compensation for the loop which is in control.

# OPERATION

## CURRENT LIMIT AND ZERO CURRENT DETECTION

The LT3120 incorporates inductor current limiting. The average current mode control loop clamps the average current in the inductor to 9.5A (typical). This ensures a smooth transition into current limit and protects against current levels beyond the capability of the IC.

An additional maximum peak current limit of 12.6A (typical) limits the instantaneous current in the inductor and may be triggered briefly on hard output shorts prior to the average current loop responding.

The LT3120 incorporates dedicated zero current detection comparators to minimize reverse current during switching and provide discontinuous mode operation. The zero current detection thresholds are adjusted based on operating conditions to avoid subharmonic switching and may result in small amounts of negative current under some conditions. When the part is being controlled by the MPPC control loop, the zero cross comparator threshold is set to approximately 150mA to help prevent any reverse current from discharging the output storage element.

## SOFT-START

The LT3120 soft-start circuit minimizes input current transients and output voltage overshoot on initial power-up. The required timing components for soft-start are internal to the LT3120 and produce a typical soft-start duration of 6ms. The internal soft-start circuit slowly ramps the command signal to the current mode control loop (VC pin voltage). In doing so, the inductor current is also slowly increased, starting from zero. Soft-start is reset by the $V_{CC}$ UVLO, the EN/UVLO pin accurate enable comparator, and thermal shutdown.

## MAXIMUM POWER POINT CONTROL (MPPC)

The MPPC input of the LT3120 can be used with an optional external voltage divider to dynamically adjust the commanded inductor current in order to maintain a minimum input voltage. This is primarily useful when using resistive sources, such as photovoltaic panels, to maximize input power transfer and prevent $V_{IN}$ from dropping too low under load. Referring to Figure 5, the MPPC pin is internally connected to the noninverting input of a transconductance amplifier. If the MPPC pin voltage falls below the reference voltage, the output of the amplifier reduces the commanded average inductor current (VC pin voltage) to reduce the input current and regulate $V_{IN}$ to the programmed minimum voltage.

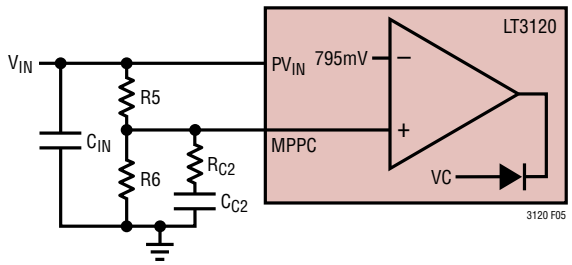



**Figure 5. MPPC Pin Configuration**

External compensation may also be required and is generally provided by a series resistor and capacitor connected between the MPPC pin and GND. This compensation network is in parallel with the lower resistor of the $V_{IN}$ voltage divider network.

## PROGRAMMABLE OUTPUT CURRENT

The LT3120 includes an optional programmable current limit that can be used to control current to the output load. The current limit circuit requires an external sense resistor $R_{SEN}$ connected between ISP and ISN and a programming resistor from PROG to ground.

The current sense amplifier outputs a current from the PROG pin that is proportional to the voltage between pins ISP and ISN. Output current limiting will begin when the voltage on the PROG pin reaches 795mV.

The current output from the PROG pin is equal to Equation 2.

$$I_{PROG} = 2\mu A/mV \bullet R_{SEN} \bullet I_{OUT} \quad (2)$$

Independent value selection for $R_{SEN}$ and $R_{PROG}$ allow designs to trade-off current sense accuracy and power loss in the sense element. The output current is programmed using Equation 3.

$$I_{LIMIT} = 795V/(2 \bullet R_{SEN} \bullet R_{PROG}) \quad (3)$$

## OPERATION

The value for $R_{SEN}$ should be selected to limit the maximum voltage between ISP and ISN to 25mV at current limit.

For current monitoring applications, the values for $R_{SEN}$ and $R_{PROG}$ should be selected to not exceed 700mV on the PROG pin.

When current sensing is not used, the ISP and ISN pins should be tied to $PV_{OUT}$ and the PROG pin should be tied to $V_{CC}$.

### Burst Mode OPERATION

When the SYNC/MODE pin is held low, the LT3120 is configured for Burst Mode operation. As a result, the buck-boost DC/DC converter will operate with continuous PWM switching until the output current drops to low levels at which point the converter will automatically transition to power saving Burst Mode operation. When operating in Burst Mode operation, the LT3120 will go into a sleep state when the output voltage achieves its nominal regulation level. The sleep state halts PWM switching and powers down all nonessential functions of the IC, reducing the quiescent current of the LT3120 to just 30µA (typical). This greatly improves overall power conversion efficiency for light loads. Since the converter is not switching in sleep, the output voltage will slowly decay at a rate determined by the output load resistance and the output capacitor value. When the output voltage has decayed by a small amount, the LT3120 will wake and initiate PWM switching operation until the output voltage on $V_{OUT}$ is restored to the previous level. If the load is very light, the LT3120 may only need to switch for a few cycles to restore $V_{OUT}$ and will sleep for extended periods of time, significantly improving efficiency. If the load is suddenly increased above the burst transition threshold, the part will automatically enter continuous PWM operation until the load is once again reduced. Note that Burst Mode operation is inhibited until soft-start is completed and $V_{OUT}$ has reached regulation. Burst Mode operation is also inhibited when the MPPC loop is in control.

### POWER GOOD INDICATOR

The LT3120 provides an open-drain PGOOD output that pulls low if $V_{OUT}$ falls more than 8% (typical) below its programmed value. When $V_{OUT}$ rises to within 6.8% (typical) of its programmed value, the internal PGOOD pull-down will turn off and PGOOD will go high if an external pull-up resistor has been provided. An internal filter prevents nuisance trips of PGOOD due to short transients on $V_{OUT}$. Note that PGOOD can be pulled up to any voltage, as long as the absolute maximum rating of 27V is not exceeded. The PGOOD function is active when the EN/UVLO pin voltage is above the logic enable threshold of 0.8V (typical). When the EN/UVLO pin voltage is below 0.8V (typical) and the $V_{CC}$ supply is still present, the PGOOD pull-down will be enabled.

### THERMAL CONSIDERATIONS

The power switches in the LT3120 are designed to operate continuously with currents up to the internal current limit thresholds. Operating at high current levels results in significant heat generated within the IC. In addition, in many applications the $V_{CC}$ regulator is operated with large input-to-output voltage differentials resulting in significant additional power dissipation in the pass element. As a result, careful consideration must be given to the thermal environment of the IC in order to optimize efficiency and ensure that the LT3120 is able to provide its full-rated output current. Specifically, the exposed thermal pad of the LQFN must be soldered to the PC board. The PC board should be designed to maximize the conduction of heat out of the IC package, maximizing vias from the thermal pad connection to a large area of exposed copper. Additional benefit can be realized through the use of thinner printed circuit boards, and higher layer counts with internal layers tied to the thermal vias. These steps minimize thermal resistance of the PCB, allowing for operation over a wider temperature range and greater output current levels. If the die temperature exceeds approximately 165°C, the IC will enter overtemperature shutdown and all switching will be inhibited. The part will remain disabled until the die cools by approximately 10°C. The soft-start circuit is re-initialized in over temperature shutdown to provide a smooth recovery when the fault condition is removed.

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### $V_{CC}$ Capacitor Selection

The $V_{CC}$ output on the LT3120 is generated from the input voltage by an internal low dropout regulator. The $V_{CC}$ regulator has been designed for stable operation with a wide range of output capacitors. For most applications, a 4.7µF low ESR ceramic capacitor is a good choice. The capacitor should connect to the $V_{CC}$ pin and ground through the shortest traces possible.

### Bootstrapping the $V_{CC}$ Regulator

For output voltages between 4.5V and 6V, the $V_{CC}$ regulator can be supplied using a diode from $V_{OUT}$ to $V_{CC}$ as shown in Figure 6. The appropriate diode should be selected to ensure that the output voltage, less the diode forward voltage, is within the acceptable external forcing voltage of 4.2V to 5.5V. This may be accomplished through the use of Schottky diodes or silicon diodes. In either case, the diode should have sufficient current handling capability to drive the $V_{CC}$ pin.

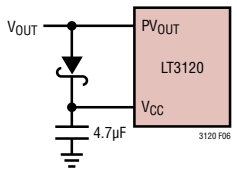


**Figure 6. Bootstrapping $V_{CC}$ from $V_{OUT}$**

For applications that use an output voltage that is beyond the maximum ratings for the $V_{CC}$ pin (e.g. $V_{OUT}$ = 7V), a diode-OR can be used between the input voltage and output voltage to power the internal $V_{CC}$ regulator. This is accomplished by tying the diode-OR node to the $V_{IN}$ pin and connecting the $PV_{IN}$ pins to the input source. In this configuration, an additional bypass capacitor is required between the $V_{IN}$ pin and GND in addition to the bypass capacitor located between $PV_{IN}$ and GND. This configuration is shown in Figure 7.

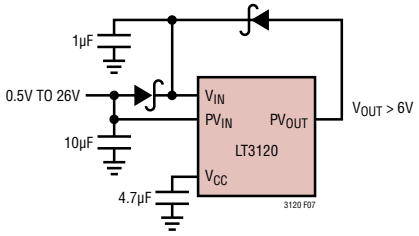


**Figure 7. Diode-OR of Input Supply and $V_{OUT}$ Powers $V_{CC}$ Regulator**

### Programming Custom $V_{IN}$ UVLO thresholds

With the addition of an external resistive divider connected to $V_{IN}$ as shown in Figure 8, the EN/UVLO pin can be used to program the input voltage at which the LT3120 is enabled and disabled.

For a rising input voltage, the LT3120 is enabled when $V_{IN}$ reaches a threshold given by Equation 4, where R1 and R2 are the values of the resistor divider resistors.

$$V_{TH(RISING)} = 1.205V\left(\frac{R1+R2}{R2}\right) \quad (4)$$

To ensure robust operation in the presence of noise, the EN/UVLO pin has two forms of hysteresis. A fixed 90mV hysteresis within the EN/UVLO pin comparator provides hysteresis equal to 7.5% of the input turn-on voltage independent of the resistor divider values. In addition, an internal hysteresis current that is sourced from the EN/UVLO pin generates an additive level of hysteresis which can be programmed by the value of R1 to increase the overall hysteresis to suit the requirements of specific applications.

Once the IC is enabled, it will remain enabled until the input voltage drops below the comparator threshold by the hysteresis voltage, $V_{HYST}$, as given by Equation 5 where R1 and R2 are the values of the voltage divider.

$$V_{HYST} = R1 \bullet 0.25\mu A + \left(\frac{R1+R2}{R2}\right) \bullet 0.09V \quad (5)$$

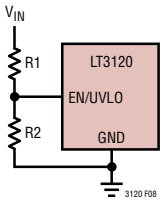


**Figure 8. Setting the Input UVLO and Hysteresis**

Therefore, the rising UVLO threshold and the amount of hysteresis can be independently programmed via appropriate selection of resistors R1 and R2. For high levels of hysteresis, the value of R1 can become larger than is desirable in a practical implementation. In such cases, the

## APPLICATIONS INFORMATION

amount of hysteresis can be increased further through the addition of an additional resistor $R_H$, as shown in Figure 9.

When using the additional $R_H$ resistor, the rising EN/UVLO pin threshold remains as given by the original equation and the hysteresis is given by Equation 6.

$$V_{HYST} = \left(\frac{R_H R2 + R_H R1 + R1R2}{R2}\right)0.25\mu A + \left(\frac{R1+R2}{R2}\right)0.09V \quad (6)$$

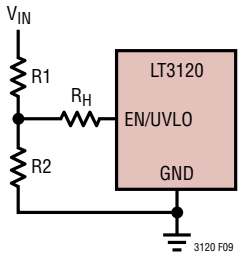


**Figure 9. Increasing Input UVLO Hysteresis**

To improve the noise robustness and accuracy of the UVLO threshold, the EN/UVLO pin input can be filtered by adding a 470pF capacitor from EN/UVLO to GND. Larger valued capacitors should not be utilized because they could interfere with operation of the hysteresis.

### Switching Frequency Selection

The switching frequency is set by the value of a resistor connected between the RT pin and ground. The switching frequency is related to the resistor value by Equation 7 where $R_T$ is the resistance:

$$f_{SW} \cong \frac{100MHz}{8+(1.2 \bullet R_T / k\Omega)} \quad (7)$$

Higher switching frequencies facilitate the use of smaller inductors as well as smaller input and output filter capacitors which results in a smaller solution size and reduced component height. However, higher switching frequencies also generally reduce conversion efficiency due to the increased switching losses.

### Output Capacitor Selection

A low ESR output capacitor should be utilized at the buck-boost converter output in order to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent option as they have low ESR and are available in small footprints. The capacitor value should be chosen large enough to reduce the output voltage ripple to acceptable levels. Neglecting the capacitor ESR and ESL, the peak-to-peak output voltage ripple can be calculated by Equation 8, where $f_{SW}$ is the switching frequency, $C_{OUT}$ is the output capacitance, $t_{LOW}$ is the switch pin minimum low time, and $I_{LOAD}$ is the output current. Curves for the value of $t_{LOW}$ as a function of switching frequency and temperature can be found in Typical Performance Characteristics section.

$$\Delta V_{P-P(BUCK)} \cong \frac{I_{LOAD} t_{LOW}}{C_{OUT}}$$
$$\Delta V_{P-P(BOOST)} \cong \frac{I_{LOAD}}{f_{SW} C_{OUT}}\left(\frac{V_{OUT} - V_{IN} + t_{LOW} f_{SW} V_{IN}}{V_{OUT}}\right) \quad (8)$$

The output voltage ripple increases with load current and is generally higher in boost mode than in buck mode. These expressions only take into account the output voltage ripple that results from the output current being discontinuous. They provide a good approximation to the ripple at any significant load current but underestimate the output voltage ripple at very light loads where output voltage ripple is dominated by the inductor current ripple.

In addition to output voltage ripple generated across the output capacitance, there is also output voltage ripple produced across the internal resistance of the output capacitor. The ESR-generated output voltage ripple is proportional to the series resistance of the output capacitor and is given by Equation 9 where $R_{ESR}$ is the series resistance of the output capacitor and all other terms are as previously defined.

$$\Delta V_{P-P(BUCK)} \cong \frac{I_{LOAD} \bullet R_{ESR}}{1 - t_{LOW} \bullet f_{SW}} \cong I_{LOAD} \bullet R_{ESR}$$
$$\Delta V_{P-P(BOOST)} \cong \frac{I_{LOAD} \bullet R_{ESR} \bullet V_{OUT}}{V_{IN}(1 - t_{LOW} \bullet f_{SW})} \cong I_{LOAD} \bullet R_{ESR}\left(\frac{V_{OUT}}{V_{IN}}\right) \quad (9)$$

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### Input Capacitor Selection

$PV_{IN}$ pins carry the full inductor current and provides power to internal control circuits in the IC. To minimize input voltage ripple and ensure proper operation of the IC, a low ESR bypass capacitor with a value of at least 10µF should be located as close to this pin as possible. The traces connecting this capacitor to $PV_{IN}$ and the ground plane should be made as short as possible. The $V_{IN}$ pin provides power to the $V_{CC}$ regulator and other internal circuitry. If the PCB trace connecting $V_{IN}$ to $PV_{IN}$ is long, it may be necessary to add an additional small value bypass capacitor near the $V_{IN}$ pin.

When powered through long leads or from a high ESR power source, a larger value bulk input capacitor may be required. In such applications, a 47µF to 100µF electrolytic capacitor in parallel with a 1µF ceramic capacitor generally yields a high performance, low cost solution.

When powered through an inductive connection such as a long cable, the inductance of the power source and the input bypass capacitor form a high-Q resonant LC filter. In such applications, hot-plugging into a powered source can lead to a significant voltage overshoot, even up to twice the nominal input source voltage. Care must be taken in such situations to ensure that the absolute maximum input voltage rating of the LT3120 is not violated. See Analog Devices Application Note 88 for solutions to increase damping in the input filter and minimize this voltage overshoot.

### Inductor Selection

The choice of inductor used in LT3120 application circuits influences the maximum deliverable output current, the converter bandwidth, the magnitude of the inductor current ripple and the overall converter efficiency. The inductor must have a low DC series resistance, when compared to the internal switch resistance (25mΩ), or output current capability and efficiency will be compromised. Larger inductor values reduce inductor current ripple but may not increase output current capability as is the case with peak current mode control. Larger value inductors also tend to have a higher DC series resistance for a given case size, which will have a negative impact on efficiency. Larger values of inductance will also lower the right half plane zero (RHPZ) frequency when operating in boost mode, which can compromise loop stability. Nearly all LT3120 application circuits deliver the best performance with an inductor value between 1.5µH and 15µH. Buck mode only applications can use the larger inductor values as they are unaffected by the RHPZ, while mostly boost applications generally require inductance on the lower end of this range depending on how large the step-up ratio is. Regardless of inductor value, the saturation current rating should be selected such that it is greater than the worst-case average inductor current plus half of the ripple current.

The peak-to-peak inductor current ripple for each operational mode can be calculated using Equation 10, where $f_{SW}$ is the programmed switching frequency, L is the inductance and $t_{LOW}$ is the switch pin minimum low time, typically 70ns.

$$\Delta I_{L(P\text{-}P)(BUCK)} \cong \frac{V_{OUT}}{L}\left(\frac{V_{IN}-V_{OUT}}{V_{IN}}\right)\left(\frac{1}{f_{SW}}-t_{LOW}\right)$$
$$\Delta I_{L(P\text{-}P)(BOOST)} \cong \frac{V_{IN}}{L}\left(\frac{V_{OUT}-V_{IN}}{V_{OUT}}\right)\left(\frac{1}{f_{SW}}-t_{LOW}\right) \quad (10)$$

It should be noted that the worst-case peak-to-peak inductor ripple current occurs when the duty cycle in buck mode is minimum (highest $V_{IN}$) and in boost mode when the duty cycle is 50% ($V_{OUT} \cong 2 \bullet V_{IN}$).

As an example, if $V_{IN}$ (minimum) = 2.5V and $V_{IN}$ (maximum) = 15V, $V_{OUT}$ = 5V, $f_{SW}$ = 1MHz and L = 4.7µH, the peak-to-peak inductor ripples at the voltage extremes (15V $V_{IN}$ for buck and 2.5V $V_{IN}$ for boost). See Equation 11.

$$\Delta I_{L(P\text{-}P)(BUCK)} \cong \frac{5V}{4.7\mu H}\left(\frac{15V-5V}{15V}\right)\bullet 930ns = 659mA$$
$$\Delta I_{L(P\text{-}P)(BOOST)} \cong \frac{2.5V}{4.7\mu H}\left(\frac{5V-2.5V}{5V}\right)\bullet 930ns = 247mA \quad (11)$$

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One half of this inductor ripple current must be added to the highest expected average inductor current in order to select the proper saturation current rating for the inductor.

### Programming the Output Voltage

The output voltage is set via the external resistive divider comprised of resistors $R_{TOP}$ and $R_{BOT}$ as shown in Figure 4. The resistor divider values determine the output regulation voltage according to Equation 12.

$$V_{OUT} = 0.795V \bullet \left(1 + \frac{R_{TOP}}{R_{BOT}}\right) \quad (12)$$

### Programming the MPPC Voltage

The LT3120 includes an MPPC function to optimize performance when operating from current limited input sources. Using an external voltage divider from $V_{IN}$, the MPPC function takes control of the average inductor current when necessary to maintain a minimum input voltage $V_{MPPC}$, as programmed by the user. (See Figure 5).

$$V_{MPPC} = 0.795V \bullet \left(1 + \frac{R5}{R6}\right) \quad (13)$$

This is useful for such applications as photovoltaic powered converters, since the maximum power transfer point occurs when the photovoltaic panel is operated at approximately 75% of its open-circuit voltage. For example, when operating from a photovoltaic panel with an open-circuit voltage of 10V, the maximum power transfer point will be when the panel is loaded such that its output voltage is about 7.5V.

When using the MPPC function, the input capacitor should be sized between 100µF and 470µF. Resistor R6 should be chosen between 50k and 250k. Lower values will result in smaller undershoot of the MPPC tracking point during line and load transient conditions, but will draw more current from the input supply. For this example, a value of 100kΩ will be used. The value of R5 can then be determined using Equation 14 to set the desired input MPPC voltage.

$$R5 = \left(\frac{V_{MPPC}}{0.795V} - 1\right) \bullet R6 = \left(\frac{7.5V}{0.795V} - 1\right) \bullet 100k\Omega \quad (14)$$

$$= 843k\Omega \cong 845k\Omega$$

Using these resistor values, the MPPC function is programmed to control the maximum input current so as to maintain $V_{IN}$ at a minimum of 7.56V. Note that if the photovoltaic panel can provide more power than the LT3120 can draw or the load requires, the input voltage will rise above the programmed MPPC point. Higher input voltages do not present a problem so long as the input voltage does not exceed the maximum operating input voltage. For photovoltaic panel applications, it may be also desirable to use the programmable EN/UVLO feature to disable the part when $V_{IN}$ drops too low due to lack of sufficient light. Using the EN/UVLO pin provides a well-controlled behavior when the input power source is dropping out by halting switching to prevent discharge of the output. This custom input UVLO voltage should be programmed to be below the MPPC tracking voltage with sufficient margin to ensure the part does not disable under transient conditions.

The MPPC loop requires compensation to maintain stability of the input voltage regulation loop. This can be accomplished by means of a pole-zero pair on the MPPC pin created with a series RC network in parallel with the lower MPPC resistor R6 as shown in Figure 5.

The pole and zero locations should be selected to create a low frequency pole at or below approximately 360Hz and a zero at a frequency that is scaled based on the size of the input capacitor. Equation 15 determines the values for the compensation capacitor $C_{C2}$, and zero resistor $R_{C2}$.

$$C_{C2} = \frac{1}{2\pi \bullet R_6 \bullet 360Hz}$$

$$R_{C2} = \frac{C_{IN}}{2\pi \bullet C_{C2}} \quad (15)$$

Using the divider values from the previous example and a 220µF input capacitor, the value of the compensation components can be calculated as shown in Equation 16.

$$C_{C2} = \frac{1}{2\pi \bullet 100k\Omega \bullet 360Hz} = 4.42nF \cong 4.3nF$$

$$R_{C2} = \frac{220\mu F}{2\pi \bullet 4.3nF} = 8.14k\Omega \cong 8.25k\Omega \quad (16)$$

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### PROG Programming

A current sense amplifier monitors the voltage between the ISP and ISN pins and outputs a proportional current from the PROG pin. The voltage on the PROG pin is compared to a temperature stable reference voltage of 0.795V, and if the PROG pin voltage exceeds this reference value the inductor current is scaled back to maintain the desired level of output current. The output current limit is configured using a resistor connected between the PROG pin and GND. A small capacitor may optionally be placed in parallel with the resistor. The values for the RC components are calculated using Equation 17.

$$R_{PROG} = \frac{0.795V}{2\frac{mA}{V} \bullet R_{SEN} \bullet I_{OUT}} \qquad (17)$$

$$C_{PROG} = \frac{3300nF \bullet \Omega}{R_{PROG}}$$

### Compensation of the Buck-Boost Converter

The LT3120 incorporates an average current mode control architecture which consists of two control loops. Both the inner average current mode control loop and outer control loop require compensation to maintain stability. The inner current mode control loop is internally compensated to maintain wide bandwidth and good transient response. For many applications, the inner current loop can be treated like a voltage controlled current source (VCCS). This current source is commanded by the voltage error amplifier to regulate the output load formed primarily by the load resistance ($R_{LOAD}$) and output capacitor ($C_{OUT}$). This simplified version is illustrated in Figure 10, showing the key components that need to be considered when compensating the converter.

With a full-scale command on VC, the LT3120 buck-boost converter will generate an average inductor current of 9.5A. With a VC voltage range of 200mV to 900mV, the resulting current gain for the inner average current loop is 13.6A/V. Similar to peak current mode control, the inner average current mode control loop effectively turns the inductor into a current source over the frequency range of interest, resulting in a frequency response from the power stage that exhibits a single pole (–20dB/decade) roll off. The output capacitor ($C_{OUT}$) and load resistance ($R_{LOAD}$) form the normally dominant low frequency pole and the effective series resistance of the output capacitor and its capacitance form a zero, usually at a high enough frequency to be ignored. A potentially troublesome right half plane zero (RHPZ) is also encountered if the LT3120 is operated in boost mode. The RHPZ causes an increase in gain, like a zero, but a decrease in phase, like a pole.

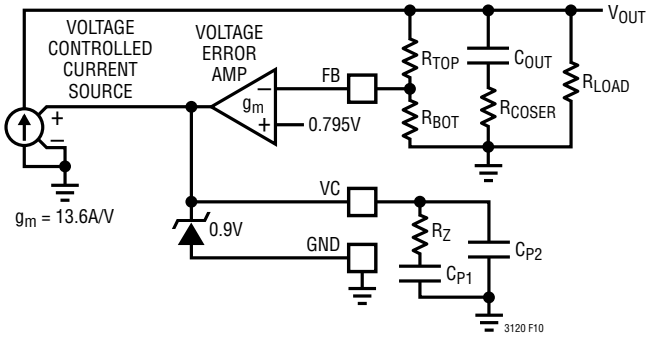


**Figure 10. Simplified Representation of Control Loop Components**

This will ultimately limit the maximum converter bandwidth that can be achieved with the LT3120. The RHPZ is not present when operating in buck mode. The overall open loop gain at DC is the product of the Equation 18 through Equation 20.

Voltage Error Amplifier Gain:

$$G_{EA} = g_m \bullet R_{EA} = 120\mu s \bullet 5M\Omega = 600 \qquad (18)$$

Voltage Divider Gain:

$$\frac{V_{FB}}{V_{OUT}} = \frac{0.795V}{V_{OUT}} \qquad (19)$$

Current Loop Transconductance:

$$G_{CS} = \frac{9.5A}{0.7V} = 13.6A/V \qquad (20)$$

It is important to note that $G_{CS}$ is the transconductance gain from the control voltage VC to the inductor current level, which equals the output current level in buck mode. In boost mode, the output current level will be reduced

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by the efficiency divided by the boost ratio (see Equation 21 and Equation 22). Refer to the typical curves for efficiency information.

$$G_{CS(OUT)} = 13.6A/V \text{ (Buck Mode)} \quad (21)$$

$$G_{CS(OUT)} = 13.6A/V \bullet \frac{V_{IN}}{2V_{OUT}} \bullet Eff \text{ (Boost Mode)} \quad (22)$$

Frequency dependent terms that affect the loop gain are given by Equation 23 through Equation 26.

Output Load Pole (P1)

$$f_{P1} = \frac{2}{2\pi \bullet R_{LOAD} \bullet C_{OUT}} \quad (23)$$

Error Amplifier Compensation (P2, Z1)

$$f_{P2} = \frac{1}{2\pi \bullet R_{EA} C_C} \text{ Hz (close to DC)} \quad (24)$$

$$f_{Z1} = \frac{1}{2\pi \bullet R_Z \bullet C_C} \text{ Hz} \quad (25)$$

Right Half Plane Zero

$$f_{RHPZ} = \frac{V_{IN}^2 \bullet R_{LOAD}}{V_{OUT}^2 \bullet 2\pi \bullet L} \text{ Hz} \quad (26)$$

In some cases it may not be possible to achieve sufficient loop bandwidth and phase margin using a simple RC network connected to the VC pin. In these cases additional compensation may be required. This is accomplished by the addition of a feed forward RC network in parallel with the top resistor of the feedback divider. A small feed forward capacitor alone may be sufficient in some applications.

A common situation that may require a feed forward network is when the converter is operating in boost mode and the closed loop crossover frequency ($f_{CC}$) is close the Right Half Plane Zero. This may be done in order to reduce output capacitance requirements by increasing the loop bandwidth. Due to the additional phase loss introduced by the RHPZ, a simple RC compensation network on the VC pin may not be able to provide sufficient phase boost to stabilize the loop.

### Compensation Example

This section will demonstrate how to derive and select the compensation components for a 5V output supplying 3A from an input voltage as low as 3V. The compensation is designed for the worse case boost mode operation which typically represents the worse case stability. Designing compensation for most other applications is simply a matter of substituting in different values to the equations given in the example and reviewing the resulting Bode Plot, adjusting as needed. Since the compensation design procedure uses a simplified model of the LT3120, results should be checked using time domain step response tests to validate the effectiveness of the compensation chosen. It is assumed that values and types for capacitors and the inductor will be selected based on the guidance given elsewhere in this data sheet. Particular attention should be paid to voltage biasing effects on capacitors used for input and output bypassing. Similarly, it is assumed that inductor values and current ratings are selected based on application requirements.

Example Operating Conditions:

$V_{IN}$ = 3V to 20V

$V_{OUT}$ = 5V

$I_{LOAD(MAX)}$ = 3A

$C_{OUT}$ = 150µF

L = 2.2µH

$f_{SW}$ = 1MHz

First it is necessary to determine the lowest frequency for $f_{RHPZ}$ (see Equation 27). This will determine the maximum bandwidth that can safely be configured for the converter while operating in boost mode.

$$f_{RHPZ} = \frac{V_{IN}^2 \bullet R_{LOAD}}{V_{OUT}^2 \bullet 2\pi \bullet L} = 43.4kHz \quad (27)$$

In order to ensure sufficient safety margin, the closed loop crossover frequency ($f_{CC}$) should be sufficiently below the RHPZ frequency to account for variability of the internal components of the IC as well as variability of external influences on the converter response at the cost of possibly higher loop bandwidth. If sufficient phase margin exists at the crossover frequency, a higher loop

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bandwidth may be realizable while still maintaining stability and good transient response. In this example, we will use cross over frequency equal to one sixth of the RHPZ frequency (see Equation 28).

$$f_{CC} = \frac{f_{RHPZ}}{7} \cong 6.2kHz \quad (28)$$

The RHPZ will have a negligible effect on the gain at the loop crossover, however it will have a phase contribution that must be considered (see Equation 29).

$$\varphi_{RHPZ} = -1 \bullet \tan^{-1}\left(\frac{fcc}{f_{RHPZ}}\right) = -1 \bullet \tan^{-1}\left(\frac{1}{7}\right) = -8.1^\circ \quad (29)$$

Since the converter will be operating in boost mode, the $G_{CS}$ term must be scaled to represent the commanded output current.

Looking in the Typical Curves section, we find the efficiency to be roughly 80%. Using this information, the effective output current gain can be calculated using Equation 30.

$$G_{CS(OUT)} = \left(G_{CS} \bullet \frac{V_{IN}}{2V_{OUT}} \bullet Eff\right) = 3.265 \, {}^{A}/_{V} \quad (30)$$

Using this information, the gain and phase contributions from the output filter are calculated using Equation 31.

$$G_{OUT} = G_{CS(OUT)} \bullet \sqrt{\frac{R_{LOAD}{}^2}{\left({}^{fcc}/_{fP1}\right)^2 + 1}} = 1.098$$

$$\varphi_{P1} = -1 \bullet \tan^{-1}\left(\frac{fcc}{f_{P1}}\right) = -1 \bullet \tan^{-1}\left(\frac{6200}{1273}\right) = -78.4^\circ \quad (31)$$

Choosing a phase margin of 50 degrees, the required phase boost from the compensation network is determined by summing together the phase contributions that were calculated in Equation 31. A phase contribution of –90° is assumed for P2.

$$\varphi_{Z1} = 50 - \varphi_{P2} - \varphi_{P1} - \varphi_{RHPZ} - 180 = 46.5^\circ \quad (32)$$

The compensation network gain is used to adjust the loop gain to crossover at the desired frequency. Using the feedback divider gain and output gain, the compensation network gain is calculated using Equation 33

$$G_{COMP} = \left(\frac{V_{REF}}{V_{OUT}} \bullet G_{OUT}\right)^{-1} = 5.727 \quad (33)$$

The compensation network resistor is then found using the error amplifier transconductance and the required compensation gain found in Equation 33.

$$R_Z = \frac{G_{COMP}}{g_m} = \frac{5.727}{120\mu s} = 47.7k\Omega \quad (34)$$

With the value of $R_Z$ now known, the compensation capacitor can be chosen to place the zero Z1 in the correct location.

$$C_{P1} = \frac{\tan(\varphi_{Z1})}{2\pi \bullet f_{CC} \bullet R_Z} = 565pF \quad (35)$$

Selecting standard value components, values of $R_Z$ = 47.5kΩ and $C_{P1}$ = 560pF are used.

### PCB Layout Considerations

The LT3120 buck-boost converter switches large currents at high frequencies. Special attention should be paid to the PC board layout to ensure a stable, noise-free and efficient application circuit. Figure 11 shows a representative PCB to outline some of the primary considerations. A few key guidelines are provided below.

1. The parasitic inductance and resistance of all circulating high current paths should be minimized. This can be accomplished by keeping the routes to all bold components in Figures 11 as short and as wide as possible. Capacitor ground connections should via down to the ground plane by way of the shortest route possible. The bypass capacitors on $PV_{IN}$, $PV_{OUT}$ and $V_{CC}$ should be placed as close to the IC as possible and should have the shortest possible paths to ground.

## APPLICATIONS INFORMATION

2. The exposed pad is the electrical ground connection for the LT3120. Multiple vias should connect the back pad directly to the ground plane. In addition, maximization of the metallization connected to the back pad will improve the thermal environment and improve the power handling capabilities of the IC.
3. There should be an uninterrupted ground plane under the entire converter in order to minimize the cross sectional area of the high frequency current loops. This minimizes EMI and reduces the inductive drops in these loops thereby minimizing SW pin overshoot and ringing.
4. Connections to all of the components shown in bold should be made as wide as possible to reduce the series resistance. This will improve efficiency and maximize the output current capability of the buck-boost converter.
5. To prevent large circulating currents in the ground plane from disrupting operation of the LT3120, all small-signal grounds should return directly to GND by way of a dedicated Kelvin route. This includes the ground connection for the RT pin resistor, and the ground connection for the feedback network as shown in Figure 11.
6. Keep the routes connecting to the high impedance, noise sensitive inputs FB and RT as short as possible to reduce noise pick-up.

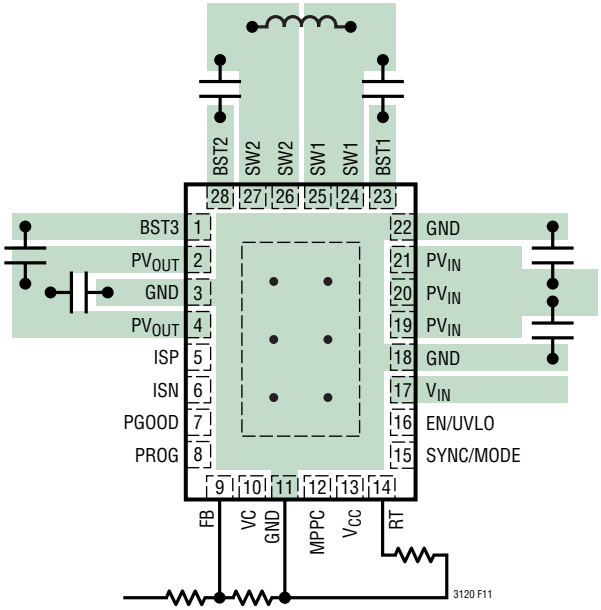
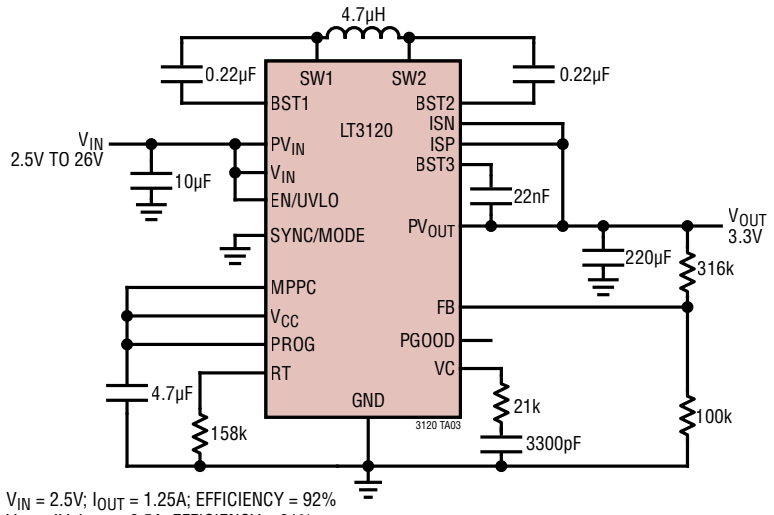



**Figure 11. PCB Layout**

# TYPICAL APPLICATIONS

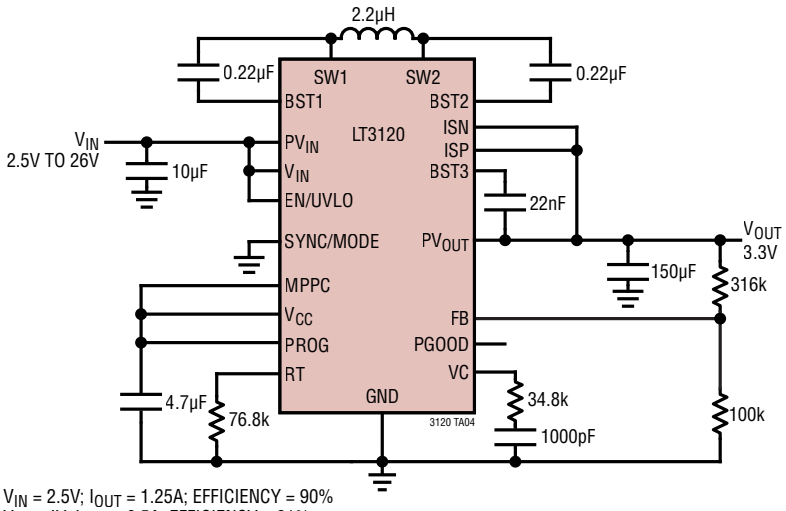
## 3.3V APPLICATION EXAMPLES

### 500kHz Wide Input Regulator




$V_{IN}$ = 2.5V; $I_{OUT}$ = 1.25A; EFFICIENCY = 92%
$V_{IN}$ = 4V; $I_{OUT}$ = 6.5A; EFFICIENCY = 81%

### 1MHz Wide Input Regulator

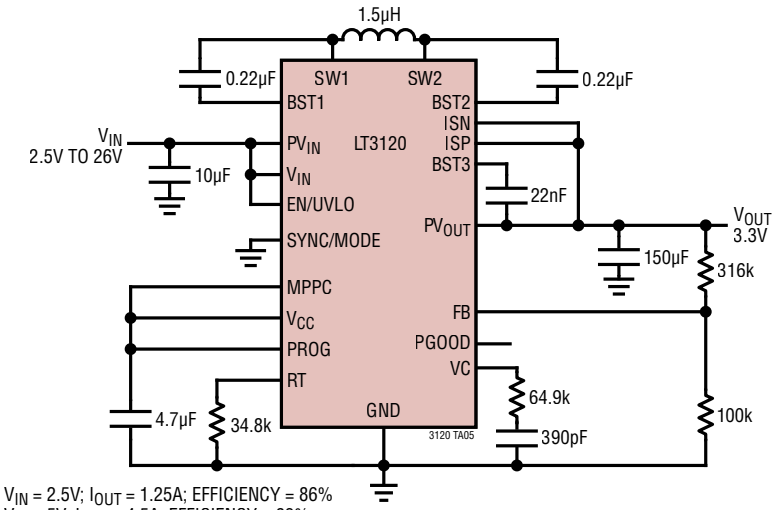



$V_{IN}$ = 2.5V; $I_{OUT}$ = 1.25A; EFFICIENCY = 90%
$V_{IN}$ = 4V; $I_{OUT}$ = 6.5A; EFFICIENCY = 81%

# TYPICAL APPLICATIONS

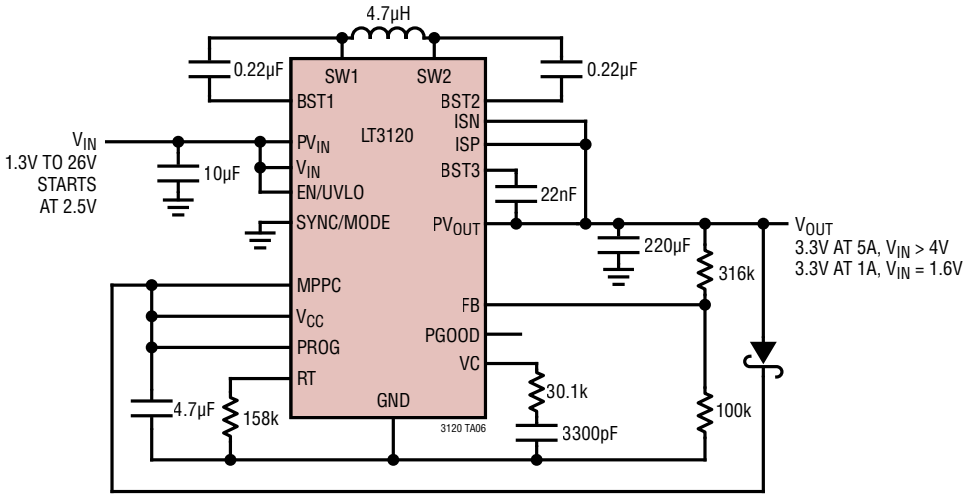
## 3.3V APPLICATION EXAMPLES

### 2MHz Wide Input Regulator




$V_{IN}$ = 2.5V; $I_{OUT}$ = 1.25A; EFFICIENCY = 86%
$V_{IN}$ = 5V; $I_{OUT}$ = 4.5A; EFFICIENCY = 83%

### 500kHz Wide Input Regulator with $V_{CC}$ Boot Strap Option

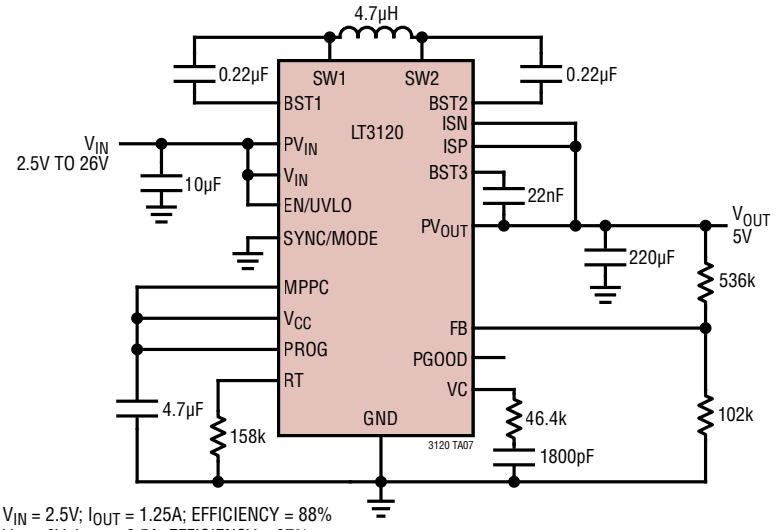



$V_{IN}$ = 1.6V; $I_{OUT}$ = 1A; EFFICIENCY = 85%
$V_{IN}$ = 2.5V; $I_{OUT}$ = 1.25A; EFFICIENCY = 92%
$V_{IN}$ = 4V; $I_{OUT}$ = 5A; EFFICIENCY = 87%

# TYPICAL APPLICATIONS

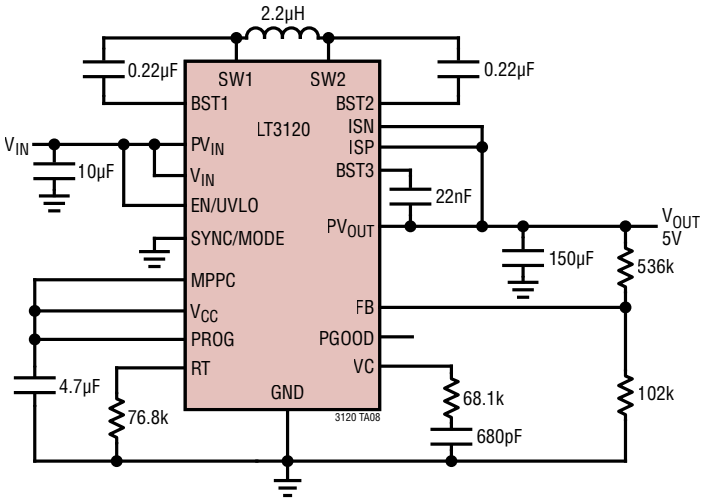
## 5V APPLICATION EXAMPLES

### 500kHz Wide Input Regulator




$V_{IN}$ = 2.5V; $I_{OUT}$ = 1.25A; EFFICIENCY = 88%
$V_{IN}$ = 6V; $I_{OUT}$ = 6.5A; EFFICIENCY = 87%

### 1MHz Wide Input Regulator

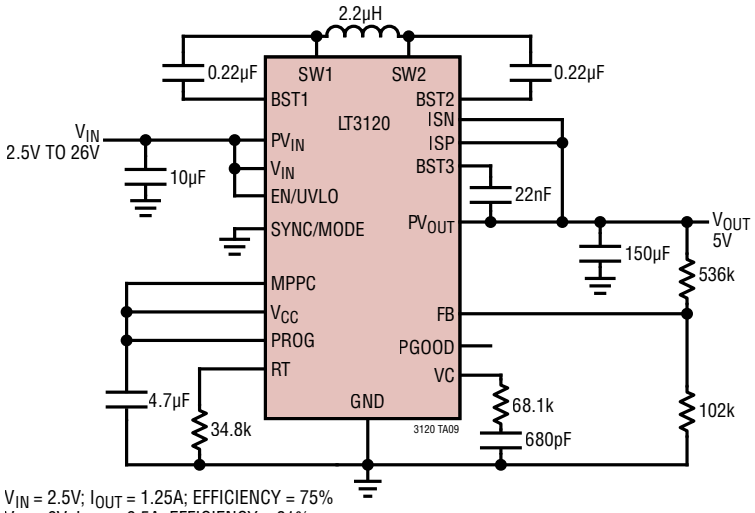



$V_{IN}$ = 2.5V; $I_{OUT}$ = 1.25A; EFFICIENCY = 85%
$V_{IN}$ = 5V; $I_{OUT}$ = 6.5A; EFFICIENCY = 86%

# TYPICAL APPLICATIONS

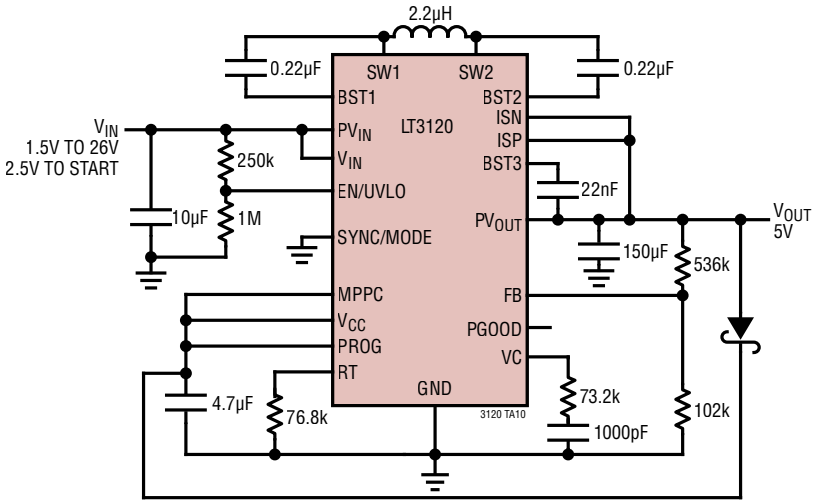
## 5V APPLICATION EXAMPLES

### 2MHz Wide Input Regulator




$V_{IN}$ = 2.5V; $I_{OUT}$ = 1.25A; EFFICIENCY = 75%
$V_{IN}$ = 6V; $I_{OUT}$ = 6.5A; EFFICIENCY = 81%

### 1MHz Wide Input Regulator with $V_{CC}$ Boot Strap Option

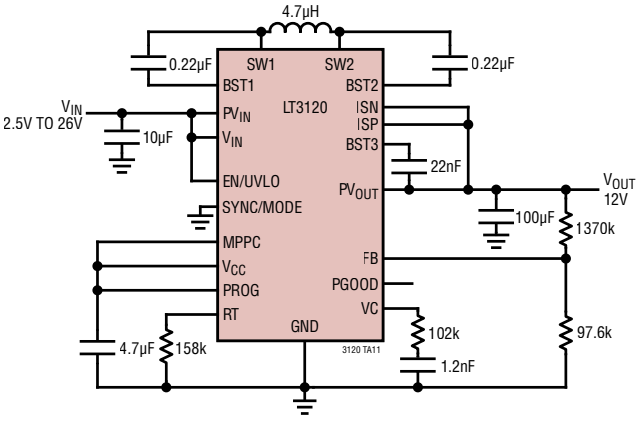



$V_{IN}$ = 1.6V; $I_{OUT}$ = 1A; EFFICIENCY = 73%
$V_{IN}$ = 2.5V; $I_{OUT}$ = 1.25A; EFFICIENCY = 88%
$V_{IN}$ = 6V; $I_{OUT}$ = 6.5A; EFFICIENCY = 85%

# TYPICAL APPLICATIONS

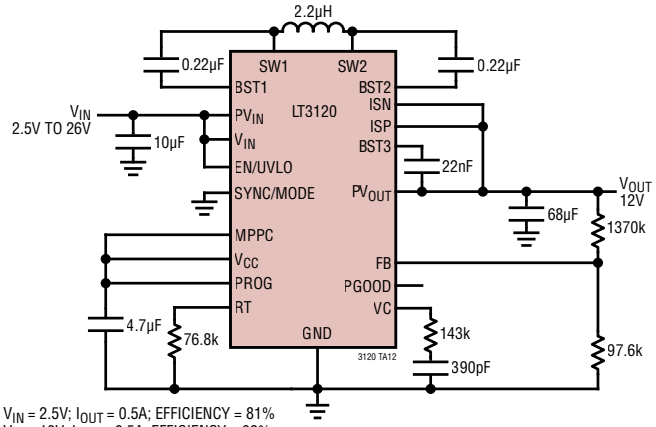
## 12V APPLICATION EXAMPLES

### 500kHz Wide Input Regulator



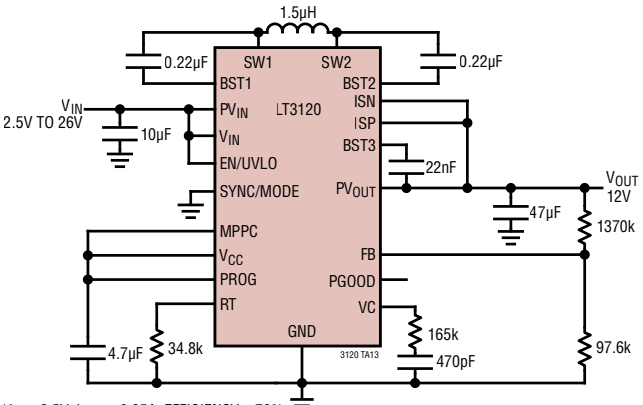

$V_{IN}$ = 2.5V; $I_{OUT}$ = 0.5A; EFFICIENCY = 82%
$V_{IN}$ = 13V; $I_{OUT}$ = 6.5A; EFFICIENCY = 92%

### 1MHz Wide Input Regulator




$V_{IN}$ = 2.5V; $I_{OUT}$ = 0.5A; EFFICIENCY = 81%
$V_{IN}$ = 13V; $I_{OUT}$ = 6.5A; EFFICIENCY = 92%

### 2MHz Wide Input Regulator

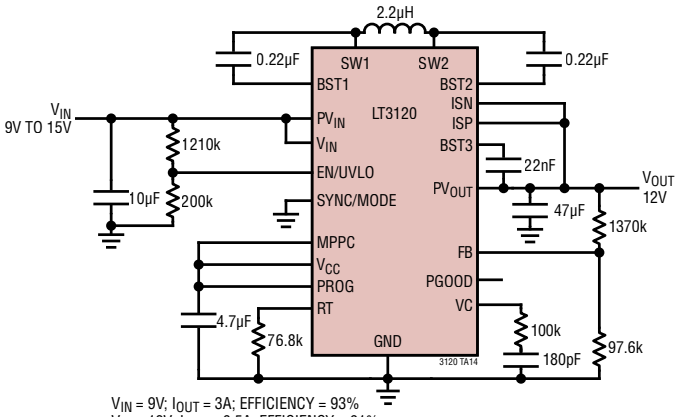



$V_{IN}$ = 2.5V; $I_{OUT}$ = 0.25A; EFFICIENCY = 78%
$V_{IN}$ = 13V; $I_{OUT}$ = 5A; EFFICIENCY = 89%

# TYPICAL APPLICATIONS

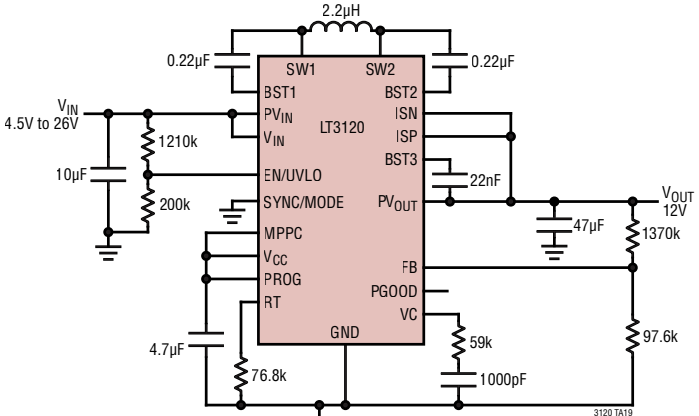
## 12V APPLICATION EXAMPLES

### 1MHz Narrow Input Regulator



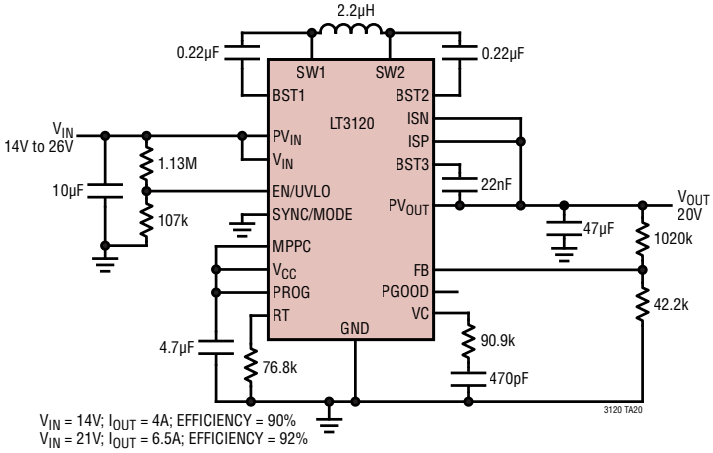

$V_{IN}$ = 9V; $I_{OUT}$ = 3A; EFFICIENCY = 93%
$V_{IN}$ = 13V; $I_{OUT}$ = 6.5A; EFFICIENCY = 91%
ENABLE AT $V_{IN}$ > 8.5V

### 1MHz 12V Line Conditioner




$V_{IN}$ = 9V; $I_{OUT}$ = 1.25A; EFFICIENCY = 95%
$V_{IN}$ = 13V; $I_{OUT}$ = 6.5A; EFFICIENCY = 92%

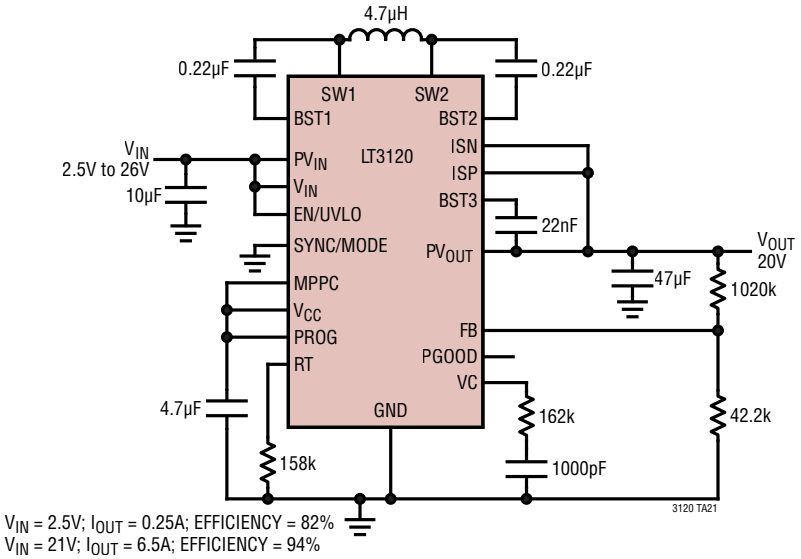
### 1MHz 20V Line Conditioner




$V_{IN}$ = 14V; $I_{OUT}$ = 4A; EFFICIENCY = 90%
$V_{IN}$ = 21V; $I_{OUT}$ = 6.5A; EFFICIENCY = 92%

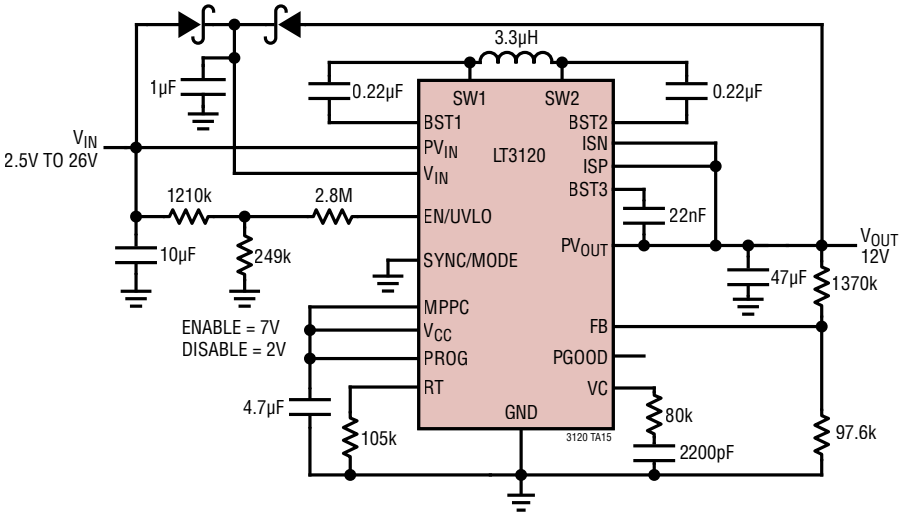
# TYPICAL APPLICATIONS

**500kHz 20V Wide Input Regulator**



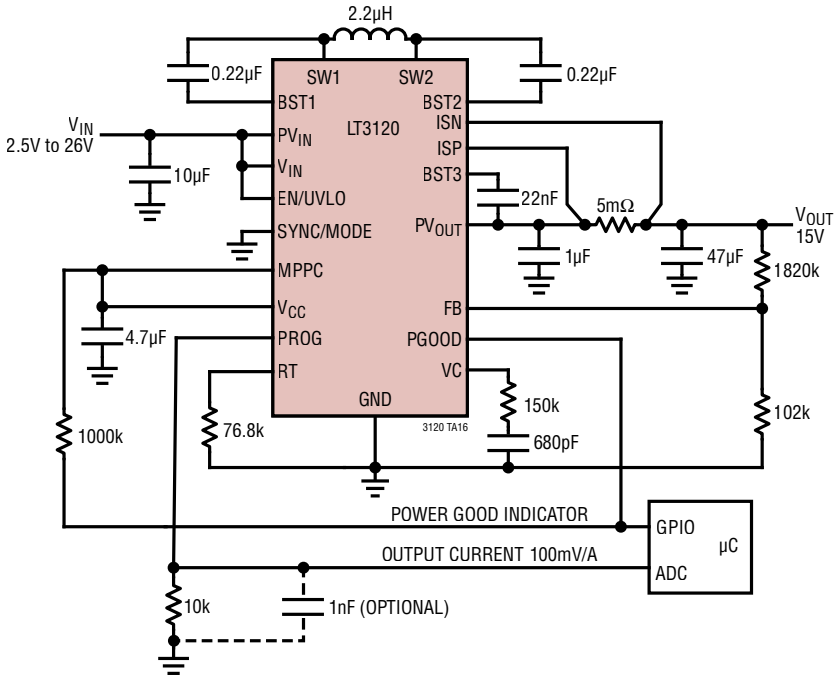

$V_{IN}$ = 2.5V; $I_{OUT}$ = 0.25A; EFFICIENCY = 82%
$V_{IN}$ = 21V; $I_{OUT}$ = 6.5A; EFFICIENCY = 94%

**750kHz, 12V Regulator with Input Supply Run Down**

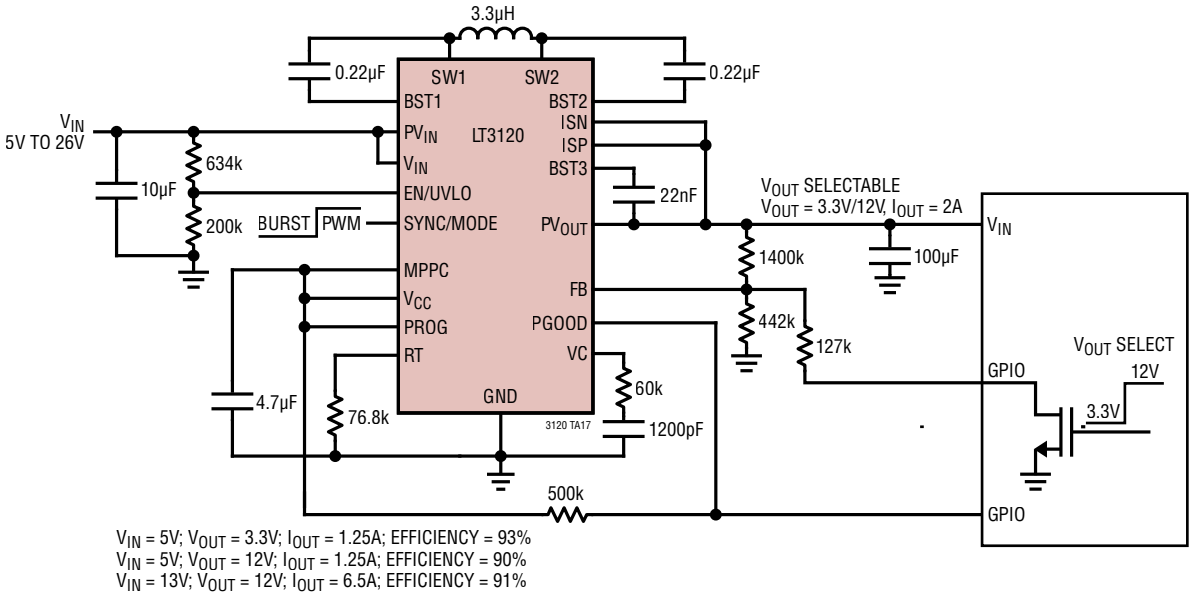


# TYPICAL APPLICATIONS

### 15V, 1MHz Regulator with Output Current Monitoring



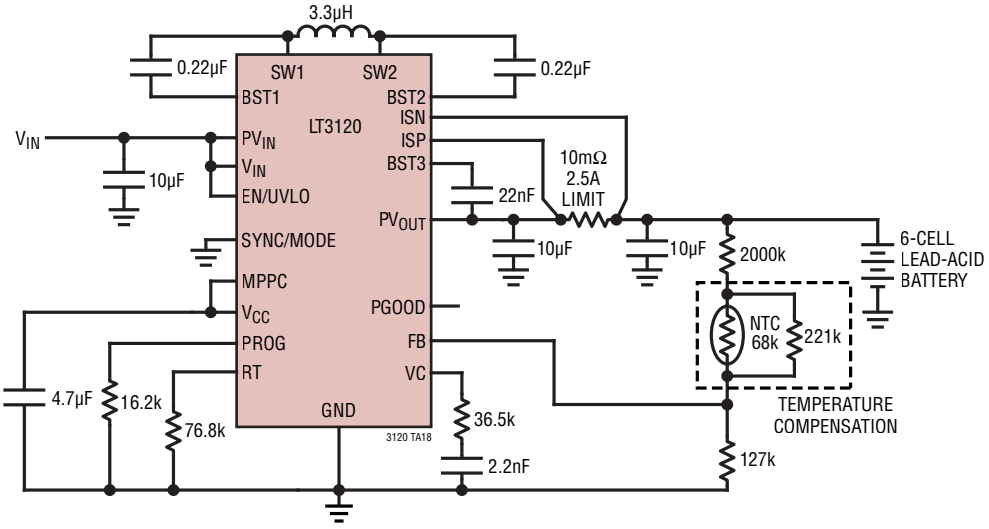

### Selectable 12V or 3.3V Output Regulator




$V_{IN}$ = 5V; $V_{OUT}$ = 3.3V; $I_{OUT}$ = 1.25A; EFFICIENCY = 93%
$V_{IN}$ = 5V; $V_{OUT}$ = 12V; $I_{OUT}$ = 1.25A; EFFICIENCY = 90%
$V_{IN}$ = 13V; $V_{OUT}$ = 12V; $I_{OUT}$ = 6.5A; EFFICIENCY = 91%

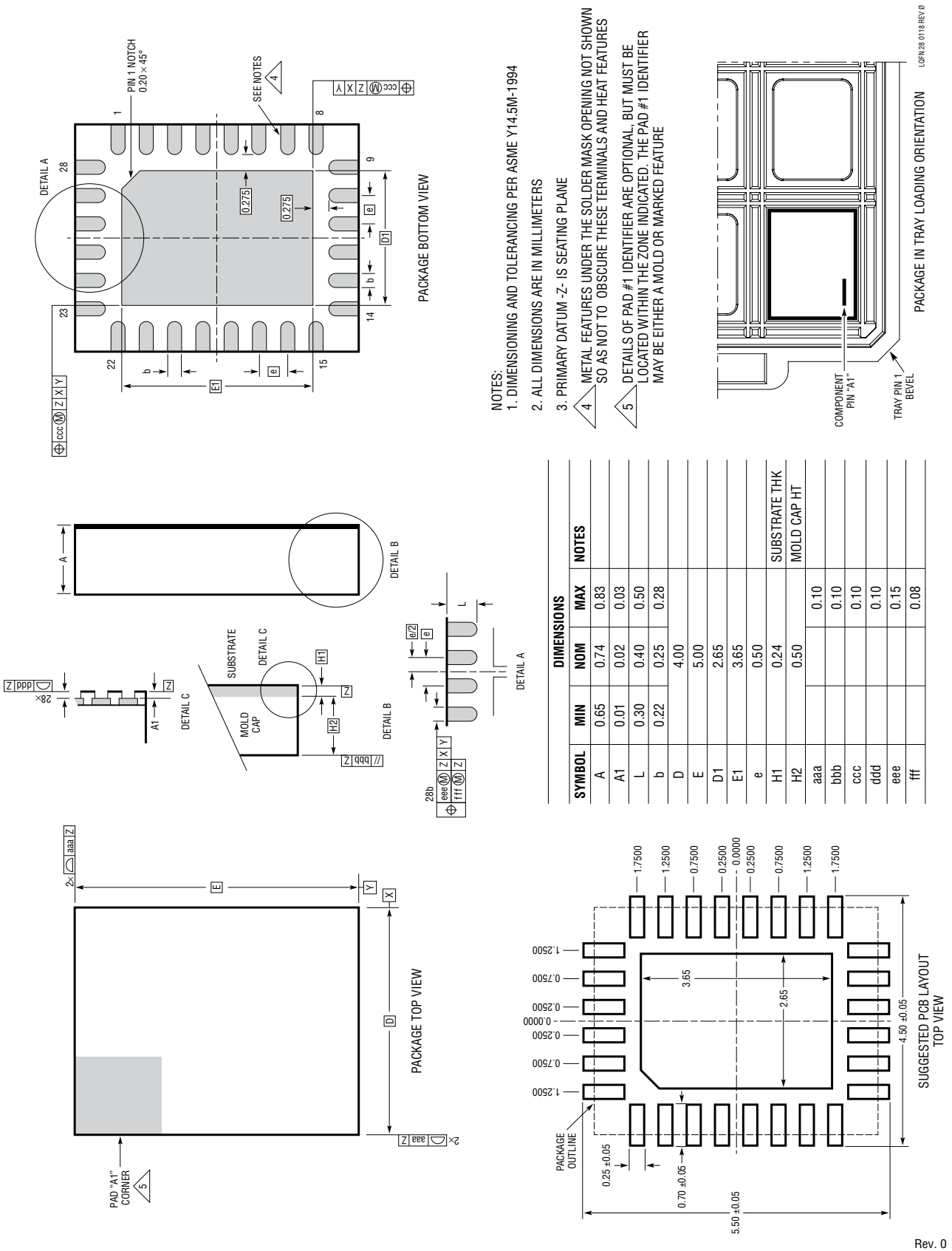
# TYPICAL APPLICATIONS

**1MHz, 2.5A Wide Input Lead Acid Charger**



# PACKAGE DESCRIPTION

**LQFN Package**
**28-Lead (5mm × 4mm × 0.74mm)**
(Reference LTC DWG # 05-08-1603 Rev Ø)

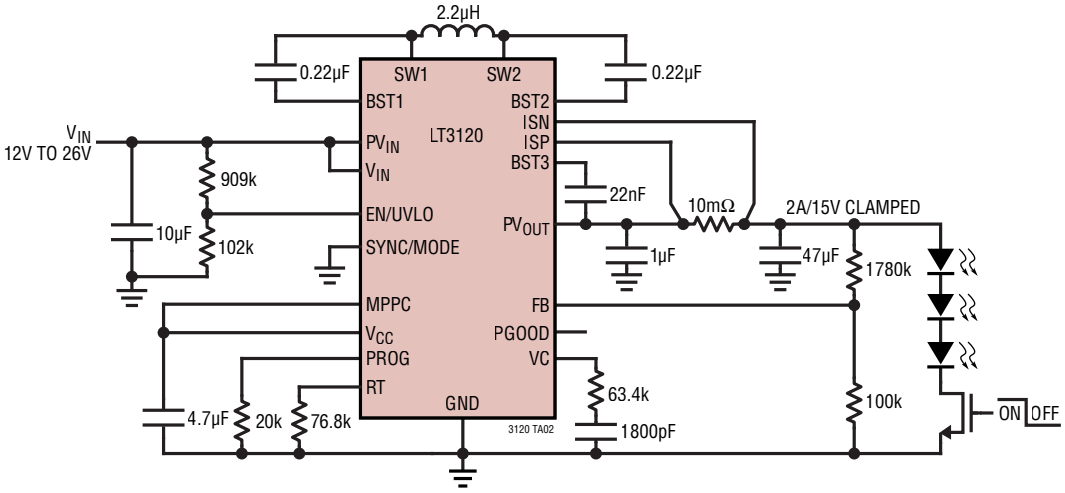



| DIMENSIONS | | | | |
|---|---|---|---|---|
| SYMBOL | MIN | NOM | MAX | NOTES |
| A | 0.65 | 0.74 | 0.83 | |
| A1 | 0.01 | 0.02 | 0.03 | |
| L | 0.30 | 0.40 | 0.50 | |
| b | 0.22 | 0.25 | 0.28 | |
| D | | 4.00 | | |
| E | | 5.00 | | |
| D1 | | 2.65 | | |
| E1 | | 3.65 | | |
| e | | 0.50 | | |
| H1 | 0.24 | | | SUBSTRATE THK |
| H2 | 0.50 | | | MOLD CAP HT |
| aaa | | | 0.10 | |
| bbb | | | 0.10 | |
| ccc | | | 0.10 | |
| ddd | | | 0.10 | |
| eee | | | 0.15 | |
| fff | | | 0.08 | |

Rev. 0

## TYPICAL APPLICATION

**1MHz, 2A LED Output with 15V Clamp Voltage**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC3112 | 15V, 2.5A Synchronous Buck-Boost | $V_{IN}$ = 2.7V to 15V, $V_{OUT}$ = 2.5V to 14V, $I_Q$ = 40µA, $I_{SD}$ < 1µA, DFN and TSSOP Packages |
| LTC3122 | 15V, 2.5A Synchronous Step-Up DC/DC Converter with Output Disconnect | $V_{IN}$ = 1.8V to 5.5V, $V_{OUT}$ = 2.2V to 15V, $I_Q$ = 25µA, $I_{SD}$ < 1µA, DFN and MSOP Packages |
| LTC3124 | 15V, 5A 2-Phase Synchronous Step-Up DC/DC Converter with Output Disconnect | $V_{IN}$ = 1.8V to 5.5V, $V_{OUT}$ = 2.5V to 15V, $I_Q$ = 25µA, $I_{SD}$ < 1µA, DFN and TSSOP Packages |
| LTC3119 | 18V, 5A Synchronous Buck-Boost | $V_{IN}$ = 2.5V to 18V, $V_{OUT}$ = 0.8V to 18V, $I_Q$ = 35µA, $I_{SD}$ < 3µA, QFN and TSSOP Packages |
| LTC3115-1/ LTC3115-2 | 40V, 2A Synchronous Buck-Boost | $V_{IN}$ = 2.7V to 40V, $V_{OUT}$ = 2.7V to 40V, $I_Q$ = 30µA, $I_{SD}$ < 3µA, DFN and TSSOP Packages |
| LT3942 | 36V, 2A Synchronous Buck-Boost Converter and LED Driver | $V_{IN}$ = 3V to 36V, $V_{OUT}$ = 0V to 36V, 4mm × 5mm QFN-28 Package |
| LT8390/ LT8390A | High Efficiency, 2MHz, Synchronous, 4-Switch Buck-Boost Controller | $V_{IN}$ = 4V to 60V, $I_{SD}$ ≤ 1µA, TSSOP-28E and 4mm × 5mm QFN-28 Packages |

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