CY7S1049G
CY7S1049GE

# 4-Mbit (512K words × 8-bit) Static RAM with PowerSnooze™ and Error Correcting Code (ECC)

## Features

- High speed
  - Access time ($t_{AA}$) = 10 ns / 15 ns
- Ultra-low power Deep-Sleep (DS) current
  - $I_{DS}$ = 15 µA
- Low active and standby currents
  - Active Current $I_{CC}$ = 38-mA typical
  - Standby Current $I_{SB2}$ = 6-mA typical
- Wide operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V
- Embedded ECC for single-bit error correction[1, 2]
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- 1.0-V data retention
- TTL- compatible inputs and outputs
- Available in Pb-free 44-pin TSOP II, and 36-pin (400-mil) molded SOJ

## Functional Description

The CY7S1049G/CY7S1049GE[1] is a high-performance PowerSnooze™ static RAM organized as 512K words × 8 bits. This device features fast access times (10 ns) and a unique ultra-low power Deep-Sleep mode[3]. With Deep-Sleep mode currents as low as 15 µA, the CY7S1049G/CY7S1049GE devices combine the best features of fast and low- power SRAMs in industry-standard package options. The device also features embedded ECC. logic which can detect and correct single-bit errors in the accessed location.

Deep-Sleep input ($\overline{DS}$) must be deasserted HIGH for normal operating mode.

To perform data writes, assert the Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW, and provide the data and address on device data pins ($I/O_0$ through $I/O_7$) and address pins ($A_0$ through $A_{18}$) respectively.

To perform data reads, assert the Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) inputs LOW and provide the required address on the address lines. Read data is accessible on the I/O lines ($I/O_0$ through $I/O_7$).

The device is placed in a low-power Deep-Sleep mode when the Deep-Sleep input ($\overline{DS}$) is asserted LOW. In this state, the device is disabled for normal operation and is placed in a low power data retention mode. The device can be activated by deasserting the Deep-Sleep input ($\overline{DS}$) to HIGH.

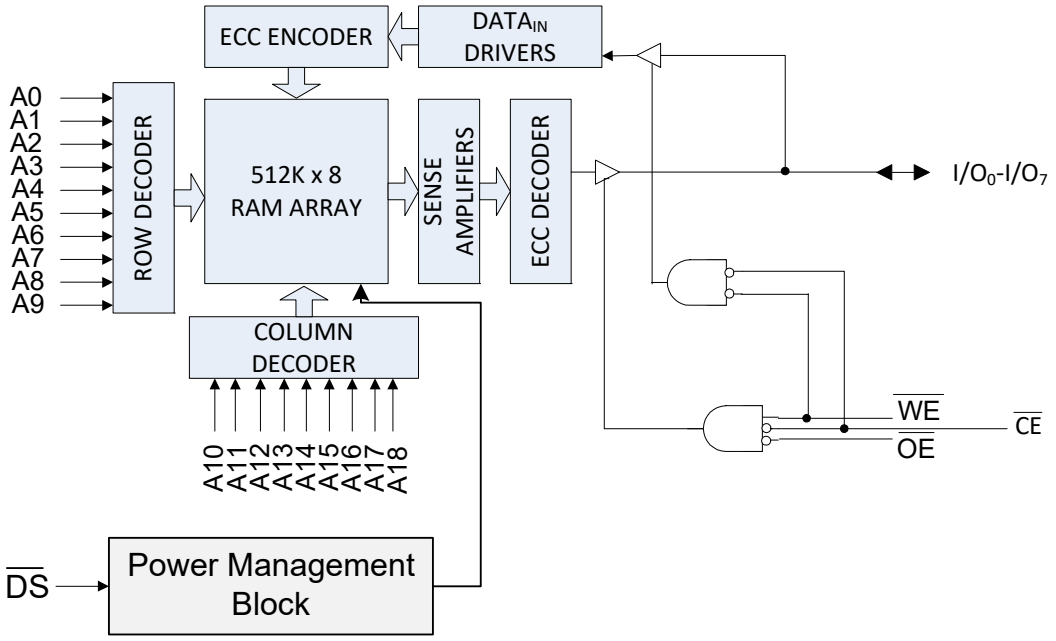
The CY7S1049G is available in 44-pin TSOP II, and 36-pin Molded SOJ (400 Mils).

## Product Portfolio

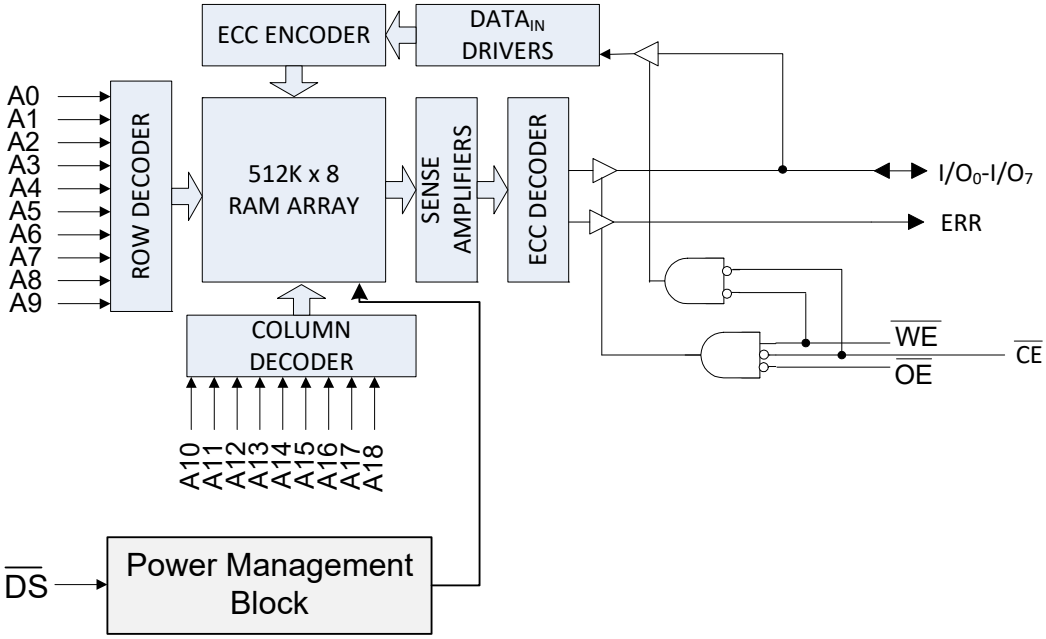
| Product[4] | Range | $V_{CC}$ Range (V) | Speed (ns) | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Operating $I_{CC}$, (mA) $f = f_{max}$ | | Standby, $I_{SB2}$ (mA) | | Deep-Sleep current (µA) | |
| | | | | Typ [5] | Max | Typ [5] | Max | Typ [5] | Max |
| CY7S1049G(E)18 | Industrial | 1.65 V–2.2 V | 15 | – | 40 | 6 | 8 | – | 15 |
| CY7S1049G(E)30 | | 2.2 V–3.6 V | 10 | 38 | 45 | | | | |
| CY7S1049G(E) | | 4.5–5.5 V | 10 | 38 | 45 | | | | |

**Notes**
1. This device does not support automatic write back on error detection.
2. SER FIT Rate <0.1 FIT/Mb. Refer AN88889 for details.
3. Refer AN89371 for details on PowerSnooze™ feature.
4. ERR pin is available only for devices which have ERR option "E" in the ordering code. Refer Ordering Information on page 17 for details.
5. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = 1.8 V (for $V_{CC}$ range of 1.65 V–2.2 V), $V_{CC}$ = 3 V (for $V_{CC}$ range of 2.2 V–3.6 V), and $V_{CC}$ = 5 V (for $V_{CC}$ range of 4.5 V–5.5 V), $T_A$ = 25 °C.

## Logic Block Diagram – CY7S1049G




## Logic Block Diagram – CY7S1049GE



## Contents

## Pin Configurations

**Figure 1. 44-pin TSOP II pinout without ERR [6]**

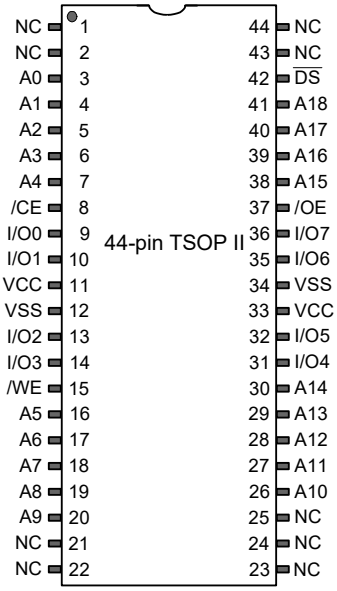
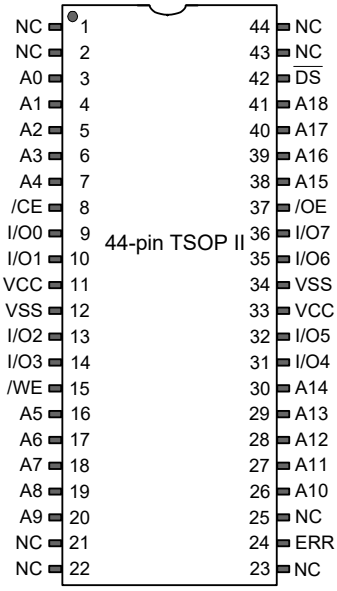



**Figure 2. 44-pin TSOP II pinout with ERR [6, 7]**




**Notes**
6. NC pins are not connected internally to the die.
7. ERR is an output pin.

## Pin Configurations (continued)

**Figure 3. 36-pin SOJ pinout without ERR [8]**

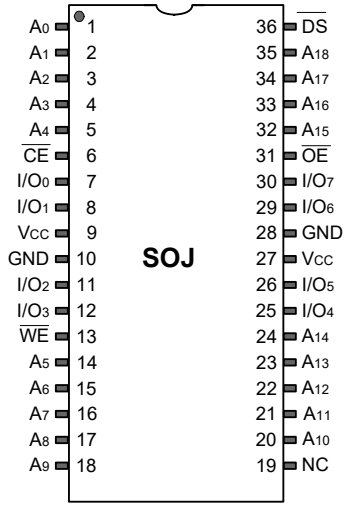
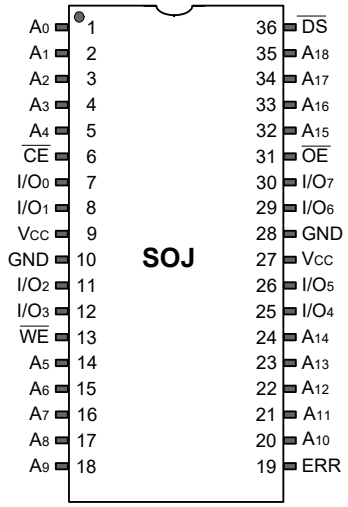



**Figure 4. 36-pin SOJ pinout with ERR [8, 9]**




**Notes**
8. NC pins are not connected internally to the die.
9. ERR is an output pin.

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage on $V_{CC}$ relative to GND [10] ..... –0.5 V to $V_{CC}$ + 0.5 V

DC voltage applied to outputs in HI-Z State [10] ..... –0.5 V to $V_{CC}$ + 0.5 V

DC input voltage [10] ..... –0.5 V to $V_{CC}$ + 0.5 V

Current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... > 2001 V

Latch-up current ..... > 140 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Industrial | –40 °C to +85 °C | 1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V |

## DC Electrical Characteristics

Over the Operating Range of –40 °C to +85 °C

| Parameter | Description | | Test Conditions | 10 ns/ 15 ns | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ [11] | Max | |
| $V_{OH}$ | Output HIGH voltage | 1.65 V to 2.2 V | $V_{CC}$ = Min, $I_{OH}$ = –0.1 mA | 1.4 | – | – | V |
| | | 2.2 V to 2.7 V | $V_{CC}$ = Min, $I_{OH}$ = –1.0 mA | 2 | – | – | |
| | | 2.7 V to 3.6 V | $V_{CC}$ = Min, $I_{OH}$ = –4.0 mA | 2.4 | – | – | |
| | | 4.5 V to 5.5 V | $V_{CC}$ = Min, $I_{OH}$ = –4.0 mA | 2.4 | – | – | |
| | | 4.5 V to 5.5 V | $V_{CC}$ = Min, $I_{OH}$ = –0.1 mA | $V_{CC}$ – 0.5 [12] | – | – | |
| $V_{OL}$ | Output LOW voltage | 1.65 V to 2.2 V | $V_{CC}$ = Min, $I_{OL}$ = 0.1 mA | – | – | 0.2 | V |
| | | 2.2 V to 2.7 V | $V_{CC}$ = Min, $I_{OL}$ = 2 mA | – | – | 0.4 | |
| | | 2.7 V to 3.6 V | $V_{CC}$ = Min, $I_{OL}$ = 8 mA | – | – | 0.4 | |
| | | 4.5 V to 5.5 V | $V_{CC}$ = Min, $I_{OL}$ = 8 mA | – | – | 0.4 | |
| $V_{IH}$ [10, 13] | Input HIGH voltage | 1.65 V to 2.2 V | – | 1.4 | – | $V_{CC}$ + 0.2 | V |
| | | 2.2 V to 2.7 V | – | 2 | – | $V_{CC}$ + 0.3 | |
| | | 2.7 V to 3.6 V | – | 2 | – | $V_{CC}$ + 0.3 | |
| | | 4.5 V to 5.5 V | – | 2 | – | $V_{CC}$ + 0.5 | |
| $V_{IL}$ [10, 13] | Input LOW voltage | 1.65 V to 2.2 V | – | –0.2 | – | 0.4 | V |
| | | 2.2 V to 2.7 V | – | –0.3 | – | 0.6 | |
| | | 2.7 V to 3.6 V | – | –0.3 | – | 0.8 | |
| | | 4.5 V to 5.5 V | – | –0.5 | – | 0.8 | |
| $I_{IX}$ | Input leakage current | | GND ≤ $V_{IN}$ ≤ $V_{CC}$ | –1 | – | +1 | µA |
| $I_{OZ}$ | Output leakage current | | GND ≤ $V_{OUT}$ ≤ $V_{CC}$, Output disabled | –1 | – | +1 | µA |
| $I_{CC}$ | $V_{CC}$ operating supply current | | $V_{CC}$ = Max, $I_{OUT}$ = 0 mA, CMOS levels, f = 100 MHz | – | 38 | 45 | mA |
| | | | $V_{CC}$ = Max, $I_{OUT}$ = 0 mA, CMOS levels, f = 66.7 MHz | – | – | 40 | |
| $I_{SB1}$ | Standby current – TTL inputs | | Max $V_{CC}$, $\overline{CE}$ ≥ $V_{IH}$, $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$ | – | – | 15 | mA |

**Notes**

10. $V_{IL}$ (min) = –2.0 V and $V_{IH}$ (max) = $V_{CC}$ + 2 V for pulse durations of less than 20 ns.
11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = 1.8 V (for $V_{CC}$ range of 1.65 V–2.2 V), $V_{CC}$ = 3 V (for $V_{CC}$ range of 2.2 V–3.6 V), and $V_{CC}$ = 5 V (for $V_{CC}$ range of 4.5 V–5.5 V), $T_A$ = 25 °C.
12. Guaranteed by design and not tested.
13. For the $\overline{DS}$ pin, $V_{IH}$ (min) is $V_{CC}$ – 0.2 V and $V_{IL}$ (max) is 0.2 V.

## DC Electrical Characteristics (continued)

Over the Operating Range of –40 °C to +85 °C

| Parameter | Description | Test Conditions | 10 ns/ 15 ns | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ [11] | Max | |
| $I_{SB2}$ | Standby current – CMOS inputs | Max $V_{CC}$, $\overline{CE} \geq V_{CC} - 0.2$ V, $\overline{DS} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0 | – | 6 | 8 | mA |
| $I_{DS}$ | Deep-Sleep current | Max $V_{CC}$, $\overline{CE} \geq V_{CC} - 0.2$ V, $\overline{DS} \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0 | – | – | 15 | µA |

## Capacitance

| Parameter [14] | Description | Test Conditions | All packages | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A = 25$ °C, f = 1 MHz, $V_{CC(typ)}$ | 10 | pF |
| $C_{OUT}$ | I/O capacitance | | 10 | pF |

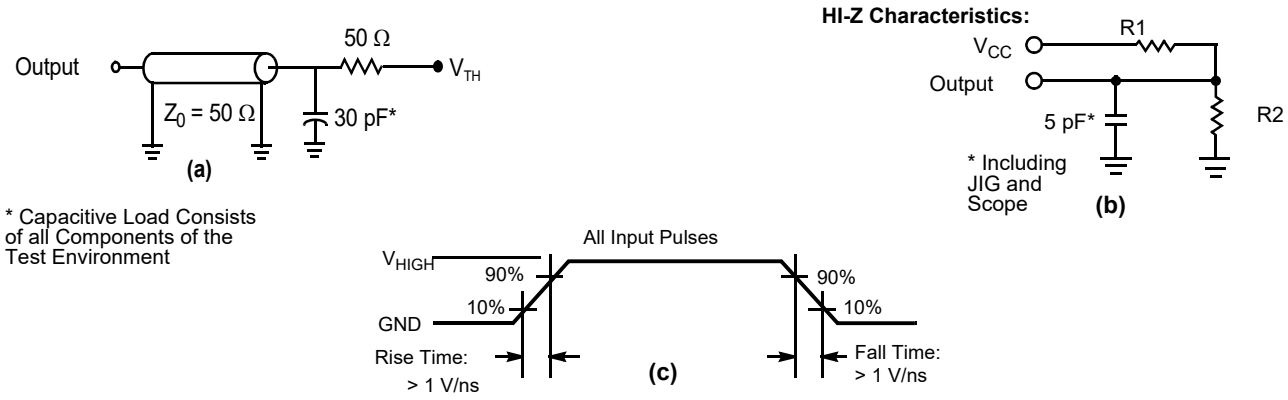
## Thermal Resistance

| Parameter [14] | Description | Test Conditions | 36-pin SOJ Package | 44-pin TSOP II Package | Unit |
|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 59.52 | 68.85 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 31.48 | 15.97 | °C/W |

**Note**
14. Tested initially and after any design or process changes that may affect these parameters.

## AC Test Loads and Waveforms

**Figure 5. AC Test Loads and Waveforms** [15]




| Parameters | 1.8 V | 3.0 V | 5.0 V | Unit |
|---|---|---|---|---|
| R1 | 1667 | 317 | 317 | Ω |
| R2 | 1538 | 351 | 351 | Ω |
| $V_{TH}$ | $V_{CC}$/2 | 1.5 | 1.5 | V |
| $V_{HIGH}$ | 1.8 | 3.0 | 3.0 | V |

**Note**
15. Full-device AC operation assumes a 100-µs ramp time from 0 to $V_{CC(min)}$ or 100-µs wait time after $V_{CC}$ stabilization.

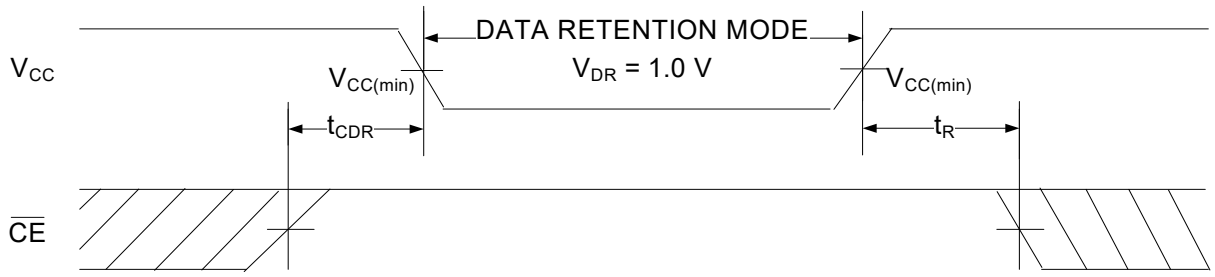
## Data Retention Characteristics

Over the Operating Range of –40 °C to +85 °C

| Parameter | Description | Conditions [16] | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for data retention | – | 1.0 | – | V |
| $I_{CCDR}$ | Data retention current | $V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2$ V, $\overline{DS} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V | – | 8 | mA |
| $t_{CDR}$ [17] | Chip deselect to data retention time | – | 0 | – | ns |
| $t_R$ [17, 18] | Operation recovery time | 2.2 V < $V_{CC} \leq$ 5.5 V | 10 | – | ns |
| | | $V_{CC} \leq$ 2.2 V | 15 | – | ns |

## Data Retention Waveform

**Figure 6. Data Retention Waveform [18]**



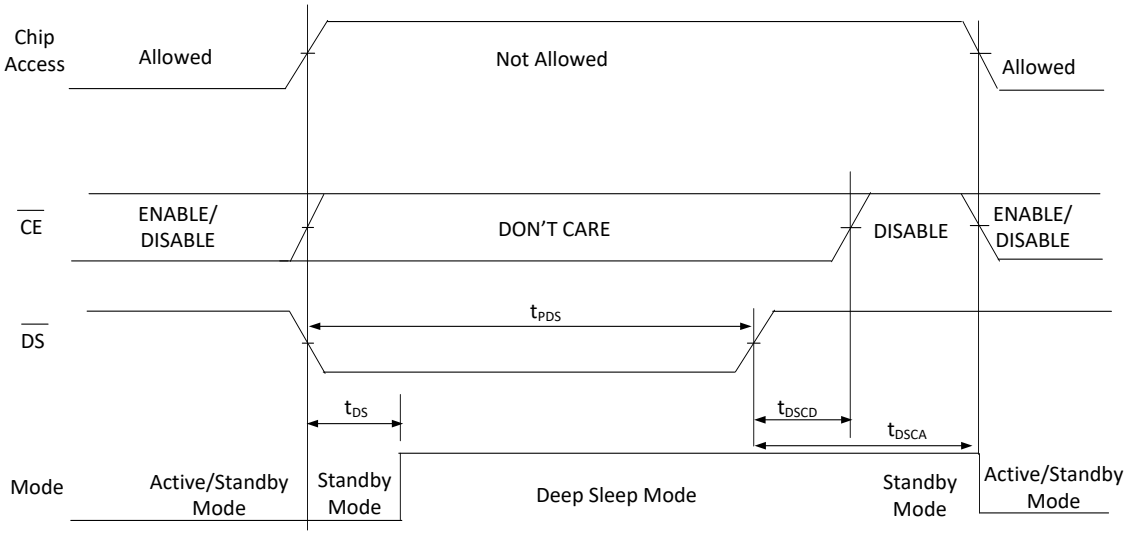

**Notes**
16. $\overline{DS}$ signal must be HIGH during Data Retention Mode.
17. These parameters are guaranteed by design.
18. Full-device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.

## Deep-Sleep Mode Characteristics

Over the Operating Range of –40 °C to +85 °C

| Parameter | Description | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $I_{DS}$ | Deep-Sleep mode current | $V_{CC} = V_{CC}$ (max), $\overline{DS} \le 0.2$ V, $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V | – | 15 | µA |
| $t_{PDS}$[19] | Minimum time for $\overline{DS}$ to be LOW for part to successfully exit Deep-Sleep mode | – | 100 | – | ns |
| $t_{DS}$[20] | $\overline{DS}$ assertion to Deep-Sleep mode transition time | – | – | 1 | ms |
| $t_{DSCD}$[19] | $\overline{DS}$ deassertion to chip disable | If $t_{PDS} \ge t_{PDS(min)}$ | – | 100 | µs |
| | | If $t_{PDS} < t_{PDS(min)}$ | – | 0 | µs |
| $t_{DSCA}$ | $\overline{DS}$ deassertion to chip access (Active/Standby) | If $t_{PDS} \ge t_{PDS(min)}$ | 300 | – | µs |
| | | If $t_{PDS} < t_{PDS(min)}$ | | | |

**Figure 7. Active, Standby, and Deep-Sleep Operation Modes**




**Notes**

19. $\overline{CE}$ must be pulled HIGH within $t_{DSCD}$ time of $\overline{DS}$ de-assertion to avoid SRAM data loss.
20. After assertion of $\overline{DS}$ signal, device will take a maximum of $t_{DS}$ time to stabilize to Deep-Sleep current $I_{DS}$. During this period, $\overline{DS}$ signal must continue to be asserted to logic level LOW to keep the device in Deep-Sleep mode.

## AC Switching Characteristics

Over the Operating Range of –40 °C to +85 °C

| Parameter [21] | Description | 10 ns | | 15 ns | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| **Read Cycle** | | | | | | |
| $t_{RC}$ | Read cycle time | 10 | – | 15 | – | ns |
| $t_{AA}$ | Address to data valid | – | 10 | – | 15 | ns |
| $t_{OHA}$ | Data hold from address change | 3 | – | 3 | – | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to data valid | – | 10 | – | 15 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to data valid | – | 4.5 | – | 8 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to low impedance [22, 23, 24] | 0 | – | 0 | – | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to HI-Z [22, 23, 24] | – | 5 | – | 8 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to low impedance [22, 23, 24] | 3 | – | 3 | – | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to HI-Z [22, 23, 24] | – | 5 | – | 8 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to power-up [24] | 0 | – | 0 | – | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to power-down [24] | – | 10 | – | 15 | ns |
| **Write Cycle** [25, 26] | | | | | | |
| $t_{WC}$ | Write cycle time | 10 | – | 15 | – | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to write end | 7 | – | 12 | – | ns |
| $t_{AW}$ | Address setup to write end | 7 | – | 12 | – | ns |
| $t_{HA}$ | Address hold from write end | 0 | – | 0 | – | ns |
| $t_{SA}$ | Address setup to write start | 0 | – | 0 | – | ns |
| $t_{PWE}$ | $\overline{WE}$ pulse width | 7 | – | 12 | – | ns |
| $t_{SD}$ | Data setup to write end | 5 | – | 8 | – | ns |
| $t_{HD}$ | Data hold from write end | 0 | – | 0 | – | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to low impedance [22, 23, 24] | 3 | – | 3 | – | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to HI-Z [22, 23, 24] | – | 5 | – | 8 | ns |

**Notes**

21. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to $V_{CC}$ (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in part (a) of Figure 5 on page 8, unless specified otherwise.
22. $t_{HZOE}$, $t_{HZCE}$, $t_{HZWE}$, $t_{LZOE}$, $t_{LZCE}$, and $t_{LZWE}$ are specified with a load capacitance of 5 pF as in (b) of Figure 5 on page 8. Transition is measured ±200 mV from steady state voltage.
23. At any temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any device.
24. These parameters are guaranteed by design.
25. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = $V_{IL}$, $\overline{CE}$ = $V_{IL}$ ,$\overline{DS}$ = $V_{IH}$ and $\overline{WE}$, $\overline{CE}$, signals must be LOW and $\overline{DS}$ must be HIGH to initiate a write, and a HIGH transition of any of $\overline{WE}$, $\overline{CE}$, signals or LOW transition on $\overline{DS}$ signal can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
26. The minimum write pulse width for Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be the sum of $t_{HZWE}$ and $t_{SD}$.

## Switching Waveforms

**Figure 8. Read Cycle No. 1 of CY7S1049G (Address Transition Controlled)** [27, 28, 29]

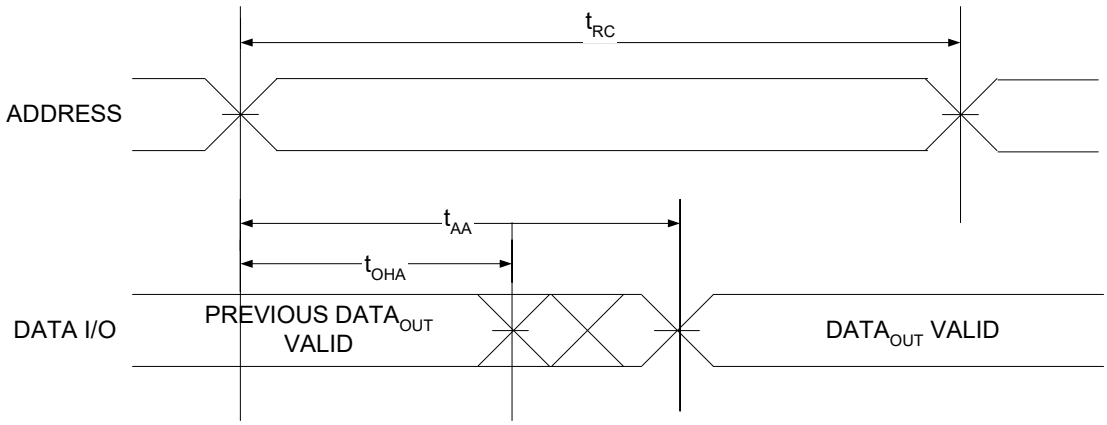
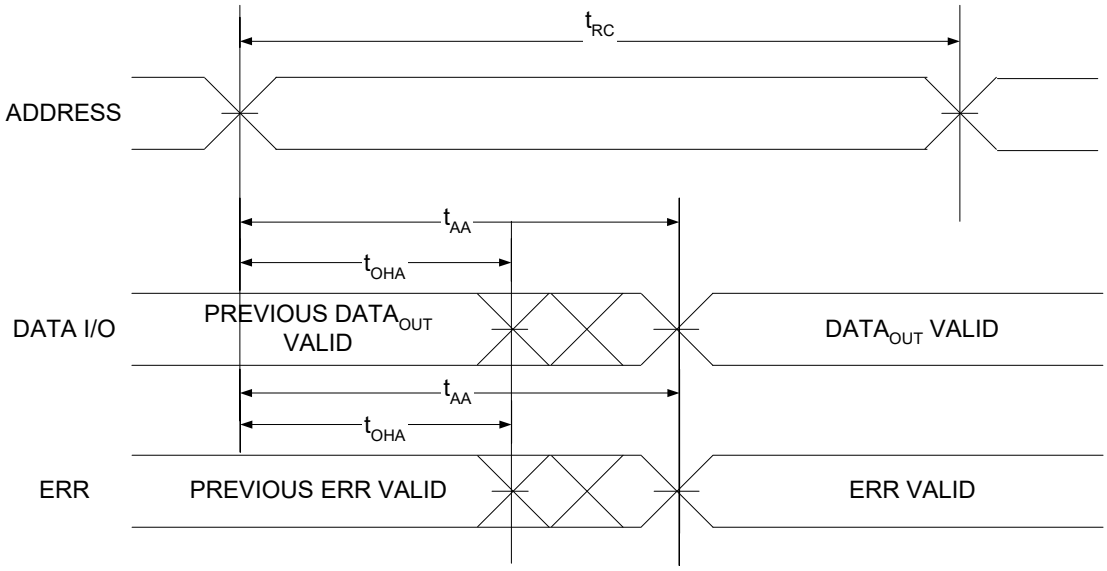


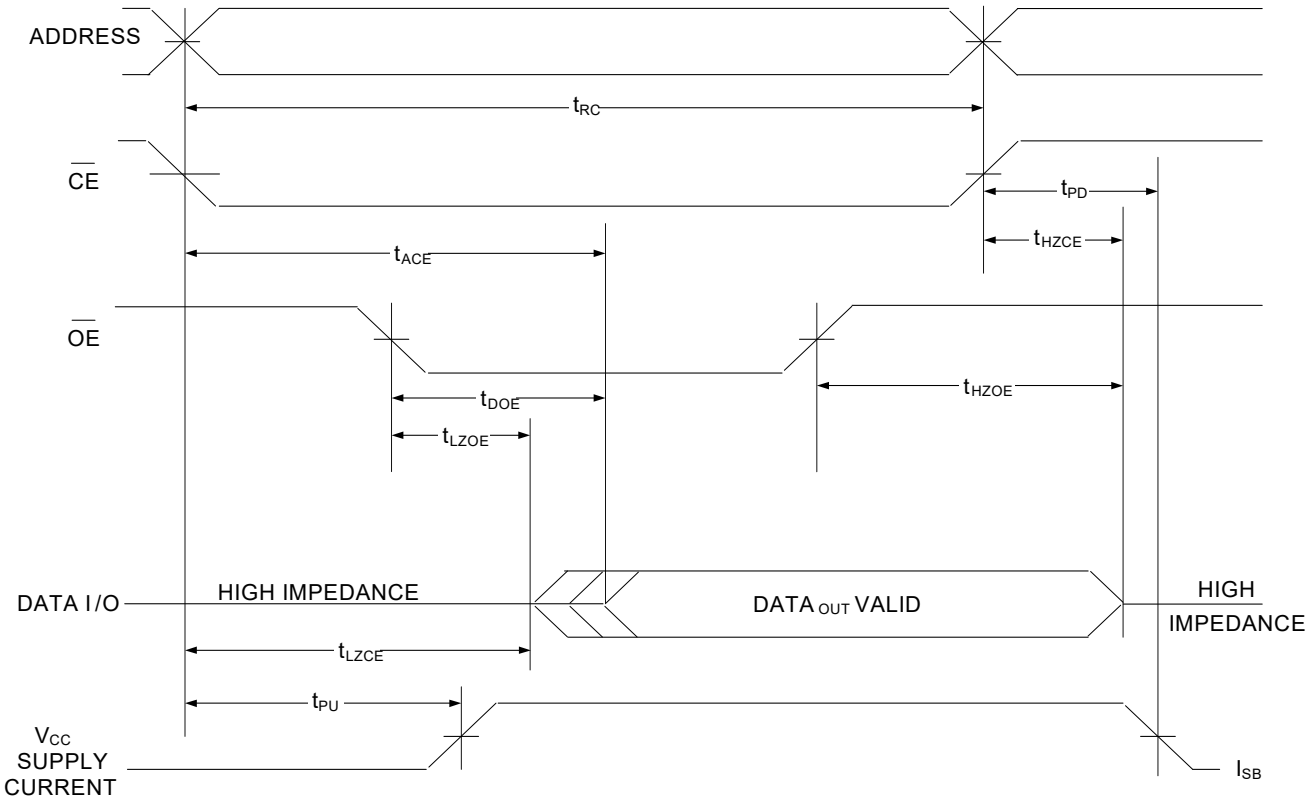

**Figure 9. Read Cycle No. 2 of CY7S1041GE (Address Transition Controlled)** [27, 28, 29]




**Notes**
27. The device is continuously selected. $\overline{OE}$ = $V_{IL}$, $\overline{CE}$ = $V_{IL}$.
28. $\overline{WE}$ is HIGH for read cycle.
29. $\overline{DS}$ is HIGH for chip access.

## Switching Waveforms (continued)

**Figure 10. Read Cycle No. 3 ($\overline{OE}$ Controlled) [30, 31, 32]**




**Notes**
30. $\overline{WE}$ is HIGH for read cycle.
31. Address valid prior to or coincident with $\overline{CE}$ LOW transition.
32. $\overline{DS}$ must be HIGH for chip access.

## Switching Waveforms (continued)

**Figure 11. Write Cycle No. 1 ($\overline{CE}$ Controlled)** [33, 34, 35]

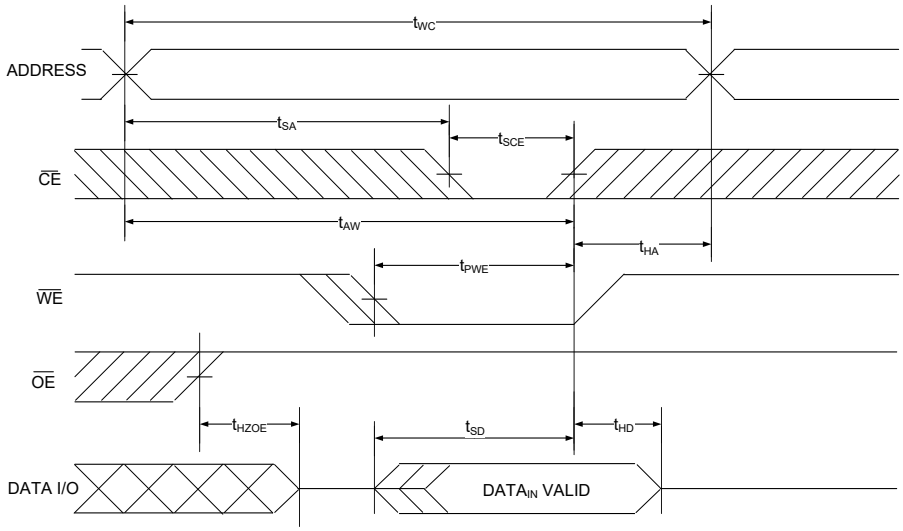
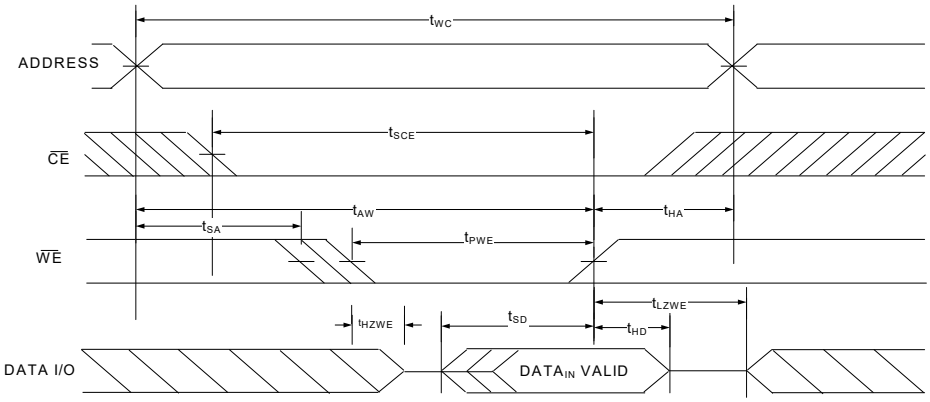



**Figure 12. Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)** [33, 34, 35, 36]

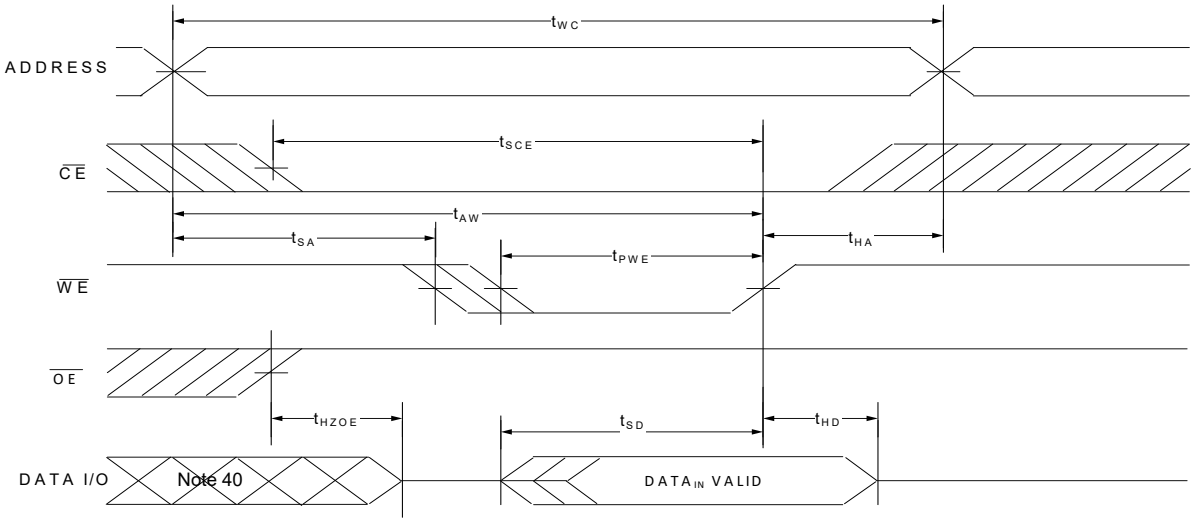



**Notes**

33. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = $V_{IL}$, $\overline{CE}$ = $V_{IL}$, $\overline{DS}$ = $V_{IH}$ and $\overline{WE}$, $\overline{CE}$ signals must be LOW and $\overline{DS}$ must be HIGH to initiate a write, and a HIGH transition of any of $\overline{WE}$, $\overline{CE}$ signals or LOW transition on $\overline{DS}$ signal can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
34. Data I/O is in HI-Z state if $\overline{CE}$ = $V_{IH}$, or $\overline{OE}$ = $V_{IH}$.
35. $\overline{DS}$ must be HIGH for chip access.
36. The minimum write pulse width for Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of $t_{HZWE}$ and $t_{SD}$.

## Switching Waveforms (continued)

**Figure 13. Write Cycle No. 3 ($\overline{WE}$ Controlled) [37, 38, 39]**




**Notes**

37. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = $V_{IL}$, $\overline{CE}$ = $V_{IL}$, $\overline{DS}$ = $V_{IH}$ and $\overline{WE}$, $\overline{CE}$, signals must be LOW and $\overline{DS}$ must be HIGH to initiate a write, and a HIGH transition of any of $\overline{WE}$, $\overline{CE}$, signals or LOW transition on $\overline{DS}$ signal can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
38. Data I/O is in HI-Z state if $\overline{CE}$ = $V_{IH}$, or $\overline{OE}$ = $V_{IH}$ or $\overline{DS}$ = $V_{IL}$.
39. $\overline{DS}$ must be HIGH for chip access.
40. During this period, the I/Os are in output state. Do not apply input signals.

## Truth Table

| $\overline{DS}$ | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $I/O_0$–$I/O_7$ | Mode | Power |
|---|---|---|---|---|---|---|
| H | H | X[41] | X[41] | HIGH-Z | Standby | Standby ($I_{SB}$) |
| H | L | L | H | Data out | Read all bits | Active ($I_{CC}$) |
| H | L | X | L | Data in | Write all bits | Active ($I_{CC}$) |
| H | L | H | H | HI-Z | Selected, outputs disabled | Active ($I_{CC}$) |
| L[42] | X | X | X | HI-Z | Deep-Sleep | Deep-Sleep Ultra Low Power ($I_{DS}$) |

## ERR Output – CY7S1049GE

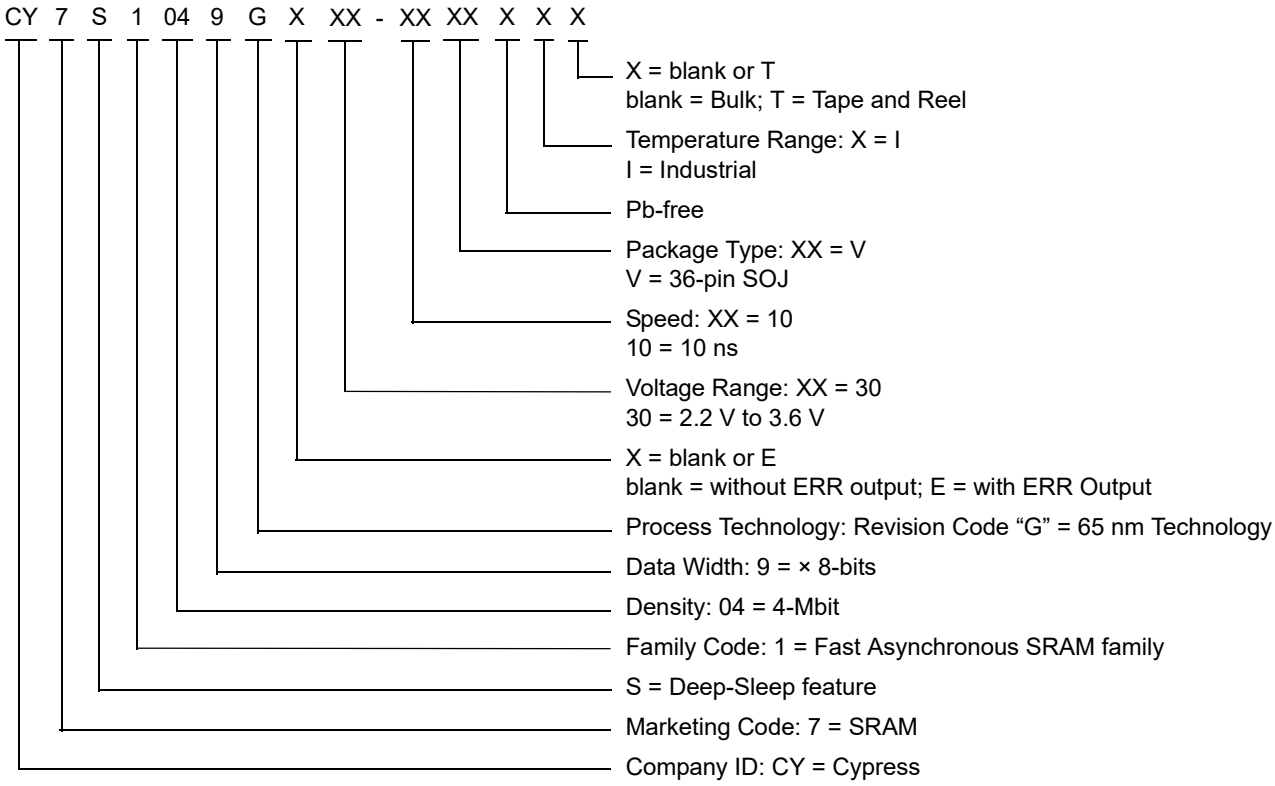
| Output [43] | Mode |
|---|---|
| 0 | Read operation, no single-bit error in the stored data. |
| 1 | Read operation, single-bit error detected and corrected. |
| High-Z | Device deselected / outputs disabled / Write operation |

**Notes**
41. The input voltage levels on these pins should be either at $V_{IH}$ or $V_{IL}$.
42. $V_{IL}$ on $\overline{DS}$ must be $\leq$ 0.2 V.
43. ERR is an Output pin.If not used, this pin should be left floating.

## Ordering Information

| Speed (ns) | Voltage Range | Ordering Code | Package Diagram | Package Type (All Pb-free) | Operating Range |
|---|---|---|---|---|---|
| 10 | 2.2 V–3.6 V | CY7S1049G30-10VXI | 51-85090 | 36-pin SOJ | Industrial |
| | | CY7S1049G30-10VXIT | 51-85090 | 36-pin SOJ, Tape and Reel | |
| | | CY7S1049GE30-10VXI | 51-85090 | 36-pin SOJ, ERR Output | |
| | | CY7S1049GE30-10VXIT | 51-85090 | 36-pin SOJ, ERR Output, Tape and Reel | |

### Ordering Code Definitions



## Package Diagrams

**Figure 14. 36-pin SOJ V36.4 (Molded) Package Outline, 51-85090**

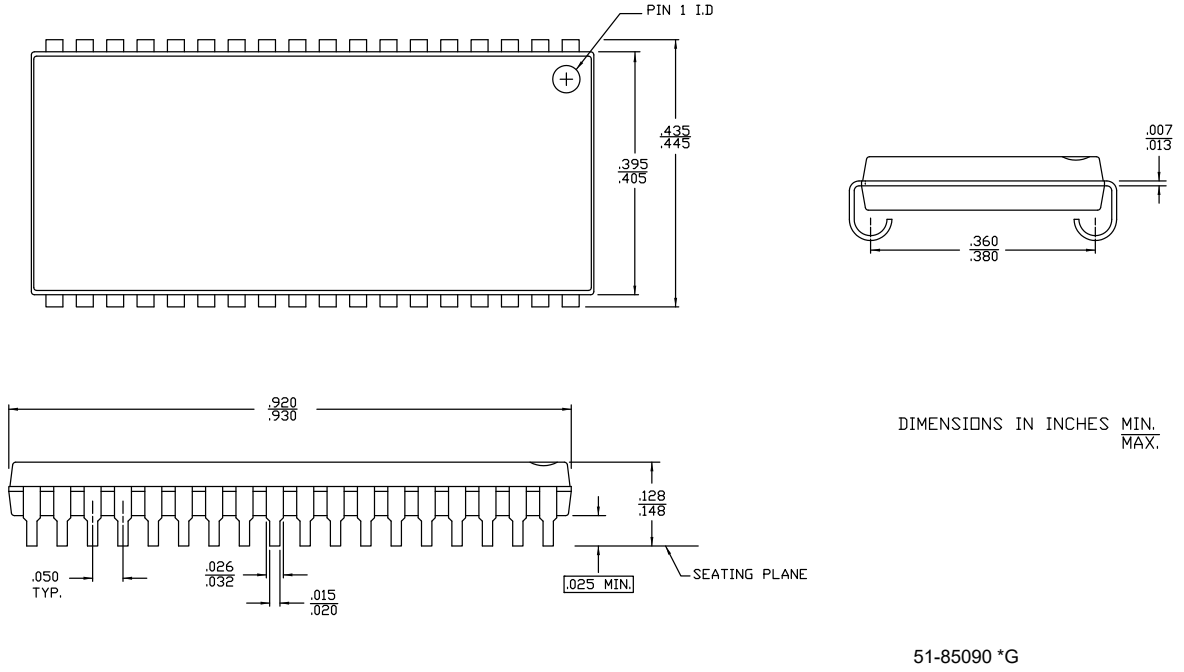
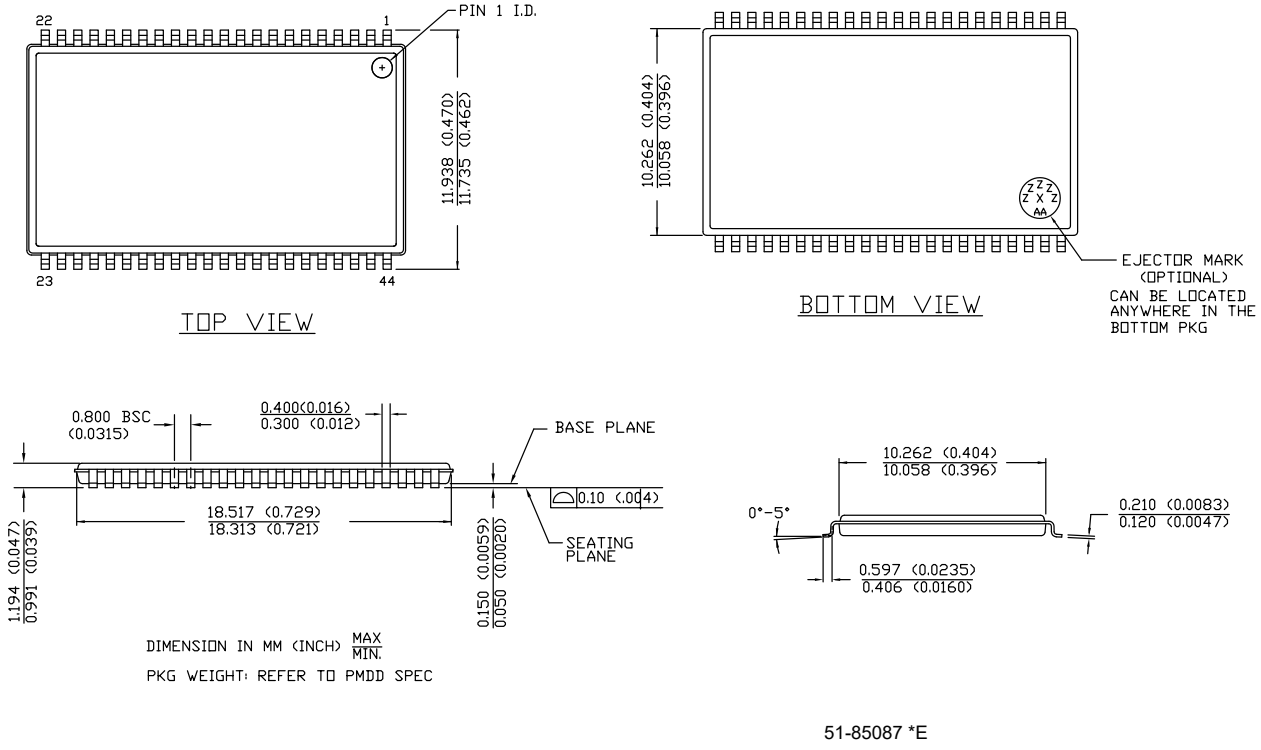



**Figure 15. 44-pin TSOP II Package Outline, 51-85087**



## Acronyms

| Acronym | Description |
|---|---|
| $\overline{CE}$ | Chip Enable |
| CMOS | Complementary Metal Oxide Semiconductor |
| I/O | Input/Output |
| $\overline{OE}$ | Output Enable |
| SOJ | Small-Outline J-lead |
| SRAM | Static Random Access Memory |
| TSOP | Thin Small Outline Package |
| TTL | Transistor-Transistor Logic |
| $\overline{WE}$ | Write Enable |
| ECC | Write Enable |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degrees Celsius |
| MHz | megahertz |
| µA | microampere |
| µs | microsecond |
| mA | milliampere |
| mm | millimeter |
| ns | nanosecond |
| Ω | ohm |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY7S1049G/CY7S1049GE, 4-Mbit (512K words × 8-bit) Static RAM with PowerSnooze™ and Error Correcting Code (ECC)<br>Document Number: 001-95414 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *B | 5025315 | VINI | 11/24/2015 | Changed status from Preliminary to Final. |
| *C | 5090263 | NILE | 01/18/2016 | Updated Ordering Information:<br>Updated part numbers.<br>Completing Sunset Review. |
| *D | 5428860 | NILE | 09/07/2016 | Updated Functional Description:<br>Added Note 1 and referred the same note in “CY7S1049G/CY7S1049GE”.<br>Updated Maximum Ratings:<br>Updated Note 10 (Replaced “2 ns” with “20 ns”).<br>Updated DC Electrical Characteristics:<br>Changed minimum value of $V_{OH}$ parameter from 2.2 V to 2.4 V corresponding to Operating Range “2.7 V to 3.6 V” and Test Condition “$V_{CC}$ = Min, $I_{OH}$ = –4.0 mA”.<br>Changed minimum value of $V_{IH}$ parameter from 2.2 V to 2 V corresponding to Operating Range “4.5 V to 5.5 V”.<br>Updated Ordering Information:<br>Updated part numbers.<br>Updated to new template. |
| *E | 5981584 | AESATMP8 | 12/01/2017 | Updated logo and Copyright. |
| *F | 6120487 | NILE | 04/03/2018 | Updated Features:<br>Referred Note 1 in “Embedded ECC for single-bit error correction”.<br>Added Note 2 and referred the same note in “Embedded ECC for single-bit error correction”.<br>Updated Functional Description:<br>Added Note 3 and referred the same note at the end of sentence “This device features fast access times (10 ns) and a unique ultra-low power Deep-Sleep mode”.<br>Updated to new template.<br>Completing Sunset Review. |

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