CY62146G MoBL® Automotive

4-Mbit (256K words × 16 bit) Static RAM with Error-Correcting Code (ECC)

Features

- AEC-Q100 qualified
- High speed: 45 ns
- Temperature Range
  - Automotive-A: -40 °C to +85 °C
- Ultra-low standby power
  - Typical standby current: 3.5 µA
- Embedded ECC for single-bit error correction[1]
- Voltage range: 2.2 V to 3.6 V, 4.5 V to 5.5 V
- 1.0-V data retention
- TTL-compatible inputs and outputs
- Pb-free 44-pin TSOP II package

Functional Description

CY62146G is high-performance CMOS low-power (MoBL) SRAM devices with embedded ECC.

Device is accessed by asserting the chip enable ($\overline{CE}$) input LOW.

Data writes are performed by asserting the Write Enable ($\overline{WE}$) input LOW, while providing the data on I/O_0 through I/O_{15} and address on A_0 through A_{17} pins. The Byte High Enable ($\overline{BHE}$) and Byte Low Enable ($\overline{BLE}$) inputs control write operations to the upper and lower bytes of the specified memory location. $\overline{BHE}$ controls I/O_8 through I/O_{15} and $\overline{BLE}$ controls I/O_0 through I/O_7.

Data reads are performed by asserting the Output Enable ($\overline{OE}$) input and providing the required address on the address lines. Read data is accessible on the I/O lines (I/O_0 through I/O_{15}). Byte accesses can be performed by asserting the required byte enable signal ($\overline{BHE}$ or $\overline{BLE}$) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O_0 through I/O_{15}) are placed in a HI-Z state when the device is deselected ($\overline{CE}$ HIGH), or control signals are de-asserted ($\overline{OE}$, $\overline{BLE}$, $\overline{BHE}$).

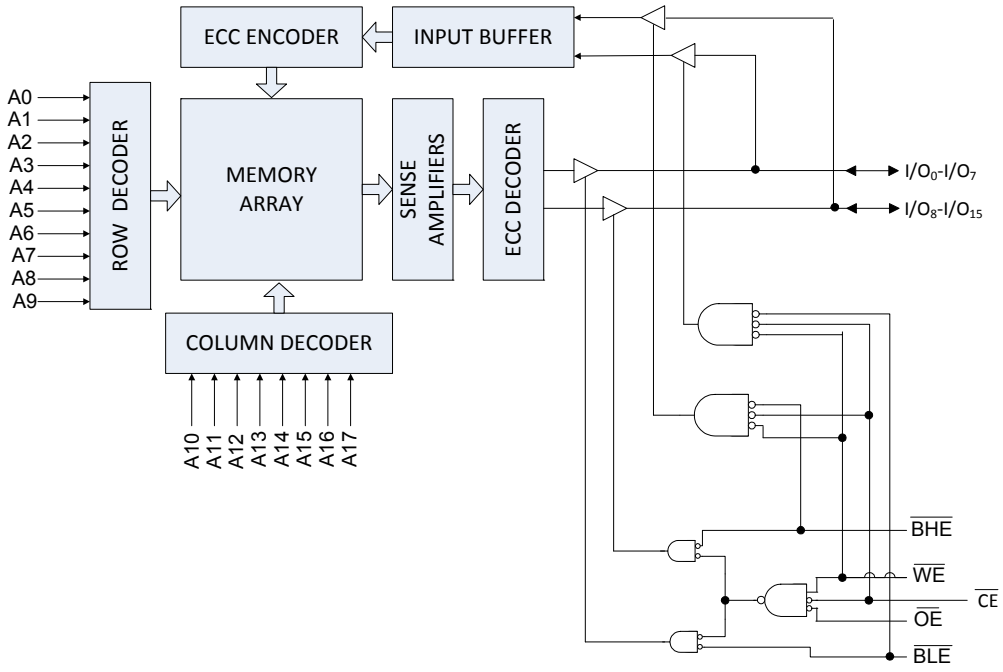
The logic block diagram is on page 2.

Product Portfolio

Product	Features and Options (see Pin Configuration – CY62146G on page 4)	Range	V_{CC} Range (V)	Speed (ns)	Power Dissipation			
					Operating I_{CC} (mA) f = f_{max}		Standby, I_{SB2} (µA)	
					Typ[2]	Max	Typ[2]	Max
CY62146G30	Single Chip Enable	Automotive-A	2.2 V–3.6 V	45	15	20	3.5	8.7
CY62146G			4.5 V–5.5 V					

Notes
1. This device does not support automatic write-back on error detection.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V) and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.

Logic Block Diagram – CY62146G



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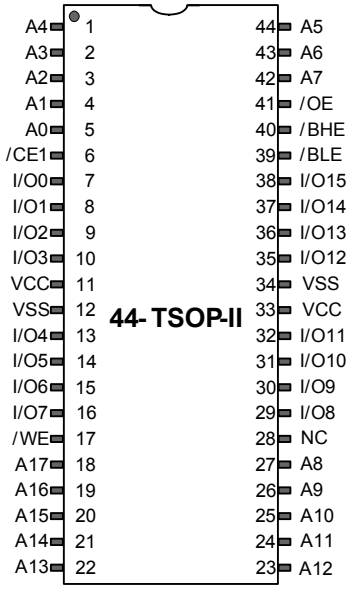
Pin Configuration – CY62146G

Figure 1. 44-pin TSOP II pinout – CY62146G [3]



Note
3. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to + 150 °C

Ambient temperature with power applied ..... –55 °C to + 125 °C

Supply voltage to ground potential[4] ..... –0.3 V to V_{CC} + 0.3 V

DC voltage applied to outputs in HI-Z state[4] ..... –0.3 V to V_{CC} + 0.3 V

DC input voltage[4] ..... –0.3 V to V_{CC} + 0.3 V

Output current into outputs (in low state) ..... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) ..... >2001 V

Latch-up current ..... >140 mA

Operating Range

Grade	Ambient Temperature	V_{CC}
Automotive-A	–40 °C to +85 °C	2.2 V to 3.6 V
		4.5 V to 5.5 V

DC Electrical Characteristics

Over the operating range

Parameter	Description		Test Conditions		45 ns (Automotive-A)			Unit
					Min	Typ	Max	
V_{OH}	Output HIGH voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OH} = –0.1 mA		2	–	–	V
		2.7 V to 3.6 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –1.0 mA		2.4	–	–	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OH} = –0.1 mA		V_{CC} – 0.5[5]	–	–	
V_{OL}	Output LOW voltage	2.2 V to 2.7 V	V_{CC} = Min, I_{OL} = 0.1 mA		–	–	0.4	V
		2.7 V to 3.6 V	V_{CC} = Min, I_{OL} = 2.1 mA		–	–	0.4	
		4.5 V to 5.5 V	V_{CC} = Min, I_{OL} = 2.1 mA		–	–	0.4	
V_{IH}	Input HIGH voltage	2.2 V to 2.7 V	–		1.8	–	V_{CC} + 0.3[4]	V
		2.7 V to 3.6 V	–		2	–	V_{CC} + 0.3[4]	
		4.5 V to 5.5 V	–		2.2	–	V_{CC} + 0.5[4]	
V_{IL}	Input LOW voltage	2.2 V to 2.7 V	–		–0.3[4]	–	0.6	V
		2.7 V to 3.6 V	–		–0.3[4]	–	0.8	
		4.5 V to 5.5 V	–		–0.5[4]	–	0.8	
I_{IX}	Input leakage current		GND ≤ V_{IN} ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current		GND ≤ V_{OUT} ≤ V_{CC}, Output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current		Max V_{CC}, I_{OUT} = 0 mA, CMOS levels	f = f_{MAX}	–	15	20	mA
				f = 1 MHz	–	3.5	6	

Note
4. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = V_{CC} + 2 V for pulse durations of less than 20 ns.
5. This parameter is guaranteed by design and not tested.

DC Electrical Characteristics (continued)

Over the operating range

Parameter	Description	Test Conditions	45 ns (Automotive-A)			Unit
			Min	Typ	Max	
I_{SB1}[6]	Automatic power down current – CMOS inputs; V_{CC} = 2.2 V to 3.6 V and 4.5 V to 5.5 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = f_{max} (address and data only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$, and $\overline{BLE}$), Max V_{CC}	–	3.5	8.7	µA
I_{SB2}[6]	Automatic power down current – CMOS inputs V_{CC} = 2.2 V to 3.6 V and 4.5 V to 5.5 V	$\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, Max V_{CC}	–	3.5	8.7	µA

Notes
6. Chip enable ($\overline{CE}$) must be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.

Capacitance

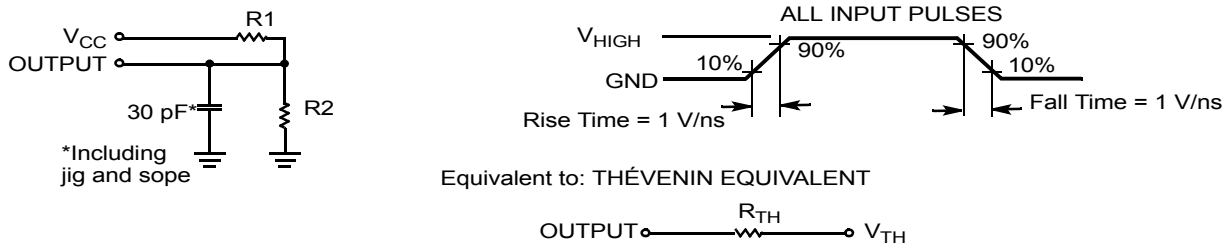
Parameter [7]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [7]	Description	Test Conditions	44-pin TSOP II	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	66.82	°C/W
Θ_{JC}	Thermal resistance (junction to case)		15.97	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms[8]



Parameters	2.5 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Notes
7. Tested initially and after any design or process changes that may affect these parameters.
8. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ ≥ 100 µs or stable at $V_{CC(min)}$ ≥ 100 µs.

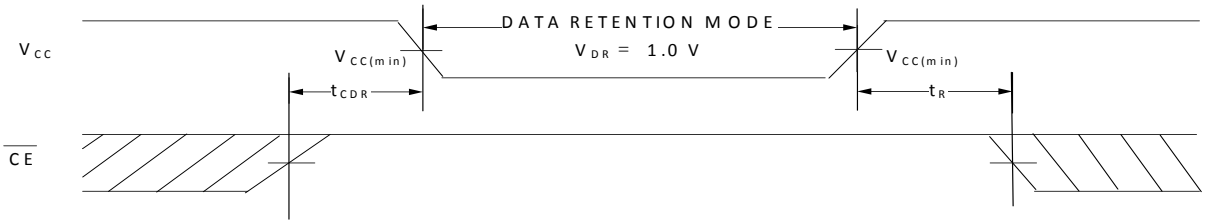
Data Retention Characteristics

Over the Operating range

Parameter	Description	Conditions (Automotive-A)	Min	Typ [9]	Max	Unit
V_{DR}	V_{CC} for data retention	–	1	–	–	V
I_{CCDR}[10, 11]	Data retention current	Vcc = 1.2 V $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	13	µA
t_{CDR}[12]	Chip deselect to data retention time	–	0	–	–	ns
t_R[12, 13]	Operation recovery time	–	45	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V) and V_{CC} = 5 V (for V_{CC} range of 4.5 V–5.5 V), T_A = 25 °C.
10. Chip enable ($\overline{CE}$) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. I_{CCDR} is guaranteed only after device is first powered up to $V_{CC(min)}$ and then brought down to V_{DR}.
12. These parameters are guaranteed by design.
13. Full-device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.

AC Switching Characteristics

Parameter [14]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to Low impedance[15, 16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to HI-Z[15, 16, 17]	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low impedance[15, 16]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to HI-Z[15, 16, 17]	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up[16]	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to power-down[16]	–	45	ns
t_{DBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to data valid	–	22	ns
t_{LZBE}	$\overline{BLE}$ / $\overline{BHE}$ LOW to Low impedance[15, 16]	5	–	ns
t_{HZBE}	$\overline{BLE}$ / $\overline{BHE}$ HIGH to HI-Z[15, 16, 17]	–	18	ns
Write Cycle [18, 19]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{BW}	$\overline{BLE}$ / $\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to HI-Z[15, 16, 17]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low impedance[15, 16]	10	–	ns

Notes

14. Test conditions assume a signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.
15. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
16. These parameters are guaranteed by design.
17. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high-impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
19. The minimum pulse width in Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1 of CY62146G (Address Transition Controlled) [20]

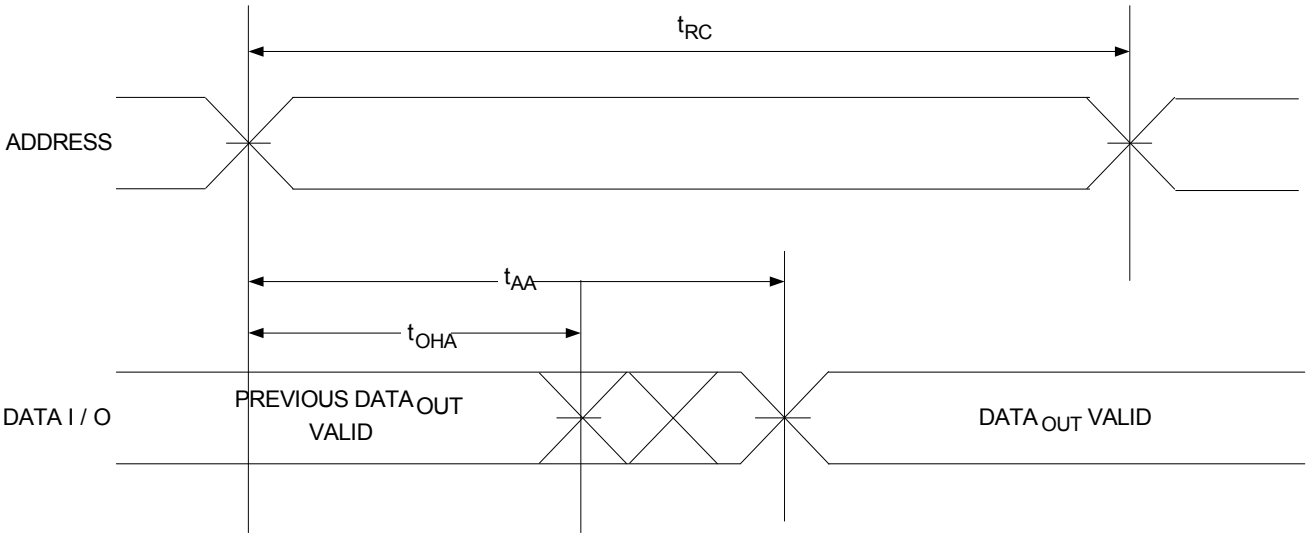
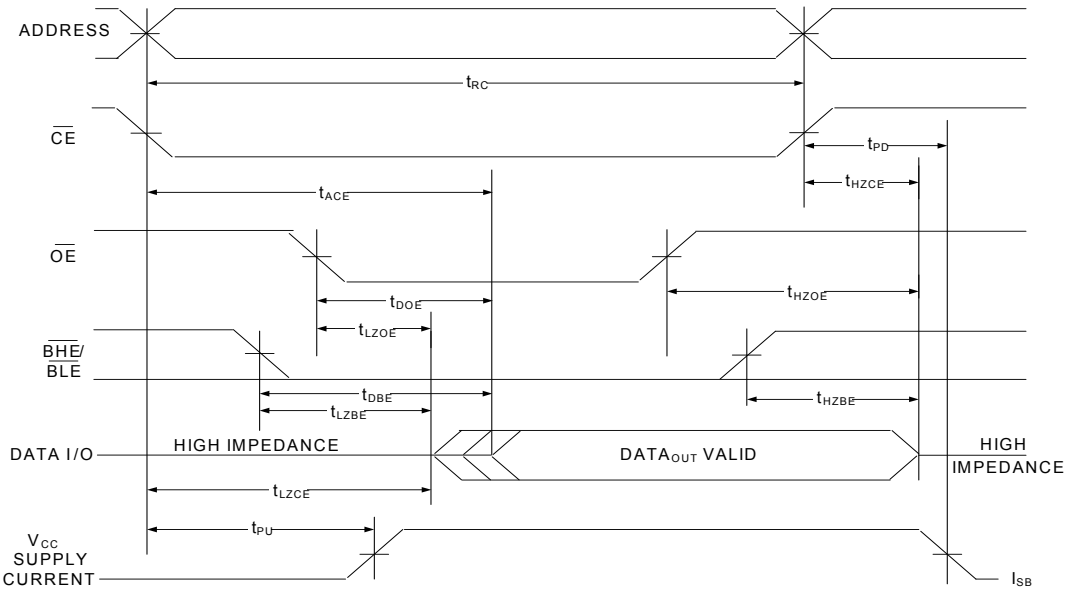


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [21, 22]

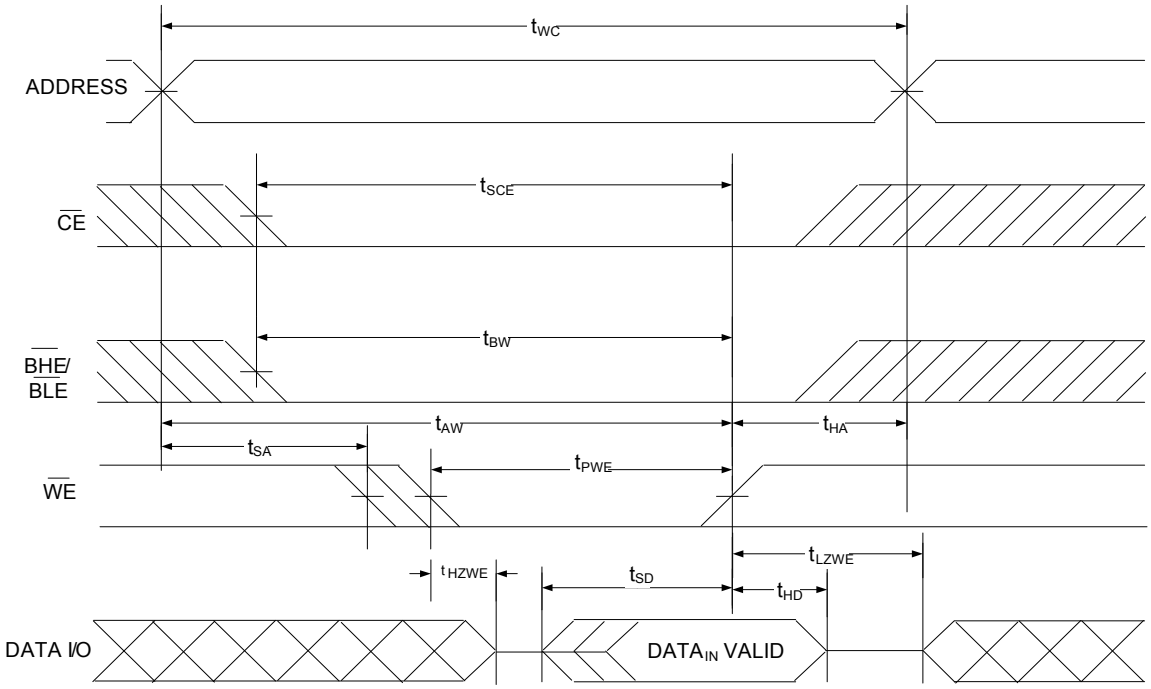


Notes

20. The device is continuously selected. $\overline{OE}$ = V_{IL}, $\overline{CE}$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}.
21. $\overline{WE}$ is HIGH for Read cycle.
22. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled) [23, 24]



Notes

23. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
24. Data I/O is in a HI-Z state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{CE}$ Controlled) [25, 26]

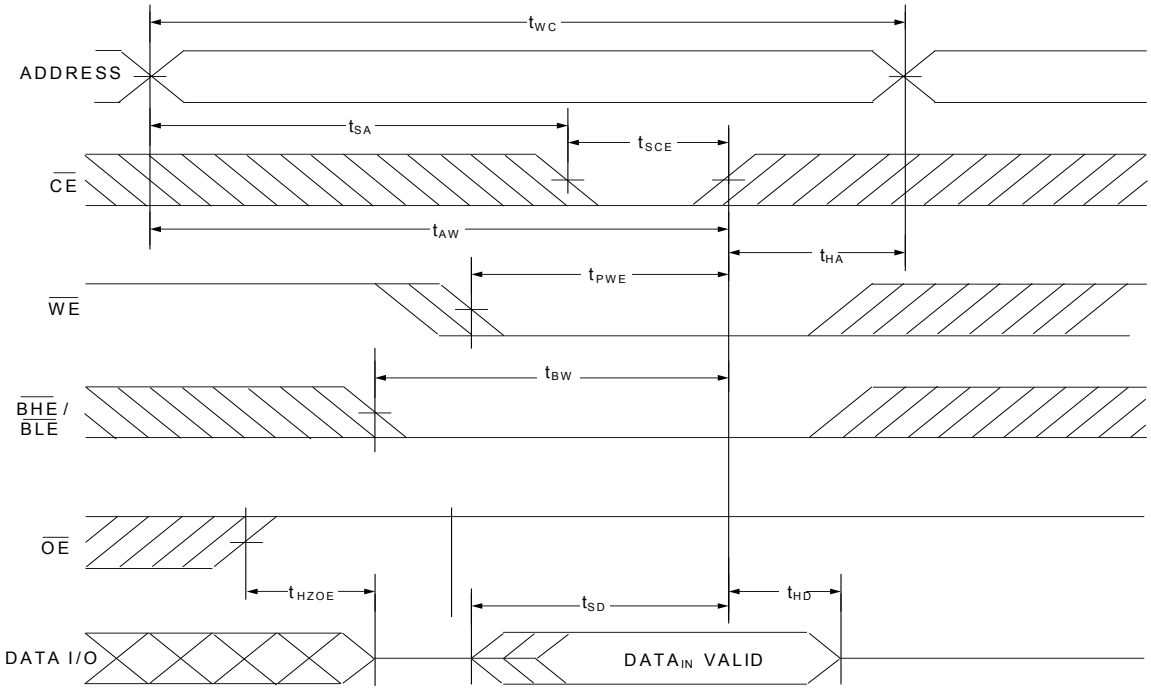
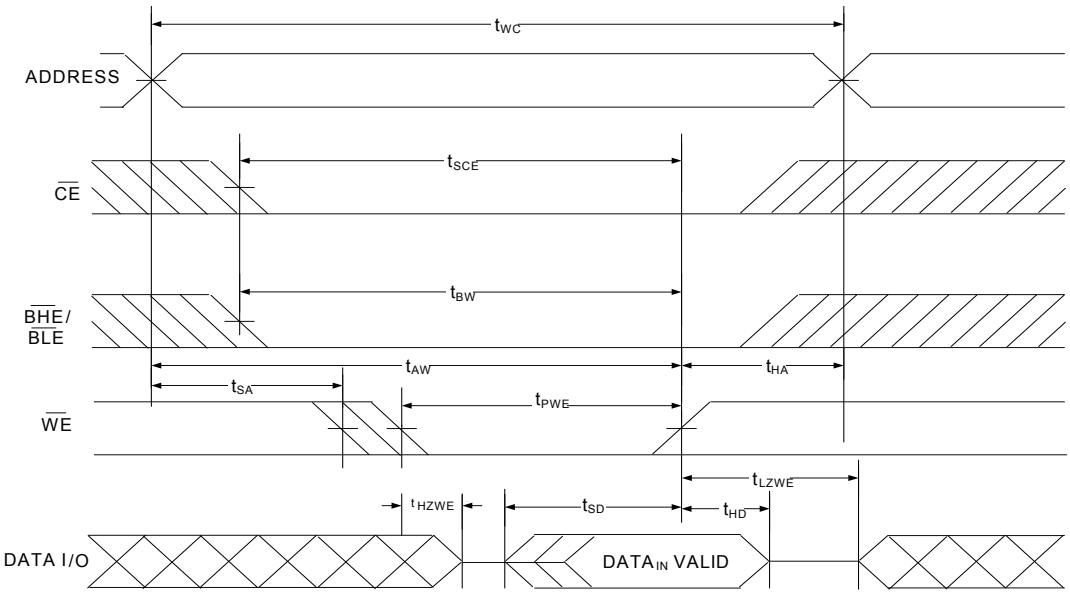


Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [25, 26, 27]

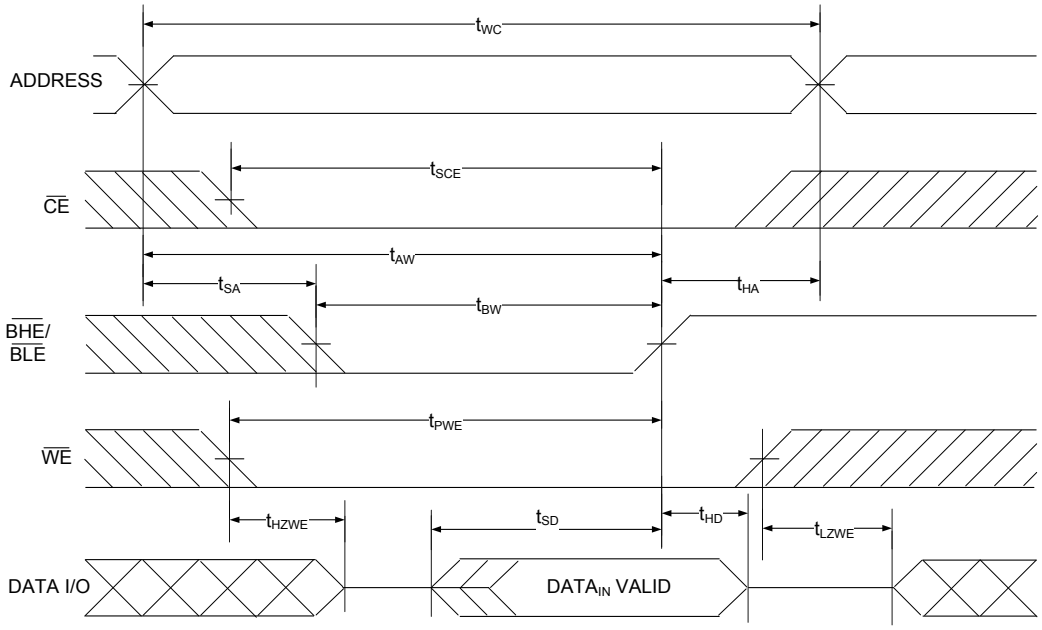


Notes

25. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE}_1$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
26. Data I/O is in HI-Z state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.
27. The minimum write pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be sum of t_{HZWE} and t_{SD}.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 4 ($\overline{BHE}$/$\overline{BLE}$ Controlled) [28, 29]



Notes

28. The internal write time of the memory is defined by the overlap of $\overline{WE}$ = V_{IL}, $\overline{CE_1}$ = V_{IL}, $\overline{BHE}$ or $\overline{BLE}$ or both = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
29. Data I/O is in a HI-Z state if $\overline{CE}$ = V_{IH}, or $\overline{OE}$ = V_{IH} or $\overline{BHE}$, and/or $\overline{BLE}$ = V_{IH}.

Truth Table – CY62146G

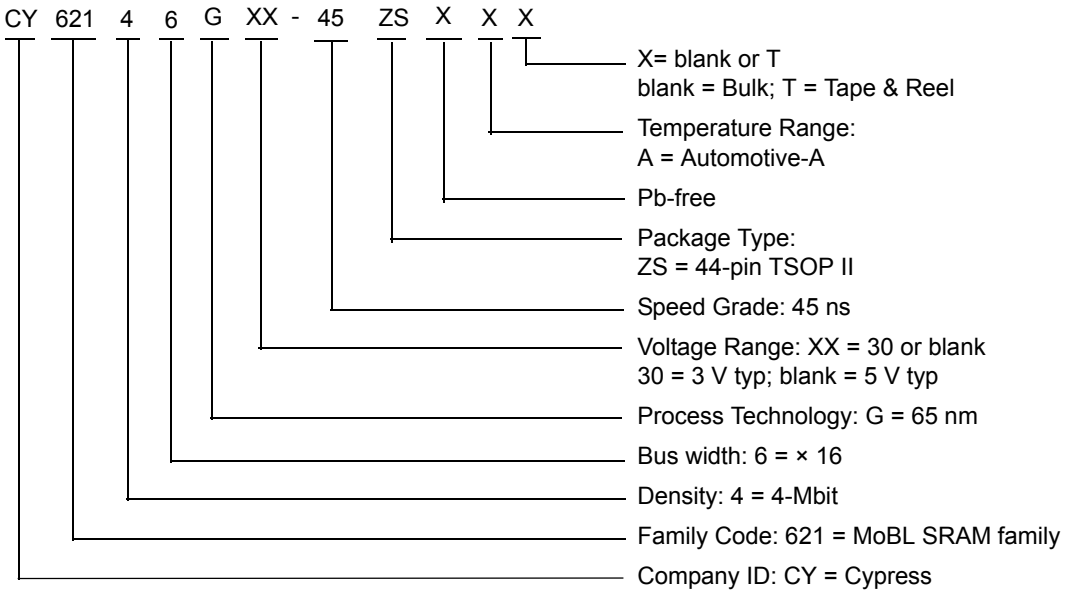
$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	HI-Z	Deselect/Power-down	Standby (I_{SB})
X[30]	X	X	H	H	HI-Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data Out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data Out (I/O_0–I/O_7); HI-Z (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	L	L	H	HI-Z (I/O_0–I/O_7); Data Out (I/O_8–I/O_{15})	Read	Active (I_{CC})
L	H	H	X	X	HI-Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data In (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data In (I/O_0–I/O_7); HI-Z (I/O_8–I/O_{15})	Write	Active (I_{CC})
L	L	X	L	H	HI-Z (I/O_0–I/O_7); Data In (I/O_8–I/O_{15})	Write	Active (I_{CC})

Notes
30. The ‘X’ (Don’t care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

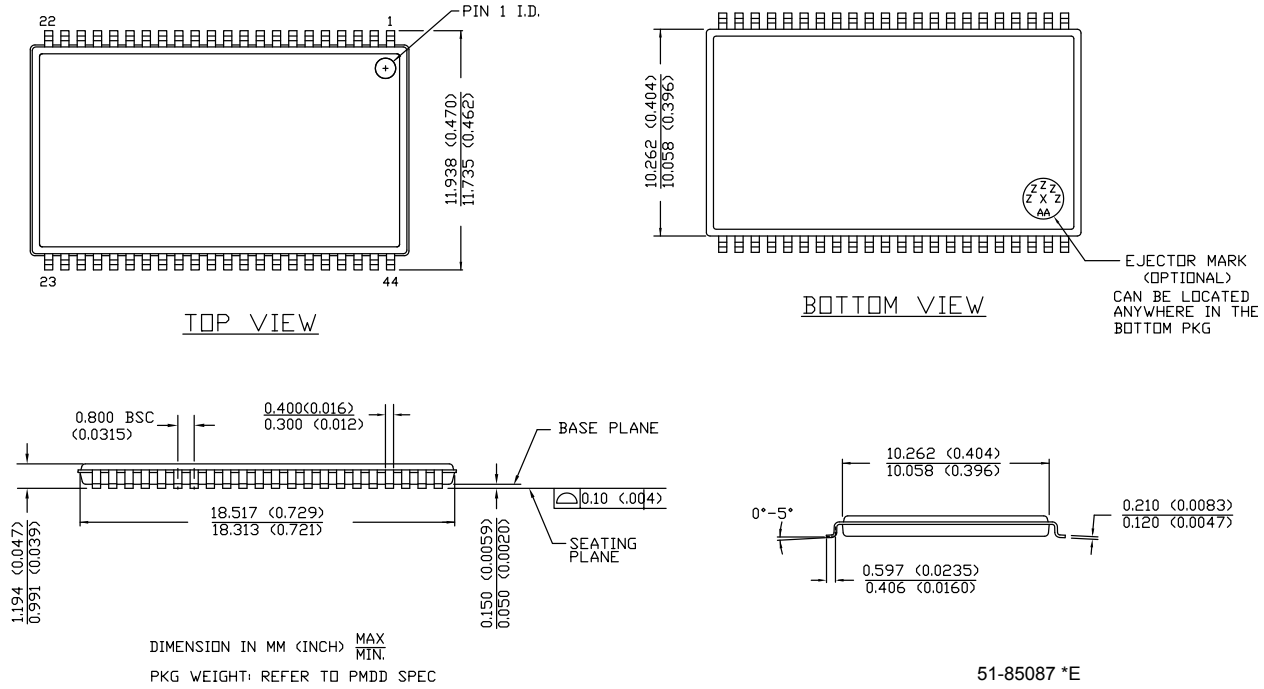
Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type	Operating Range
45	2.2 V–3.6 V	CY62146G30-45ZSXA	51-85087	44-pin TSOP II	Automotive-A
		CY62146G30-45ZSXAT	51-85087	44-pin TSOP II, Tape & Reel	
	4.5 V–5.5 V	CY62146G-45ZSXA	51-85087	44-pin TSOP II	
		CY62146G-45ZSXAT	51-85087	44-pin TSOP II, Tape & Reel	

Ordering Code Definitions



Package Diagrams

Figure 10. 44-pin TSOP Z44-II Package Outline, 51-85087



Acronyms

Acronym	Description
$\overline{BHE}$	Byte High Enable
$\overline{BLE}$	Byte Low Enable
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62146G MoBL® Automotive, 4-Mbit (256K words × 16 bit) Static RAM with Error-Correcting Code (ECC) Document Number: 002-03594				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*A	5035945	NILE	12/09/2015	Changed status from Preliminary to Final.
*B	5427239	NILE	09/23/2016	Updated Features: Added “AEC-Q100 qualified”. Updated Maximum Ratings: Updated Note 4 (Replaced “2 ns” with “20 ns”). Updated DC Electrical Characteristics: Changed minimum value of V_{OH} parameter from 2.2 V to 2.4 V corresponding to Operating Range “2.7 V to 3.6 V” and Test Condition “V_{CC} = Min, I_{OH} = –1.0 mA”. Changed minimum value of V_{IH} parameter from 2.0 V to 1.8 V corresponding to Operating Range “2.2 V to 2.7 V”. Updated Ordering Information: Updated part numbers. Updated to new template. Completing Sunset Review.
*C	5975694	AESATMP8	11/24/2017	Updated logo and Copyright.

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