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CY14B101LA
CY14B101NA

1-Mbit (128 K × 8/64 K × 16) nvSRAM

Features

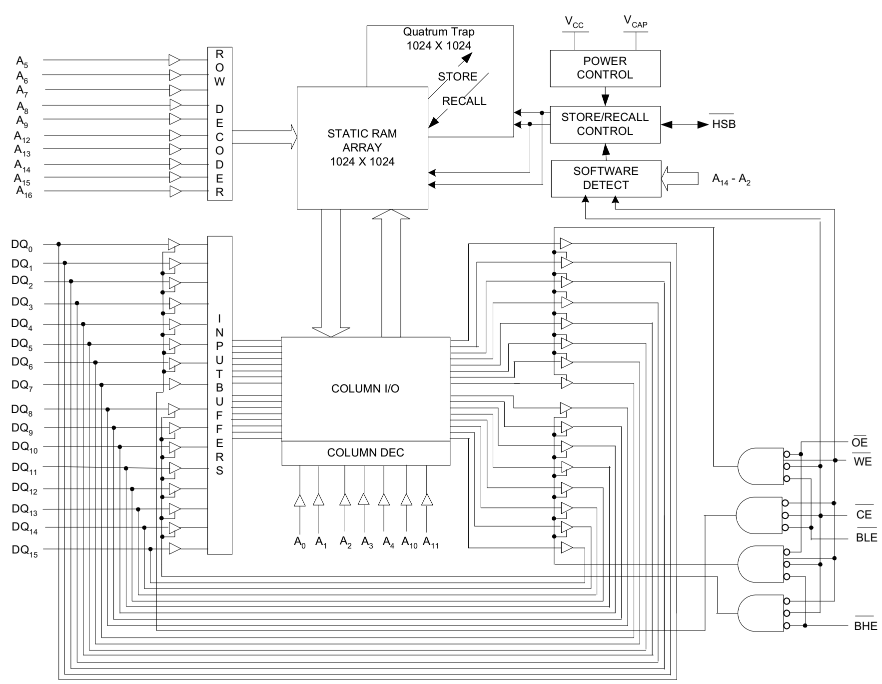
- 20 ns, 25 ns, and 45 ns access times
- Internally organized as 128 K × 8 (CY14B101LA) or 64 K × 16 (CY14B101NA)
- Hands off automatic STORE on power-down with only a small capacitor
- STORE to QuantumTrap nonvolatile elements initiated by software, device pin, or AutoStore on power-down
- RECALL to SRAM initiated by software or power-up
- Infinite read, write, and RECALL cycles
- 1 million STORE cycles to QuantumTrap
- 20 year data retention
- Single 3 V +20% to –10% operation
- Industrial temperature
- Packages
  - 32-pin small-outline integrated circuit (SOIC)
  - 44-/54-pin thin small outline package (TSOP) Type II
  - 48-pin shrink small-outline package (SSOP)
  - 48-ball fine-pitch ball grid array (FBGA)
- Pb-free and restriction of hazardous substances (RoHS) compliant

Functional Description

The Cypress CY14B101LA/CY14B101NA is a fast static RAM (SRAM), with a nonvolatile element in each memory cell. The memory is organized as 128 K bytes of 8 bits each or 64 K words of 16 bits each. The embedded nonvolatile elements incorporate QuantumTrap technology, producing the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while independent nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power-down. On power-up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

For a complete list of related resources, click here.

Logic Block Diagram [1, 2, 3]



Notes
1. Address A_0–A_{16} for × 8 configuration and Address A_0–A_{15} for × 16 configuration.
2. Data DQ_0–DQ_7 for × 8 configuration and Data DQ_0–DQ_{15} for × 16 configuration.
3. BHE and BLE are applicable for × 16 configuration only.

Contents

Pinouts

Figure 1. Pin Diagram – 44-pin TSOP II

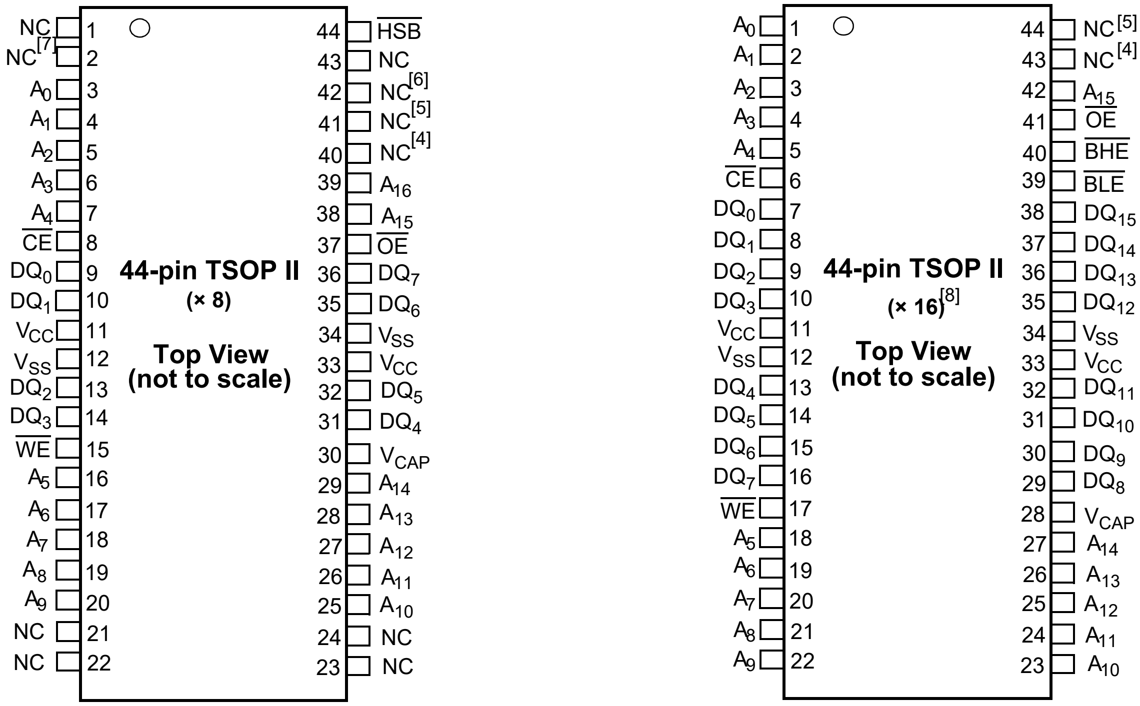
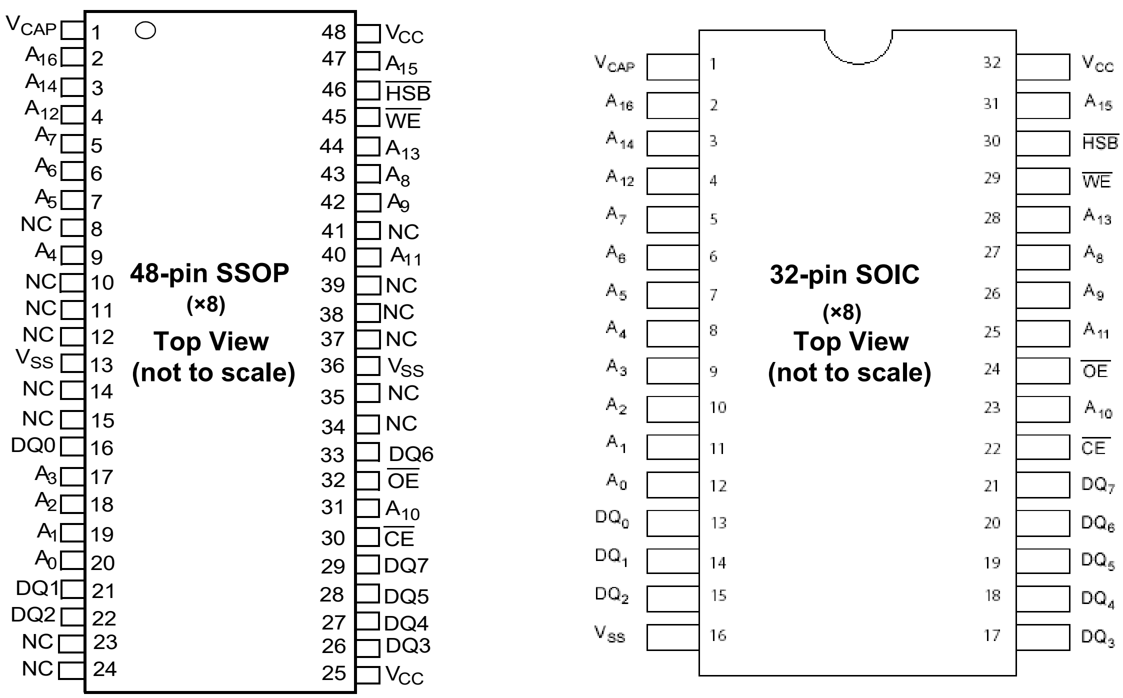


Figure 2. Pin Diagram – 48-pin SSOP and 32-pin SOIC

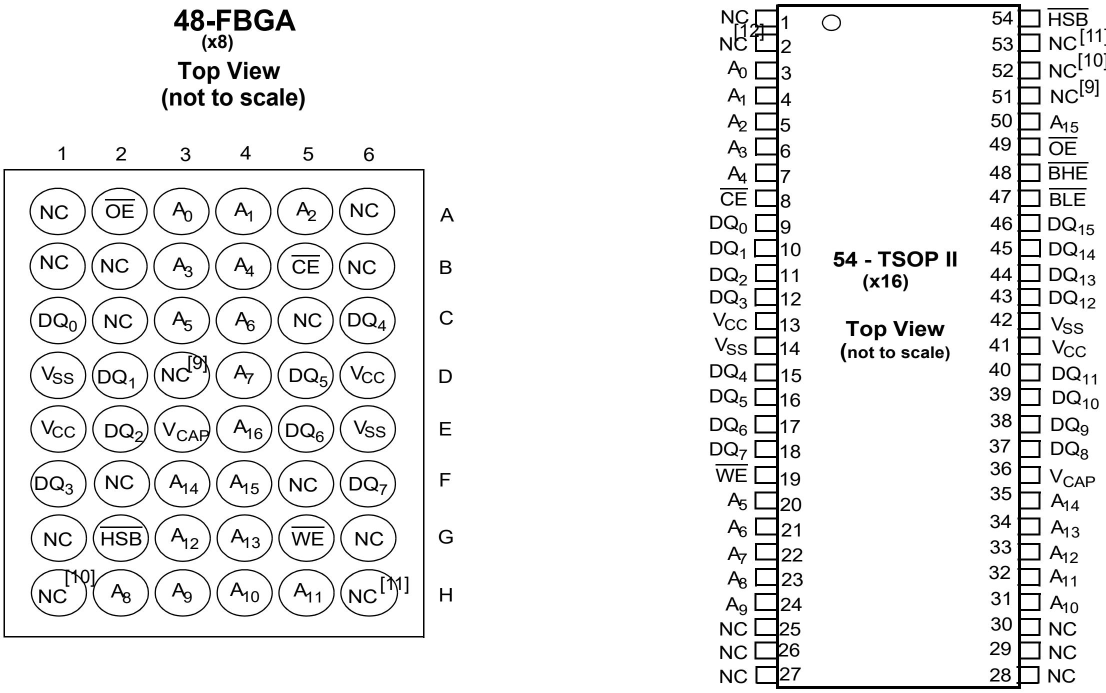


Notes

4. Address expansion for 2-Mbit. NC pin not connected to die.
5. Address expansion for 4-Mbit. NC pin not connected to die.
6. Address expansion for 8-Mbit. NC pin not connected to die.
7. Address expansion for 16-Mbit. NC pin not connected to die.
8. HSB pin is not available in 44-pin TSOP II (× 16) package.

Pinouts (continued)

Figure 3. 48-ball FBGA and 54-pin TSOP II pinout



Notes

9. Address expansion for 2-Mbit. NC pin not connected to die.
10. Address expansion for 4-Mbit. NC pin not connected to die.
11. Address expansion for 8-Mbit. NC pin not connected to die.
12. Address expansion for 16-Mbit. NC pin not connected to die.

Pin Definitions

Pin Name	I/O Type	Description
A_0–A_{16}	Input	Address inputs. Used to select one of the 131,072 bytes of the nvSRAM for × 8 configuration.
A_0–A_{15}		Address inputs. Used to select one of the 65,536 words of the nvSRAM for × 16 configuration.
DQ_0–DQ_7	Input/Output	Bidirectional data I/O lines for × 8 configuration. Used as input or output lines depending on operation.
DQ_0–DQ_{15}		Bidirectional Data I/O Lines for × 16 configuration. Used as input or output lines depending on operation.
$\overline{WE}$	Input	Write Enable input, Active LOW. When the chip is enabled and $\overline{WE}$ is LOW, data on the I/O pins is written to the specific address location.
$\overline{CE}$	Input	Chip Enable input, Active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	Input	Output Enable, Active LOW. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. I/O pins are tristated on deasserting $\overline{OE}$ HIGH.
$\overline{BHE}$	Input	Byte High Enable, Active LOW. Controls DQ_{15}–DQ_8.
$\overline{BLE}$	Input	Byte Low Enable, Active LOW. Controls DQ_7–DQ_0.
V_{SS}	Ground	Ground for the device. Must be connected to the ground of the system.
V_{CC}	Power supply	Power supply inputs to the device. 3.0 V +20%, –10%
$\overline{HSB}$[13]	Input/Output	Hardware STORE Busy ($\overline{HSB}$). When LOW, this output indicates that a Hardware STORE is in progress. When pulled LOW, external to the chip, it initiates a nonvolatile STORE operation. After each Hardware and Software STORE operation $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then a weak internal pull-up resistor keeps this pin HIGH (external pull-up resistor connection optional).
V_{CAP}	Power supply	AutoStore capacitor. Supplies power to the nvSRAM during power loss to store data from SRAM to nonvolatile elements.
NC	No connect	No connect. This pin is not connected to the die.

Note
13. $\overline{HSB}$ pin is not available in 44-pin TSOP II (× 16) package.

Device Operation

The CY14B101LA/CY14B101NA nvSRAM is made up of two functional components paired in the same physical cell. They are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to the SRAM (the RECALL operation). Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations, SRAM read and write operations are inhibited. The CY14B101LA/CY14B101NA supports infinite reads and writes similar to a typical SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 1 million STORE operations. See the Truth Table For SRAM Operations on page 18 for a complete description of read and write modes.

SRAM Read

The CY14B101LA/CY14B101NA performs a read cycle when $\overline{\text{CE}}$ and $\overline{\text{OE}}$ are LOW and $\overline{\text{WE}}$ and $\overline{\text{HSB}}$ are HIGH. The address specified on pins A_{0-16} or A_{0-15} determines which of the 131,072 data bytes or 65,536 words of 16 bits each are accessed. Byte enables ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$) determine which bytes are enabled to the output, in the case of 16-bit words. When the read is initiated by an address transition, the outputs are valid after a delay of t_{AA} (read cycle 1). If the read is initiated by $\overline{\text{CE}}$ or $\overline{\text{OE}}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (read cycle 2). The data output repeatedly responds to address changes within the t_{AA} access time without the need for transitions on any control input pins. This remains valid until another address change or until $\overline{\text{CE}}$ or $\overline{\text{OE}}$ is brought HIGH, or $\overline{\text{WE}}$ or $\overline{\text{HSB}}$ is brought LOW.

SRAM Write

A write cycle is performed when $\overline{\text{CE}}$ and $\overline{\text{WE}}$ are LOW and $\overline{\text{HSB}}$ is HIGH. The address inputs must be stable before entering the write cycle and must remain stable until $\overline{\text{CE}}$ or $\overline{\text{WE}}$ goes HIGH at the end of the cycle. The data on the common I/O pins DQ_{0-15} are written into the memory if the data is valid t_{SD} before the end of a $\overline{\text{WE}}$-controlled write or before the end of a $\overline{\text{CE}}$-controlled write. The Byte Enable inputs ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$) determine which bytes are written, in the case of 16-bit words. Keep $\overline{\text{OE}}$ HIGH during the entire write cycle to avoid data bus contention on common I/O lines. If $\overline{\text{OE}}$ is left LOW, internal circuitry turns off the output buffers t_{HZWE} after $\overline{\text{WE}}$ goes LOW.

AutoStore Operation

The CY14B101LA/CY14B101NA stores data to the nvSRAM using one of the following three storage operations: Hardware STORE activated by $\overline{\text{HSB}}$; Software STORE activated by an address sequence; AutoStore on device power-down. The AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14B101LA/CY14B101NA.

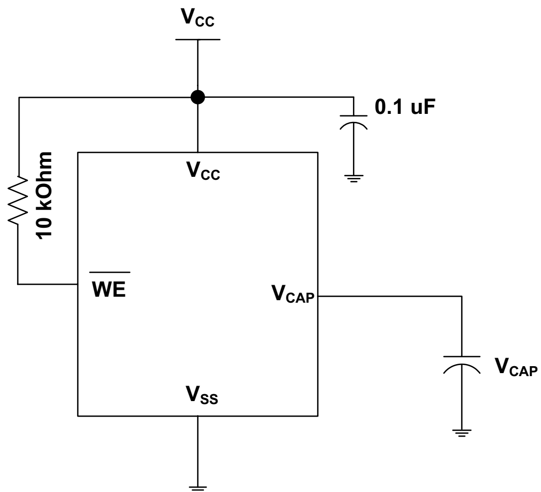
During a normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Note If the capacitor is not connected to V_{CAP} pin, AutoStore must be disabled using the soft sequence specified in Preventing AutoStore on page 8. In case AutoStore is enabled without a capacitor on V_{CAP} pin, the device attempts an AutoStore operation without sufficient charge to complete the store. This corrupts the data stored in nvSRAM.

Figure 4 shows the proper connection of the storage capacitor (V_{CAP}) for automatic STORE operation. See the DC Electrical Characteristics on page 9 for the size of V_{CAP}. The voltage on the V_{CAP} pin is driven to V_{CC} by a regulator on the chip. A pull-up should be placed on $\overline{\text{WE}}$ to hold it inactive during power-up. This pull-up is effective only if the $\overline{\text{WE}}$ signal is tristate during power-up. Many MPUs tristate their controls on power-up. This should be verified when using the pull-up. When the nvSRAM comes out of power-on-RECALL, the MPU must be active or the $\overline{\text{WE}}$ held inactive until the MPU comes out of reset.

To reduce unnecessary nonvolatile stores, AutoStore and Hardware STORE operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place. The $\overline{\text{HSB}}$ signal is monitored by the system to detect if an AutoStore cycle is in progress.

Figure 4. AutoStore Mode



Hardware STORE Operation

The CY14B101LA/CY14B101NA provides the $\overline{\text{HSB}}$[14] pin to control and acknowledge the STORE operations. Use the $\overline{\text{HSB}}$ pin to request a Hardware STORE cycle. When the $\overline{\text{HSB}}$ pin is driven LOW, the CY14B101LA/CY14B101NA conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle only begins if a write to the SRAM has taken place since the last STORE or RECALL cycle. The $\overline{\text{HSB}}$ pin also acts as an open drain driver (internal 100 kΩ weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

Note After each Hardware and Software STORE operation $\overline{\text{HSB}}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then remains HIGH by internal 100 kΩ pull-up resistor.

Note
14. $\overline{\text{HSB}}$ pin is not available in 44-pin TSOP II (× 16) package.

SRAM write operations that are in progress when HSB is driven LOW by any means are given time (t_{DELAY}) to complete before the STORE operation is initiated. However, any SRAM write cycles requested after HSB goes LOW are inhibited until HSB returns HIGH. In case the write latch is not set, HSB is not driven LOW by the CY14B101LA/CY14B101NA. But any SRAM read and write cycles are inhibited until HSB is returned HIGH by MPU or other external source.

During any STORE operation, regardless of how it is initiated, the CY14B101LA/CY14B101NA continues to drive the HSB pin LOW, releasing it only when the STORE is complete. Upon completion of the STORE operation, the nvSRAM memory access is inhibited for t_{LZHSB} time after HSB pin returns HIGH. Leave the HSB unconnected if it is not used.

Hardware RECALL (Power-up)

During power-up or after any low power condition ($V_{CC}< V_{SWITCH}$), an internal RECALL request is latched. When V_{CC} again exceeds the V_{SWITCH} on power up, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete. During this time, the HSB pin is driven LOW by the HSB driver and all reads and writes to nvSRAM are inhibited.

Software STORE

Data is transferred from the SRAM to the nonvolatile memory by a software address sequence. The CY14B101LA/CY14B101NA Software STORE cycle is initiated by executing sequential CE or OE controlled read cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence, or the sequence is aborted and no STORE or RECALL takes place.

To initiate the Software STORE cycle, the following read sequence must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8FC0 Initiate STORE cycle

The software sequence may be clocked with CE controlled reads or OE controlled reads, with WE kept HIGH for all the six READ sequences. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. HSB is driven LOW. After the t_{STORE} cycle time is fulfilled, the SRAM is activated again for the read and write operation.

Software RECALL

Data is transferred from the nonvolatile memory to the SRAM by a software address sequence. A Software RECALL cycle is initiated with a sequence of read operations in a manner similar to the Software STORE initiation. To initiate the RECALL cycle, the following sequence of CE or OE controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4C63 Initiate RECALL cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared. Next, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is again ready for read and write operations. The RECALL operation does not alter the data in the nonvolatile elements.

Table 1. Mode Selection

CE	WE	OE	BHE, BLE[15]	A_{15}–A_0[16]	Mode	I/O	Power
H	X	X	X	X	Not selected	Output high Z	Standby
L	H	L	L	X	Read SRAM	Output data	Active
L	L	X	L	X	Write SRAM	Input data	Active
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output data Output data Output data Output data Output data Output data	Active[17]

Notes
15. BHE and BLE are applicable for x16 configuration only.
16. While there are 17 address lines on the CY14B101LA (16 address lines on the CY14B101NA), only the 13 address lines (A_{14} - A_2) are used to control software modes. Rest of the address lines are do not care.
17. The six consecutive address locations must be in the order listed. WE must be HIGH during all six cycles to enable a nonvolatile cycle.

Table 1. Mode Selection (continued)

CE	WE	OE	BHE, BLE[15]	A_{15}–A_0[16]	Mode	I/O	Power
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output data Output data Output data Output data Output data Output data	Active[18]
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile STORE	Output data Output data Output data Output data Output data Output high Z	Active I_{CC2}[18]
L	H	L	X	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile RECALL	Output data Output data Output data Output data Output data Output high Z	Active[18]

Preventing AutoStore

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the Software STORE initiation. To initiate the AutoStore disable sequence, the following sequence of CE or OE controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8B45 AutoStore Disable

The AutoStore is reenabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the Software RECALL initiation. To initiate the AutoStore enable sequence, the following sequence of CE or OE controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or reenabled, a manual STORE operation (Hardware or Software) must be issued to save the AutoStore state through subsequent power-down cycles. The part comes from the factory with AutoStore enabled and 0x00 written in all cells.

Data Protection

The CY14B101LA/CY14B101NA protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and write operations. The low voltage condition is detected when V_{CC} is less than V_{SWITCH}. If the CY14B101LA/CY14B101NA is in a write mode (both CE and WE are LOW) at power-up, after a RECALL or STORE, the write is inhibited until the SRAM is enabled after t_{LZHSB} (HSB to output active). This protects against inadvertent writes during power-up or brown out conditions.

Note

18. The six consecutive address locations must be in the order listed. WE must be HIGH during all six cycles to enable a nonvolatile cycle.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Maximum accumulated storage time:
At 150 °C ambient temperature .... 1000 h
At 85 °C ambient temperature .... 20 Years

Maximum junction temperature .... 150 °C

Supply voltage on V_{CC} relative to V_{SS} ....–0.5 V to 4.1 V

Voltage applied to outputs in High Z state .... –0.5 V to V_{CC} + 0.5 V

Input voltage .... –0.5 V to V_{CC} + 0.5 V

Transient voltage (< 20 ns) on any pin to ground potential .... –2.0 V to V_{CC} + 2.0 V

Package power dissipation capability (T_A = 25 °C) .... 1.0 W

Surface mount Pb soldering temperature (3 Seconds) .... +260 °C

DC output current (1 output at a time, 1s duration) .... 15 mA

Static discharge voltage (per MIL-STD-883, Method 3015) .... > 2001 V

Latch up current .... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	2.7 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	Min	Typ [19]	Max	Unit
V_{CC}	Power supply voltage		2.7	3.0	3.6	V
I_{CC1}	Average V_{CC} current	t_{RC} = 20 ns t_{RC} = 25 ns t_{RC} = 45 ns Values obtained without output loads (I_{OUT} = 0 mA)	–	–	70 70 52	mA mA mA
I_{CC2}	Average V_{CC} current during STORE	All inputs don't care, V_{CC} = Max Average current for duration t_{STORE}	–	–	10	mA
I_{CC3}	Average V_{CC} current at t_{RC} = 200 ns, $V_{CC(Typ)}$, 25 °C	All inputs cycling at CMOS levels. Values obtained without output loads (I_{OUT} = 0 mA)	–	35	–	mA
I_{CC4}	Average V_{CAP} current during AutoStore cycle	All inputs don't care. Average current for duration t_{STORE}	–	–	5	mA
I_{SB}	V_{CC} standby current	$\overline{CE} \geq (V_{CC} - 0.2$ V). $V_{IN} \leq 0.2$ V or $\geq (V_{CC} - 0.2$ V). Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz	–	–	5	mA
I_{IX}[20]	Input leakage current (except $\overline{HSB}$)	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$	–1	–	+1	μA
	Input leakage current (for $\overline{HSB}$)	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$	–100	–	+1	μA
I_{OZ}	Off-state output leakage current	V_{CC} = Max, $V_{SS} \leq V_{OUT} \leq V_{CC}$, $\overline{CE}$ or $\overline{OE} \geq V_{IH}$ or $\overline{BHE}/\overline{BLE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$	–1	–	+1	μA
V_{IH}	Input HIGH voltage		2.0	–	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage		V_{SS} – 0.5	–	0.8	V
V_{OH}	Output HIGH voltage	I_{OUT} = –2 mA	2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OUT} = 4 mA	–	–	0.4	V

Notes

19. Typical values are at 25 °C, $V_{CC} = V_{CC(Typ)}$. Not 100% tested.
20. The $\overline{HSB}$ pin has I_{OUT} = -2 μA for V_{OH} of 2.4 V when both active high and low drivers are disabled. When they are enabled standard V_{OH} and V_{OL} are valid. This parameter is characterized but not tested.

DC Electrical Characteristics (continued)

Over the Operating Range

Parameter	Description	Test Conditions	Min	Typ [19]	Max	Unit
V_{CAP}[21]	Storage capacitor	Between V_{CAP} pin and V_{SS}	61	68	180	μF
V_{VCAP}[22, 23]	Maximum voltage driven on V_{CAP} pin by the device	V_{CC} = Max	–	–	V_{CC}	V

Data Retention and Endurance

Over the Operating Range

Parameter	Description	Min	Unit
$DATA_R$	Data retention	20	Years
NV_C	Nonvolatile STORE operations	1,000	K

Capacitance

Parameter[23]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance (except $\overline{BHE}$, $\overline{BLE}$ and $\overline{HSB}$)	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(Typ)}$	7	pF
	Input capacitance (for $\overline{BHE}$, $\overline{BLE}$ and $\overline{HSB}$)		8	pF
C_{OUT}	Output capacitance (except $\overline{HSB}$)		7	pF
	Output capacitance (for $\overline{HSB}$)		8	pF

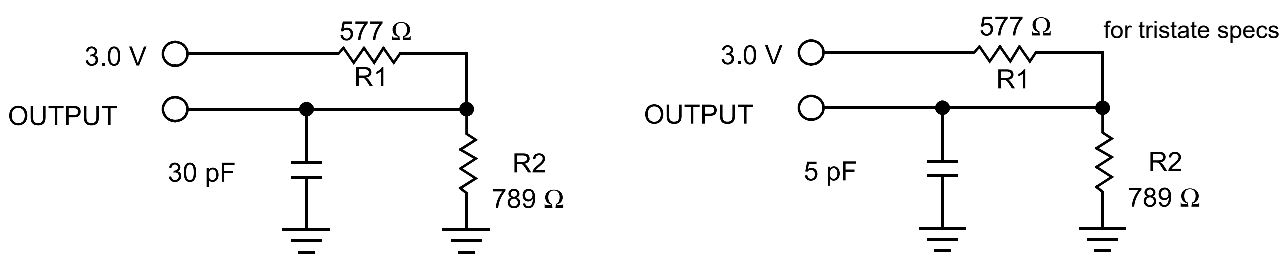
Thermal Resistance

Parameter[23]	Description	Test Conditions	54-pin TSOP II	48-pin SSOP	48-ball FBGA	44-pin TSOP II	32-pin SOIC	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	36.4	37.47	48.19	41.74	41.55	°C/W
Θ_{JC}	Thermal resistance (junction to case)		10.13	24.71	6.5	11.90	24.43	°C/W

Notes
21. Min V_{CAP} value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max V_{CAP} value guarantees that the capacitor on V_{CAP} is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore it is always recommended to use a capacitor within the specified min and max limits. See application note AN43593 for more details on V_{CAP} options.
22. Maximum voltage on V_{CAP} pin (V_{VCAP}) is provided for guidance when choosing the V_{CAP} capacitor. The voltage rating of the V_{CAP} capacitor across the operating temperature range should be higher than the V_{VCAP} voltage.
23. These parameters are guaranteed by design and are not tested.

AC Test Loads

Figure 5. AC Test Loads



AC Test Conditions

Input pulse levels ....0 V to 3 V
Input rise and fall times (10%–90%) .... $\leq$ 3 ns
Input and output timing reference levels .... 1.5 V

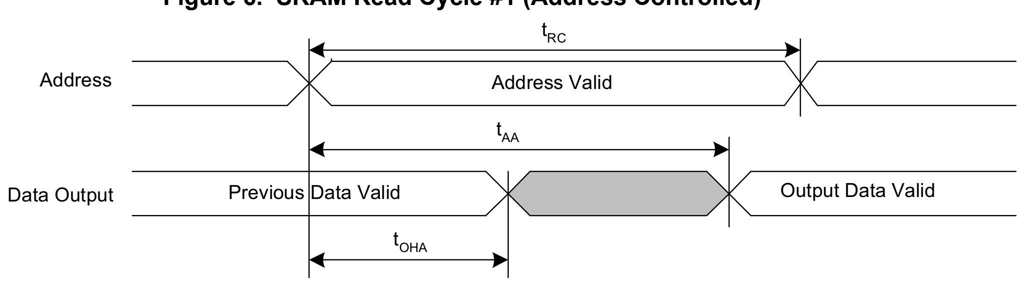
AC Switching Characteristics

Over the Operating Range

Parameters [24]		Description	20 ns		25 ns		45 ns		Unit
Cypress Parameter	Alt Parameter		Min	Max	Min	Max	Min	Max	
SRAM Read Cycle									
t_{ACE}	t_{ACS}	Chip enable access time	–	20	–	25	–	45	ns
t_{RC} [25]	t_{RC}	Read cycle time	20	–	25	–	45		ns
t_{AA} [26]	t_{AA}	Address access time	–	20	–	25	–	45	ns
t_{DOE}	t_{OE}	Output enable to data valid	–	10	–	12	–	20	ns
t_{OHA} [26]	t_{OH}	Output hold after address change	3	–	3	–	3	–	ns
t_{LZCE} [27, 28]	t_{LZ}	Chip enable to output active	3	–	3	–	3	–	ns
t_{HZCE} [27, 28]	t_{HZ}	Chip disable to output inactive	–	8	–	10	–	15	ns
t_{LZOE} [27, 28]	t_{OLZ}	Output enable to output active	0	–	0	–	0	–	ns
t_{HZOE} [27, 28]	t_{OHZ}	Output disable to output inactive	–	8	–	10	–	15	ns
t_{PU} [27]	t_{PA}	Chip enable to power active	0	–	0	–	0	–	ns
t_{PD} [27]	t_{PS}	Chip disable to power standby	–	20	–	25	–	45	ns
t_{DBE}[[27]	–	Byte enable to data valid	–	10	–	12	–	20	ns
t_{LZBE} [27]	–	Byte enable to output active	0	–	0	–	0		ns
t_{HZBE} [27]	–	Byte disable to output inactive	–	8	–	10	–	15	ns
SRAM Write Cycle									
t_{WC}	t_{WC}	Write cycle time	20	–	25	–	45	–	ns
t_{PWE}	t_{WP}	Write pulse width	15	–	20	–	30	–	ns
t_{SCE}	t_{CW}	Chip enable to end of write	15	–	20	–	30	–	ns
t_{SD}	t_{DW}	Data setup to end of write	8	–	10	–	15	–	ns
t_{HD}	t_{DH}	Data hold after end of write	0	–	0	–	0	–	ns
t_{AW}	t_{AW}	Address setup to end of write	15	–	20	–	30	–	ns
t_{SA}	t_{AS}	Address setup to start of write	0	–	0	–	0	–	ns
t_{HA}	t_{WR}	Address hold after end of write	0	–	0	–	0	–	ns
t_{HZWE} [27, 28, 29]	t_{WZ}	Write enable to output disable	–	8	–	10	–	15	ns
t_{LZWE} [27, 28]	t_{OW}	Output active after end of write	3	–	3	–	3	–	ns
t_{BW}	–	Byte enable to end of write	15	–	20	–	30	–	ns

Switching Waveforms

Figure 6. SRAM Read Cycle #1 (Address Controlled) [25, 26, 30]



Notes

24. Test conditions assume signal transition time of 3 ns or less, timing reference levels of $V_{CC}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in Figure 5 on page 11.
25. $\overline{WE}$ must be HIGH during SRAM read cycles.
26. Device is continuously selected with $\overline{CE}$, $\overline{OE}$, and $\overline{BHE}/\overline{BLE}$ LOW.
27. These parameters are guaranteed by design and are not tested.
28. Measured ±200 mV from steady state output voltage.
29. If $\overline{WE}$ is low when $\overline{CE}$ goes low, the outputs remain in the high impedance state.
30. $\overline{HSB}$ must remain HIGH during Read and Write cycles.

Switching Waveforms (continued)

Figure 7. SRAM Read Cycle #2 ($\overline{CE}$ and $\overline{OE}$ Controlled) [31, 32, 33]

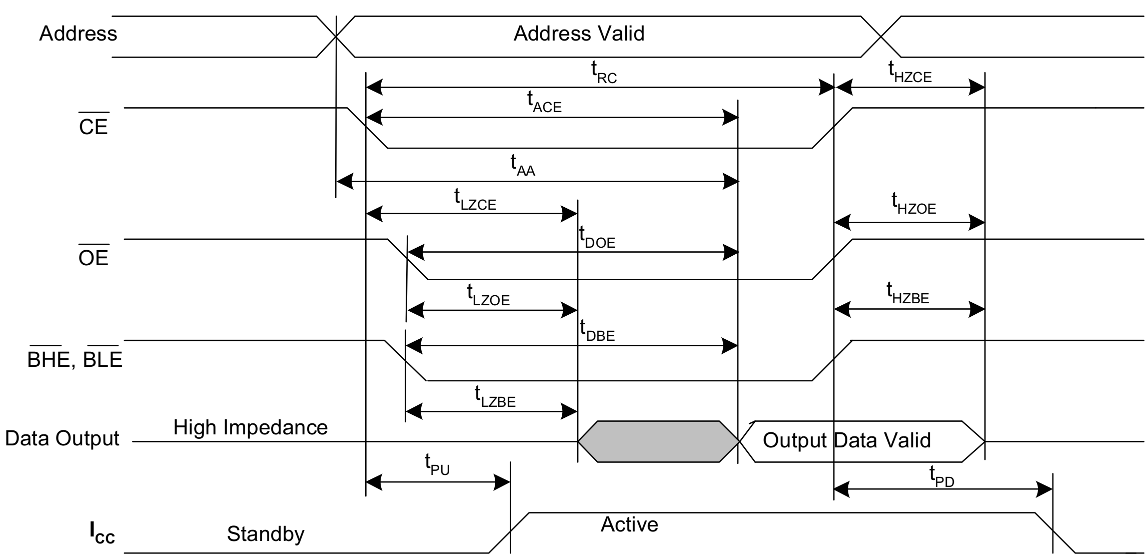
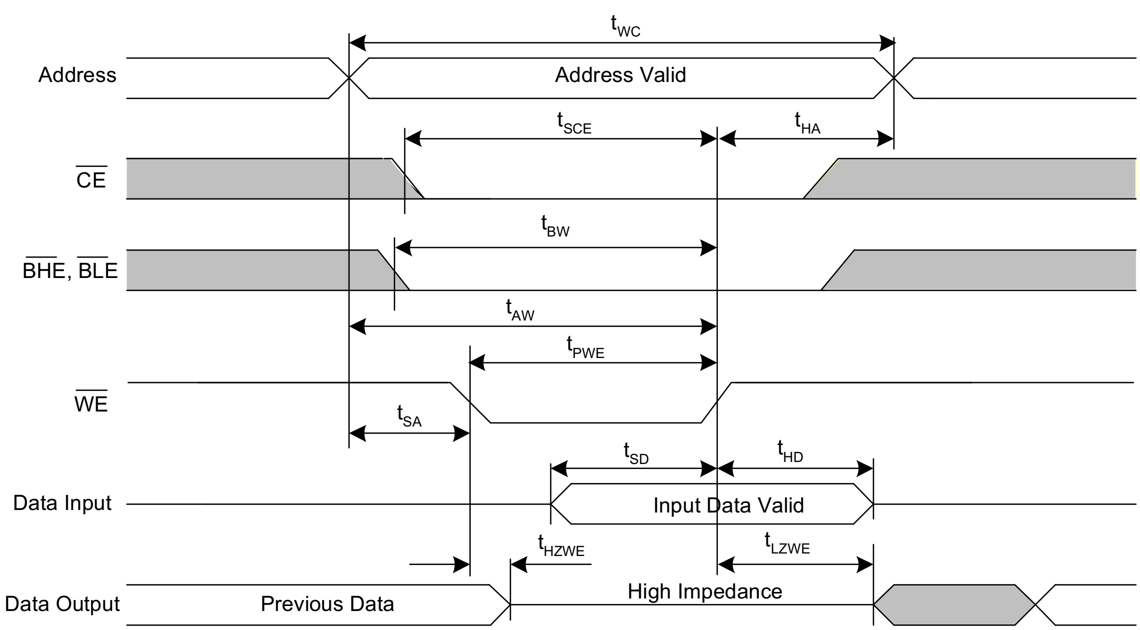


Figure 8. SRAM Write Cycle #1 ($\overline{WE}$ Controlled) [31, 33, 34, 35]



Notes

31. $\overline{BHE}$ and $\overline{BLE}$ are applicable for × 16 configuration only.
32. $\overline{WE}$ must be HIGH during SRAM read cycles.
33. $\overline{HSB}$ must remain HIGH during Read and Write cycles.
34. $\overline{CE}$ or $\overline{WE}$ must be $\geq V_{IH}$ during address transitions.
35. If $\overline{WE}$ is low when $\overline{CE}$ goes low, the outputs remain in the high impedance state.

Switching Waveforms (continued)

Figure 9. SRAM Write Cycle #2 ($\overline{CE}$ Controlled) [36, 37, 38, 39]

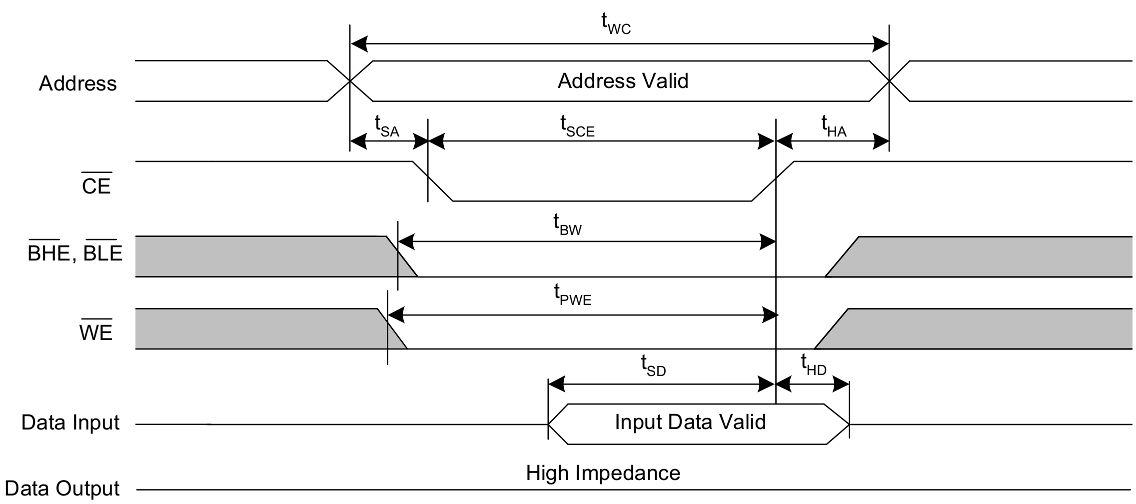
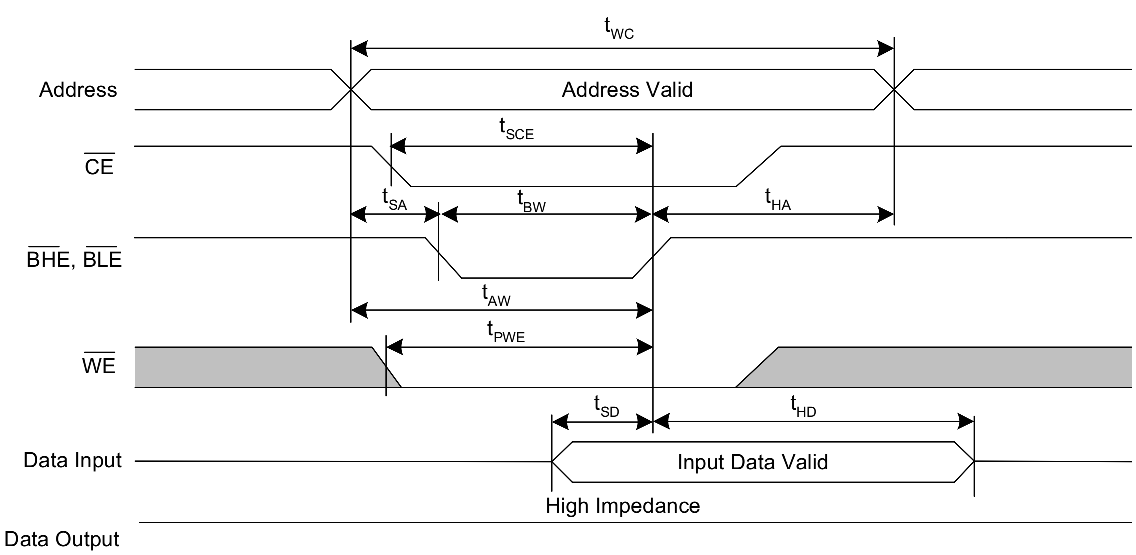


Figure 10. SRAM Write Cycle #3 ($\overline{BHE}$ and $\overline{BLE}$ Controlled) [36, 37, 38, 39]



Notes

36. $\overline{BHE}$ and $\overline{BLE}$ are applicable for × 16 configuration only.
37. If $\overline{WE}$ is low when $\overline{CE}$ goes low, the outputs remain in the high-impedance state.
38. $\overline{HSB}$ must remain HIGH during Read and Write cycles.
39. $\overline{CE}$ or $\overline{WE}$ must be $\geq V_{IH}$ during address transitions.

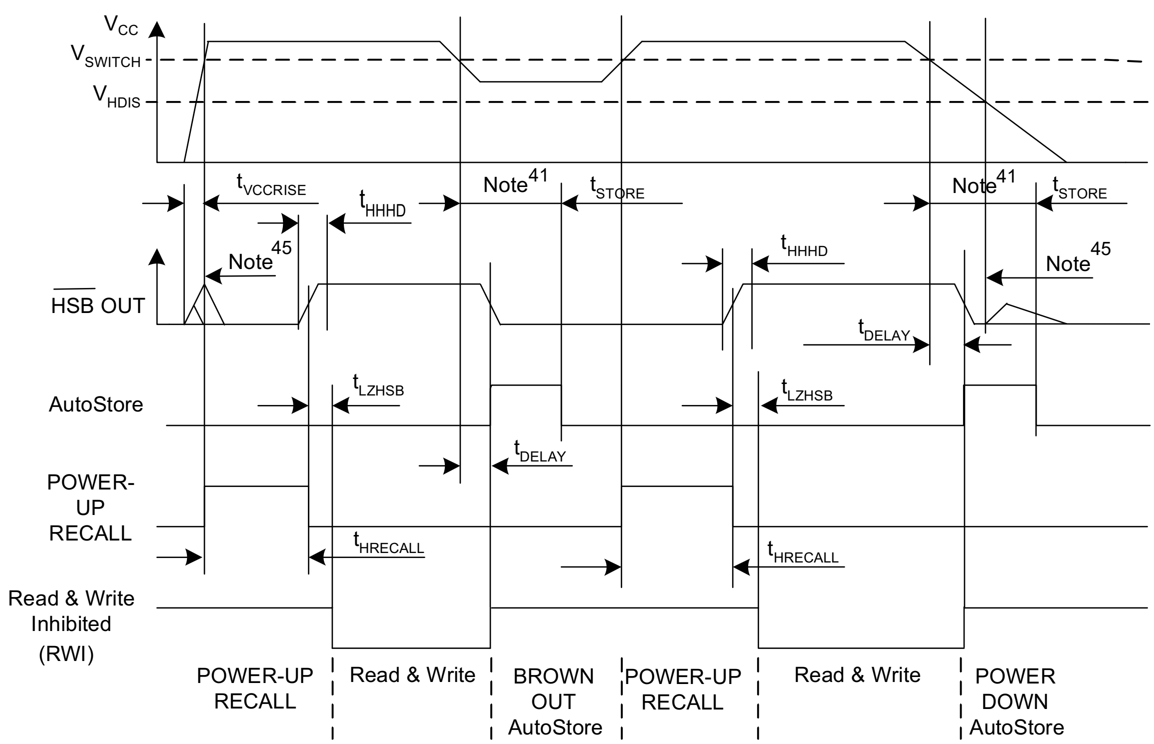
AutoStore/Power-Up RECALL

Over the Operating Range

Parameter	Description	20 ns		25 ns		45 ns		Unit
		Min	Max	Min	Max	Min	Max	
$t_{HRECALL}$ [40]	Power-Up RECALL duration	–	20	–	20	–	20	ms
t_{STORE} [41]	STORE cycle duration	–	8	–	8	–	8	ms
t_{DELAY} [42]	Time allowed to complete SRAM write cycle	–	20	–	25	–	25	ns
V_{SWITCH}	Low voltage trigger level	–	2.65	–	2.65	–	2.65	V
$t_{VCCRISE}$ [43]	V_{CC} rise time	150	–	150	–	150	–	μs
V_{HDIS} [43]	$\overline{HSB}$ output disable voltage	–	1.9	–	1.9	–	1.9	V
t_{LZHSB} [43]	$\overline{HSB}$ to output active time	–	5	–	5	–	5	μs
t_{HHHD} [43]	$\overline{HSB}$ High active time	–	500	–	500	–	500	ns

Switching Waveforms

Figure 11. AutoStore or Power-Up RECALL [44]



Notes
40. $t_{HRECALL}$ starts from the time V_{CC} rises higher than V_{SWITCH}.
41. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
42. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time t_{DELAY}.
43. These parameters are guaranteed by design and are not tested.
44. Read and Write cycles are ignored during STORE, RECALL, and while V_{CC} is lower than V_{SWITCH}.
45. During power-up and power-down, $\overline{HSB}$ glitches when $\overline{HSB}$ pin is pulled up through an external resistor.

Software Controlled STORE/RECALL Cycle

Over the Operating Range

Parameter[46, 47]	Description	20 ns		25 ns		45 ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	STORE/RECALL initiation cycle time	20	–	25	–	45	–	ns
t_{SA}	Address setup time	0	–	0	–	0	–	ns
t_{CW}	Clock pulse width	15	–	20	–	30	–	ns
t_{HA}	Address hold time	0	–	0	–	0	–	ns
t_{RECALL}	RECALL duration	–	200	–	200	–	200	μs

Switching Waveforms

Figure 12. $\overline{CE}$ and $\overline{OE}$ Controlled Software STORE/RECALL Cycle [47]

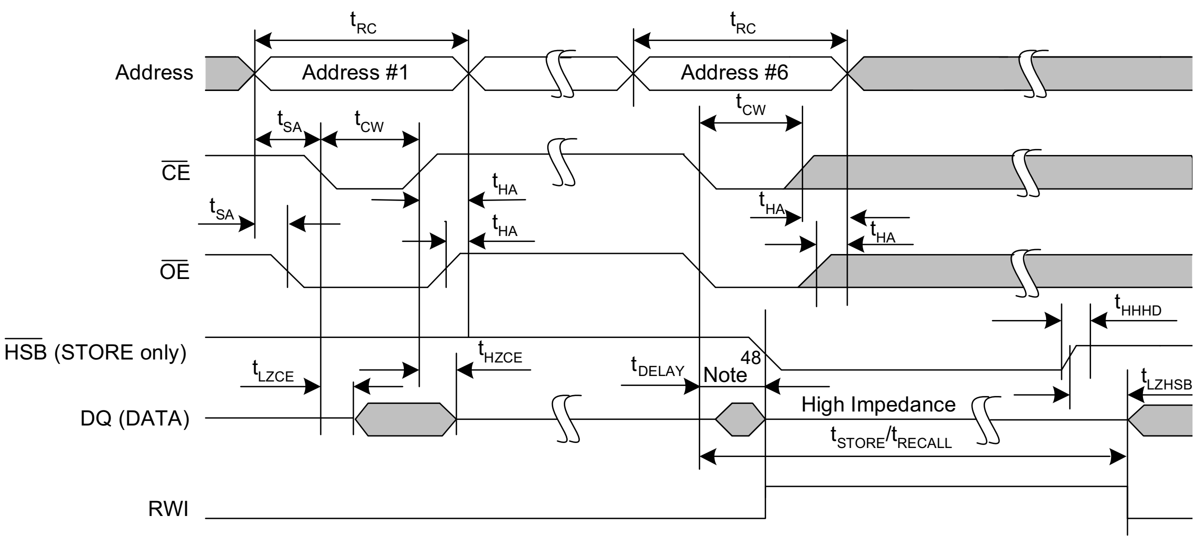
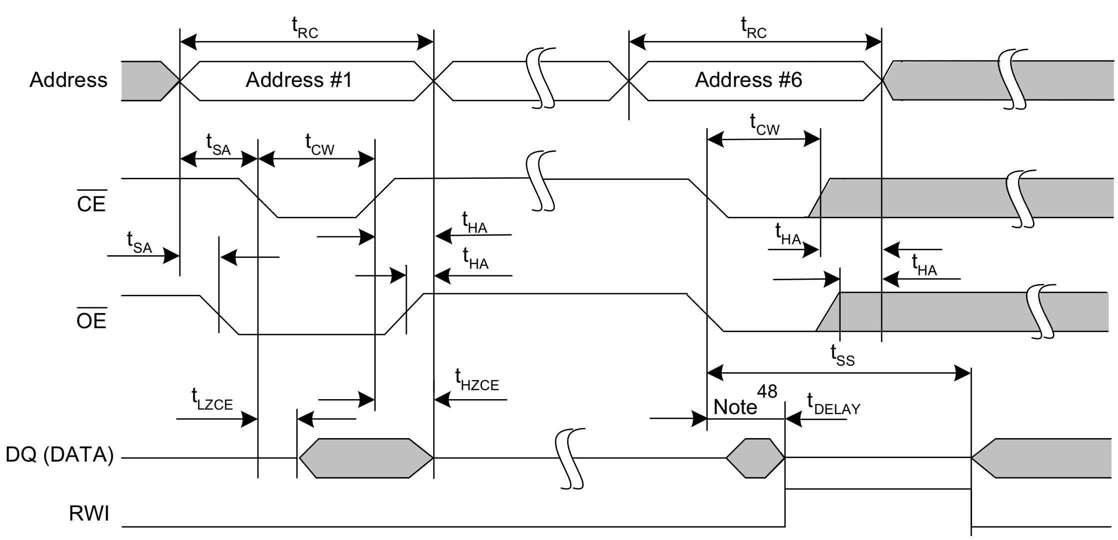


Figure 13. AutoStore Enable/Disable Cycle [47]



Notes
46. The software sequence is clocked with $\overline{CE}$ controlled or $\overline{OE}$ controlled reads.
47. The six consecutive addresses must be read in the order listed in Table 1 on page 7. $\overline{WE}$ must be HIGH during all six consecutive cycles.
48. DQ output data at the sixth read may be invalid because the output is disabled at t_{DELAY} time.

Hardware STORE Cycle

Over the Operating Range

Parameter	Description	20 ns		25 ns		45 ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{DHSB}	$\overline{HSB}$ to output active time when write latch not set	–	20	–	25	–	25	ns
t_{PHSB}	Hardware STORE pulse width	15	–	15	–	15	–	ns
t_{SS} [49, 50]	Soft sequence processing time	–	100	–	100	–	100	µs

Switching Waveforms

Figure 14. Hardware STORE Cycle [51]

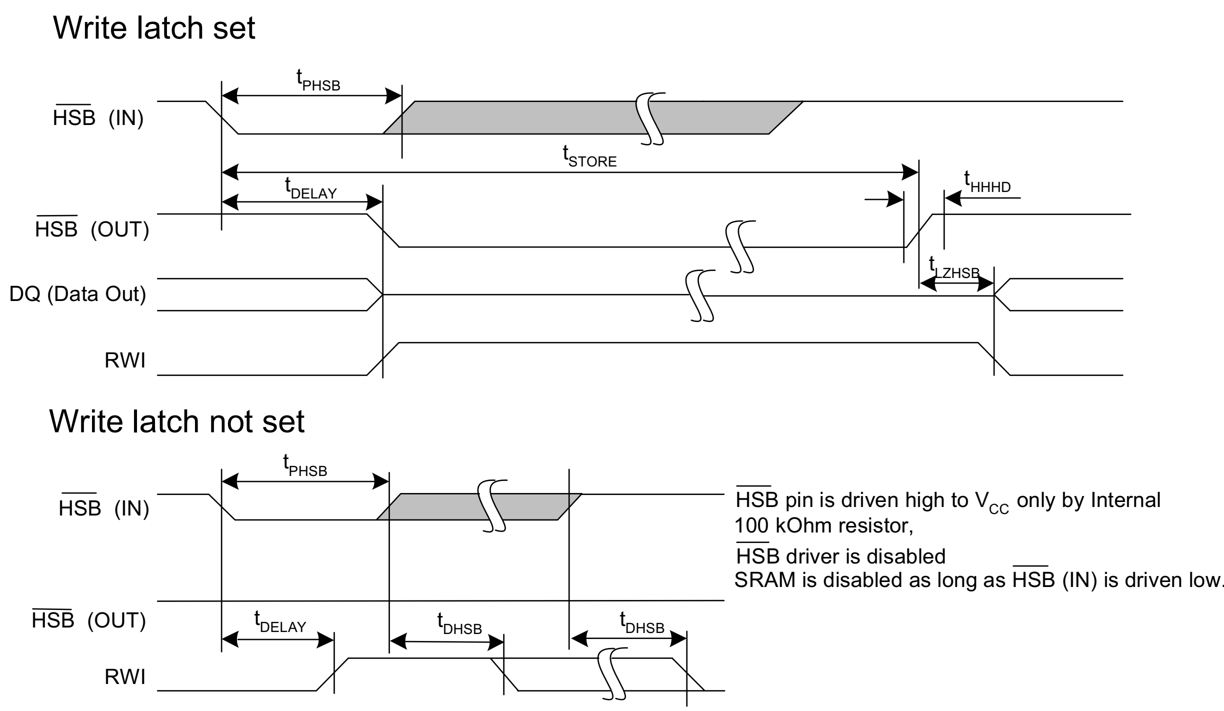
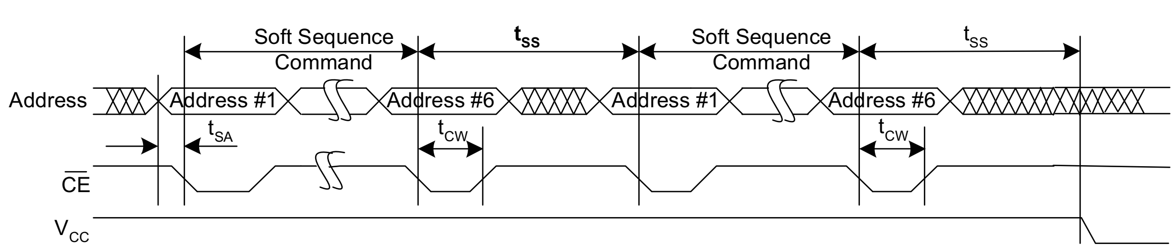


Figure 15. Soft Sequence Processing [49, 50]



Notes

49. This is the amount of time it takes to take action on a soft sequence command. V_{CC} power must remain HIGH to effectively register command.
50. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.
51. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.

Truth Table For SRAM Operations

$\overline{HSB}$ must remain HIGH for SRAM operations

Table 2. Truth Table for × 8 Configuration

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs[52]	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby
L	H	L	Data Out (DQ_0–DQ_7);	Read	Active
L	H	H	High Z	Output disabled	Active
L	L	X	Data in (DQ_0–DQ_7);	Write	Active

Table 3. Truth Table for × 16 Configuration

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$[53]	$\overline{BLE}$[53]	Inputs/Outputs[52]	Mode	Power
H	X	X	X	X	High Z	Deselect/Power-down	Standby
L	X	X	H	H	High Z	Output disabled	Active
L	H	L	L	L	Data Out (DQ_0–DQ_{15})	Read	Active
L	H	L	H	L	Data Out (DQ_0–DQ_7); DQ_8–DQ_{15} in High Z	Read	Active
L	H	L	L	H	Data Out (DQ_8–DQ_{15}); DQ_0–DQ_7 in High Z	Read	Active
L	H	H	L	L	High Z	Output disabled	Active
L	H	H	H	L	High Z	Output disabled	Active
L	H	H	L	H	High Z	Output disabled	Active
L	L	X	L	L	Data In (DQ_0–DQ_{15})	Write	Active
L	L	X	H	L	Data In (DQ_0–DQ_7); DQ_8–DQ_{15} in High Z	Write	Active
L	L	X	L	H	Data In (DQ_8–DQ_{15}); DQ_0–DQ_7 in High Z	Write	Active

Notes

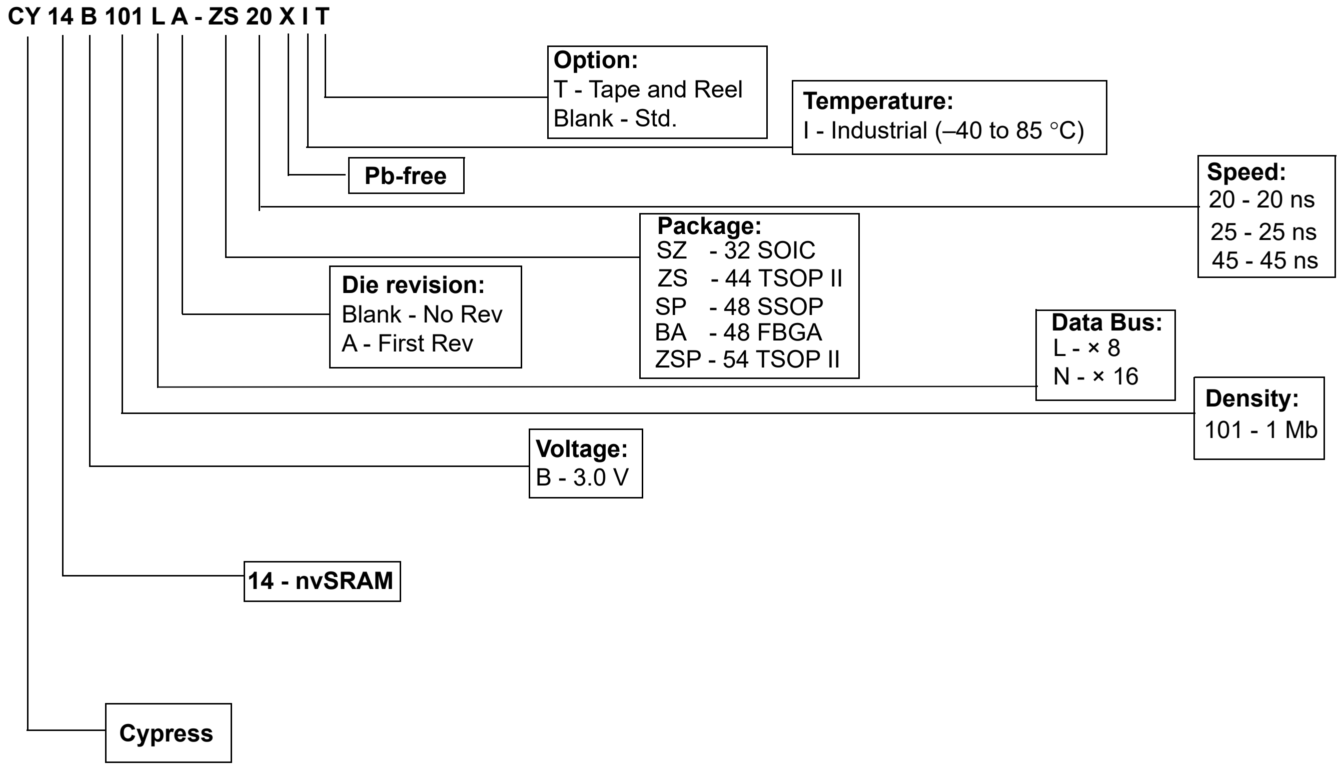
52. Data DQ_0–DQ_7 for × 8 configuration and Data DQ_0–DQ_{15} for × 16 configuration.
53. $\overline{BHE}$ and $\overline{BLE}$ are applicable for × 16 configuration only.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
20	CY14B101LA-ZS20XIT	51-85087	44-pin TSOP II	Industrial
	CY14B101LA-ZS20XI	51-85087	44-pin TSOP II	
25	CY14B101LA-SZ25XIT	51-85127	32-pin SOIC	Industrial
	CY14B101LA-SZ25XI	51-85127	32-pin SOIC	
	CY14B101LA-ZS25XIT	51-85087	44-pin TSOP II	
	CY14B101LA-ZS25XI	51-85087	44-pin TSOP II	
	CY14B101LA-SP25XIT	51-85061	48-pin SSOP	
	CY14B101LA-SP25XI	51-85061	48-pin SSOP	
	CY14B101LA-BA25XIT	51-85128	48-ball FBGA	
	CY14B101LA-BA25XI	51-85128	48-ball FBGA	
	CY14B101NA-ZS25XIT	51-85087	44-pin TSOP II	
	CY14B101NA-ZS25XI	51-85087	44-pin TSOP II	
45	CY14B101LA-SZ45XIT	51-85127	32-pin SOIC	Industrial
	CY14B101LA-SZ45XI	51-85127	32-pin SOIC	
	CY14B101LA-ZS45XIT	51-85087	44-pin TSOP II	
	CY14B101LA-ZS45XI	51-85087	44-pin TSOP II	
	CY14B101LA-SP45XIT	51-85061	48-pin SSOP	
	CY14B101LA-SP45XI	51-85061	48-pin SSOP	
	CY14B101LA-BA45XIT	51-85128	48-ball FBGA	
	CY14B101LA-BA45XI	51-85128	48-ball FBGA	
	CY14B101NA-ZS45XIT	51-85087	44-pin TSOP II	
	CY14B101NA-ZS45XI	51-85087	44-pin TSOP II	

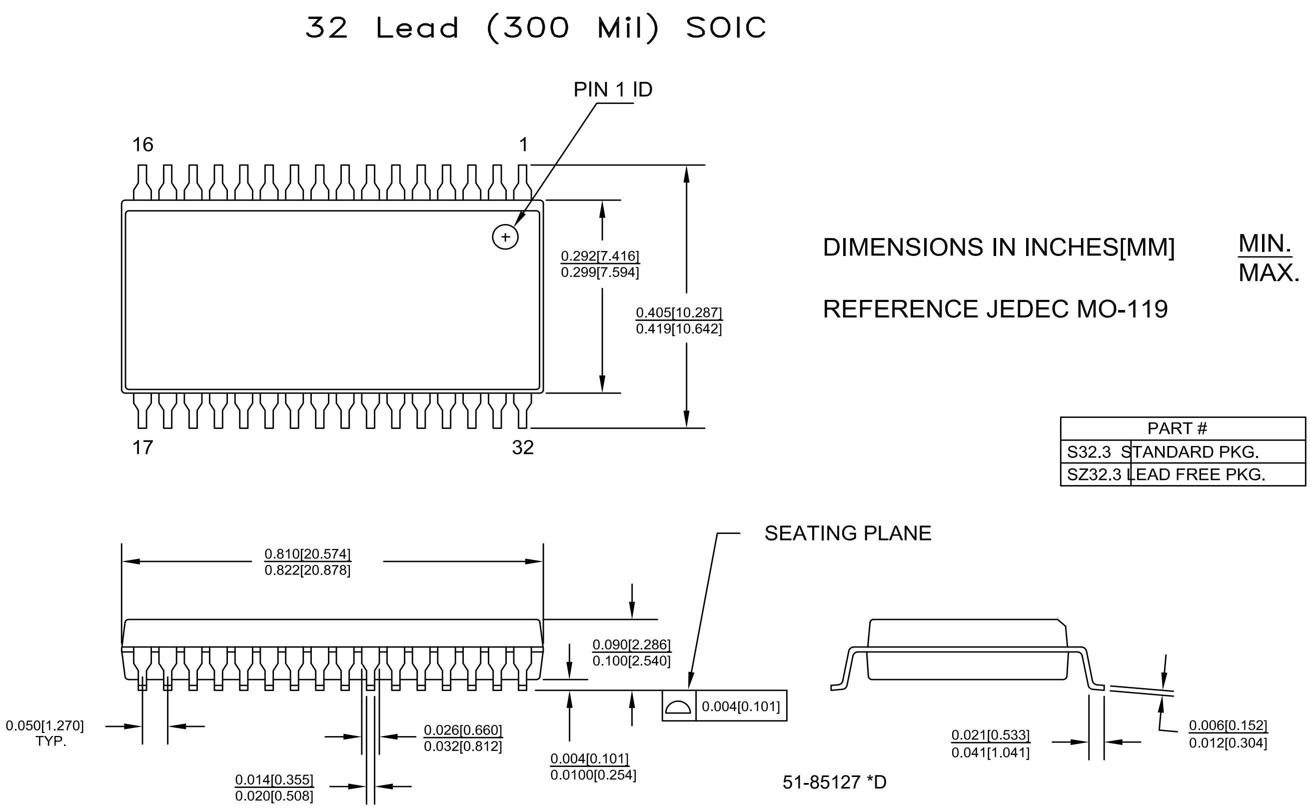
All the above parts are Pb-free.

Ordering Code Definitions



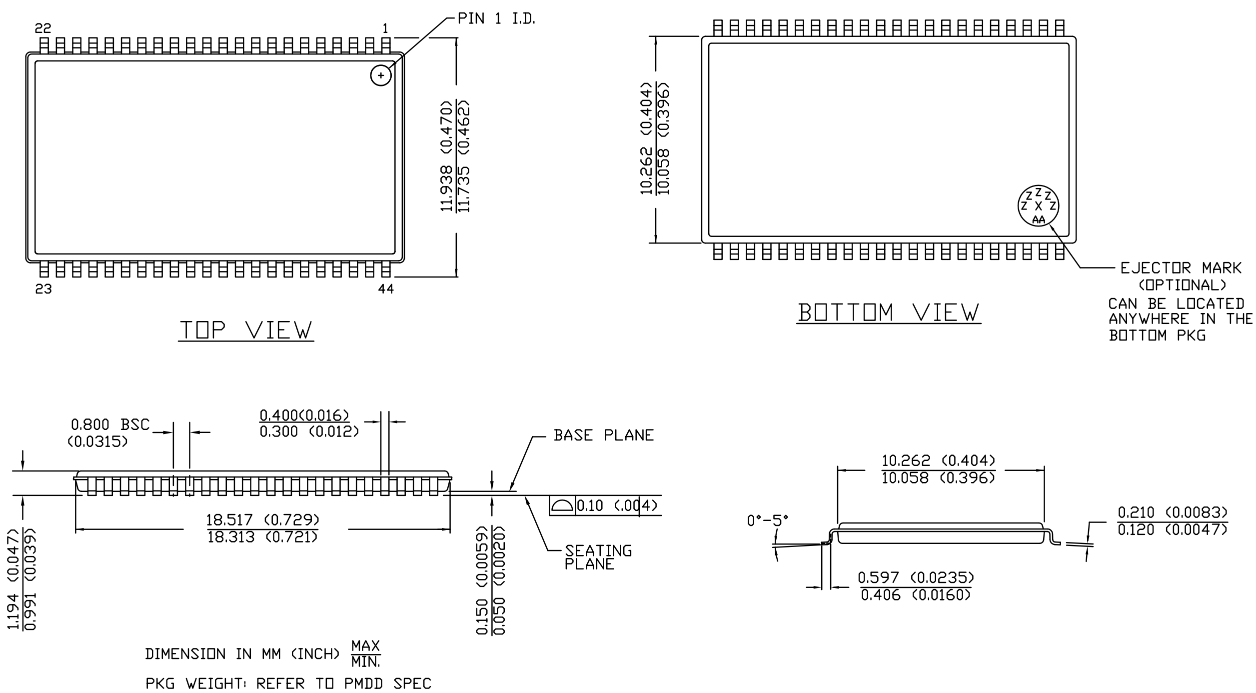
Package Diagrams

Figure 16. 32-pin SOIC (300 Mil) Package Outline, 51-85127



Package Diagrams (continued)

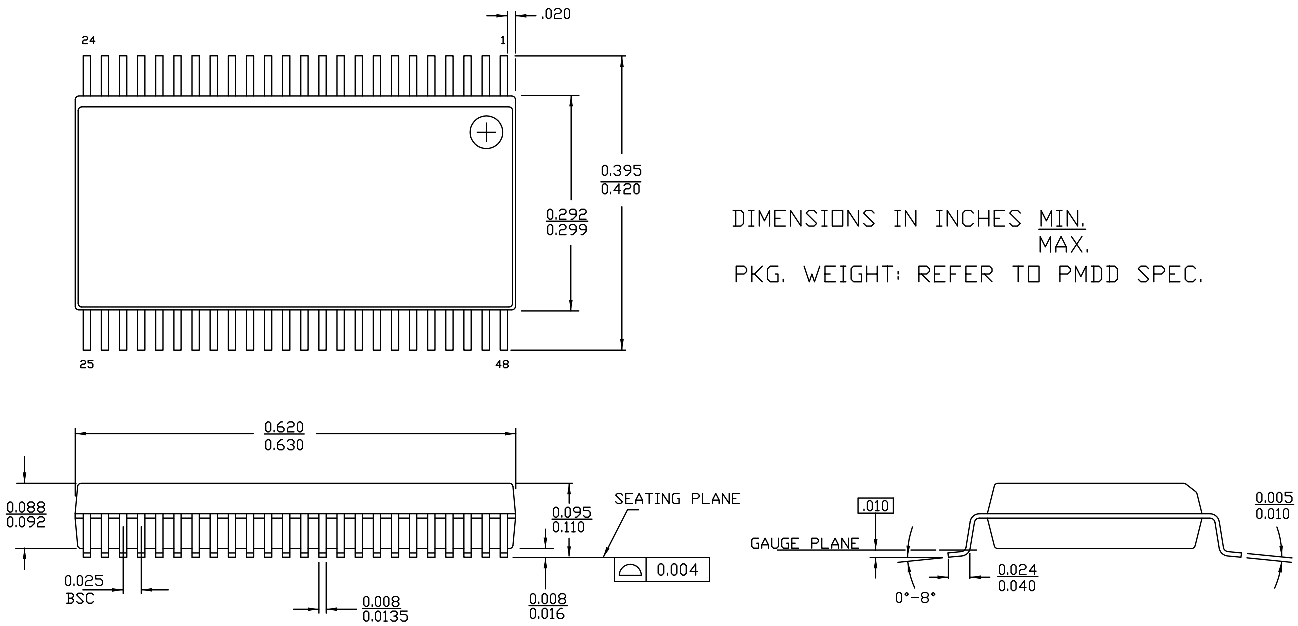
Figure 17. 44-pin TSOP II Package Outline, 51-85087



51-85087 *E

Package Diagrams (continued)

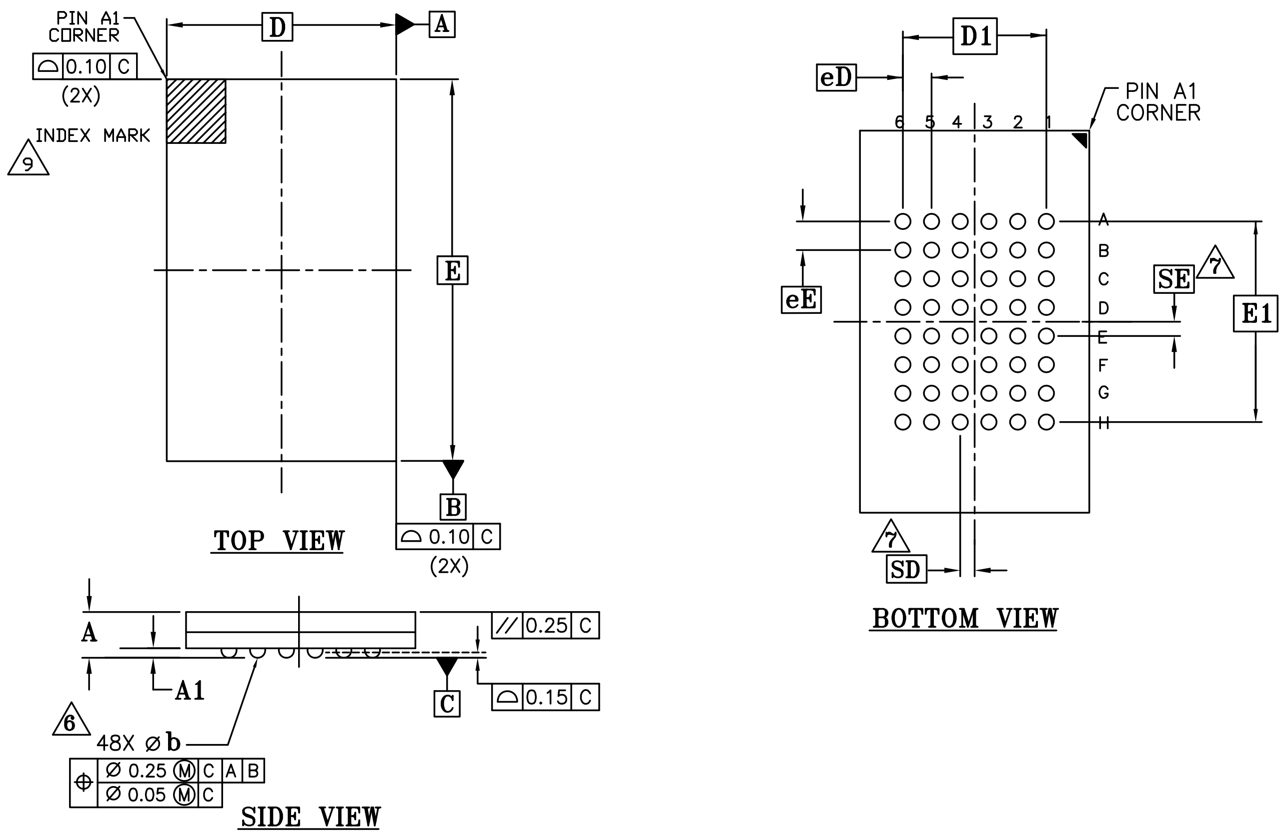
Figure 18. 48-pin SSOP (300 Mils) Package Outline, 51-85061



51-85061 *F

Package Diagrams (continued)

Figure 19. 48-ball FBGA (6 × 10 × 1.2 mm) Package Outline, 51-85128



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.16	–	–
D	6.00 BSC		
E	10.00 BSC		
D1	3.75 BSC		
E1	5.25 BSC		
MD	6		
ME	8		
N	48		
⌀b	0.25	0.30	0.35
eE	0.75 BSC		
eD	0.75 BSC		
SD	0.375 BSC		
SE	0.375 BSC		

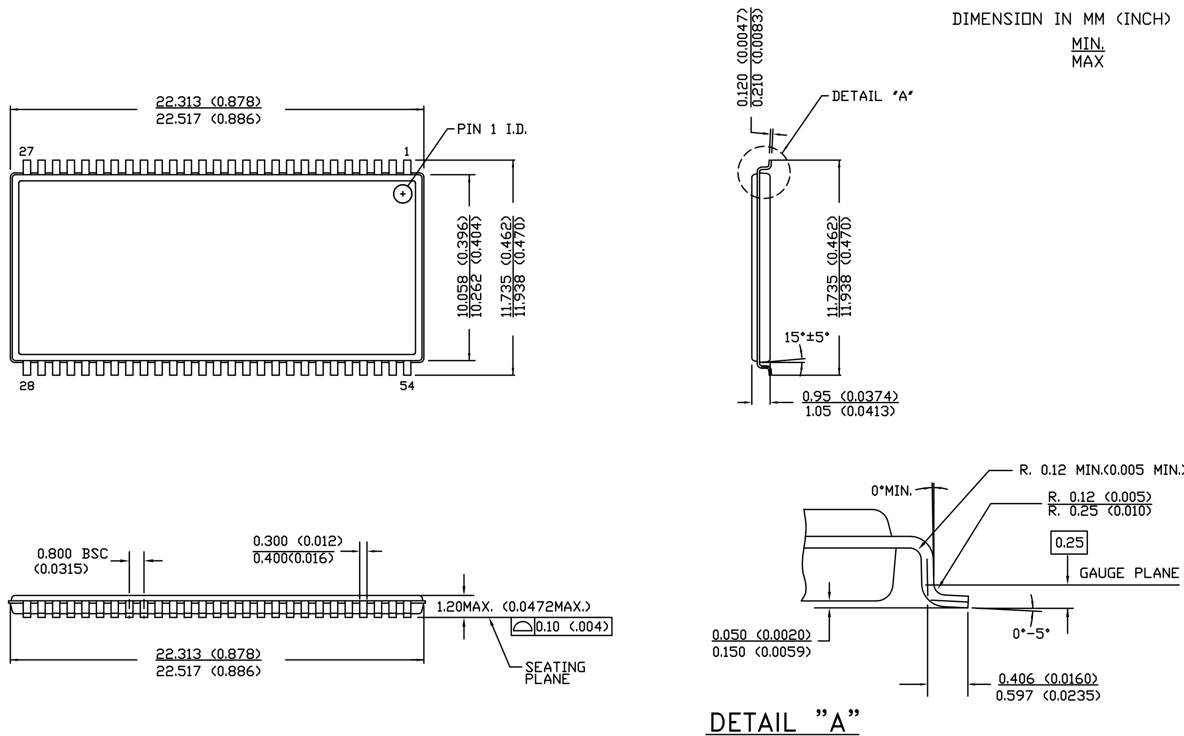
NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

51-85128 *I

Package Diagrams (continued)

Figure 20. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Package Outline, 51-85160



51-85160 *E

Acronyms

Acronym	Description
$\overline{\text{BHE}}$	byte high enable
$\overline{\text{BLE}}$	byte low enable
$\overline{\text{CE}}$	chip enable
CMOS	complementary metal oxide semiconductor
EIA	electronic industries alliance
FBGA	fine-pitch ball grid array
$\overline{\text{HSB}}$	hardware store busy
I/O	input/output
nvSRAM	non-volatile static random access memory
$\overline{\text{OE}}$	output enable
RoHS	restriction of hazardous substances
RWI	read and write inhibited
SOIC	small outline integrated circuit
SRAM	static random access memory
SSOP	shrink small outline package
TSOP	thin small outline package
$\overline{\text{WE}}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
µA	microampere
µF	microfarad
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY14B101LA/CY14B101NA, 1-Mbit (128 K × 8/64 K × 16) nvSRAM Document Number: 001-42879			
Rev.	**ECN No.**	**Submission Date**	**Description of Change**
**	2050747	01/31/08	New data sheet.
*A	2607447	11/14/08	Removed 15 ns access speed Updated “Features” Updated Logic block diagram Added footnote 1 2, 3 and 7 Pin definition: Updated $\overline{WE}$, $\overline{HSB}$ and NC pin description Page 4: Updated SRAM READ, SRAM WRITE, AutoStore operation description Updated Figure 4 Page 4: Updated Hardware store operation and Hardware RECALL (Powerup) description Page 4: Updated Software store and software recall description Footnote 1 and 11 referenced for Mode selection Table Added footnote 11 Updated footnote 9 and 10 Page 6: updated Data protection description Maximum Ratings:Added Max. Accumulated storage time Changed Output short circuit current parameter name to DC output current Changed I_{CC2} from 6 mA to 10 mA Changed I_{CC3} from 15 mA to 35 mA Changed I_{CC4} from 6 mA to 5 mA Changed I_{SB} from 3 mA to 5 mA Added I_{IX} for HSB Updated $I_{CC1,}$ $I_{CC3,}$ I_{SB} and I_{OZ} Test conditions Changed V_{CAP} voltage min value from 68 µF to 61 µF Added V_{CAP} voltage max value to 180 µF Updated footnote 12 and 13 Added footnote 14 Added Data retention and Endurance Table Added thermal resistance value to 48-pin FBGA and 44-pin TSOP II packages Updated Input Rise and Fall time in AC test Conditions Referenced footnote 17 to t_{OHA} parameter Updated All switching waveforms Updated footnote 17 Added footnote 20 Added Figure 10 (SRAM WRITE CYCLE:$\overline{BHE}$ and $\overline{BLE}$ controlled) Changed t_{STORE} max value from 12.5 ms to 8 ms Updated t_{DELAY} value Added V_{HDIS}, t_{HHHD} and t_{LZHSB} parameters Updated footnote 24 Added footnote 26 and 27 Software controlled STORE/RECALL Table: Changed t_{AS} to t_{SA} Changed t_{GHAX} to t_{HA} Changed t_{HA} value from 1 ns to 0 ns Added Figure 13 Added t_{DHSB} parameter Changed t_{HLHX} to t_{PHSB} Updated t_{SS} from 70 µs to 100 µs Added truth table for SRAM operations Updated ordering information and part numbering nomenclature
*B	2654484	02/05/09	Changed status from Advance information to Preliminary. Referenced Note 15 to parameters t_{LZCE}, t_{HZCE}, $t_{LZOE,}$ $t_{HZOE,}$ t_{LZWE} and t_{HZWE} Updated Figure 12

Document History Page (continued)

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Rev.	**ECN No.**	**Submission Date**	**Description of Change**
*C	2733909	07/09/09	Removed 48-ball FBGA package and added 54-pin TSOP II Package Corrected typo error in pin diagram of 48-pin SSOP Page 4; Added note to AutoStore Operation description Page 4; Updated Hardware STORE (HSB) Operation description Page 5; Updated Software STORE Operation description Added best practices Updated V_{HDIS} parameter description Updated t_{DELAY} parameter description Updated footnote 24 and added footnote 29
*D	2757348	08/28/09	Changed status from Preliminary to Final. Removed commercial temperature related specs Updated thermal resistance values for all the packages
*E	2793420	10/27/09	Updated 48-pin SSOP package diagram
*F	2839453	01/06/10	Changed STORE cycles to QuantumTrap from 200 K to 1 Million Added Contents
*G	2894534	03/17/10	Removed inactive parts from Ordering Information table. Updated links in Sales, Solutions, and Legal Information. Updated Package Diagrams.
*H	2922854	04/26/10	Pin Definitions: Added more clarity on HSB pin operation Hardware STORE Operation: Added more clarity on HSB pin operation Table 1: Added more clarity on BHE/BLE pin operation Updated HSB pin operation in Figure 11 Updated footnote 45 Updated package diagram 51-85087
*I	2958648	06/22/10	Added 48-Ball FBGA package related information Updated package diagram 51-85128 Updated template and added Acronym table
*J	3074645	10/29/10	48 FBGA package: 16 Mb address expansion is not supported Removed inactive parts from Ordering Information table. CY14B101NA-ZS20XIT, CY14B101NA-ZS20XI Added Document Conventions table
*K	3134300	01/11/2011	Updated style format Updated input capacitance for BHE and BLE pin Updated input and output capacitance for HSB pin Fixed typo in Figure 11
*L	3313245	07/14/2011	Updated DC Electrical Characteristics (Added Note 21 and referred the same note in V_{CAP} parameter). Updated Thermal Resistance (Θ_{JA} and Θ_{JC} values for 48-ball FBGA package). Updated AC Switching Characteristics (Added Note 24 and referred the same note in Parameters). Updated Package Diagrams.
*M	3457594	12/07/2011	Updated Package Diagrams.
*N	3542240	03/06/2012	Footnote 48 made visible. Modified Figure 13.
*O	3659138	08/14/2012	Updated Maximum Ratings (Changed “Ambient temperature with power applied” to “Maximum junction temperature”). Updated DC Electrical Characteristics (Added V_{VCAP} parameter and its details, added Note 22 and referred the same note in V_{VCAP} parameter, also referred Note 23 in V_{VCAP} parameter). Updated Package Diagrams (spec 51-85160 (Changed revision from *C to *D)).
*P	3769328	10/08/2012	Updated Ordering Information (Added CY14B101LA-BA25XI and CY14B101LA-BA25XIT). Updated Package Diagrams (spec 51-85087 (Changed revision from *D to *E), spec 51-85061 (Changed revision from *E to *F)).

Document History Page (continued)

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*Q	4567905	11/12/2014	Added related documentation hyperlink in page 1. Updated Package Diagrams spec 51-85160 (Changed revision from *D to *E),
*R	5716066	05/09/2015	Updated Package Diagrams. Updated Cypress Logo and Copyright.
*S	6867685	04/24/2020	Updated spec 51-85128 *G to *I in Package Diagrams.

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