VC7215 Virtex-7 FPGA GTH Transceiver Characterization Board

User Guide

UG972 (v1.3) October 17, 2014

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/06/2013	1.0	Initial Xilinx release.
07/30/2013	1.1	Revised Table 1-17. Replaced the Master User Constraint File (UCF) appendix with Appendix C, Master Constraints File Listing. Updated links.
12/18/2013	1.2	Updated Table 1-7 through Table 1-12 and Table 1-18.
10/17/2014	1.3	The number of 7 series GTH transceiver power modules supplied with the VC7215 board changed from four to two. The module vendor changed from Intersil, Texas Instruments, Bellnix, or Lineage to General Electric. The VC7215 Board XDC Listing changed.

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Chapter 1

VC7215 Board Features and Operation

This chapter describes the components, features, and operation of the VC7215 Virtex®-7 FPGA GTH Transceiver Characterization Board. The VC7215 board provides the hardware environment for characterizing and evaluating the GTH transceivers available on the Virtex-7 XC7VX690T-3FFG1927E FPGA. The VC7215 board schematic, bill-of-material (BOM), layout files and reference designs are available online at the Virtex-7 FPGA VC7215 Characterization Kit website.

FPGA Compatibility

The VC7215 board is provided with Virtex-7 XC7VX690T-3FFG1927E FPGA. The board also supports all device densities (i.e., XC7VX415T, XC7VX485T, XC7VX550T, and XC7VX690T devices) in the pin-compatible FFG1927 package. However, certain interfaces that are available in larger density devices might not be available in the XC7VX690T device (for example: GTH QUAD_110, GTH QUAD_111, GTH QUAD_112, and so on).

VC7215 Board Features

- Virtex-7 XC7VX690T-3FFG1927E FPGA
- Onboard power supplies for all necessary voltages
- Power connectors for optional use of external power supplies
- Digilent USB JTAG programming port
- System ACE™ tool Secure Digital (SD) controller
- Two power modules supporting Virtex-7 FPGA GTH transceiver power requirements
- A fixed, 200 MHz 2.5V LVDS oscillator wired to multi-region clock capable (MRCC) inputs
- Two pairs of differential MRCC inputs with SMA connectors
- SuperClock-2 module supporting multiple frequencies
- Twenty Samtec BullsEye connector pads for the GTH transceivers and reference clocks
- Power status LEDs
- General purpose DIP switches, LEDs, pushbuttons, and test I/O
- Two VITA 57.1 FPGA mezzanine card (FMC) high pin count (HPC) connectors
- USB-to-UART bridge
- I2C bus

- PMBus connectivity to onboard digital power supplies
- Active cooling for the FPGA

The VC7215 board block diagram is shown in Figure 1-1.

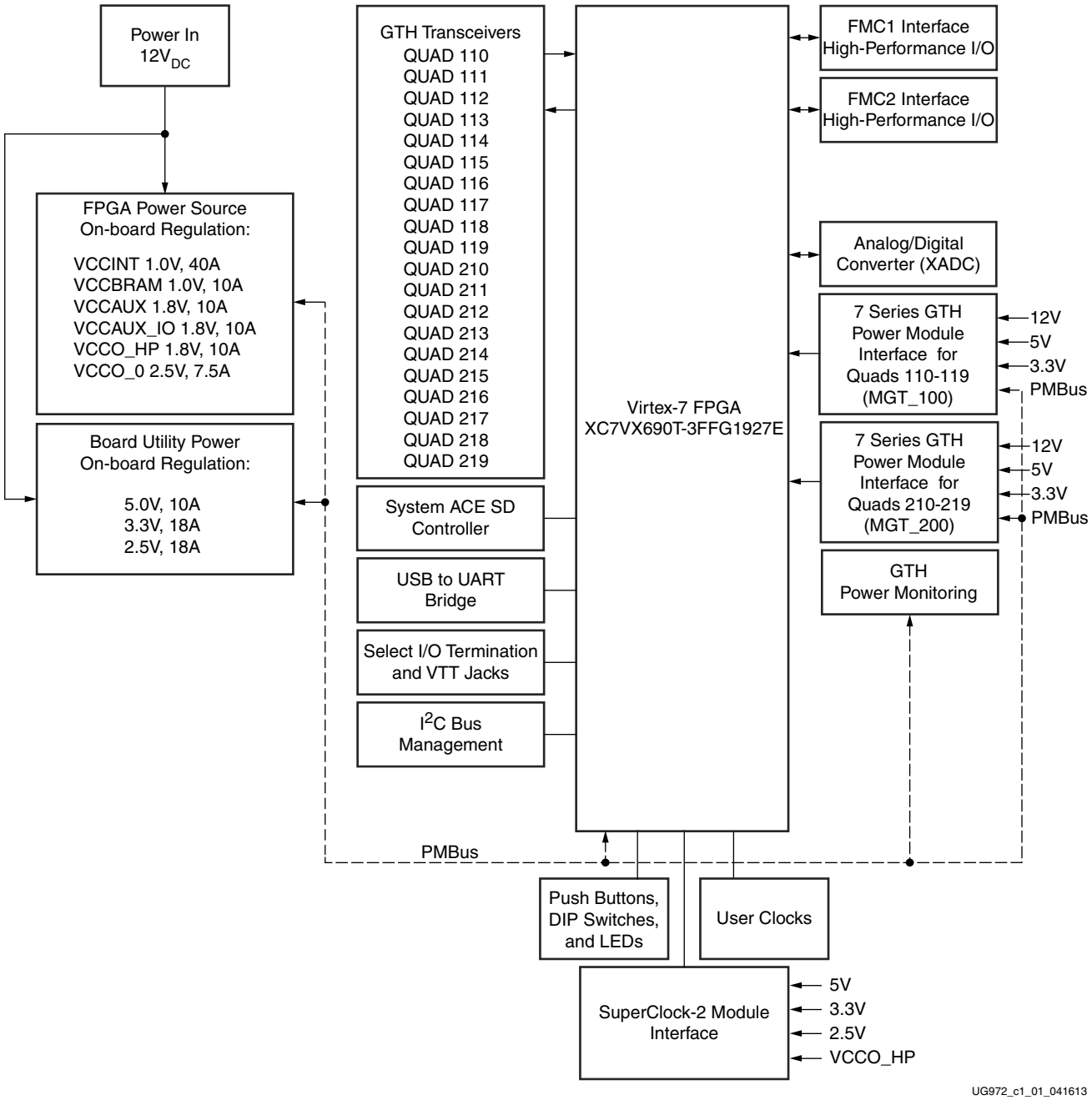

Figure 1-1: **VC7215 Board Block Diagram**

Detailed Description

Figure 1-2 shows the VC7215 board described in this user guide. Each numbered feature that is referenced in Figure 1-2 is described in Table 1-1 and the sections that follow.

Caution! The VC7215 board can be damaged by electrostatic discharge (ESD). Follow standard ESD prevention measures when handling the board.

Caution! Do not remove the rubber feet from the board. The feet provide clearance to prevent short circuits on the back side of the board.

Note: Figure 1-2 is for reference only and might not reflect the current revision of the board.

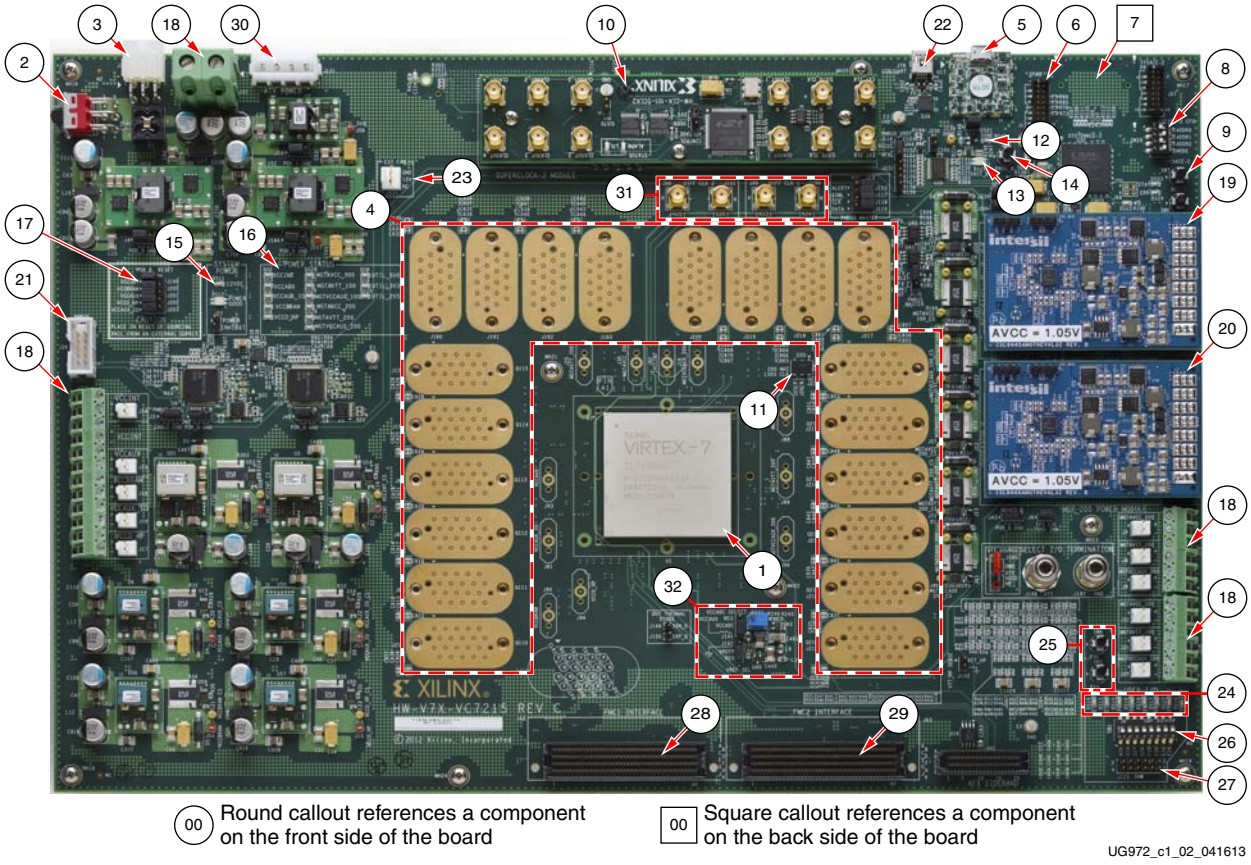

Figure 1-2: **VC7215 Board Features. Callouts Listed in Table 1-1**

Table 1-1: **VC7215 Board Feature Descriptions**

Figure 1-2 Callout	Reference Designator	Feature Description
1	U1	Virtex-7 XC7VX690T-3FFG1927E FPGA, page 15
2	SW1	Power switch, page 9
3	J2	12V Mini-Fit connector, page 9
4	J210, J84, J85, J86, J158, J159, J160, J161, J162, J163, J211, J212, J213, J214, J215, J216, J217, J218, J219, J220	GTH transceiver connector pads Q110 , Q111, Q112, Q113, Q114, Q115, Q116, Q117, Q118, Q119, Q210, Q211, Q212, Q213, Q214, Q215, Q216, Q217, Q218, Q219, page 22
5	U17	USB JTAG connector (micro-B receptacle), page 15
6	J1	JTAG connector (alternate access for programming cables), page 15
7	U30	System ACE tool SD card connector (back-side of board), page 15
8	SW28	System ACE tool SD configuration address DIP switches, page 17
9	SW7	System ACE tool SD RESET button, page 17
10		SuperClock-2 module, page 19
11	U35	200 MHz 2.5V LVDS oscillator, page 18
12	DS21	FPGA DONE status LED, page 17
13	DS25	FPGA INIT_B status LED, page 17
14	SW3	FPGA PROG_B pushbutton, page 17
15	DS11	12V power status LED, page 9
16	DS1, DS2, DS3, DS4, DS5, DS6, DS7, DS8, DS9, DS10, DS26, DS27, DS28, DS29	Status LEDS for FPGA logic, transceiver and utility power
17	J199, J200, J201, J202, J203	Power regulation jumpers for onboard regulators, page 12
18	J28, J29, J31, J32	External power supply connectors, page 9 and page 12
19		Bank 110-119 GTH transceiver power supply module (MGT_100), page 13
20		Bank 210-219 GTH transceiver power supply module (MGT_200), page 12
21	J26	PMBUS connector, page 12
22	J79	Connector for USB to UART bridge (mini-B receptacle), page 36
23	J121	Power connector for active heatsink, page 14
24	DS13, DS14, DS15, DS16, DS17, DS18, DS19, DS20	User LEDs (active-High), page 20
25	SW4, SW5	User pushbuttons (active-High), page 21
26	SW2	User DIP switches (active-High), page 21
27	J125	User I/O header, page 21
28	JA2	FMC1 connector, page 37
29	JA3	FMC2 connector page 37
30	J131	ATX power connector page 9
31	J98, J99, J100, J101	SMA connectors to differential MRCC pins on FPGA, page 18
32	J141, J142, R233	Jumpers and potentiometer for XADC reference and analog supply set-up, page 47

Power Management

Board 12V Input Power

VC7215 board receives 12V main power through J2 (callout 3, Figure 1-2) using the 12V AC adapter that is provided with the VC7215 Characterization Kit. J2 is a 6-pin (2 x 3), right angle, Mini-Fit connector.

Caution! When supplying 12V through J2, use only the power supply provided for use with this board (Xilinx® part number 3800033).

Caution! Do **NOT** use a 6-pin, PC ATX power supply connector with J2. The pinout of the 6-pin, PC ATX connector is not compatible J2 and the board will be damaged if an attempt is made to power it from a PC ATX power supply connector.

12V power can also be provided through:

- Connector J131 (callout 30, Figure 1-2) which accepts an ATX hard drive 4-pin power plug
- Connector J31 (callout 18, Figure 1-2) which can be connected to a bench-top power supply

Caution! Because connector J31 provides no reverse polarity protection, use a power supply with a current limit set at 6A max.

Caution! Do **NOT** apply 12V power to more than a single input source. For example, do not apply power to J31 and J131 at the same time.

Power Switch

Main board power is turned on or off using switch SW1 (callout 2, Figure 1-2). When the switch is in the ON position, power is applied to the board and green LED DS11 illuminates (callout 15, Figure 1-2).

Onboard Power Regulation

Figure 1-3 shows the onboard power supply architecture.

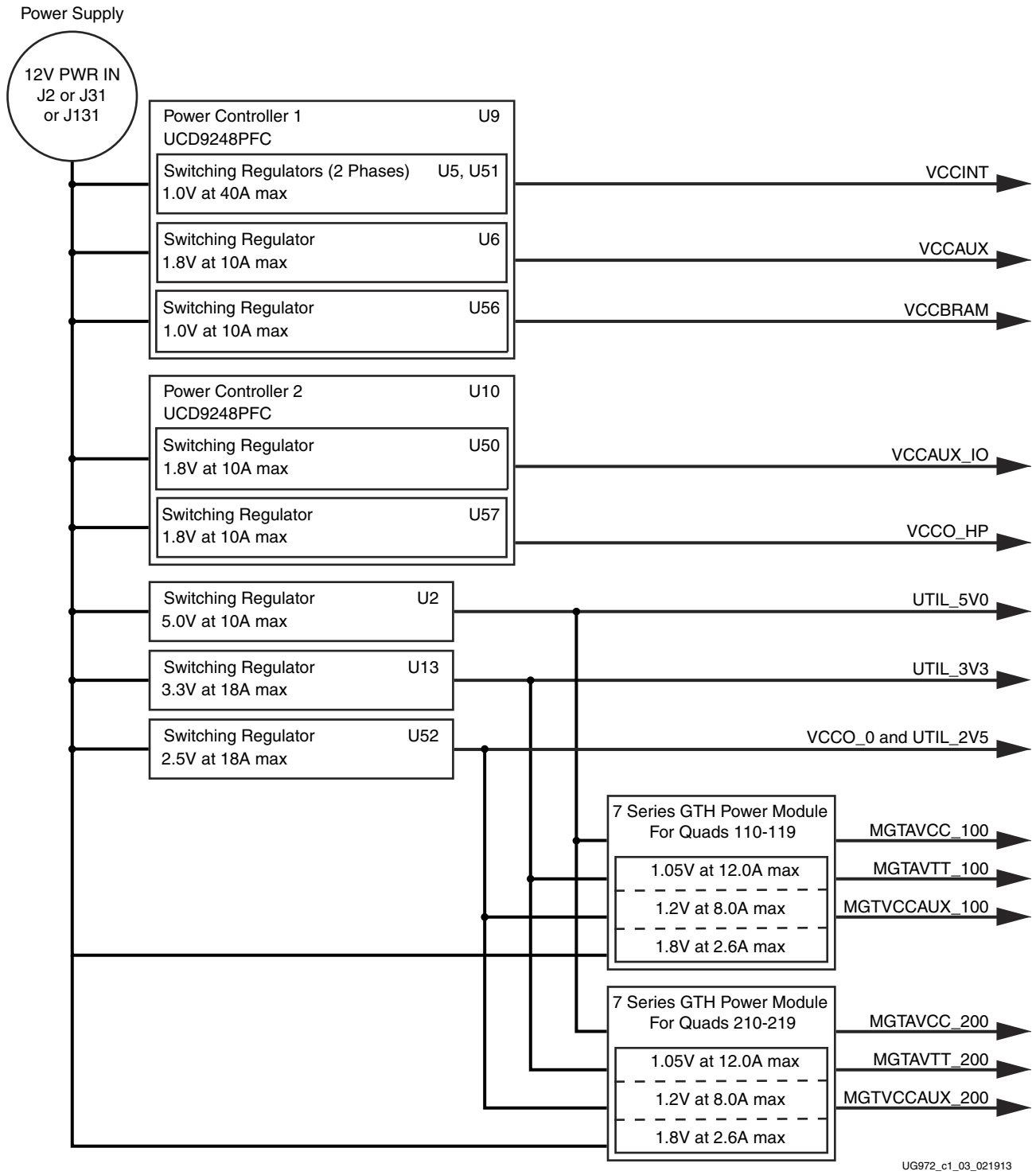

Figure 1-3: **VC7215 Board Power Supply Block Diagram**

The VC7215 board uses power regulators and PMBus compliant digital PWM system controllers from Texas Instruments to supply the FPGA logic and utility voltages listed in Table 1-2. The board can also be configured to use an external bench power supply for each voltage. See Using External Power Sources.

Table 1-2: **Onboard Power System Devices**

Device Part Number	Reference Designator(s)	Description	Power Rail Net Name	Voltage
FPGA Logic				
UCD9248PFC	U9	Digital PWM system controller, PMBUS address 52		
PTD08A020W	U5, U51	Adjustable(1) switching regulator, 40A (two phases at 20A/phase), 0.6V to 3.6V	VCCINT	1.0V
PTD08A010W	U6	Adjustable(1) switching regulator, 10A, 0.6V to 3.6V	VCCAUX	1.8V
PTD08A010W	U56	Adjustable(1) switching regulator 10A, 0.6V to 3.6V	VCCBRAM	1.0V
UCD9248PFC	U10	Digital PWM system controller, PMBUS address 53		
PTD08A010W	U50	Adjustable(1) switching regulator, 40A (two phases @ 20A/phase), 0.6V to 3.6V	VCCAUX_IO	1.8V (default)
PTD08A010W	U57	Adjustable switching regulator, 10A, 0.6V to 3.6V	VCCO_HP	1.8V
Utility				
PTH12060W	U2	Fixed switching regulator, 10A	UTIL_5V0	5.0V
PTH12020W	U13	Fixed switching regulator, 18A	UTIL_3V3	3.3V
PTH12020W	U52	Fixed switching regulator, 18A	UTIL_2V5	2.5V
GTH Transceivers (monitoring only)				
UCD9248PFC(2)	U11	Digital PWM system controller, PMBUS address 54		
UCD9248PFC(2)	U18	Digital PWM system controller, PMBUS address 55		
XADC(3)				
ADP123	U43	Adjustable LDO regulator	VCCADC_ADP	1.8V (default)
REF3012	U45	Fixed LDO regulator	VREF_3012	1.25V
System ACE Tool SD				
ADP123	U21	Fixed LDO regulator	VCC_1V2	1.2V

Notes:

1. The output voltages of regulators controlled by a UCD9248 can be reprogrammed using the Texas Instruments Fusion Digital Power Designer application (www.ti.com/tool/fusion_digital_power_designer). However, **extreme caution must be taken when attempting to modify any of the onboard regulators. An incorrectly programmed regulator can damage onboard components**.
2. The UCD9248PFC (U11) at Address 54 monitors MGTAVCC_100, MGTAVTT_100, and MGTVCCAUX_100 rail voltages and current levels and the UCD9248PFC (U18) at Address 55 monitors MGTAVCC_200, MGTAVTT_200, and MGTVCCAUX_200 rail voltages and current levels. These can be observed in real time using the Texas Instruments Fusion Digital Power Designer application (see Monitoring Voltage and Current, page 12). Transceiver supply voltages cannot be changed from this controller.
3. For information on XADC see *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 1].

Using External Power Sources

Callout 18, Figure 1-2

Each voltage rail for the FPGA logic and GTH transceivers has an associated connector (or connectors) that can be used to provide power from an external source (Table 1-3). The connectors are Euro-Mag spring-clamp terminal blocks.

Caution! Do **NOT** apply power to any of the FPGA logic power supply connectors without first disabling the associated regulator or regulators. Failing to disable the regulator can damage the board.

Each onboard FPGA Logic regulator can be disabled by using its respective Power Regulation jumper (callout 17, Figure 1-2) shown in Table 1-3. A regulator is disabled by moving its Power Regulation jumper from POR_B to RESET.

Table 1-3: **FPGA Logic and GTH Transceiver Rails**

	Power Rail Net Name	External Supply Connector(s)	Power Regulation Jumper
FPGA Logic	VCCINT	J32	J199
	VCCAUX		J201
	VCCBRAM		J200
	VCCAUX_IO		J203
	VCCO_HP		J202
GTH Transceiver	MGTAVCC_100	J28	None(1)
	MGTAVTT_100		None(1)
	MGTVCCAUX_100		None(1)
	MGTAVCC_200	J29	None(1)
	MGTAVTT_200		None(1)
	MGTVCCAUX_200		None(1)

Notes:

1. The GTH power module must be removed before providing external power to any of the transceiver rails (see 7 Series GTH Transceiver Power Module, page 13).

Default Jumper and Switch Positions

A list of jumpers and switches and their required positions for normal board operation is provided in Appendix A, Default Jumper Settings.

Monitoring Voltage and Current

Voltage and current monitoring and control are available for FPGA logic and transceiver power rails through Texas Instruments' Fusion Digital Power graphical user interface (GUI). The three onboard TI power controllers (U9 at PMBUS address 52, U10 at PMBUS address 53, U11 at PMBUS address 54, and U18 at PMBUS address 55) are wired to the same PMBus. The PMBus connector, J26 (callout 21, Figure 1-2), is provided for use with the TI USB Interface Adapter PMBus pod and associated TI GUI.

References

More information about the power system components used by the VC7215 board are available from the Texas Instruments digital power website [Ref 2].

7 Series GTH Transceiver Power Module

There are two 7 series GTH transceiver power modules (callout 19 and 20, Figure 1-2). The MGT_100 Power Module supplies the MGTAVCC_100, MGTAVTT_100, and MGTVCCAUX_100 power rails which connect to Quads 110 through 119 of the FPGA GTH transceivers. The MGT_200 Power Module supplies the MGTAVCC_200, MGTAVTT_200, and MGTVCCAUX_200 power rails which connect to Quads 210 through 219 of the FPGA GTH transceivers. Two 7 series GTH power modules from a third-party vendor are provided with the VC7215 board for evaluation. The modules can be plugged into connectors J66 and J97 or J10 and J72 in the outlined and labeled power module locations shown in Figure 1-4.

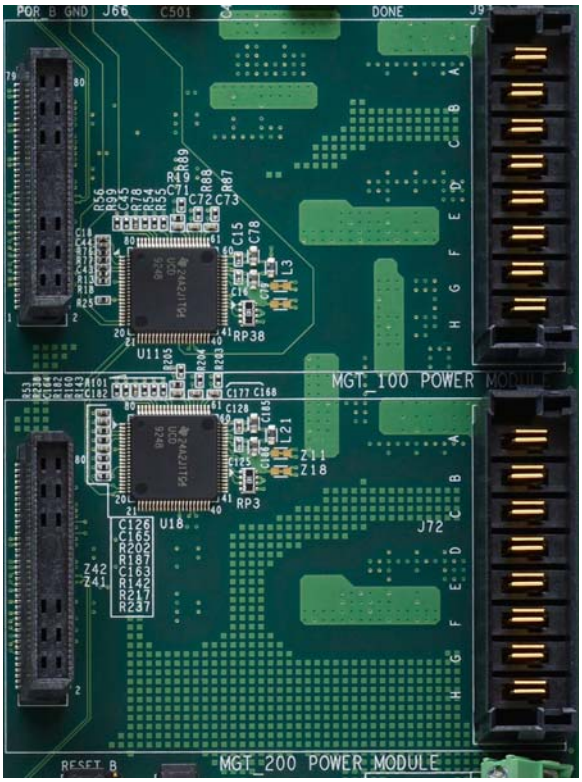

Figure 1-4: **Mounting Location, 7 Series GTH Transceiver Power Modules**

Table 1-4 lists the nominal voltage values for the MGTAVCC_100, MGTAVTT_100, MGTVCCAUX_100, MGTAVCC_200, MGTAVTT_200, and MGTVCCAUX_200 power rails. It also lists the maximum current rating for each rail supplied by 7 series GTX/GTH modules included with the VC7215 board.

Table 1-4: **7 Series GTX/GTH Transceiver Power Module**

GTH Transceiver Rail Net Name	Nominal Voltage	Maximum Current Rating
MGTAVCC_100	1.05V	12A
MGTAVTT_100	1.2V	8A
MGTVCCAUX_100	1.8V	2.6A
MGTAVCC_200	1.05V	12A
MGTAVTT_200	1.2V	8A
MGTVCCAUX_200	1.8V	2.6A

Each GTH transceiver rail comes with an associated connector that can be used to provide external power. These external supply connectors are described in Table 1-3.

Caution! The 7 series GTH module **MUST** be removed when providing external power to the GTH transceiver rails.

Information about the two 7 series GTH power supply modules included with the VC7215 Characterization Kit is available from the vendor websites [Ref 3].

Active Heatsink Power Connector

Callout 23, Figure 1-2

An active heatsink (Figure 1-5) is provided for the FPGA. A 12V fan is affixed to the heatsink and is powered from the 3-pin friction lock header J121 (Figure 1-6).

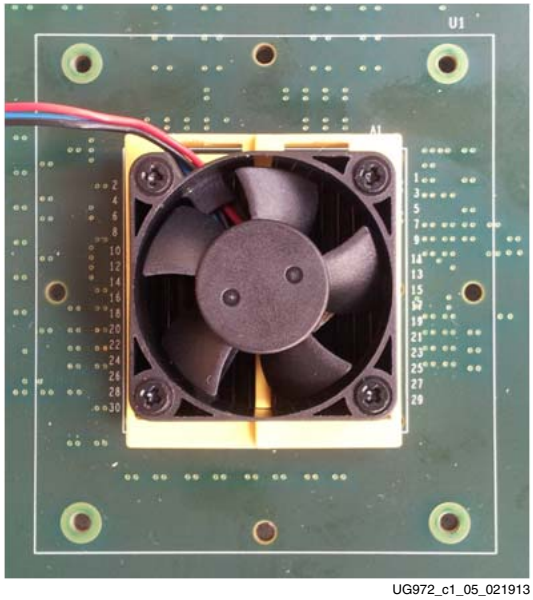

Figure 1-5: **Active FPGA Heatsink**

The fan power connections are detailed in Table 1-5:

Table 1-5: **Fan Power Connections**

Fan Wire	Header Pin
Black	J121.1 - GND
Red	J121.2 - 12V
Blue	J121.3 - NC

Figure 1-6 shows the heatsink fan power connector J121.

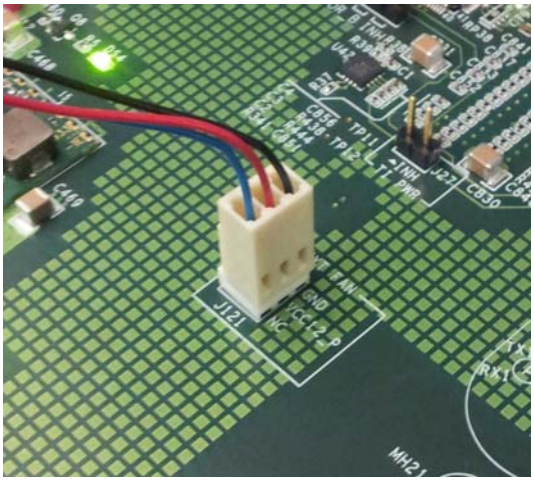

Figure 1-6: **Heatsink Fan Power Connector J121**

Virtex-7 FPGA

The VC7215 board is populated with the Virtex-7 XC7VX690T-3FFG1927E FPGA at U1 (callout 1, Figure 1-2). For further information on Virtex-7 FPGAs, see *7 Series FPGAs Overview* (DS180) [Ref 4].

FPGA Configuration

The FPGA is configured via JTAG using one of the following options:

- USB JTAG connector (callout 5, Figure 1-2)
- System ACE tool SD (callout 7, Figure 1-2)
- JTAG cable connector (callout 6, Figure 1-2)

The VC7215 board comes with an embedded USB-to-JTAG configuration module (U17) which allows a host computer to access the board JTAG chain using a Standard A to Micro-B USB cable. Alternately, the FPGA can be configured using the System ACE tool from an SD memory card installed in U30 (see System ACE Tool SD Configuration Address DIP Switches, page 17). Finally, a JTAG connector (J1) is available to provide access to the JTAG chain using one of the Xilinx configuration cables—Platform Cable USB, Platform Cable USB II or Parallel Cable IV (PCIV).

The JTAG chain of the board is illustrated in Figure 1-7. By default only the Virtex-7 FPGA and the System ACE tool SD controller are part of the chain (J5 jumper OFF). Installing the J5 jumper adds the FMC interfaces as well.

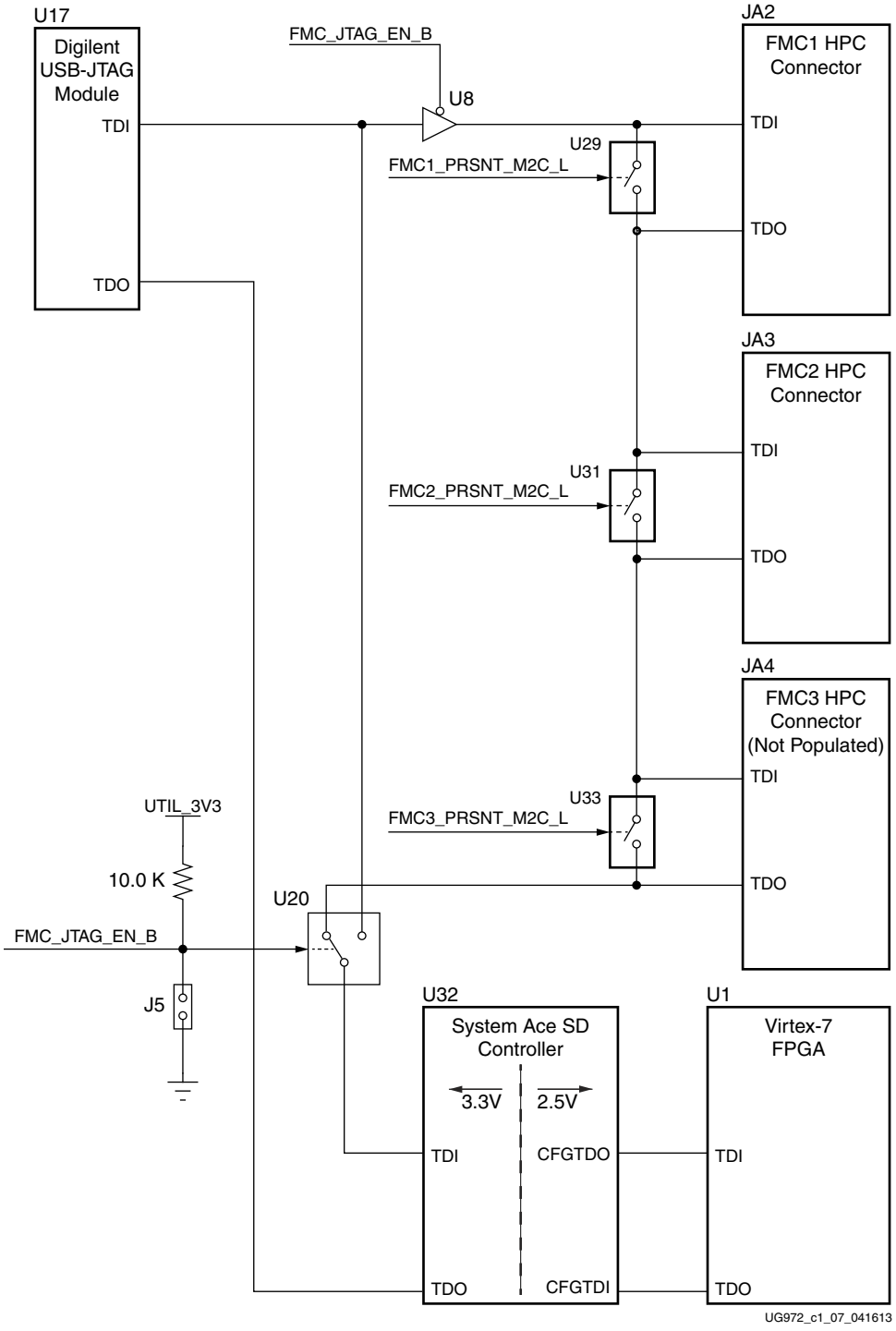

Figure 1-7: **JTAG Chain**

PROG_B Pushbutton

Pressing the PROG pushbutton SW3 (callout 14, Figure 1-2) grounds the active-Low program pin of the FPGA.

DONE LED

The DONE LED DS21 (callout 12, Figure 1-2) indicates the state of the DONE pin of the FPGA. When the DONE pin is High, DS21 lights indicating the FPGA is successfully configured.

INIT LED

The dual-color INIT LED DS25 (callout 13, Figure 1-2) indicates the FPGA's initialization status. During FPGA initialization the INIT LED illuminates RED. When FPGA initialization has completed the LED illuminates GREEN.

System ACE Tool SD Controller

The onboard System ACE tool SD controller U32 allows storage of multiple configuration files on a Secure Digital (SD) card. These configuration files can be used to program the FPGA. The SD card connects to the SD card connector U30 (callout 7, Figure 1-2) located directly below the System ACE tool SD controller on the back side of the board.

System ACE Tool SD Controller Reset

Pressing the SYSACE-2 RESET pushbutton SW7 (callout 9, Figure 1-2) resets the System ACE tool SD controller. The reset pin is an active-Low input.

System ACE Tool SD Configuration Address DIP Switches

DIP switch SW28 shown in Figure 1-8 selects one of the eight configuration bitstream addresses in the SD memory card. A switch is in the ON position if set to the far right and in the OFF position if set to the far left. The MODE bit (switch position 4) is not used and can be set either ON or OFF. SW28 is shown in Figure 1-2 as callout 8.

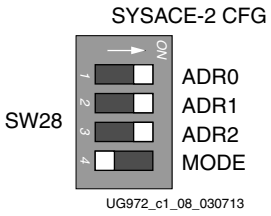

Figure 1-8: **Configuration Address DIP Switch (SW28)**

The switch settings for selecting each address are shown in Table 1-6.

Table 1-6: **SW28 DIP Switch Configuration**

Configuration Bitstream Address	ADR2	ADR1	ADR0
0	ON	ON	ON
1	ON	ON	OFF
2	ON	OFF	ON
3	ON	OFF	OFF
4	OFF	ON	ON
5	OFF	ON	OFF
6	OFF	OFF	ON
7	OFF	OFF	OFF

200 MHz 2.5V LVDS Oscillator

U35 (callout 11, Figure 1-2).

The VC7215 board has one 200 MHz 2.5V LVDS oscillator (U35) connected to multi-region clock capable (MRCC) inputs on the FPGA. Table 1-7 lists the FPGA pin connections to the LVDS oscillator.

Table 1-7: **LVDS Oscillator MRCC Connections**

FPGA (U1)				Schematic Net Name	Device (U35)		
Pin	Function	Direction	I/O Standard		Pin	Function	Direction
J25	SYSTEM CLOCK_P	Input	LVDS	LVDS_OSC_P	4	200 MHz LVDS oscillator	Output
J26	SYSTEM CLOCK_N	Input	LVDS	LVDS_OSC_N	5	201 MHz LVDS oscillator	Output

Differential SMA MRCC Pin Inputs

Callout 31, Figure 1-2.

The VC7215 board provides two pairs of differential SMA transceiver clock inputs that can be used for connecting to an external function generator. The FPGA MRCC pins are connected to the SMA connectors as shown in Table 1-8.

Table 1-8: **Differential SMA Clock Connections**

FPGA (U1)				Schematic Net Name	SMA Connector
Pin	Function	Direction	I/O Standard		
K23	USER CLOCK_1_P	Input	LVDS_25	CLK_DIFF_1_P	J99
K24	USER CLOCK_1_N	Input	LVDS_25	CLK_DIFF_1_N	J100
H20	USER CLOCK_2_P	Input	LVDS_25	CLK_DIFF_2_P	J98
G20	USER CLOCK_2_N	Input	LVDS_25	CLK_DIFF_2_N	J101

SuperClock-2 Module

Callout 10, Figure 1-2.

The SuperClock-2 module connects to the clock module interface connector (J82) and provides a programmable, low-noise and low-jitter clock source for the VC7215 board. The clock module maps to FPGA I/O by way of 24 control pins, 3 LVDS pairs, 1 regional clock pair, and 1 reset pin. Table 1-9 shows the FPGA I/O mapping for the SuperClock-2 module interface. The VC7215 board also supplies UTIL_5V0, UTIL_3V3, UTIL_2V5 and VCCO_HP input power to the clock module interface.

Table 1-9: **SuperClock-2 FPGA I/O Mapping**

FPGA (U1)				Schematic Net Name	J82 Pin		
Pin	Function	Direction	I/O Standard		Pin	Function	Direction
K12	Clock recovery	Input	LVDS_25	CM_LVDS1_P	1	Clock recovery	Output
J12	Clock recovery	Input	LVDS_25	CM_LVDS1_N	3	Clock recovery	Output
C32	Clock recovery	Input	LVDS_25	CM_LVDS2_P	9	Clock recovery	Output
C33	Clock recovery	Input	LVDS_25	CM_LVDS2_N	11	Clock recovery	Output
T33	Clock recovery	Output	LVDS	CM_LVDS3_P	17	Clock recovery	Input
R33	Clock recovery	Output	LVDS	CM_LVDS3_N	19	Clock recovery	Input
L21	Regional clock	Input	LVDS_25	CM_GCLK_P	25	Global clock	Output
K21	Regional clock	Input	LVDS_25	CM_GCLK_N	27	Global clock	Output
B21	Control I/O	In/Out	LVCMOS18	CM_CTRL_0	61	NC	-
A21	Control I/O	In/Out	LVCMOS18	CM_CTRL_1	63	NC	-
B20	Control I/O	In/Out	LVCMOS18	CM_CTRL_2	65	NC	-
A20	Control I/O	Output	LVCMOS18	CM_CTRL_3	67	DEC	Input
C22	Control I/O	Output	LVCMOS18	CM_CTRL_4	69	INC	Input
B22	Control I/O	Output	LVCMOS18	CM_CTRL_5	71	ALIGN	Input
D20	Control I/O	In/Out	LVCMOS18	CM_CTRL_6	73	NC	-
C20	Control I/O	In/Out	LVCMOS18	CM_CTRL_7	75	NC	-
D22	Control I/O	In/Out	LVCMOS18	CM_CTRL_8	77	NC	-
D21	Control I/O	In/Out	LVCMOS18	CM_CTRL_9	79	LOL	
E22	Control I/O	Output	LVCMOS18	CM_CTRL_10	81	INT_ALRM	Input
E21	Control I/O	Output	LVCMOS18	CM_CTRL_11	83	C1B	Input
G21	Control I/O	Output	LVCMOS18	CM_CTRL_12	85	C2B	Input
F21	Control I/O	Output	LVCMOS18	CM_CTRL_13	87	C3B	Input
F20	Control I/O	Output	LVCMOS18	CM_CTRL_14	89	C1A	Input
F19	Control I/O	Output	LVCMOS18	CM_CTRL_15	91	C2A	Input
H22	Control I/O	In/Out	LVCMOS18	CM_CTRL_16	93	NC	-

Table 1-9: **SuperClock-2 FPGA I/O Mapping *(Cont'd)***

FPGA (U1)				Schematic Net Name	J82 Pin		
Pin	Function	Direction	I/O Standard		Pin	Function	Direction
G22	Control I/O	Output	LVCMOS18	CM_CTRL_17	95	CS0_C3A	Input
J19	Control I/O	Output	LVCMOS18	CM_CTRL_18	97	CS1_C4A	Input
H19	Control I/O	In/Out	LVCMOS18	CM_CTRL_19	99	NC	-
L19	Control I/O	In/Out	LVCMOS18	CM_CTRL_20	101	NC	-
K19	Control I/O	In/Out	LVCMOS18	CM_CTRL_21	103	NC	-
M20	Control I/O	In/Out	LVCMOS18	CM_CTRL_22	105	NC	-
L20	Control I/O	In/Out	LVCMOS18	CM_CTRL_23	107	NC	-
N20	CM_RESET	Output	LVCMOS18	CM_RST	66	RESET_B	Input

User LEDs (Active-High)

Callout 24, Figure 1-2.

DS13 through DS20 are eight active-High LEDs that are connected to user I/O pins on the FPGA as shown in Table 1-11 These LEDs can be used to indicate status or any other purpose determined by the user.

Table 1-10: **User LEDs**

FPGA (U1)				Schematic Net Name	Reference Designator
Pin	Function	Direction	I/O Standard		
T28	User LED	Output	LVCMOS18	APP_LED1	DS19
T29	User LED	Output	LVCMOS18	APP_LED2	DS20
R28	User LED	Output	LVCMOS18	APP_LED3	DS17
R29	User LED	Output	LVCMOS18	APP_LED4	DS18
U30	User LED	Output	LVCMOS18	APP_LED5	DS16
T30	User LED	Output	LVCMOS18	APP_LED6	DS15
R27	User LED	Output	LVCMOS18	APP_LED7	DS13
P27	User LED	Output	LVCMOS18	APP_LED8	DS14

User DIP Switches (Active-High) and I/O Header

Callout 26, Figure 1-2.

The DIP switch SW2 provides a set of eight active-High switches that are connected to user I/O pins on the FPGA as shown in Table 1-11. These pins can be used to set control pins or any other purpose determined by the user. Six of the eight I/Os also map to 2 x 6 test header J125 providing external access for these pins (callout 27, Figure 1-2.).

Table 1-11: **User DIP Switches**

FPGA (U1)				Schematic Net Name	SW2 DIP Switch Pin	J125 Test Header Pin
Pin	Function	Direction	I/O Standard			
A26	User switch	Input	LVCMOS18	USER_SW1	1	2
D26	User switch	Input	LVCMOS18	USER_SW2	2	4
D27	User switch	Input	LVCMOS18	USER_SW3	3	6
G28	User switch	Input	LVCMOS18	USER_SW4	4	8
F28	User switch	Input	LVCMOS18	USER_SW5	5	10
F26	User switch	Input	LVCMOS18	USER_SW6	6	12
E26	User switch	Input	LVCMOS18	USER_SW7	7	-
F29	User switch	Input	LVCMOS18	USER_SW8	8	-

Figure 1-9 Shows the user test I/O connector J125 (Callout 27, Figure 1-2).

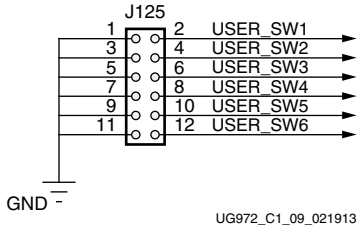

Figure 1-9: **User Test I/O**

User Pushbuttons (Active-High)

Callout 25, Figure 1-2.

SW4 and SW5 are active-High user pushbuttons that are connected to user I/O pins on the FPGA as shown in Table 1-12. These switches can be used for any purpose determined by the user.

Table 1-12: **User Pushbuttons**

FPGA (U1)				Schematic Net Name	Reference Designator
Pin	Function	Direction	I/O Standard		
P29	User pushbutton	Input	LVCMOS18	USER_PB1	SW5
P30	User pushbutton	Input	LVCMOS18	USER_PB2	SW4

GTH Transceivers and Reference Clocks

Callout 4, Figure 1-2.

The VC7215 board provides access to all GTH transceiver and reference clock pins on the FPGA as shown in Figure 1-10. The GTH transceivers are grouped into twenty sets of four RX-TX *lanes*. Four lanes are referred to as a *Quad*.

Note: Figure 1-10 is for reference only and might not reflect the current revision of the board.

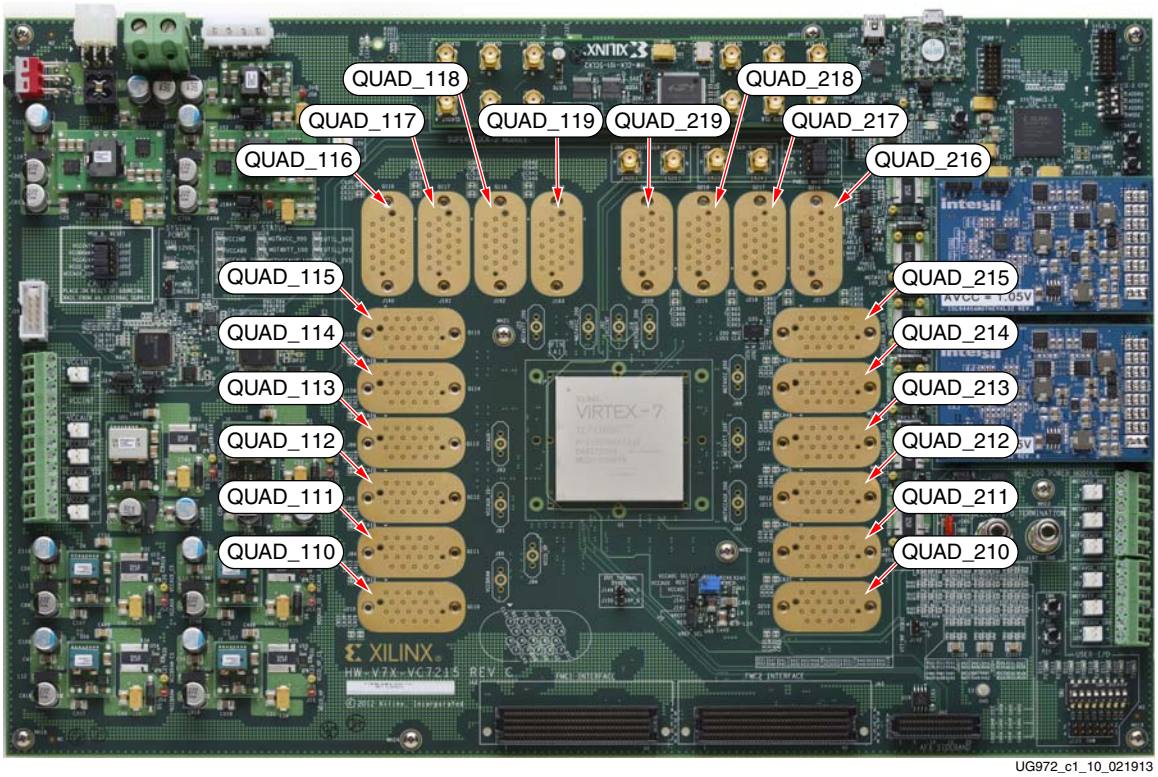

Figure 1-10: **GTH Quad Locations**

Each GTH Quad and its associated reference clocks (CLK0 and CLK1) are brought out to a connector pad which interfaces with Samtec BullsEye connectors used with the Samtec HDR-155805-01-BEYE cable assembly. Contact Samtec, Inc. for information about this or other cable assemblies. Figure 1-11 *A* shows the connector pad. Figure 1-11 *B* shows the connector pinout.

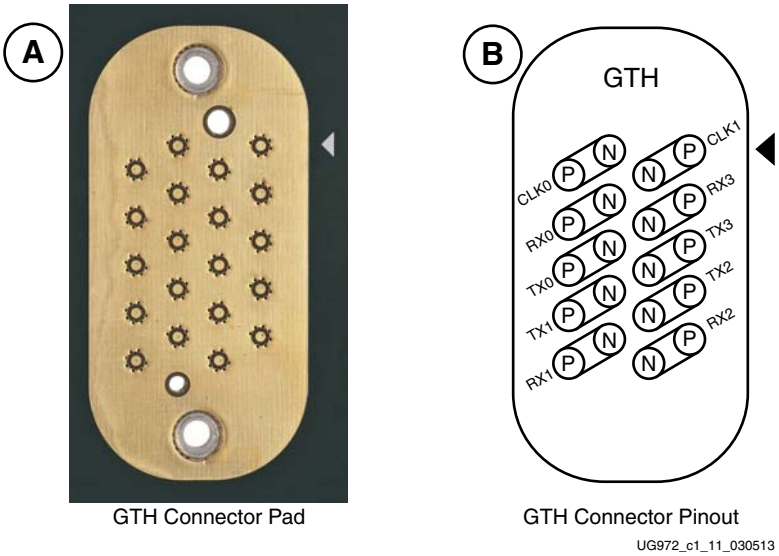

Figure 1-11: **A – GTH Connector Pad. B – GTH Connector Pinout**

Information for each GTH transceiver pin is shown in Table 1-13.

Table 1-13: **GTH Transceiver Pins**

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
BD4	110_TX0_P	110	J210	3,007.264
BD3	110_TX0_N	110	J210	3,006.803
BD8	110_RX0_P	110	J210	3,687.350
BD7	110_RX0_N	110	J210	3,686.383
BB4	110_TX1_P	110	J210	3,000.265
BB3	110_TX1_N	110	J210	2,999.405
BC6	110_RX1_P	110	J210	2,955.467
BC5	110_RX1_N	110	J210	2,954.645
BA2	110_TX2_P	110	J210	2,679.987
BA1	110_TX2_N	110	J210	2,680.900
BA6	110_RX2_P	110	J210	2,774.794
BA5	110_RX2_N	110	J210	2,775.443
AY4	110_TX3_P	110	J210	3,029.227
AY3	110_TX3_N	110	J210	3,029.367

Table 1-13: **GTH Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
AW6	110_RX3_P	110	J210	3,444.541
AW5	110_RX3_N	110	J210	3,447.802
AW2	111_TX0_P	111	J84	2,653.975
AW1	111_TX0_N	111	J84	2,657.079
AV8	111_RX0_P	111	J84	3,070.041
AV7	111_RX0_N	111	J84	3,071.014
AV4	111_TX1_P	111	J84	2,659.803
AV3	111_TX1_N	111	J84	2,659.337
AU6	111_RX1_P	111	J84	2,761.781
AU5	111_RX1_N	111	J84	2,762.547
AU2	111_TX2_P	111	J84	2,384.913
AU1	111_TX2_N	111	J84	2,385.809
AR6	111_RX2_P	111	J84	2,417.450
AR5	111_RX2_N	111	J84	2,416.883
AT4	111_TX3_P	111	J84	2,637.402
AT3	111_TX3_N	111	J84	2,637.118
AP8	111_RX3_P	111	J84	3,043.576
AP7	111_RX3_N	111	J84	3,044.249
AR2	112_TX0_P	112	J85	2,355.559
AR1	112_TX0_N	112	J85	2,355.477
AN6	112_RX0_P	112	J85	2,998.649
AN5	112_RX0_N	112	J85	2,998.656
AP4	112_TX1_P	112	J85	2,272.773
AP3	112_TX1_N	112	J85	2,273.319
AM4	112_RX1_P	112	J85	2,494.839
AM3	112_RX1_N	112	J85	2,494.185
AN2	112_TX2_P	112	J85	2,125.078
AN1	112_TX2_N	112	J85	2,124.972
AM8	112_RX2_P	112	J85	2,219.955
AM7	112_RX2_N	112	J85	2,220.921
AL2	112_TX3_P	112	J85	2,331.421
AL1	112_TX3_N	112	J85	2,331.954

Table 1-13: **GTH Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
AL6	112_RX3_P	112	J85	2,737.788
AL5	112_RX3_N	112	J85	2,737.357
AK4	113_TX0_P	113	J86	2,323.767
AK3	113_TX0_N	113	J86	2,325.420
AK8	113_RX0_P	113	J86	2,706.046
AK7	113_RX0_N	113	J86	2,706.014
AJ2	113_TX1_P	113	J86	2,114.639
AJ1	113_TX1_N	113	J86	2,112.051
AJ6	113_RX1_P	113	J86	2,090.293
AJ5	113_RX1_N	113	J86	2,091.162
AH4	113_TX2_P	113	J86	2,322.908
AH3	113_TX2_N	113	J86	2,327.099
AG6	113_RX2_P	113	J86	2,208.492
AG5	113_RX2_N	113	J86	2,209.388
AG2	113_TX3_P	113	J86	2,377.519
AG1	113_TX3_N	113	J86	2,376.455
AE6	113_RX3_P	113	J86	2,760.234
AE5	113_RX3_N	113	J86	2,759.530
AF4	114_TX0_P	114	J158	2,645.061
AF3	114_TX0_N	114	J158	2,644.809
AD8	114_RX0_P	114	J158	2,863.584
AD7	114_RX0_N	114	J158	2,864.338
AE2	114_TX1_P	114	J158	2,306.044
AE1	114_TX1_N	114	J158	2,306.417
AC6	114_RX1_P	114	J158	2,291.825
AC5	114_RX1_N	114	J158	2,291.760
AD4	114_TX2_P	114	J158	2,565.991
AD3	114_TX2_N	114	J158	2,566.865
AA6	114_RX2_P	114	J158	2,346.848
AA5	114_RX2_N	114	J158	2,345.193
AC2	114_TX3_P	114	J158	2,633.814
AC1	114_TX3_N	114	J158	2,634.574

Table 1-13: **GTH Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
Y8	114_RX3_P	114	J158	2,877.390
Y7	114_RX3_N	114	J158	2,877.820
AB4	115_TX0_P	115	J159	2,916.494
AB3	115_TX0_N	115	J159	2,917.440
W6	115_RX0_P	115	J159	3,080.958
W5	115_RX0_N	115	J159	3,081.481
AA2	115_TX1_P	115	J159	2,549.664
AA1	115_TX1_N	115	J159	2,550.337
V8	115_RX1_P	115	J159	2,589.272
V7	115_RX1_N	115	J159	2,589.696
Y4	115_TX2_P	115	J159	3,119.901
Y3	115_TX2_N	115	J159	3,120.520
U6	115_RX2_P	115	J159	2,944.000
U5	115_RX2_N	115	J159	2,943.036
W2	115_TX3_P	115	J159	3,108.232
W1	115_TX3_N	115	J159	3,109.173
T8	115_RX3_P	115	J159	3,479.067
T7	115_RX3_N	115	J159	3,479.740
V4	116_TX0_P	116	J160	4,352.459
V3	116_TX0_N	116	J160	4,352.437
R6	116_RX0_P	116	J160	4,524.963
R5	116_RX0_N	116	J160	4,525.768
U2	116_TX1_P	116	J160	4,019.195
U1	116_TX1_N	116	J160	4,018.721
P8	116_RX1_P	116	J160	4,139.923
P7	116_RX1_N	116	J160	4,140.868
T4	116_TX2_P	116	J160	3,917.183
T3	116_TX2_N	116	J160	3,917.365
N6	116_RX2_P	116	J160	3,859.511
N5	116_RX2_N	116	J160	3,859.948
R2	116_TX3_P	116	J160	3,860.137
R1	116_TX3_N	116	J160	3,860.684

Table 1-13: **GTH Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
M8	116_RX3_P	116	J160	4,351.143
M7	116_RX3_N	116	J160	4,351.778
P4	117_TX0_P	117	J161	3,626.643
P3	117_TX0_N	117	J161	3,627.185
L6	117_RX0_P	117	J161	3,985.210
L5	117_RX0_N	117	J161	3,985.666
N2	117_TX1_P	117	J161	3,281.241
N1	117_TX1_N	117	J161	3,281.932
K8	117_RX1_P	117	J161	3,553.837
K7	117_RX1_N	117	J161	3,553.205
M4	117_TX2_P	117	J161	3,285.948
M3	117_TX2_N	117	J161	3,286.416
J6	117_RX2_P	117	J161	3,067.789
J5	117_RX2_N	117	J161	3,068.071
L2	117_TX3_P	117	J161	3,227.549
L1	117_TX3_N	117	J161	3,228.364
H8	117_RX3_P	117	J161	3,527.155
H7	117_RX3_N	117	J161	3,526.272
K4	118_TX0_P	118	J162	3,033.888
K3	118_TX0_N	118	J162	3,034.436
G6	118_RX0_P	118	J162	3,214.624
G5	118_RX0_N	118	J162	3,215.185
J2	118_TX1_P	118	J162	2,778.395
J1	118_TX1_N	118	J162	2,778.076
F8	118_RX1_P	118	J162	2,703.607
F7	118_RX1_N	118	J162	2,704.210
H4	118_TX2_P	118	J162	2,637.512
H3	118_TX2_N	118	J162	2,637.907
E6	118_RX2_P	118	J162	2,427.464
E5	118_RX2_N	118	J162	2,426.598
G2	118_TX3_P	118	J162	2,738.950
G1	118_TX3_N	118	J162	2,739.384

Table 1-13: **GTH Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
D8	118_RX3_P	118	J162	2,929.867
D7	118_RX3_N	118	J162	2,929.191
F4	119_TX0_P	119	J163	2,470.952
F3	119_TX0_N	119	J163	2,470.508
D4	119_RX0_P	119	J163	2,667.345
D3	119_RX0_N	119	J163	2,667.593
E2	119_TX1_P	119	J163	2,286.863
E1	119_TX1_N	119	J163	2,287.817
C6	119_RX1_N	119	J163	2,202.572
C5	119_RX1_P	119	J163	2,202.035
C2	119_TX2_P	119	J163	2,087.486
C1	119_TX2_N	119	J163	2,087.181
B8	119_RX2_P	119	J163	1,890.517
B7	119_RX2_N	119	J163	1,887.993
B4	119_TX3_P	119	J163	2,239.094
B3	119_TX3_N	119	J163	2,238.981
A6	119_RX3_P	119	J163	2,273.639
A5	119_RX3_N	119	J163	2,272.645
BD41	210_TX0_P	210	J211	3,320.819
BD42	210_TX0_N	210	J211	3,321.813
BD37	210_RX0_P	210	J211	3,274.937
BD38	210_RX0_N	210	J211	3,270.265
BB41	210_TX1_P	210	J211	3,526.528
BB42	210_TX1_N	210	J211	3,525.716
BC39	210_RX1_N	210	J211	3,721.742
BC40	210_RX1_P	210	J211	3,723.010
BA43	210_TX2_P	210	J211	3,035.282
BA44	210_TX2_N	210	J211	3,035.158
BA39	210_RX2_P	210	J211	3,712.827
BA40	210_RX2_N	210	J211	3,713.677
AY41	210_TX3_P	210	J211	3,019.921
AY42	210_TX3_N	210	J211	3,020.473

Table 1-13: **GTH Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
AW39	210_RX3_P	210	J211	3,027.159
AW40	210_RX3_N	210	J211	3,026.511
AW43	211_TX0_P	211	J212	2,920.578
AW44	211_TX0_N	211	J212	2,921.118
AV37	211_RX0_P	211	J212	3,016.840
AV38	211_RX0_N	211	J212	3,016.977
AV41	211_TX1_P	211	J212	3,176.101
AV42	211_TX1_N	211	J212	3,175.138
AU39	211_RX1_N	211	J212	3,425.550
AU40	211_RX1_P	211	J212	3,425.690
AU43	211_TX2_P	211	J212	2,770.109
AU44	211_TX2_N	211	J212	2,770.945
AR39	211_RX2_P	211	J212	3,321.487
AR40	211_RX2_N	211	J212	3,322.217
AT41	211_TX3_P	211	J212	2,888.387
AT42	211_TX3_N	211	J212	2,887.666
AP37	211_RX3_P	211	J212	2,760.624
AP38	211_RX3_N	211	J212	2,761.338
AR43	212_TX0_P	212	J213	2,348.489
AR44	212_TX0_N	212	J213	2,349.025
AN39	212_RX0_P	212	J213	2,383.538
AN40	212_RX0_N	212	J213	2,387.815
AP41	212_TX1_P	212	J213	2,601.132
AP42	212_TX1_N	212	J213	2,601.825
AM41	212_RX1_N	212	J213	3,029.551
AM42	212_RX1_P	212	J213	3,028.152
AN43	212_TX2_P	212	J213	2,429.196
AN44	212_TX2_N	212	J213	2,428.850
AM37	212_RX2_P	212	J213	3,033.246
AM38	212_RX2_N	212	J213	3,034.206
AL43	212_TX3_P	212	J213	2,317.039
AL44	212_TX3_N	212	J213	2,316.315

Table 1-13: **GTH Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
AL39	212_RX3_P	212	J213	2,396.121
AL40	212_RX3_N	212	J213	2,396.072
AK41	213_TX0_P	213	J214	2,346.175
AK42	213_TX0_N	213	J214	2,346.990
AK37	213_RX0_P	213	J214	2,381.466
AK38	213_RX0_N	213	J214	2,381.833
AJ43	213_TX1_P	213	J214	2,432.437
AJ44	213_TX1_N	213	J214	2,432.937
AJ39	213_RX1_N	213	J214	2,739.984
AJ40	213_RX1_P	213	J214	2,736.917
AH41	213_TX2_P	213	J214	2,563.379
AH42	213_TX2_N	213	J214	2,562.817
AG39	213_RX2_P	213	J214	2,853.921
AG40	213_RX2_N	213	J214	2,853.472
AG43	213_TX3_P	213	J214	2,365.781
AG44	213_TX3_N	213	J214	2,368.019
AE39	213_RX3_P	213	J214	2,357.919
AE40	213_RX3_N	213	J214	2,358.755
AF41	214_TX0_P	214	J215	2,570.779
AF42	214_TX0_N	214	J215	2,571.422
AD37	214_RX0_P	214	J215	2,537.751
AD38	214_RX0_N	214	J215	2,537.056
AE43	214_TX1_P	214	J215	2,632.986
AE44	214_TX1_N	214	J215	2,636.508
AC39	214_RX1_N	214	J215	3,036.866
AC40	214_RX1_P	214	J215	3,035.890
AD41	214_TX2_P	214	J215	2,812.615
AD42	214_TX2_N	214	J215	2,813.316
AA39	214_RX2_P	214	J215	2,951.694
AA40	214_RX2_N	214	J215	2,951.831
AC43	214_TX3_P	214	J215	2,565.631
AC44	214_TX3_N	214	J215	2,566.536

Table 1-13: **GTH Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
Y37	214_RX3_P	214	J215	2,575.805
Y38	214_RX3_N	214	J215	2,576.762
AB41	215_TX0_P	215	J216	3,125.800
AB42	215_TX0_N	215	J216	3,126.229
W39	215_RX0_P	215	J216	2,686.530
W40	215_RX0_N	215	J216	2,685.804
AA43	215_TX1_P	215	J216	3,165.278
AA44	215_TX1_N	215	J216	3,165.568
V37	215_RX1_N	215	J216	3,532.402
V38	215_RX1_P	215	J216	3,532.608
Y41	215_TX2_P	215	J216	3,412.748
Y42	215_TX2_N	215	J216	3,413.167
U39	215_RX2_P	215	J216	3,544.758
U40	215_RX2_N	215	J216	3,544.316
W43	215_TX3_P	215	J216	3,055.687
W44	215_TX3_N	215	J216	3,056.105
T37	215_RX3_P	215	J216	3,184.724
T38	215_RX3_N	215	J216	3,185.388
V41	216_TX0_P	216	J217	4,180.552
V42	216_TX0_N	216	J217	4,179.142
R39	216_RX0_P	216	J217	3,983.357
R40	216_RX0_N	216	J217	3,982.090
U43	216_TX1_P	216	J217	4,218.664
U44	216_TX1_N	216	J217	4,218.925
P37	216_RX1_N	216	J217	4,535.540
P38	216_RX1_P	216	J217	4,535.293
T41	216_TX2_P	216	J217	4,140.552
T42	216_TX2_N	216	J217	4,140.260
N39	216_RX2_P	216	J217	4,109.444
N40	216_RX2_N	216	J217	4,110.239
R43	216_TX3_P	216	J217	3,751.163
R44	216_TX3_N	216	J217	3,751.006

Table 1-13: **GTH Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
M37	216_RX3_P	216	J217	3,681.370
M38	216_RX3_N	216	J217	3,682.014
P41	217_TX0_P	217	J218	3,550.319
P42	217_TX0_N	217	J218	3,549.440
L39	217_RX0_P	217	J218	3,138.201
L40	217_RX0_N	217	J218	3,138.950
N43	217_TX1_P	217	J218	3,411.648
N44	217_TX1_N	217	J218	3,412.097
K37	217_RX1_N	217	J218	3,666.743
K38	217_RX1_P	217	J218	3,667.504
M41	217_TX2_P	217	J218	3,439.798
M42	217_TX2_N	217	J218	3,438.997
J39	217_RX2_P	217	J218	3,364.642
J40	217_RX2_N	217	J218	3,364.211
L43	217_TX3_P	217	J218	2,999.813
L44	217_TX3_N	217	J218	2,999.225
H37	217_RX3_P	217	J218	2,995.639
H38	217_RX3_N	217	J218	3,000.180
K41	218_TX0_P	218	J219	2,860.638
K42	218_TX0_N	218	J219	2,860.658
G39	218_RX0_P	218	J219	2,599.622
G40	218_RX0_N	218	J219	2,599.510
J43	218_TX1_P	218	J219	2,901.583
J44	218_TX1_N	218	J219	2,902.251
F37	218_RX1_N	218	J219	3,121.497
F38	218_RX1_P	218	J219	3,120.545
H41	218_TX2_P	218	J219	2,723.452
H42	218_TX2_N	218	J219	2,723.199
E39	218_RX2_P	218	J219	2,809.058
E40	218_RX2_N	218	J219	2,808.229
G43	218_TX3_P	218	J219	2,437.777
G44	218_TX3_N	218	J219	2,437.587

Table 1-13: **GTH Transceiver Pins *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector	Trace Length (mils)
D37	218_RX3_P	218	J219	2,445.660
D38	218_RX3_N	218	J219	2,444.571
F41	219_TX0_P	219	J220	2,732.834
F42	219_TX0_N	219	J220	2,730.574
D41	219_RX0_P	219	J220	2,474.774
D42	219_RX0_N	219	J220	2,474.613
E43	219_TX1_P	219	J220	2,770.829
E44	219_TX1_N	219	J220	2,770.985
C39	219_RX1_N	219	J220	2,982.354
C40	219_RX1_P	219	J220	2,982.771
C43	219_TX2_P	219	J220	2,617.648
C44	219_TX2_N	219	J220	2,618.244
B37	219_RX2_P	219	J220	2,676.816
B38	219_RX2_N	219	J220	2,676.364
B41	219_TX3_P	219	J220	2,354.483
B42	219_TX3_N	219	J220	2,355.925
A39	219_RX3_P	219	J220	2,075.675
A40	219_RX3_N	219	J220	2,077.022

Information for each GTH transceiver clock input is shown in Table 1-14.

Table 1-14: **GTH Transceiver Reference Clock Inputs**

U1 FPGA Pin	Net Name	Quad	Connector
AY8	110_REFCLK0_P	110	J210
AY7	110_REFCLK0_N	110	J210
BB8	110_REFCLK1_P	110	J210
BB7	110_REFCLK1_N	110	J210
AR10	111_REFCLK0_P	111	J84
AR9	111_REFCLK0_N	111	J84
AT8	111_REFCLK1_P	111	J84
AT7	111_REFCLK1_N	111	J84
AL10	112_REFCLK0_P	112	J85
AL9	112_REFCLK0_N	112	J85
AN10	112_REFCLK1_P	112	J85

Table 1-14: **GTH Transceiver Reference Clock Inputs *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector
AN9	112_REFCLK1_N	112	J85
AF8	113_REFCLK0_P	113	J86
AF7	113_REFCLK0_N	113	J86
AH8	113_REFCLK1_P	113	J86
AH7	113_REFCLK1_N	113	J86
AA10	114_REFCLK0_P	114	J158
AA9	114_REFCLK0_N	114	J158
AB8	114_REFCLK1_P	114	J158
AB7	114_REFCLK1_N	114	J158
U10	115_REFCLK0_P	115	J159
U9	115_REFCLK0_N	115	J159
W10	115_REFCLK1_P	115	J159
W9	115_REFCLK1_N	115	J159
N10	116_REFCLK0_P	116	J160
N9	116_REFCLK0_N	116	J160
R10	116_REFCLK1_P	116	J160
R9	116_REFCLK1_N	116	J160
J10	117_REFCLK0_P	117	J161
J9	117_REFCLK0_N	117	J161
L10	117_REFCLK1_P	117	J161
L9	117_REFCLK1_N	117	J161
E10	118_REFCLK0_P	118	J162
E9	118_REFCLK0_N	118	J162
G10	118_REFCLK1_P	118	J162
G9	118_REFCLK1_N	118	J162
A10	119_REFCLK0_P	119	J163
A9	119_REFCLK0_N	119	J163
C10	119_REFCLK1_P	119	J163
C9	119_REFCLK1_N	119	J163
AY37	210_REFCLK0_P	210	J211
AY38	210_REFCLK0_N	210	J211
BB37	210_REFCLK1_P	210	J211
BB38	210_REFCLK1_N	210	J211

Table 1-14: **GTH Transceiver Reference Clock Inputs *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector
AR35	211_REFCLK0_P	211	J212
AR36	211_REFCLK0_N	211	J212
AT37	211_REFCLK1_P	211	J212
AT38	211_REFCLK1_N	211	J212
AL35	212_REFCLK0_P	212	J213
AL36	212_REFCLK0_N	212	J213
AN35	212_REFCLK1_P	212	J213
AN36	212_REFCLK1_N	212	J213
AF37	213_REFCLK0_P	213	J214
AF38	213_REFCLK0_N	213	J214
AH37	213_REFCLK1_P	213	J214
AH38	213_REFCLK1_N	213	J214
AA35	214_REFCLK0_P	214	J215
AA36	214_REFCLK0_N	214	J215
AB37	214_REFCLK1_P	214	J215
AB38	214_REFCLK1_N	214	J215
U35	215_REFCLK0_P	215	J216
U36	215_REFCLK0_N	215	J216
W35	215_REFCLK1_P	215	J216
W36	215_REFCLK1_N	215	J216
N35	216_REFCLK0_P	216	J217
N36	216_REFCLK0_N	216	J217
R35	216_REFCLK1_P	216	J217
R36	216_REFCLK1_N	216	J217
J35	217_REFCLK0_P	217	J218
J36	217_REFCLK0_N	217	J218
L35	217_REFCLK1_P	217	J218
L36	217_REFCLK1_N	217	J218
E35	218_REFCLK0_P	218	J219
E36	218_REFCLK0_N	218	J219
G35	218_REFCLK1_P	218	J219
G36	218_REFCLK1_N	218	J219
A35	219_REFCLK0_P	219	J220

Table 1-14: **GTH Transceiver Reference Clock Inputs *(Cont'd)***

U1 FPGA Pin	Net Name	Quad	Connector
A36	219_REFCLK0_N	219	J220
C35	219_REFCLK1_P	219	J220
C36	219_REFCLK1_N	219	J220

Table 1-15: **GTH Transceiver Reference Clock Inputs**

U1 FPGA Pin	Net Name	Quad	Connector
R8	115_REFCLK0_P	115	J83
R7	115_REFCLK0_N	115	J83
U8	115_REFCLK1_P	115	J83
U7	115_REFCLK1_N	115	J83
L8	116_REFCLK0_P	116	J84
L7	116_REFCLK0_N	116	J84
N8	116_REFCLK1_P	116	J84
N7	116_REFCLK1_N	116	J84
G8	117_REFCLK0_P	117	J85
G7	117_REFCLK0_N	117	J85
J8	117_REFCLK1_P	117	J85
J7	117_REFCLK1_N	117	J85
C8	118_REFCLK0_P	118	J86
C7	118_REFCLK0_N	118	J86
E8	118_REFCLK1_P	118	J86
E7	118_REFCLK1_N	118	J86

USB-to-UART Bridge

Callout 22, Figure 1-2.

A USB-to-UART bridge (U34, Silicon Laboratories CP2103) is provided for serial communication between a host computer and the FPGA over a USB cable. The USB connector on the board is a mini-B receptacle (J79) and its pinout is shown in Table 1-16.

Table 1-16: **USB Mini-B Receptacle Pin Assignments and Signals**

J79 Pin	Signal Name	Description
1	VBUS	+5V into the CP2103 USB-to-UART bridge at U34. Used to sense USB network connection.
2	USB_DATA_N	Bidirectional differential serial data (N-side).
3	USB_DATA_P	Bidirectional differential serial data (P-side).
5	GROUND	Signal ground.

The CP2103 supports an I/O voltage range of 1.8V to 3.3V. Xilinx UART IP is expected to be implemented in the FPGA fabric. The FPGA supports the USB-to-UART bridge using four signal pins:

- Transmit (TX)
- Receive (RX)
- Request to Send (RTS)
- Clear to Send (CTS)

Connections of these signals between the FPGA and the CP2103 are listed in Table 1-17.

Table 1-17: **FPGA to UART Connections**

FPGA (U1)				Schematic Net Name	Device (U34)		
Pin	Function	Direction	I/O STANDARD		Pin	Function	Direction
A25	RTS	Output	LVCMOS18	USB_CTS_I_B	22	CTS	Input
A24	CTS	Input	LVCMOS18	USB_RTS_0_B	23	RTS	Output
C24	TX	Output	LVCMOS18	USB_RXD_I	24	RXD	Input
C23	RX	Input	LVCMOS18	USB_TXD_0	25	TXD	Output

The bridge device also provides as many as 4 GPIO signals that can be defined by the user for status and control information (Table 1-18).

Table 1-18: **CP2103 USB-to-UART Bridge User GPIO**

FPGA (U1)				Schematic Net Name	Device (U34)		
Pin	Function	Direction	I/O Standard		Pin	Function	Direction
B33	SelectIO	In/Out	LVCMOS18	USB_GPIO_0	19	GPIO	In/Out
A23	SelectIO	In/Out	LVCMOS18	USB_GPIO_1	18	GPIO	In/Out
C25	SelectIO	In/Out	LVCMOS18	USB_GPIO_2	17	GPIO	In/Out
B25	SelectIO	In/Out	LVCMOS18	USB_GPIO_3	16	GPIO	In/Out

A royalty-free software driver named Virtual COM Port (VCP) is available from Silicon Laboratories. This driver permits the CP2103 USB-to-UART bridge to appear as a COM port to the host computer communications application software (for example, HyperTerminal or TeraTerm). The VCP driver must be installed on the host computer prior to establishing communications with the VC7215 board.

FPGA Mezzanine Card HPC Interface

Callout 28 and 29, Figure 1-2.

The VC7215 board features two high pin count (HPC) connectors as defined by the VITA 57.1 FPGA Mezzanine card (FMC) specification. The FMC HPC connector is a 10 x 40 position socket. See Appendix B, VITA 57.1 FMC Connector Pinouts for a cross-reference of signal names to pin coordinates.

FMC1 HPC connector JA2 provides connectivity for:

- 68 differential user defined pairs:
  - 34 LA pairs
  - 17 HA pairs
  - 17 HB pairs
- 4 differential clocks

FMC2 HPC connector JA3 provides connectivity for:

- 68 differential user defined pairs:
  - 34 LA pairs
  - 17 HA pairs
  - 17 HB pairs
- 4 differential clocks

Note: The V_{ADJ} voltage on the FMC HPC connectors tracks VCCO_HP.

The FMC HPC connectors on the VC7215 board are identified as FMC1 at JA2 and FMC2 at JA3. The connections for each of these connectors are listed in Table 1-19 and Table 1-20, page 42 respectively.

Table 1-19: **VITA 57.1 FMC1 HPC Connections at JA2**

U1 FPGA Pin	Net Name	FMC Pin
AT18	FMC1_CLK0_M2C_P	H4
AU18	FMC1_CLK0_M2C_N	H5
AU17	FMC1_CLK1_M2C_P	G2
AU16	FMC1_CLK1_M2C_N	G3
AT21	FMC1_CLK2_BIDIR_P	K4
AU21	FMC1_CLK2_BIDIR_N	K5
AT20	FMC1_CLK3_BIDIR_P	J2
AT19	FMC1_CLK3_BIDIR_N	J3
AV14	FMC1_HA00_CC_P	F4
AW14	FMC1_HA00_CC_N	F5
AW11	FMC1_HA01_CC_P	E2
AW10	FMC1_HA01_CC_N	E3
BB12	FMC1_HA02_P	K7
BC12	FMC1_HA02_N	K8
BD12	FMC1_HA03_P	J6
BD11	FMC1_HA03_N	J7
BB13	FMC1_HA04_P	F7
BC13	FMC1_HA04_N	F8
BC14	FMC1_HA05_P	E6

Table 1-19: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
BD14	FMC1_HA05_N	E7
BC10	FMC1_HA06_P	K10
BD10	FMC1_HA06_N	K11
AM15	FMC1_HA07_P	J9
AN15	FMC1_HA07_N	J10
AK18	FMC1_HA08_P	F10
AL18	FMC1_HA08_N	F11
AM17	FMC1_HA09_P	E9
AM16	FMC1_HA09_N	E10
AJ16	FMC1_HA10_P	K13
AK16	FMC1_HA10_N	K14
AL16	FMC1_HA11_P	J12
AL15	FMC1_HA11_N	J13
AJ22	FMC1_HA12_P	F13
AJ21	FMC1_HA12_N	F14
AM20	FMC1_HA13_P	E12
AN19	FMC1_HA13_N	E13
AK22	FMC1_HA14_P	J15
AK21	FMC1_HA14_N	J16
AL21	FMC1_HA15_P	F16
AL20	FMC1_HA15_N	F17
AK19	FMC1_HA16_P	E15
AL19	FMC1_HA16_N	E16
AU20	FMC1_HB00_CC_P	K25
AV19	FMC1_HB00_CC_N	K26
BB22	FMC1_HB01_P	J24
BB21	FMC1_HB01_N	J25
BC22	FMC1_HB02_P	F22
BD22	FMC1_HB02_N	F23
BC20	FMC1_HB03_P	E21
BD19	FMC1_HB03_N	E22
BD21	FMC1_HB04_P	F25
BD20	FMC1_HB04_N	F26

Table 1-19: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
BA21	FMC1_HB05_P	E24
BB20	FMC1_HB05_N	E25
AU22	FMC1_HB06_CC_P	K28
AV22	FMC1_HB06_CC_N	K29
BA20	FMC1_HB07_P	J27
BA19	FMC1_HB07_N	J28
AW22	FMC1_HB08_P	F28
AY22	FMC1_HB08_N	F29
AV20	FMC1_HB09_P	E27
AW20	FMC1_HB09_N	E28
AW21	FMC1_HB10_P	K31
AY21	FMC1_HB10_N	K32
AW19	FMC1_HB11_P	J30
AY19	FMC1_HB11_N	J31
AP21	FMC1_HB12_P	F31
AP20	FMC1_HB12_N	F32
AR22	FMC1_HB13_P	E30
AR21	FMC1_HB13_N	E31
AN20	FMC1_HB14_P	K34
AP19	FMC1_HB14_N	K35
AN22	FMC1_HB15_P	J33
AP22	FMC1_HB15_N	J34
AM22	FMC1_HB16_P	F34
AM21	FMC1_HB16_N	F35
AU13	FMC1_LA00_CC_P	G6
AV13	FMC1_LA00_CC_N	G7
AV12	FMC1_LA01_CC_P	D8
AW12	FMC1_LA01_CC_N	D9
AJ14	FMC1_LA02_P	H7
AK14	FMC1_LA02_N	H8
AM13	FMC1_LA03_P	G9
AM12	FMC1_LA03_N	G10
AK13	FMC1_LA04_P	H10

Table 1-19: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AK12	FMC1_LA04_N	H11
AN13	FMC1_LA05_P	D11
AN12	FMC1_LA05_N	D12
AL14	FMC1_LA06_P	C10
AL13	FMC1_LA06_N	C11
AN14	FMC1_LA07_P	H13
AP14	FMC1_LA07_N	H14
AR13	FMC1_LA08_P	G12
AR12	FMC1_LA08_N	G13
AU12	FMC1_LA09_P	D14
AU11	FMC1_LA09_N	D15
AT14	FMC1_LA10_P	C14
AT13	FMC1_LA10_N	C15
AU10	FMC1_LA11_P	H16
AV10	FMC1_LA11_N	H17
AY13	FMC1_LA12_P	G15
BA13	FMC1_LA12_N	G16
AY12	FMC1_LA13_P	D17
AY11	FMC1_LA13_N	D18
BA11	FMC1_LA14_P	C18
BA10	FMC1_LA14_N	C19
AY14	FMC1_LA15_P	H19
BA14	FMC1_LA15_N	H20
BB11	FMC1_LA16_P	G18
BB10	FMC1_LA16_N	G19
AU15	FMC1_LA17_CC_P	D20
AV15	FMC1_LA17_CC_N	D21
AV18	FMC1_LA18_CC_P	C22
AV17	FMC1_LA18_CC_N	C23
BA18	FMC1_LA19_P	H22
BB18	FMC1_LA19_N	H23
BC19	FMC1_LA20_P	G21
BC18	FMC1_LA20_N	G22

Table 1-19: **VITA 57.1 FMC1 HPC Connections at JA2 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
BB17	FMC1_LA21_P	H25
BC17	FMC1_LA21_N	H26
BD17	FMC1_LA22_P	G24
BD16	FMC1_LA22_N	G25
BC15	FMC1_LA23_P	D23
BD15	FMC1_LA23_N	D24
BB16	FMC1_LA24_P	H28
BB15	FMC1_LA24_N	H29
AW17	FMC1_LA25_P	G27
AY16	FMC1_LA25_N	G28
AY18	FMC1_LA26_P	D26
AY17	FMC1_LA26_N	D27
AW16	FMC1_LA27_P	C26
AW15	FMC1_LA27_N	C27
BA16	FMC1_LA28_P	H31
BA15	FMC1_LA28_N	H32
AP16	FMC1_LA29_P	G30
AR16	FMC1_LA29_N	G31
AR18	FMC1_LA30_P	H34
AR17	FMC1_LA30_N	H35
AT16	FMC1_LA31_P	G33
AT15	FMC1_LA31_N	G34
AN17	FMC1_LA32_P	H37
AP17	FMC1_LA32_N	H38
AM18	FMC1_LA33_P	G36
AN18	FMC1_LA33_N	G37
AP15	FMC1_PRSNT_M2C_L	H2

Table 1-20: **VITA 57.1 FMC2 HPC Connections at JA3**

U1 FPGA Pin	Net Name	FMC Pin
AU30	FMC2_CLK0_M2C_P	H4
AV30	FMC2_CLK0_M2C_N	H5
AU28	FMC2_CLK1_M2C_P	G2

Table 1-20: **VITA 57.1 FMC2 HPC Connections at JA3 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AV29	FMC2_CLK1_M2C_N	G3
AV32	FMC2_CLK2_BIDIR_P	K4
AW32	FMC2_CLK2_BIDIR_N	K5
AV34	FMC2_CLK3_BIDIR_P	J2
AV35	FMC2_CLK3_BIDIR_N	J3
AT23	FMC2_HA00_CC_P	F4
AU23	FMC2_HA00_CC_N	F5
AT24	FMC2_HA01_CC_P	E2
AT25	FMC2_HA01_CC_N	E3
AM25	FMC2_HA02_P	K7
AM26	FMC2_HA02_N	K8
AK23	FMC2_HA03_P	J6
AK24	FMC2_HA03_N	J7
AK26	FMC2_HA04_P	F7
AL26	FMC2_HA04_N	F8
AL24	FMC2_HA05_P	E6
AL25	FMC2_HA05_N	E7
AJ25	FMC2_HA06_P	K10
AJ26	FMC2_HA06_N	K11
AM30	FMC2_HA07_P	J9
AN30	FMC2_HA07_N	J10
AK27	FMC2_HA08_P	F10
AK28	FMC2_HA08_N	F11
AM27	FMC2_HA09_P	E9
AM28	FMC2_HA09_N	E10
AJ29	FMC2_HA10_P	K13
AK29	FMC2_HA10_N	K14
AL28	FMC2_HA11_P	J12
AL29	FMC2_HA11_N	J13
BB35	FMC2_HA12_P	F13
BC35	FMC2_HA12_N	F14
BC32	FMC2_HA13_P	E12
BC33	FMC2_HA13_N	E13

Table 1-20: **VITA 57.1 FMC2 HPC Connections at JA3 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
BB33	FMC2_HA14_P	J15
BC34	FMC2_HA14_N	J16
BD31	FMC2_HA15_P	F16
BD32	FMC2_HA15_N	F17
BD34	FMC2_HA16_P	E15
BD35	FMC2_HA16_N	E16
AU33	FMC2_HB00_CC_P	K25
AV33	FMC2_HB00_CC_N	K26
AK33	FMC2_HB01_P	J24
AL33	FMC2_HB01_N	J25
AJ30	FMC2_HB02_P	F22
AJ31	FMC2_HB02_N	F23
AK31	FMC2_HB03_P	E21
AL31	FMC2_HB03_N	E22
AJ32	FMC2_HB04_P	F25
AK32	FMC2_HB04_N	F26
AL30	FMC2_HB05_P	E24
AM31	FMC2_HB05_N	E25
AU31	FMC2_HB06_CC_P	K28
AU32	FMC2_HB06_CC_N	K29
AM32	FMC2_HB07_P	J27
AM33	FMC2_HB07_N	J28
AN32	FMC2_HB08_P	F28
AN33	FMC2_HB08_N	F29
AR33	FMC2_HB09_P	E27
AT33	FMC2_HB09_N	E28
AP31	FMC2_HB10_P	K31
AP32	FMC2_HB10_N	K32
AR31	FMC2_HB11_P	J30
AR32	FMC2_HB11_N	J31
AW34	FMC2_HB12_P	F31
AW35	FMC2_HB12_N	F32
AY33	FMC2_HB13_P	E30

Table 1-20: **VITA 57.1 FMC2 HPC Connections at JA3 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AY34	FMC2_HB13_N	E31
BA34	FMC2_HB14_P	K34
BA35	FMC2_HB14_N	K35
AY32	FMC2_HB15_P	J33
BA33	FMC2_HB15_N	J34
BB31	FMC2_HB16_P	F34
BB32	FMC2_HB16_N	F35
AU25	FMC2_LA00_CC_P	G6
AU26	FMC2_LA00_CC_N	G7
AV23	FMC2_LA01_CC_P	D8
AV24	FMC2_LA01_CC_N	D9
BD25	FMC2_LA02_P	H7
BD26	FMC2_LA02_N	H8
BB23	FMC2_LA03_P	G9
BC23	FMC2_LA03_N	G10
BB25	FMC2_LA04_P	H10
BC25	FMC2_LA04_N	H11
BC24	FMC2_LA05_P	D11
BD24	FMC2_LA05_N	D12
BA26	FMC2_LA06_P	C10
BB26	FMC2_LA06_N	C11
BA24	FMC2_LA07_P	H13
BA25	FMC2_LA07_N	H14
AW26	FMC2_LA08_P	G12
AY26	FMC2_LA08_N	G13
AY23	FMC2_LA09_P	D14
BA23	FMC2_LA09_N	D15
AV25	FMC2_LA10_P	C14
AW25	FMC2_LA10_N	C15
AW24	FMC2_LA11_P	H16
AY24	FMC2_LA11_N	H17
AN23	FMC2_LA12_P	G15
AN24	FMC2_LA12_N	G16

Table 1-20: **VITA 57.1 FMC2 HPC Connections at JA3 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AT26	FMC2_LA13_P	D17
AU27	FMC2_LA13_N	D18
AP24	FMC2_LA14_P	C18
AP25	FMC2_LA14_N	C19
AN25	FMC2_LA15_P	H19
AP26	FMC2_LA15_N	H20
AL23	FMC2_LA16_P	G18
AM23	FMC2_LA16_N	G19
AV27	FMC2_LA17_CC_P	D20
AV28	FMC2_LA17_CC_N	D21
AW30	FMC2_LA18_CC_P	C22
AW31	FMC2_LA18_CC_N	C23
BC27	FMC2_LA19_P	H22
BD27	FMC2_LA19_N	H23
BD29	FMC2_LA20_P	G21
BD30	FMC2_LA20_N	G22
BB27	FMC2_LA21_P	H25
BB28	FMC2_LA21_N	H26
BB30	FMC2_LA22_P	G24
BC30	FMC2_LA22_N	G25
BC28	FMC2_LA23_P	D23
BC29	FMC2_LA23_N	D24
BA29	FMC2_LA24_P	H28
BA30	FMC2_LA24_N	H29
AW29	FMC2_LA25_P	G27
AY29	FMC2_LA25_N	G28
AW27	FMC2_LA26_P	D26
AY27	FMC2_LA26_N	D27
AY31	FMC2_LA27_P	C26
BA31	FMC2_LA27_N	C27
AY28	FMC2_LA28_P	H31
BA28	FMC2_LA28_N	H32
AN27	FMC2_LA29_P	G30

Table 1-20: **VITA 57.1 FMC2 HPC Connections at JA3 *(Cont'd)***

U1 FPGA Pin	Net Name	FMC Pin
AP27	FMC2_LA29_N	G31
AT28	FMC2_LA30_P	H34
AT29	FMC2_LA30_N	H35
AP29	FMC2_LA31_P	G33
AP30	FMC2_LA31_N	G34
AR28	FMC2_LA32_P	H37
AR29	FMC2_LA32_N	H38
AN28	FMC2_LA33_P	G36
AN29	FMC2_LA33_N	G37
AT30	FMC2_PRSNT_M2C_L	H2

XADC

7 series FPGAs provide an analog front end (XADC) block. The XADC block includes a dual 12-bit, 1 MSPS analog-to-digital convertor (ADC) and on-chip sensors. See *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480) [Ref 1] for details on the capabilities of the analog front end.

The VC7215 board provides two options for providing power (VCCADC) to the analog circuitry in the XADC. Either option can be selected by placing a shunt in one of two positions on the 3-pin VCCADC SELECT header, J141 (callout 32, Figure 1-2):

- **Pins 1-2 (VCCAUX):** In this configuration VCCADC is provided from VCCAUX through a low pass filter network.
- **Pin 2-3 (REG):** In this configuration VCCADC is provided by an onboard regulator, U43 (Analog Devices P/N ADP123AUJZ-R7). The output voltage of the regulator VCCADC can be adjusted using the potentiometer R233.

In addition, the VC7215 board provides two options for providing the reference voltage for the analog-to-digital converter. Either option can be selected by placing a shunt in one of two positions on the 3-pin VREF SEL header J142 (callout 32, Figure 1-2):

- **Pins 1-2 (REG):** In this configuration the ADC reference voltage is provided by an onboard, low-temperature coefficient 1.25V reference, U45 (Texas Instruments P/N REF3012AIDBZT)
- **Pin 2-3 (AGND):** In this configuration the VREFP on XADC is connected to analog ground and the ADC uses an on-chip reference.

I2C Bus Management

The I2C bus is controlled through U39, an 8-channel I2C-bus multiplexer (NXP Semiconductor PCA9547). The FPGA communicates with the multiplexer through I2C data and clock signals mapped to FPGA pins J29 and K28, respectively. The I2C idcode for the PCA9547 device is `0x70`. The bus hosts six components:

- SuperClock-2 module
- 7 Series MGT_100 GTH transceiver power supply module
- 7 Series MGT_200 GTH transceiver power supply module
- FMC1
- FMC2

An I2C component can be accessed by selecting the appropriate channel through the control register of the MUX as shown in Table 1-21.

Table 1-21: **I2C Channel Assignments**

U39 Channel	I2C Component
0	SuperClock-2 module
1	7 series MGT_100 GTH transceiver power supply module
2	FMC1
3	FMC2
4	FMC3 (Connector not populated)
5	7 series MGT_200 GTH transceiver power supply module

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Appendix A

Default Jumper Settings

Table A-1 lists the jumpers that must be installed on the VC7215 board for proper operation. These jumpers must be installed except where specifically noted in this user guide.

Note: Any jumper not listed in Table A-1 should be left open for normal operation.

Table A-1: **Default Jumper Settings**

Reference Designator	Name	Board Location	Jumper	Comments
J4	UTIL_3V3	Upper Left	POR_B (1-2)	
J184	UTIL_2V5	Upper Left	POR_B (1-2)	
J24	UTIL_5V0	Upper Left	POR_B (1-2)	
J199	VCCINT	Upper Left	POR_B (1-2)	
J200	VCCBRAM	Upper Left	POR_B (1-2)	
J201	VCCAUX	Upper Left	POR_B (1-2)	
J202	VCCO_HP	Upper Left	POR_B (1-2)	
J203	VCCAUX_IO	Upper Left	POR_B (1-2)	
J3	PMBUS CTRL	Center Left	GND (2-3)	
J48	RESET_B	Upper Left	POR_B (1-2)	
J49	RESET_B	Upper Left	POR_B (1-2)	
J141	VCCADC SELECT	Lower Center	VCCAUX (1-2)	
J142	VREF SEL	Lower Center	REG (1-2)	
J195	VTT SOURCE	Lower Right	GND (1-2)	Red 20A jumper
J43	RESET_B	Center Right	POR_B (1-2)	
J6	SPI LVL TRNS INH	Center Right	Installed	
J120	PMBUS MASTER	Upper Right	AFX CABLE (1-2)	
J50	RESET_B	Upper Right	POR_B (1-2)	
J23	SPI LVL TRNS INH	Upper Right	Installed	
J116	PMBUS_VREF	Upper Right	AFX (2-3)	
J115	PMBUS MASTER ALERT	Upper Right	AFX	

Table A-1: **Default Jumper Settings *(Cont'd)***

Reference Designator	Name	Board Location	Jumper	Comments
J117	PMBUS MASTER CTRL	Upper Right	AFX	
J118	PMBUS MASTER CLK	Upper Right	AFX	
J119	PMBUS MASTER DATA	Upper Right	AFX	

VITA 57.1 FMC Connector Pinouts

Figure B-1 provides a cross-reference of signal names to pin coordinates for the VITA 57.1 FMC HPC connector.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

UG972_aB_01_021913

Figure B-1: **FMC HPC Connector Pinout**

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Appendix C

Master Constraints File Listing

The VC7215 board master Xilinx design constraints (XDC) file template provides for designs targeting the VC7215 Virtex®-7 FPGA GTH Transceiver Characterization Board. Net names in the listed constraints correlate with net names on the VC7215 board schematic. Users must identify the appropriate pins and replace the net names below with net names in the user RTL. See *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 5] for more information.

Note: Visit the Virtex-7 FPGA VC7215 Characterization Kit website for the latest XDC file.

VC7215 Board XDC Listing

```
#FMC1
set_property PACKAGE_PIN AP15 [get_ports FMC1_PRSNT_M2C_L]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_PRSNT_M2C_L]
set_property PACKAGE_PIN AT18 [get_ports FMC1_CLK0_M2C_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK0_M2C_P]
set_property PACKAGE_PIN AU18 [get_ports FMC1_CLK0_M2C_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK0_M2C_N]
set_property PACKAGE_PIN AU17 [get_ports FMC1_CLK1_M2C_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK1_M2C_P]
set_property PACKAGE_PIN AU16 [get_ports FMC1_CLK1_M2C_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK1_M2C_N]
set_property PACKAGE_PIN AT21 [get_ports FMC1_CLK2_BIDIR_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK2_BIDIR_P]
set_property PACKAGE_PIN AU21 [get_ports FMC1_CLK2_BIDIR_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK2_BIDIR_N]
set_property PACKAGE_PIN AT20 [get_ports FMC1_CLK3_BIDIR_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK3_BIDIR_P]
set_property PACKAGE_PIN AT19 [get_ports FMC1_CLK3_BIDIR_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_CLK3_BIDIR_N]
#FMC1 LA
set_property PACKAGE_PIN AU13 [get_ports FMC1_LA00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA00_CC_P]
set_property PACKAGE_PIN AV13 [get_ports FMC1_LA00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA00_CC_N]
set_property PACKAGE_PIN AV12 [get_ports FMC1_LA01_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA01_CC_P]
set_property PACKAGE_PIN AW12 [get_ports FMC1_LA01_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA01_CC_N]
set_property PACKAGE_PIN AJ14 [get_ports FMC1_LA02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA02_P]
set_property PACKAGE_PIN AK14 [get_ports FMC1_LA02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA02_N]
set_property PACKAGE_PIN AM13 [get_ports FMC1_LA03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA03_P]
```

```
set_property PACKAGE_PIN AM12 [get_ports FMC1_LA03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA03_N]
set_property PACKAGE_PIN AK13 [get_ports FMC1_LA04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA04_P]
set_property PACKAGE_PIN AK12 [get_ports FMC1_LA04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA04_N]
set_property PACKAGE_PIN AN13 [get_ports FMC1_LA05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA05_P]
set_property PACKAGE_PIN AN12 [get_ports FMC1_LA05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA05_N]
set_property PACKAGE_PIN AL14 [get_ports FMC1_LA06_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA06_P]
set_property PACKAGE_PIN AL13 [get_ports FMC1_LA06_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA06_N]
set_property PACKAGE_PIN AN14 [get_ports FMC1_LA07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA07_P]
set_property PACKAGE_PIN AP14 [get_ports FMC1_LA07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA07_N]
set_property PACKAGE_PIN AR13 [get_ports FMC1_LA08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA08_P]
set_property PACKAGE_PIN AR12 [get_ports FMC1_LA08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA08_N]
set_property PACKAGE_PIN AU12 [get_ports FMC1_LA09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA09_P]
set_property PACKAGE_PIN AU11 [get_ports FMC1_LA09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA09_N]
set_property PACKAGE_PIN AT14 [get_ports FMC1_LA10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA10_P]
set_property PACKAGE_PIN AT13 [get_ports FMC1_LA10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA10_N]
set_property PACKAGE_PIN AU10 [get_ports FMC1_LA11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA11_P]
set_property PACKAGE_PIN AV10 [get_ports FMC1_LA11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA11_N]
set_property PACKAGE_PIN AY13 [get_ports FMC1_LA12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA12_P]
set_property PACKAGE_PIN BA13 [get_ports FMC1_LA12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA12_N]
set_property PACKAGE_PIN AY12 [get_ports FMC1_LA13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA13_P]
set_property PACKAGE_PIN AY11 [get_ports FMC1_LA13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA13_N]
set_property PACKAGE_PIN BA11 [get_ports FMC1_LA14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA14_P]
set_property PACKAGE_PIN BA10 [get_ports FMC1_LA14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA14_N]
set_property PACKAGE_PIN AY14 [get_ports FMC1_LA15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA15_P]
set_property PACKAGE_PIN BA14 [get_ports FMC1_LA15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA15_N]
set_property PACKAGE_PIN BB11 [get_ports FMC1_LA16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA16_P]
set_property PACKAGE_PIN BB10 [get_ports FMC1_LA16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA16_N]
set_property PACKAGE_PIN AU15 [get_ports FMC1_LA17_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA17_CC_P]
set_property PACKAGE_PIN AV15 [get_ports FMC1_LA17_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA17_CC_N]
set_property PACKAGE_PIN AV18 [get_ports FMC1_LA18_CC_P]
```

```
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA18_CC_P]
set_property PACKAGE_PIN AV17 [get_ports FMC1_LA18_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA18_CC_N]
set_property PACKAGE_PIN BA18 [get_ports FMC1_LA19_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA19_P]
set_property PACKAGE_PIN BB18 [get_ports FMC1_LA19_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA19_N]
set_property PACKAGE_PIN BC19 [get_ports FMC1_LA20_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA20_P]
set_property PACKAGE_PIN BC18 [get_ports FMC1_LA20_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA20_N]
set_property PACKAGE_PIN BB17 [get_ports FMC1_LA21_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA21_P]
set_property PACKAGE_PIN BC17 [get_ports FMC1_LA21_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA21_N]
set_property PACKAGE_PIN BD17 [get_ports FMC1_LA22_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA22_P]
set_property PACKAGE_PIN BD16 [get_ports FMC1_LA22_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA22_N]
set_property PACKAGE_PIN BC15 [get_ports FMC1_LA23_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA23_P]
set_property PACKAGE_PIN BD15 [get_ports FMC1_LA23_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA23_N]
set_property PACKAGE_PIN BB16 [get_ports FMC1_LA24_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA24_P]
set_property PACKAGE_PIN BB15 [get_ports FMC1_LA24_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA24_N]
set_property PACKAGE_PIN AW17 [get_ports FMC1_LA25_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA25_P]
set_property PACKAGE_PIN AY16 [get_ports FMC1_LA25_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA25_N]
set_property PACKAGE_PIN AY18 [get_ports FMC1_LA26_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA26_P]
set_property PACKAGE_PIN AY17 [get_ports FMC1_LA26_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA26_N]
set_property PACKAGE_PIN AW16 [get_ports FMC1_LA27_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA27_P]
set_property PACKAGE_PIN AW15 [get_ports FMC1_LA27_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA27_N]
set_property PACKAGE_PIN BA16 [get_ports FMC1_LA28_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA28_P]
set_property PACKAGE_PIN BA15 [get_ports FMC1_LA28_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA28_N]
set_property PACKAGE_PIN AP16 [get_ports FMC1_LA29_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA29_P]
set_property PACKAGE_PIN AR16 [get_ports FMC1_LA29_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA29_N]
set_property PACKAGE_PIN AR18 [get_ports FMC1_LA30_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA30_P]
set_property PACKAGE_PIN AR17 [get_ports FMC1_LA30_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA30_N]
set_property PACKAGE_PIN AT16 [get_ports FMC1_LA31_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA31_P]
set_property PACKAGE_PIN AT15 [get_ports FMC1_LA31_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA31_N]
set_property PACKAGE_PIN AN17 [get_ports FMC1_LA32_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA32_P]
set_property PACKAGE_PIN AP17 [get_ports FMC1_LA32_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA32_N]
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set_property PACKAGE_PIN AM18 [get_ports FMC1_LA33_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA33_P]
set_property PACKAGE_PIN AN18 [get_ports FMC1_LA33_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_LA33_N]
#FMC1 HA
set_property PACKAGE_PIN AV14 [get_ports FMC1_HA00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA00_CC_P]
set_property PACKAGE_PIN AW14 [get_ports FMC1_HA00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA00_CC_N]
set_property PACKAGE_PIN AW11 [get_ports FMC1_HA01_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA01_CC_P]
set_property PACKAGE_PIN AW10 [get_ports FMC1_HA01_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA01_CC_N]
set_property PACKAGE_PIN BB12 [get_ports FMC1_HA02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA02_P]
set_property PACKAGE_PIN BC12 [get_ports FMC1_HA02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA02_N]
set_property PACKAGE_PIN BD12 [get_ports FMC1_HA03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA03_P]
set_property PACKAGE_PIN BD11 [get_ports FMC1_HA03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA03_N]
set_property PACKAGE_PIN BB13 [get_ports FMC1_HA04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA04_P]
set_property PACKAGE_PIN BC13 [get_ports FMC1_HA04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA04_N]
set_property PACKAGE_PIN BC14 [get_ports FMC1_HA05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA05_P]
set_property PACKAGE_PIN BD14 [get_ports FMC1_HA05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA05_N]
set_property PACKAGE_PIN BC10 [get_ports FMC1_HA06_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA06_P]
set_property PACKAGE_PIN BD10 [get_ports FMC1_HA06_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA06_N]
set_property PACKAGE_PIN AM15 [get_ports FMC1_HA07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA07_P]
set_property PACKAGE_PIN AN15 [get_ports FMC1_HA07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA07_N]
set_property PACKAGE_PIN AK18 [get_ports FMC1_HA08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA08_P]
set_property PACKAGE_PIN AL18 [get_ports FMC1_HA08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA08_N]
set_property PACKAGE_PIN AM17 [get_ports FMC1_HA09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA09_P]
set_property PACKAGE_PIN AM16 [get_ports FMC1_HA09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA09_N]
set_property PACKAGE_PIN AJ16 [get_ports FMC1_HA10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA10_P]
set_property PACKAGE_PIN AK16 [get_ports FMC1_HA10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA10_N]
set_property PACKAGE_PIN AL16 [get_ports FMC1_HA11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA11_P]
set_property PACKAGE_PIN AL15 [get_ports FMC1_HA11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA11_N]
set_property PACKAGE_PIN AJ22 [get_ports FMC1_HA12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA12_P]
set_property PACKAGE_PIN AJ21 [get_ports FMC1_HA12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA12_N]
set_property PACKAGE_PIN AM20 [get_ports FMC1_HA13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA13_P]
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set_property PACKAGE_PIN AN19 [get_ports FMC1_HA13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA13_N]
set_property PACKAGE_PIN AK22 [get_ports FMC1_HA14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA14_P]
set_property PACKAGE_PIN AK21 [get_ports FMC1_HA14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA14_N]
set_property PACKAGE_PIN AL21 [get_ports FMC1_HA15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA15_P]
set_property PACKAGE_PIN AL20 [get_ports FMC1_HA15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA15_N]
set_property PACKAGE_PIN AK19 [get_ports FMC1_HA16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA16_P]
set_property PACKAGE_PIN AL19 [get_ports FMC1_HA16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HA16_N]
#FMC1 HB
set_property PACKAGE_PIN AU20 [get_ports FMC1_HB00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB00_CC_P]
set_property PACKAGE_PIN AV19 [get_ports FMC1_HB00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB00_CC_N]
set_property PACKAGE_PIN BB22 [get_ports FMC1_HB01_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB01_P]
set_property PACKAGE_PIN BB21 [get_ports FMC1_HB01_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB01_N]
set_property PACKAGE_PIN BC22 [get_ports FMC1_HB02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB02_P]
set_property PACKAGE_PIN BD22 [get_ports FMC1_HB02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB02_N]
set_property PACKAGE_PIN BC20 [get_ports FMC1_HB03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB03_P]
set_property PACKAGE_PIN BD19 [get_ports FMC1_HB03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB03_N]
set_property PACKAGE_PIN BD21 [get_ports FMC1_HB04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB04_P]
set_property PACKAGE_PIN BD20 [get_ports FMC1_HB04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB04_N]
set_property PACKAGE_PIN BA21 [get_ports FMC1_HB05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB05_P]
set_property PACKAGE_PIN BB20 [get_ports FMC1_HB05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB05_N]
set_property PACKAGE_PIN AU22 [get_ports FMC1_HB06_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB06_CC_P]
set_property PACKAGE_PIN AV22 [get_ports FMC1_HB06_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB06_CC_N]
set_property PACKAGE_PIN BA20 [get_ports FMC1_HB07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB07_P]
set_property PACKAGE_PIN BA19 [get_ports FMC1_HB07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB07_N]
set_property PACKAGE_PIN AW22 [get_ports FMC1_HB08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB08_P]
set_property PACKAGE_PIN AY22 [get_ports FMC1_HB08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB08_N]
set_property PACKAGE_PIN AV20 [get_ports FMC1_HB09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB09_P]
set_property PACKAGE_PIN AW20 [get_ports FMC1_HB09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB09_N]
set_property PACKAGE_PIN AW21 [get_ports FMC1_HB10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB10_P]
set_property PACKAGE_PIN AY21 [get_ports FMC1_HB10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB10_N]
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set_property PACKAGE_PIN AW19 [get_ports FMC1_HB11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB11_P]
set_property PACKAGE_PIN AY19 [get_ports FMC1_HB11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB11_N]
set_property PACKAGE_PIN AP21 [get_ports FMC1_HB12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB12_P]
set_property PACKAGE_PIN AP20 [get_ports FMC1_HB12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB12_N]
set_property PACKAGE_PIN AR22 [get_ports FMC1_HB13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB13_P]
set_property PACKAGE_PIN AR21 [get_ports FMC1_HB13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB13_N]
set_property PACKAGE_PIN AN20 [get_ports FMC1_HB14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB14_P]
set_property PACKAGE_PIN AP19 [get_ports FMC1_HB14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB14_N]
set_property PACKAGE_PIN AN22 [get_ports FMC1_HB15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB15_P]
set_property PACKAGE_PIN AP22 [get_ports FMC1_HB15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB15_N]
set_property PACKAGE_PIN AM22 [get_ports FMC1_HB16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB16_P]
set_property PACKAGE_PIN AM21 [get_ports FMC1_HB16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC1_HB16_N]
#FMC2
set_property PACKAGE_PIN AT30 [get_ports FMC2_PRSNT_M2C_L]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_PRSNT_M2C_L]
set_property PACKAGE_PIN AU30 [get_ports FMC2_CLK0_M2C_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK0_M2C_P]
set_property PACKAGE_PIN AV30 [get_ports FMC2_CLK0_M2C_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK0_M2C_N]
set_property PACKAGE_PIN AU28 [get_ports FMC2_CLK1_M2C_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK1_M2C_P]
set_property PACKAGE_PIN AV29 [get_ports FMC2_CLK1_M2C_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK1_M2C_N]
set_property PACKAGE_PIN AV32 [get_ports FMC2_CLK2_BIDIR_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK2_BIDIR_P]
set_property PACKAGE_PIN AW32 [get_ports FMC2_CLK2_BIDIR_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK2_BIDIR_N]
set_property PACKAGE_PIN AV34 [get_ports FMC2_CLK3_BIDIR_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK3_BIDIR_P]
set_property PACKAGE_PIN AV35 [get_ports FMC2_CLK3_BIDIR_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_CLK3_BIDIR_N]
#FMC2 LA
set_property PACKAGE_PIN AU25 [get_ports FMC2_LA00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA00_CC_P]
set_property PACKAGE_PIN AU26 [get_ports FMC2_LA00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA00_CC_N]
set_property PACKAGE_PIN AV23 [get_ports FMC2_LA01_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA01_CC_P]
set_property PACKAGE_PIN AV24 [get_ports FMC2_LA01_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA01_CC_N]
set_property PACKAGE_PIN BD25 [get_ports FMC2_LA02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA02_P]
set_property PACKAGE_PIN BD26 [get_ports FMC2_LA02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA02_N]
set_property PACKAGE_PIN BB23 [get_ports FMC2_LA03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA03_P]
set_property PACKAGE_PIN BC23 [get_ports FMC2_LA03_N]
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set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA03_N]
set_property PACKAGE_PIN BB25 [get_ports FMC2_LA04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA04_P]
set_property PACKAGE_PIN BC25 [get_ports FMC2_LA04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA04_N]
set_property PACKAGE_PIN BC24 [get_ports FMC2_LA05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA05_P]
set_property PACKAGE_PIN BD24 [get_ports FMC2_LA05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA05_N]
set_property PACKAGE_PIN BA26 [get_ports FMC2_LA06_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA06_P]
set_property PACKAGE_PIN BB26 [get_ports FMC2_LA06_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA06_N]
set_property PACKAGE_PIN BA24 [get_ports FMC2_LA07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA07_P]
set_property PACKAGE_PIN BA25 [get_ports FMC2_LA07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA07_N]
set_property PACKAGE_PIN AW26 [get_ports FMC2_LA08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA08_P]
set_property PACKAGE_PIN AY26 [get_ports FMC2_LA08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA08_N]
set_property PACKAGE_PIN AY23 [get_ports FMC2_LA09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA09_P]
set_property PACKAGE_PIN BA23 [get_ports FMC2_LA09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA09_N]
set_property PACKAGE_PIN AV25 [get_ports FMC2_LA10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA10_P]
set_property PACKAGE_PIN AW25 [get_ports FMC2_LA10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA10_N]
set_property PACKAGE_PIN AW24 [get_ports FMC2_LA11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA11_P]
set_property PACKAGE_PIN AY24 [get_ports FMC2_LA11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA11_N]
set_property PACKAGE_PIN AN23 [get_ports FMC2_LA12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA12_P]
set_property PACKAGE_PIN AN24 [get_ports FMC2_LA12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA12_N]
set_property PACKAGE_PIN AT26 [get_ports FMC2_LA13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA13_P]
set_property PACKAGE_PIN AU27 [get_ports FMC2_LA13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA13_N]
set_property PACKAGE_PIN AP24 [get_ports FMC2_LA14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA14_P]
set_property PACKAGE_PIN AP25 [get_ports FMC2_LA14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA14_N]
set_property PACKAGE_PIN AN25 [get_ports FMC2_LA15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA15_P]
set_property PACKAGE_PIN AP26 [get_ports FMC2_LA15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA15_N]
set_property PACKAGE_PIN AL23 [get_ports FMC2_LA16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA16_P]
set_property PACKAGE_PIN AM23 [get_ports FMC2_LA16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA16_N]
set_property PACKAGE_PIN AV27 [get_ports FMC2_LA17_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA17_CC_P]
set_property PACKAGE_PIN AV28 [get_ports FMC2_LA17_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA17_CC_N]
set_property PACKAGE_PIN AW30 [get_ports FMC2_LA18_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA18_CC_P]
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set_property PACKAGE_PIN AW31 [get_ports FMC2_LA18_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA18_CC_N]
set_property PACKAGE_PIN BC27 [get_ports FMC2_LA19_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA19_P]
set_property PACKAGE_PIN BD27 [get_ports FMC2_LA19_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA19_N]
set_property PACKAGE_PIN BD29 [get_ports FMC2_LA20_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA20_P]
set_property PACKAGE_PIN BD30 [get_ports FMC2_LA20_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA20_N]
set_property PACKAGE_PIN BB27 [get_ports FMC2_LA21_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA21_P]
set_property PACKAGE_PIN BB28 [get_ports FMC2_LA21_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA21_N]
set_property PACKAGE_PIN BB30 [get_ports FMC2_LA22_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA22_P]
set_property PACKAGE_PIN BC30 [get_ports FMC2_LA22_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA22_N]
set_property PACKAGE_PIN BC28 [get_ports FMC2_LA23_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA23_P]
set_property PACKAGE_PIN BC29 [get_ports FMC2_LA23_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA23_N]
set_property PACKAGE_PIN BA29 [get_ports FMC2_LA24_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA24_P]
set_property PACKAGE_PIN BA30 [get_ports FMC2_LA24_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA24_N]
set_property PACKAGE_PIN AW29 [get_ports FMC2_LA25_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA25_P]
set_property PACKAGE_PIN AY29 [get_ports FMC2_LA25_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA25_N]
set_property PACKAGE_PIN AW27 [get_ports FMC2_LA26_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA26_P]
set_property PACKAGE_PIN AY27 [get_ports FMC2_LA26_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA26_N]
set_property PACKAGE_PIN AY31 [get_ports FMC2_LA27_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA27_P]
set_property PACKAGE_PIN BA31 [get_ports FMC2_LA27_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA27_N]
set_property PACKAGE_PIN AY28 [get_ports FMC2_LA28_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA28_P]
set_property PACKAGE_PIN BA28 [get_ports FMC2_LA28_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA28_N]
set_property PACKAGE_PIN AN27 [get_ports FMC2_LA29_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA29_P]
set_property PACKAGE_PIN AP27 [get_ports FMC2_LA29_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA29_N]
set_property PACKAGE_PIN AT28 [get_ports FMC2_LA30_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA30_P]
set_property PACKAGE_PIN AT29 [get_ports FMC2_LA30_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA30_N]
set_property PACKAGE_PIN AP29 [get_ports FMC2_LA31_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA31_P]
set_property PACKAGE_PIN AP30 [get_ports FMC2_LA31_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA31_N]
set_property PACKAGE_PIN AR28 [get_ports FMC2_LA32_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA32_P]
set_property PACKAGE_PIN AR29 [get_ports FMC2_LA32_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA32_N]
set_property PACKAGE_PIN AN28 [get_ports FMC2_LA33_P]
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set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA33_P]
set_property PACKAGE_PIN AN29 [get_ports FMC2_LA33_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_LA33_N]
#FMC2 HA
set_property PACKAGE_PIN AT23 [get_ports FMC2_HA00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA00_CC_P]
set_property PACKAGE_PIN AU23 [get_ports FMC2_HA00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA00_CC_N]
set_property PACKAGE_PIN AT24 [get_ports FMC2_HA01_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA01_CC_P]
set_property PACKAGE_PIN AT25 [get_ports FMC2_HA01_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA01_CC_N]
set_property PACKAGE_PIN AM25 [get_ports FMC2_HA02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA02_P]
set_property PACKAGE_PIN AM26 [get_ports FMC2_HA02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA02_N]
set_property PACKAGE_PIN AK23 [get_ports FMC2_HA03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA03_P]
set_property PACKAGE_PIN AK24 [get_ports FMC2_HA03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA03_N]
set_property PACKAGE_PIN AK26 [get_ports FMC2_HA04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA04_P]
set_property PACKAGE_PIN AL26 [get_ports FMC2_HA04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA04_N]
set_property PACKAGE_PIN AL24 [get_ports FMC2_HA05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA05_P]
set_property PACKAGE_PIN AL25 [get_ports FMC2_HA05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA05_N]
set_property PACKAGE_PIN AJ25 [get_ports FMC2_HA06_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA06_P]
set_property PACKAGE_PIN AJ26 [get_ports FMC2_HA06_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA06_N]
set_property PACKAGE_PIN AM30 [get_ports FMC2_HA07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA07_P]
set_property PACKAGE_PIN AN30 [get_ports FMC2_HA07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA07_N]
set_property PACKAGE_PIN AK27 [get_ports FMC2_HA08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA08_P]
set_property PACKAGE_PIN AK28 [get_ports FMC2_HA08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA08_N]
set_property PACKAGE_PIN AM27 [get_ports FMC2_HA09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA09_P]
set_property PACKAGE_PIN AM28 [get_ports FMC2_HA09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA09_N]
set_property PACKAGE_PIN AJ29 [get_ports FMC2_HA10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA10_P]
set_property PACKAGE_PIN AK29 [get_ports FMC2_HA10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA10_N]
set_property PACKAGE_PIN AL28 [get_ports FMC2_HA11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA11_P]
set_property PACKAGE_PIN AL29 [get_ports FMC2_HA11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA11_N]
set_property PACKAGE_PIN BB35 [get_ports FMC2_HA12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA12_P]
set_property PACKAGE_PIN BC35 [get_ports FMC2_HA12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA12_N]
set_property PACKAGE_PIN BC32 [get_ports FMC2_HA13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA13_P]
set_property PACKAGE_PIN BC33 [get_ports FMC2_HA13_N]
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set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA13_N]
set_property PACKAGE_PIN BB33 [get_ports FMC2_HA14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA14_P]
set_property PACKAGE_PIN BC34 [get_ports FMC2_HA14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA14_N]
set_property PACKAGE_PIN BD31 [get_ports FMC2_HA15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA15_P]
set_property PACKAGE_PIN BD32 [get_ports FMC2_HA15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA15_N]
set_property PACKAGE_PIN BD34 [get_ports FMC2_HA16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA16_P]
set_property PACKAGE_PIN BD35 [get_ports FMC2_HA16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HA16_N]
#FMC2 HA
set_property PACKAGE_PIN AU33 [get_ports FMC2_HB00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB00_CC_P]
set_property PACKAGE_PIN AV33 [get_ports FMC2_HB00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB00_CC_N]
set_property PACKAGE_PIN AK33 [get_ports FMC2_HB01_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB01_P]
set_property PACKAGE_PIN AL33 [get_ports FMC2_HB01_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB01_N]
set_property PACKAGE_PIN AJ30 [get_ports FMC2_HB02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB02_P]
set_property PACKAGE_PIN AJ31 [get_ports FMC2_HB02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB02_N]
set_property PACKAGE_PIN AK31 [get_ports FMC2_HB03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB03_P]
set_property PACKAGE_PIN AL31 [get_ports FMC2_HB03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB03_N]
set_property PACKAGE_PIN AJ32 [get_ports FMC2_HB04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB04_P]
set_property PACKAGE_PIN AK32 [get_ports FMC2_HB04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB04_N]
set_property PACKAGE_PIN AL30 [get_ports FMC2_HB05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB05_P]
set_property PACKAGE_PIN AM31 [get_ports FMC2_HB05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB05_N]
set_property PACKAGE_PIN AU31 [get_ports FMC2_HB06_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB06_CC_P]
set_property PACKAGE_PIN AU32 [get_ports FMC2_HB06_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB06_CC_N]
set_property PACKAGE_PIN AM32 [get_ports FMC2_HB07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB07_P]
set_property PACKAGE_PIN AM33 [get_ports FMC2_HB07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB07_N]
set_property PACKAGE_PIN AN32 [get_ports FMC2_HB08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB08_P]
set_property PACKAGE_PIN AN33 [get_ports FMC2_HB08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB08_N]
set_property PACKAGE_PIN AR33 [get_ports FMC2_HB09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB09_P]
set_property PACKAGE_PIN AT33 [get_ports FMC2_HB09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB09_N]
set_property PACKAGE_PIN AP31 [get_ports FMC2_HB10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB10_P]
set_property PACKAGE_PIN AP32 [get_ports FMC2_HB10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB10_N]
set_property PACKAGE_PIN AR31 [get_ports FMC2_HB11_P]
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set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB11_P]
set_property PACKAGE_PIN AR32 [get_ports FMC2_HB11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB11_N]
set_property PACKAGE_PIN AW34 [get_ports FMC2_HB12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB12_P]
set_property PACKAGE_PIN AW35 [get_ports FMC2_HB12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB12_N]
set_property PACKAGE_PIN AY33 [get_ports FMC2_HB13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB13_P]
set_property PACKAGE_PIN AY34 [get_ports FMC2_HB13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB13_N]
set_property PACKAGE_PIN BA34 [get_ports FMC2_HB14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB14_P]
set_property PACKAGE_PIN BA35 [get_ports FMC2_HB14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB14_N]
set_property PACKAGE_PIN AY32 [get_ports FMC2_HB15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB15_P]
set_property PACKAGE_PIN BA33 [get_ports FMC2_HB15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB15_N]
set_property PACKAGE_PIN BB31 [get_ports FMC2_HB16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB16_P]
set_property PACKAGE_PIN BB32 [get_ports FMC2_HB16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC2_HB16_N]
#FMC3
set_property PACKAGE_PIN K18 [get_ports FMC3_PRSNT_M2C_L]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_PRSNT_M2C_L]
set_property PACKAGE_PIN K17 [get_ports FMC3_CLK0_M2C_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_CLK0_M2C_P]
set_property PACKAGE_PIN J16 [get_ports FMC3_CLK0_M2C_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_CLK0_M2C_N]
set_property PACKAGE_PIN L16 [get_ports FMC3_CLK1_M2C_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_CLK1_M2C_P]
set_property PACKAGE_PIN K16 [get_ports FMC3_CLK1_M2C_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_CLK1_M2C_N]
set_property PACKAGE_PIN H32 [get_ports FMC3_CLK2_BIDIR_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_CLK2_BIDIR_P]
set_property PACKAGE_PIN H33 [get_ports FMC3_CLK2_BIDIR_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_CLK2_BIDIR_N]
set_property PACKAGE_PIN J30 [get_ports FMC3_CLK3_BIDIR_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_CLK3_BIDIR_P]
set_property PACKAGE_PIN J31 [get_ports FMC3_CLK3_BIDIR_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_CLK3_BIDIR_N]
#FMC3 LA
set_property PACKAGE_PIN H15 [get_ports FMC3_LA00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA00_CC_P]
set_property PACKAGE_PIN H14 [get_ports FMC3_LA00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA00_CC_N]
set_property PACKAGE_PIN H13 [get_ports FMC3_LA01_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA01_CC_P]
set_property PACKAGE_PIN G13 [get_ports FMC3_LA01_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA01_CC_N]
set_property PACKAGE_PIN C15 [get_ports FMC3_LA02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA02_P]
set_property PACKAGE_PIN C14 [get_ports FMC3_LA02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA02_N]
set_property PACKAGE_PIN B15 [get_ports FMC3_LA03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA03_P]
set_property PACKAGE_PIN A15 [get_ports FMC3_LA03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA03_N]
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set_property PACKAGE_PIN B13 [get_ports FMC3_LA04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA04_P]
set_property PACKAGE_PIN B12 [get_ports FMC3_LA04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA04_N]
set_property PACKAGE_PIN A14 [get_ports FMC3_LA05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA05_P]
set_property PACKAGE_PIN A13 [get_ports FMC3_LA05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA05_N]
set_property PACKAGE_PIN C13 [get_ports FMC3_LA06_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA06_P]
set_property PACKAGE_PIN C12 [get_ports FMC3_LA06_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA06_N]
set_property PACKAGE_PIN D15 [get_ports FMC3_LA07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA07_P]
set_property PACKAGE_PIN D14 [get_ports FMC3_LA07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA07_N]
set_property PACKAGE_PIN E12 [get_ports FMC3_LA08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA08_P]
set_property PACKAGE_PIN D12 [get_ports FMC3_LA08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA08_N]
set_property PACKAGE_PIN E14 [get_ports FMC3_LA09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA09_P]
set_property PACKAGE_PIN E13 [get_ports FMC3_LA09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA09_N]
set_property PACKAGE_PIN G15 [get_ports FMC3_LA10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA10_P]
set_property PACKAGE_PIN F15 [get_ports FMC3_LA10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA10_N]
set_property PACKAGE_PIN F14 [get_ports FMC3_LA11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA11_P]
set_property PACKAGE_PIN F13 [get_ports FMC3_LA11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA11_N]
set_property PACKAGE_PIN H12 [get_ports FMC3_LA12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA12_P]
set_property PACKAGE_PIN G12 [get_ports FMC3_LA12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA12_N]
set_property PACKAGE_PIN M13 [get_ports FMC3_LA13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA13_P]
set_property PACKAGE_PIN L13 [get_ports FMC3_LA13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA13_N]
set_property PACKAGE_PIN M15 [get_ports FMC3_LA14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA14_P]
set_property PACKAGE_PIN L14 [get_ports FMC3_LA14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA14_N]
set_property PACKAGE_PIN R14 [get_ports FMC3_LA15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA15_P]
set_property PACKAGE_PIN P14 [get_ports FMC3_LA15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA15_N]
set_property PACKAGE_PIN N14 [get_ports FMC3_LA16_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA16_P]
set_property PACKAGE_PIN N13 [get_ports FMC3_LA16_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA16_N]
set_property PACKAGE_PIN H18 [get_ports FMC3_LA17_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA17_CC_P]
set_property PACKAGE_PIN G17 [get_ports FMC3_LA17_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA17_CC_N]
set_property PACKAGE_PIN J17 [get_ports FMC3_LA18_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA18_CC_P]
set_property PACKAGE_PIN H17 [get_ports FMC3_LA18_CC_N]
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set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA18_CC_N]
set_property PACKAGE_PIN C18 [get_ports FMC3_LA19_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA19_P]
set_property PACKAGE_PIN B18 [get_ports FMC3_LA19_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA19_N]
set_property PACKAGE_PIN B16 [get_ports FMC3_LA20_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA20_P]
set_property PACKAGE_PIN A16 [get_ports FMC3_LA20_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA20_N]
set_property PACKAGE_PIN D19 [get_ports FMC3_LA21_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA21_P]
set_property PACKAGE_PIN C19 [get_ports FMC3_LA21_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA21_N]
set_property PACKAGE_PIN C17 [get_ports FMC3_LA22_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA22_P]
set_property PACKAGE_PIN B17 [get_ports FMC3_LA22_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA22_N]
set_property PACKAGE_PIN A19 [get_ports FMC3_LA23_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA23_P]
set_property PACKAGE_PIN A18 [get_ports FMC3_LA23_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA23_N]
set_property PACKAGE_PIN D17 [get_ports FMC3_LA24_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA24_P]
set_property PACKAGE_PIN D16 [get_ports FMC3_LA24_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA24_N]
set_property PACKAGE_PIN E17 [get_ports FMC3_LA25_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA25_P]
set_property PACKAGE_PIN E16 [get_ports FMC3_LA25_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA25_N]
set_property PACKAGE_PIN G18 [get_ports FMC3_LA26_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA26_P]
set_property PACKAGE_PIN F18 [get_ports FMC3_LA26_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA26_N]
set_property PACKAGE_PIN G16 [get_ports FMC3_LA27_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA27_P]
set_property PACKAGE_PIN F16 [get_ports FMC3_LA27_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA27_N]
set_property PACKAGE_PIN E19 [get_ports FMC3_LA28_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA28_P]
set_property PACKAGE_PIN E18 [get_ports FMC3_LA28_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA28_N]
set_property PACKAGE_PIN P17 [get_ports FMC3_LA29_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA29_P]
set_property PACKAGE_PIN N17 [get_ports FMC3_LA29_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA29_N]
set_property PACKAGE_PIN M18 [get_ports FMC3_LA30_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA30_P]
set_property PACKAGE_PIN L18 [get_ports FMC3_LA30_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA30_N]
set_property PACKAGE_PIN P15 [get_ports FMC3_LA31_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA31_P]
set_property PACKAGE_PIN N15 [get_ports FMC3_LA31_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA31_N]
set_property PACKAGE_PIN M17 [get_ports FMC3_LA32_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA32_P]
set_property PACKAGE_PIN M16 [get_ports FMC3_LA32_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA32_N]
set_property PACKAGE_PIN T16 [get_ports FMC3_LA33_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA33_P]
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set_property PACKAGE_PIN T15 [get_ports FMC3_LA33_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_LA33_N]
#FMC2 HA
set_property PACKAGE_PIN J15 [get_ports FMC3_HA00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA00_CC_P]
set_property PACKAGE_PIN J14 [get_ports FMC3_HA00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA00_CC_N]
set_property PACKAGE_PIN K14 [get_ports FMC3_HA01_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA01_CC_P]
set_property PACKAGE_PIN K13 [get_ports FMC3_HA01_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA01_CC_N]
set_property PACKAGE_PIN T14 [get_ports FMC3_HA02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA02_P]
set_property PACKAGE_PIN R13 [get_ports FMC3_HA02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA02_N]
set_property PACKAGE_PIN N12 [get_ports FMC3_HA03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA03_P]
set_property PACKAGE_PIN M12 [get_ports FMC3_HA03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA03_N]
set_property PACKAGE_PIN U13 [get_ports FMC3_HA04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA04_P]
set_property PACKAGE_PIN T13 [get_ports FMC3_HA04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA04_N]
set_property PACKAGE_PIN R12 [get_ports FMC3_HA05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA05_P]
set_property PACKAGE_PIN P12 [get_ports FMC3_HA05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA05_N]
set_property PACKAGE_PIN R16 [get_ports FMC3_HA06_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA06_P]
set_property PACKAGE_PIN P16 [get_ports FMC3_HA06_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA06_N]
set_property PACKAGE_PIN U17 [get_ports FMC3_HA07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA07_P]
set_property PACKAGE_PIN U16 [get_ports FMC3_HA07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA07_N]
set_property PACKAGE_PIN R18 [get_ports FMC3_HA08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA08_P]
set_property PACKAGE_PIN R17 [get_ports FMC3_HA08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA08_N]
set_property PACKAGE_PIN U18 [get_ports FMC3_HA09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA09_P]
set_property PACKAGE_PIN T18 [get_ports FMC3_HA09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA09_N]
set_property PACKAGE_PIN V15 [get_ports FMC3_HA10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA10_P]
set_property PACKAGE_PIN U15 [get_ports FMC3_HA10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA10_N]
set_property PACKAGE_PIN N33 [get_ports FMC3_HA11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA11_P]
set_property PACKAGE_PIN M33 [get_ports FMC3_HA11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA11_N]
set_property PACKAGE_PIN T31 [get_ports FMC3_HA12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA12_P]
set_property PACKAGE_PIN R31 [get_ports FMC3_HA12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA12_N]
set_property PACKAGE_PIN P31 [get_ports FMC3_HA13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA13_P]
set_property PACKAGE_PIN N32 [get_ports FMC3_HA13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA13_N]
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set_property PACKAGE_PIN U32 [get_ports FMC3_HA14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA14_P]
set_property PACKAGE_PIN U33 [get_ports FMC3_HA14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HA14_N]
#FMC2 HB
set_property PACKAGE_PIN H30 [get_ports FMC3_HB00_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB00_CC_P]
set_property PACKAGE_PIN G30 [get_ports FMC3_HB00_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB00_CC_N]
set_property PACKAGE_PIN C30 [get_ports FMC3_HB01_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB01_P]
set_property PACKAGE_PIN B30 [get_ports FMC3_HB01_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB01_N]
set_property PACKAGE_PIN B33 [get_ports FMC3_HB02_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB02_P]
set_property PACKAGE_PIN A33 [get_ports FMC3_HB02_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB02_N]
set_property PACKAGE_PIN A30 [get_ports FMC3_HB03_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB03_P]
set_property PACKAGE_PIN A31 [get_ports FMC3_HB03_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB03_N]
set_property PACKAGE_PIN B31 [get_ports FMC3_HB04_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB04_P]
set_property PACKAGE_PIN B32 [get_ports FMC3_HB04_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB04_N]
set_property PACKAGE_PIN D30 [get_ports FMC3_HB05_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB05_P]
set_property PACKAGE_PIN D31 [get_ports FMC3_HB05_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB05_N]
set_property PACKAGE_PIN G31 [get_ports FMC3_HB06_CC_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB06_CC_P]
set_property PACKAGE_PIN G32 [get_ports FMC3_HB06_CC_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB06_CC_N]
set_property PACKAGE_PIN E31 [get_ports FMC3_HB07_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB07_P]
set_property PACKAGE_PIN D32 [get_ports FMC3_HB07_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB07_N]
set_property PACKAGE_PIN E32 [get_ports FMC3_HB08_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB08_P]
set_property PACKAGE_PIN E33 [get_ports FMC3_HB08_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB08_N]
set_property PACKAGE_PIN F30 [get_ports FMC3_HB09_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB09_P]
set_property PACKAGE_PIN F31 [get_ports FMC3_HB09_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB09_N]
set_property PACKAGE_PIN G33 [get_ports FMC3_HB10_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB10_P]
set_property PACKAGE_PIN F33 [get_ports FMC3_HB10_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB10_N]
set_property PACKAGE_PIN L31 [get_ports FMC3_HB11_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB11_P]
set_property PACKAGE_PIN K31 [get_ports FMC3_HB11_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB11_N]
set_property PACKAGE_PIN K32 [get_ports FMC3_HB12_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB12_P]
set_property PACKAGE_PIN J32 [get_ports FMC3_HB12_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB12_N]
set_property PACKAGE_PIN M31 [get_ports FMC3_HB13_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB13_P]
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set_property PACKAGE_PIN M32 [get_ports FMC3_HB13_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB13_N]
set_property PACKAGE_PIN L33 [get_ports FMC3_HB14_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB14_P]
set_property PACKAGE_PIN K33 [get_ports FMC3_HB14_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB14_N]
set_property PACKAGE_PIN R32 [get_ports FMC3_HB15_P]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB15_P]
set_property PACKAGE_PIN P32 [get_ports FMC3_HB15_N]
set_property IOSTANDARD LVCMOS18 [get_ports FMC3_HB15_N]
#SuperClock2_MODULE
set_property PACKAGE_PIN N20 [get_ports CM_RST]
set_property IOSTANDARD LVCMOS18 [get_ports CM_RST]
set_property PACKAGE_PIN B21 [get_ports CM_CTRL_0]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_0]
set_property PACKAGE_PIN A21 [get_ports CM_CTRL_1]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_1]
set_property PACKAGE_PIN B20 [get_ports CM_CTRL_2]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_2]
set_property PACKAGE_PIN A20 [get_ports CM_CTRL_3]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_3]
set_property PACKAGE_PIN C22 [get_ports CM_CTRL_4]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_4]
set_property PACKAGE_PIN B22 [get_ports CM_CTRL_5]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_5]
set_property PACKAGE_PIN D20 [get_ports CM_CTRL_6]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_6]
set_property PACKAGE_PIN C20 [get_ports CM_CTRL_7]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_7]
set_property PACKAGE_PIN D22 [get_ports CM_CTRL_8]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_8]
set_property PACKAGE_PIN D21 [get_ports CM_CTRL_9]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_9]
set_property PACKAGE_PIN E22 [get_ports CM_CTRL_10]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_10]
set_property PACKAGE_PIN E21 [get_ports CM_CTRL_11]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_11]
set_property PACKAGE_PIN G21 [get_ports CM_CTRL_12]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_12]
set_property PACKAGE_PIN F21 [get_ports CM_CTRL_13]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_13]
set_property PACKAGE_PIN F20 [get_ports CM_CTRL_14]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_14]
set_property PACKAGE_PIN F19 [get_ports CM_CTRL_15]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_15]
set_property PACKAGE_PIN H22 [get_ports CM_CTRL_16]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_16]
set_property PACKAGE_PIN G22 [get_ports CM_CTRL_17]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_17]
set_property PACKAGE_PIN J19 [get_ports CM_CTRL_18]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_18]
set_property PACKAGE_PIN H19 [get_ports CM_CTRL_19]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_19]
set_property PACKAGE_PIN L19 [get_ports CM_CTRL_20]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_20]
set_property PACKAGE_PIN K19 [get_ports CM_CTRL_21]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_21]
set_property PACKAGE_PIN M20 [get_ports CM_CTRL_22]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_22]
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set_property PACKAGE_PIN L20 [get_ports CM_CTRL_23]
set_property IOSTANDARD LVCMOS18 [get_ports CM_CTRL_23]
set_property PACKAGE_PIN K12 [get_ports CM_LVDS1_P]
set_property IOSTANDARD LVDS [get_ports CM_LVDS1_P]
set_property PACKAGE_PIN J12 [get_ports CM_LVDS1_N]
set_property IOSTANDARD LVDS [get_ports CM_LVDS1_N]
set_property PACKAGE_PIN C32 [get_ports CM_LVDS2_P]
set_property IOSTANDARD LVDS [get_ports CM_LVDS2_P]
set_property PACKAGE_PIN C33 [get_ports CM_LVDS2_N]
set_property IOSTANDARD LVDS [get_ports CM_LVDS2_N]
set_property PACKAGE_PIN T33 [get_ports CM_LVDS3_P]
set_property IOSTANDARD LVDS [get_ports CM_LVDS3_P]
set_property PACKAGE_PIN R33 [get_ports CM_LVDS3_N]
set_property IOSTANDARD LVDS [get_ports CM_LVDS3_N]
set_property PACKAGE_PIN L21 [get_ports CM_GCLK_P]
set_property IOSTANDARD LVDS [get_ports CM_GCLK_P]
set_property PACKAGE_PIN K21 [get_ports CM_GCLK_N]
set_property IOSTANDARD LVDS [get_ports CM_GCLK_N]
#SWITCHES
set_property PACKAGE_PIN A26 [get_ports USER_SW1]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW1]
set_property PACKAGE_PIN D26 [get_ports USER_SW2]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW2]
set_property PACKAGE_PIN D27 [get_ports USER_SW3]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW3]
set_property PACKAGE_PIN G28 [get_ports USER_SW4]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW4]
set_property PACKAGE_PIN F28 [get_ports USER_SW5]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW5]
set_property PACKAGE_PIN F26 [get_ports USER_SW6]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW6]
set_property PACKAGE_PIN E26 [get_ports USER_SW7]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW7]
set_property PACKAGE_PIN F29 [get_ports USER_SW8]
set_property IOSTANDARD LVCMOS18 [get_ports USER_SW8]
#BUTTONS
set_property PACKAGE_PIN P29 [get_ports USER_PB1]
set_property IOSTANDARD LVCMOS18 [get_ports USER_PB1]
set_property PACKAGE_PIN P30 [get_ports USER_PB2]
set_property IOSTANDARD LVCMOS18 [get_ports USER_PB2]
#SMAs
set_property PACKAGE_PIN K23 [get_ports CLK_DIFF_1_P]
set_property IOSTANDARD LVDS [get_ports CLK_DIFF_1_P]
set_property PACKAGE_PIN K24 [get_ports CLK_DIFF_1_N]
set_property IOSTANDARD LVDS [get_ports CLK_DIFF_1_N]
set_property PACKAGE_PIN H20 [get_ports CLK_DIFF_2_P]
set_property IOSTANDARD LVDS [get_ports CLK_DIFF_2_P]
set_property PACKAGE_PIN G20 [get_ports CLK_DIFF_2_N]
set_property IOSTANDARD LVDS [get_ports CLK_DIFF_2_N]
#SYSTEM CLOCKS
set_property PACKAGE_PIN J25 [get_ports LVDS_OSC_P]
set_property IOSTANDARD LVDS [get_ports LVDS_OSC_P]
set_property PACKAGE_PIN J26 [get_ports LVDS_OSC_N]
set_property IOSTANDARD LVDS [get_ports LVDS_OSC_N]
#LEDs
set_property PACKAGE_PIN T28 [get_ports APP_LED1]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED1]
set_property PACKAGE_PIN T29 [get_ports APP_LED2]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED2]
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set_property PACKAGE_PIN R28 [get_ports APP_LED3]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED3]
set_property PACKAGE_PIN R29 [get_ports APP_LED4]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED4]
set_property PACKAGE_PIN U30 [get_ports APP_LED5]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED5]
set_property PACKAGE_PIN T30 [get_ports APP_LED6]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED6]
set_property PACKAGE_PIN R27 [get_ports APP_LED7]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED7]
set_property PACKAGE_PIN P27 [get_ports APP_LED8]
set_property IOSTANDARD LVCMOS18 [get_ports APP_LED8]
#IIC
set_property PACKAGE_PIN K28 [get_ports DUT_I2C_SCL]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_I2C_SCL]
set_property PACKAGE_PIN J29 [get_ports DUT_I2C_SDA]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_I2C_SDA]
#PMBUS
set_property PACKAGE_PIN A28 [get_ports DUT_PMB_ALERT]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_PMB_ALERT]
set_property PACKAGE_PIN A29 [get_ports DUT_PMB_CTRL]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_PMB_CTRL]
set_property PACKAGE_PIN D29 [get_ports DUT_PMB_CLK]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_PMB_CLK]
set_property PACKAGE_PIN C29 [get_ports DUT_PMB_DATA]
set_property IOSTANDARD LVCMOS18 [get_ports DUT_PMB_DATA]
#USB_GPIOs
set_property PACKAGE_PIN B23 [get_ports USB_GPIO_0]
set_property IOSTANDARD LVCMOS18 [get_ports USB_GPIO_0]
set_property PACKAGE_PIN A23 [get_ports USB_GPIO_1]
set_property IOSTANDARD LVCMOS18 [get_ports USB_GPIO_1]
set_property PACKAGE_PIN C25 [get_ports USB_GPIO_2]
set_property IOSTANDARD LVCMOS18 [get_ports USB_GPIO_2]
set_property PACKAGE_PIN B25 [get_ports USB_GPIO_3]
set_property IOSTANDARD LVCMOS18 [get_ports USB_GPIO_3]
#UART
set_property PACKAGE_PIN C23 [get_ports USB_TXD_0]
set_property IOSTANDARD LVCMOS18 [get_ports USB_TXD_0]
set_property PACKAGE_PIN C24 [get_ports USB_RXD_I]
set_property IOSTANDARD LVCMOS18 [get_ports USB_RXD_I]
set_property PACKAGE_PIN A24 [get_ports USB_RTS_0_B]
set_property IOSTANDARD LVCMOS18 [get_ports USB_RTS_0_B]
set_property PACKAGE_PIN A25 [get_ports USB_CTS_I_B]
set_property IOSTANDARD LVCMOS18 [get_ports USB_CTS_I_B]
#SDIO
set_property PACKAGE_PIN F24 [get_ports SA2_SDHOST_D0]
set_property IOSTANDARD LVCMOS18 [get_ports SA2_SDHOST_D0]
set_property PACKAGE_PIN F25 [get_ports SA2_SDHOST_D1]
set_property IOSTANDARD LVCMOS18 [get_ports SA2_SDHOST_D1]
set_property PACKAGE_PIN H23 [get_ports SA2_SDHOST_D3]
set_property IOSTANDARD LVCMOS18 [get_ports SA2_SDHOST_D3]
set_property PACKAGE_PIN H24 [get_ports SA2_SDHOST_D2]
set_property IOSTANDARD LVCMOS18 [get_ports SA2_SDHOST_D2]
set_property PACKAGE_PIN F23 [get_ports SA2_SDHOST_CMD]
set_property IOSTANDARD LVCMOS18 [get_ports SA2_SDHOST_CMD]
set_property PACKAGE_PIN G25 [get_ports SA2_SDHOST_CLK]
set_property IOSTANDARD LVCMOS18 [get_ports SA2_SDHOST_CLK]
#MGTs
set_property PACKAGE_PIN AY8 [get_ports 110_REFCLK0_P]
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set_property PACKAGE_PIN AY7 [get_ports 110_REFCLK0_N]
set_property PACKAGE_PIN BB8 [get_ports 110_REFCLK1_P]
set_property PACKAGE_PIN BB7 [get_ports 110_REFCLK1_N]
set_property PACKAGE_PIN AY4 [get_ports 110_TX3_P]
set_property PACKAGE_PIN AY3 [get_ports 110_TX3_N]
set_property PACKAGE_PIN AW6 [get_ports 110_RX3_P]
set_property PACKAGE_PIN AW5 [get_ports 110_RX3_N]
set_property PACKAGE_PIN BA2 [get_ports 110_TX2_P]
set_property PACKAGE_PIN BA1 [get_ports 110_TX2_N]
set_property PACKAGE_PIN BA6 [get_ports 110_RX2_P]
set_property PACKAGE_PIN BA5 [get_ports 110_RX2_N]
set_property PACKAGE_PIN BB4 [get_ports 110_TX1_P]
set_property PACKAGE_PIN BB3 [get_ports 110_TX1_N]
set_property PACKAGE_PIN BC6 [get_ports 110_RX1_P]
set_property PACKAGE_PIN BC5 [get_ports 110_RX1_N]
set_property PACKAGE_PIN BD4 [get_ports 110_TX0_P]
set_property PACKAGE_PIN BD3 [get_ports 110_TX0_N]
set_property PACKAGE_PIN BD8 [get_ports 110_RX0_P]
set_property PACKAGE_PIN BD7 [get_ports 110_RX0_N]
set_property PACKAGE_PIN AR10 [get_ports 111_REFCLK0_P]
set_property PACKAGE_PIN AR9 [get_ports 111_REFCLK0_N]
set_property PACKAGE_PIN AT8 [get_ports 111_REFCLK1_P]
set_property PACKAGE_PIN AT7 [get_ports 111_REFCLK1_N]
set_property PACKAGE_PIN AT4 [get_ports 111_TX3_P]
set_property PACKAGE_PIN AT3 [get_ports 111_TX3_N]
set_property PACKAGE_PIN AP8 [get_ports 111_RX3_P]
set_property PACKAGE_PIN AP7 [get_ports 111_RX3_N]
set_property PACKAGE_PIN AU2 [get_ports 111_TX2_P]
set_property PACKAGE_PIN AU1 [get_ports 111_TX2_N]
set_property PACKAGE_PIN AR6 [get_ports 111_RX2_P]
set_property PACKAGE_PIN AR5 [get_ports 111_RX2_N]
set_property PACKAGE_PIN AV4 [get_ports 111_TX1_P]
set_property PACKAGE_PIN AV3 [get_ports 111_TX1_N]
set_property PACKAGE_PIN AU6 [get_ports 111_RX1_P]
set_property PACKAGE_PIN AU5 [get_ports 111_RX1_N]
set_property PACKAGE_PIN AW2 [get_ports 111_TX0_P]
set_property PACKAGE_PIN AW1 [get_ports 111_TX0_N]
set_property PACKAGE_PIN AV8 [get_ports 111_RX0_P]
set_property PACKAGE_PIN AV7 [get_ports 111_RX0_N]
set_property PACKAGE_PIN AL10 [get_ports 112_REFCLK0_P]
set_property PACKAGE_PIN AL9 [get_ports 112_REFCLK0_N]
set_property PACKAGE_PIN AN10 [get_ports 112_REFCLK1_P]
set_property PACKAGE_PIN AN9 [get_ports 112_REFCLK1_N]
set_property PACKAGE_PIN AL2 [get_ports 112_TX3_P]
set_property PACKAGE_PIN AL1 [get_ports 112_TX3_N]
set_property PACKAGE_PIN AL6 [get_ports 112_RX3_P]
set_property PACKAGE_PIN AL5 [get_ports 112_RX3_N]
set_property PACKAGE_PIN AN2 [get_ports 112_TX2_P]
set_property PACKAGE_PIN AN1 [get_ports 112_TX2_N]
set_property PACKAGE_PIN AM8 [get_ports 112_RX2_P]
set_property PACKAGE_PIN AM7 [get_ports 112_RX2_N]
set_property PACKAGE_PIN AP4 [get_ports 112_TX1_P]
set_property PACKAGE_PIN AP3 [get_ports 112_TX1_N]
set_property PACKAGE_PIN AM4 [get_ports 112_RX1_P]
set_property PACKAGE_PIN AM3 [get_ports 112_RX1_N]
set_property PACKAGE_PIN AR2 [get_ports 112_TX0_P]
set_property PACKAGE_PIN AR1 [get_ports 112_TX0_N]
set_property PACKAGE_PIN AN6 [get_ports 112_RX0_P]
set_property PACKAGE_PIN AN5 [get_ports 112_RX0_N]
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set_property PACKAGE_PIN AF8 [get_ports 113_REFCLK0_P]
set_property PACKAGE_PIN AF7 [get_ports 113_REFCLK0_N]
set_property PACKAGE_PIN AH8 [get_ports 113_REFCLK1_P]
set_property PACKAGE_PIN AH7 [get_ports 113_REFCLK1_N]
set_property PACKAGE_PIN AG2 [get_ports 113_TX3_P]
set_property PACKAGE_PIN AE6 [get_ports 113_RX3_P]
set_property PACKAGE_PIN AG1 [get_ports 113_TX3_N]
set_property PACKAGE_PIN AE5 [get_ports 113_RX3_N]
set_property PACKAGE_PIN AH4 [get_ports 113_TX2_P]
set_property PACKAGE_PIN AG6 [get_ports 113_RX2_P]
set_property PACKAGE_PIN AH3 [get_ports 113_TX2_N]
set_property PACKAGE_PIN AG5 [get_ports 113_RX2_N]
set_property PACKAGE_PIN AJ2 [get_ports 113_TX1_P]
set_property PACKAGE_PIN AJ6 [get_ports 113_RX1_P]
set_property PACKAGE_PIN AJ1 [get_ports 113_TX1_N]
set_property PACKAGE_PIN AJ5 [get_ports 113_RX1_N]
set_property PACKAGE_PIN AK4 [get_ports 113_TX0_P]
set_property PACKAGE_PIN AK8 [get_ports 113_RX0_P]
set_property PACKAGE_PIN AK3 [get_ports 113_TX0_N]
set_property PACKAGE_PIN AK7 [get_ports 113_RX0_N]
set_property PACKAGE_PIN AA10 [get_ports 114_REFCLK0_P]
set_property PACKAGE_PIN AA9 [get_ports 114_REFCLK0_N]
set_property PACKAGE_PIN AB8 [get_ports 114_REFCLK1_P]
set_property PACKAGE_PIN AB7 [get_ports 114_REFCLK1_N]
set_property PACKAGE_PIN AC2 [get_ports 114_TX3_P]
set_property PACKAGE_PIN AC1 [get_ports 114_TX3_N]
set_property PACKAGE_PIN Y8 [get_ports 114_RX3_P]
set_property PACKAGE_PIN Y7 [get_ports 114_RX3_N]
set_property PACKAGE_PIN AD4 [get_ports 114_TX2_P]
set_property PACKAGE_PIN AD3 [get_ports 114_TX2_N]
set_property PACKAGE_PIN AA6 [get_ports 114_RX2_P]
set_property PACKAGE_PIN AA5 [get_ports 114_RX2_N]
set_property PACKAGE_PIN AE2 [get_ports 114_TX1_P]
set_property PACKAGE_PIN AE1 [get_ports 114_TX1_N]
set_property PACKAGE_PIN AC6 [get_ports 114_RX1_P]
set_property PACKAGE_PIN AC5 [get_ports 114_RX1_N]
set_property PACKAGE_PIN AF4 [get_ports 114_TX0_P]
set_property PACKAGE_PIN AF3 [get_ports 114_TX0_N]
set_property PACKAGE_PIN AD8 [get_ports 114_RX0_P]
set_property PACKAGE_PIN AD7 [get_ports 114_RX0_N]
set_property PACKAGE_PIN U10 [get_ports 115_REFCLK0_P]
set_property PACKAGE_PIN U9 [get_ports 115_REFCLK0_N]
set_property PACKAGE_PIN W10 [get_ports 115_REFCLK1_P]
set_property PACKAGE_PIN W9 [get_ports 115_REFCLK1_N]
set_property PACKAGE_PIN W2 [get_ports 115_TX3_P]
set_property PACKAGE_PIN W1 [get_ports 115_TX3_N]
set_property PACKAGE_PIN T8 [get_ports 115_RX3_P]
set_property PACKAGE_PIN T7 [get_ports 115_RX3_N]
set_property PACKAGE_PIN Y4 [get_ports 115_TX2_P]
set_property PACKAGE_PIN Y3 [get_ports 115_TX2_N]
set_property PACKAGE_PIN U6 [get_ports 115_RX2_P]
set_property PACKAGE_PIN U5 [get_ports 115_RX2_N]
set_property PACKAGE_PIN AA2 [get_ports 115_TX1_P]
set_property PACKAGE_PIN AA1 [get_ports 115_TX1_N]
set_property PACKAGE_PIN V8 [get_ports 115_RX1_P]
set_property PACKAGE_PIN V7 [get_ports 115_RX1_N]
set_property PACKAGE_PIN AB4 [get_ports 115_TX0_P]
set_property PACKAGE_PIN AB3 [get_ports 115_TX0_N]
set_property PACKAGE_PIN W6 [get_ports 115_RX0_P]
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set_property PACKAGE_PIN W5 [get_ports 115_RX0_N]
set_property PACKAGE_PIN N10 [get_ports 116_REFCLK0_P]
set_property PACKAGE_PIN N9 [get_ports 116_REFCLK0_N]
set_property PACKAGE_PIN R10 [get_ports 116_REFCLK1_P]
set_property PACKAGE_PIN R9 [get_ports 116_REFCLK1_N]
set_property PACKAGE_PIN R2 [get_ports 116_TX3_P]
set_property PACKAGE_PIN R1 [get_ports 116_TX3_N]
set_property PACKAGE_PIN M8 [get_ports 116_RX3_P]
set_property PACKAGE_PIN M7 [get_ports 116_RX3_N]
set_property PACKAGE_PIN T4 [get_ports 116_TX2_P]
set_property PACKAGE_PIN T3 [get_ports 116_TX2_N]
set_property PACKAGE_PIN N6 [get_ports 116_RX2_P]
set_property PACKAGE_PIN N5 [get_ports 116_RX2_N]
set_property PACKAGE_PIN U2 [get_ports 116_TX1_P]
set_property PACKAGE_PIN U1 [get_ports 116_TX1_N]
set_property PACKAGE_PIN P8 [get_ports 116_RX1_P]
set_property PACKAGE_PIN P7 [get_ports 116_RX1_N]
set_property PACKAGE_PIN V4 [get_ports 116_TX0_P]
set_property PACKAGE_PIN V3 [get_ports 116_TX0_N]
set_property PACKAGE_PIN R6 [get_ports 116_RX0_P]
set_property PACKAGE_PIN R5 [get_ports 116_RX0_N]
set_property PACKAGE_PIN J10 [get_ports 117_REFCLK0_P]
set_property PACKAGE_PIN J9 [get_ports 117_REFCLK0_N]
set_property PACKAGE_PIN L10 [get_ports 117_REFCLK1_P]
set_property PACKAGE_PIN L9 [get_ports 117_REFCLK1_N]
set_property PACKAGE_PIN L2 [get_ports 117_TX3_P]
set_property PACKAGE_PIN L1 [get_ports 117_TX3_N]
set_property PACKAGE_PIN H8 [get_ports 117_RX3_P]
set_property PACKAGE_PIN H7 [get_ports 117_RX3_N]
set_property PACKAGE_PIN M4 [get_ports 117_TX2_P]
set_property PACKAGE_PIN M3 [get_ports 117_TX2_N]
set_property PACKAGE_PIN J6 [get_ports 117_RX2_P]
set_property PACKAGE_PIN J5 [get_ports 117_RX2_N]
set_property PACKAGE_PIN N2 [get_ports 117_TX1_P]
set_property PACKAGE_PIN N1 [get_ports 117_TX1_N]
set_property PACKAGE_PIN K8 [get_ports 117_RX1_P]
set_property PACKAGE_PIN K7 [get_ports 117_RX1_N]
set_property PACKAGE_PIN P4 [get_ports 117_TX0_P]
set_property PACKAGE_PIN P3 [get_ports 117_TX0_N]
set_property PACKAGE_PIN L6 [get_ports 117_RX0_P]
set_property PACKAGE_PIN L5 [get_ports 117_RX0_N]
set_property PACKAGE_PIN E10 [get_ports 118_REFCLK0_P]
set_property PACKAGE_PIN E9 [get_ports 118_REFCLK0_N]
set_property PACKAGE_PIN G10 [get_ports 118_REFCLK1_P]
set_property PACKAGE_PIN G9 [get_ports 118_REFCLK1_N]
set_property PACKAGE_PIN G2 [get_ports 118_TX3_P]
set_property PACKAGE_PIN G1 [get_ports 118_TX3_N]
set_property PACKAGE_PIN D8 [get_ports 118_RX3_P]
set_property PACKAGE_PIN D7 [get_ports 118_RX3_N]
set_property PACKAGE_PIN H4 [get_ports 118_TX2_P]
set_property PACKAGE_PIN H3 [get_ports 118_TX2_N]
set_property PACKAGE_PIN E6 [get_ports 118_RX2_P]
set_property PACKAGE_PIN E5 [get_ports 118_RX2_N]
set_property PACKAGE_PIN J2 [get_ports 118_TX1_P]
set_property PACKAGE_PIN J1 [get_ports 118_TX1_N]
set_property PACKAGE_PIN F8 [get_ports 118_RX1_P]
set_property PACKAGE_PIN F7 [get_ports 118_RX1_N]
set_property PACKAGE_PIN K4 [get_ports 118_TX0_P]
set_property PACKAGE_PIN K3 [get_ports 118_TX0_N]
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set_property PACKAGE_PIN G6 [get_ports 118_RX0_P]
set_property PACKAGE_PIN G5 [get_ports 118_RX0_N]
set_property PACKAGE_PIN A10 [get_ports 119_REFCLK0_P]
set_property PACKAGE_PIN A9 [get_ports 119_REFCLK0_N]
set_property PACKAGE_PIN C10 [get_ports 119_REFCLK1_P]
set_property PACKAGE_PIN C9 [get_ports 119_REFCLK1_N]
set_property PACKAGE_PIN B4 [get_ports 119_TX3_P]
set_property PACKAGE_PIN B3 [get_ports 119_TX3_N]
set_property PACKAGE_PIN A6 [get_ports 119_RX3_P]
set_property PACKAGE_PIN A5 [get_ports 119_RX3_N]
set_property PACKAGE_PIN C2 [get_ports 119_TX2_P]
set_property PACKAGE_PIN C1 [get_ports 119_TX2_N]
set_property PACKAGE_PIN B8 [get_ports 119_RX2_P]
set_property PACKAGE_PIN B7 [get_ports 119_RX2_N]
set_property PACKAGE_PIN E2 [get_ports 119_TX1_P]
set_property PACKAGE_PIN E1 [get_ports 119_TX1_N]
set_property PACKAGE_PIN C6 [get_ports 119_RX1_P]
set_property PACKAGE_PIN C5 [get_ports 119_RX1_N]
set_property PACKAGE_PIN F4 [get_ports 119_TX0_P]
set_property PACKAGE_PIN F3 [get_ports 119_TX0_N]
set_property PACKAGE_PIN D4 [get_ports 119_RX0_P]
set_property PACKAGE_PIN D3 [get_ports 119_RX0_N]
set_property PACKAGE_PIN AY37 [get_ports 210_REFCLK0_P]
set_property PACKAGE_PIN AY38 [get_ports 210_REFCLK0_N]
set_property PACKAGE_PIN BB37 [get_ports 210_REFCLK1_P]
set_property PACKAGE_PIN BB38 [get_ports 210_REFCLK1_N]
set_property PACKAGE_PIN AY41 [get_ports 210_TX3_P]
set_property PACKAGE_PIN AY42 [get_ports 210_TX3_N]
set_property PACKAGE_PIN AW39 [get_ports 210_RX3_P]
set_property PACKAGE_PIN AW40 [get_ports 210_RX3_N]
set_property PACKAGE_PIN BA43 [get_ports 210_TX2_P]
set_property PACKAGE_PIN BA44 [get_ports 210_TX2_N]
set_property PACKAGE_PIN BA39 [get_ports 210_RX2_P]
set_property PACKAGE_PIN BA40 [get_ports 210_RX2_N]
set_property PACKAGE_PIN BB41 [get_ports 210_TX1_P]
set_property PACKAGE_PIN BB42 [get_ports 210_TX1_N]
set_property PACKAGE_PIN BC39 [get_ports 210_RX1_P]
set_property PACKAGE_PIN BC40 [get_ports 210_RX1_N]
set_property PACKAGE_PIN BD41 [get_ports 210_TX0_P]
set_property PACKAGE_PIN BD42 [get_ports 210_TX0_N]
set_property PACKAGE_PIN BD37 [get_ports 210_RX0_P]
set_property PACKAGE_PIN BD38 [get_ports 210_RX0_N]
set_property PACKAGE_PIN AR35 [get_ports 211_REFCLK0_P]
set_property PACKAGE_PIN AR36 [get_ports 211_REFCLK0_N]
set_property PACKAGE_PIN AT37 [get_ports 211_REFCLK1_P]
set_property PACKAGE_PIN AT38 [get_ports 211_REFCLK1_N]
set_property PACKAGE_PIN AT41 [get_ports 211_TX3_P]
set_property PACKAGE_PIN AT42 [get_ports 211_TX3_N]
set_property PACKAGE_PIN AP37 [get_ports 211_RX3_P]
set_property PACKAGE_PIN AP38 [get_ports 211_RX3_N]
set_property PACKAGE_PIN AU43 [get_ports 211_TX2_P]
set_property PACKAGE_PIN AU44 [get_ports 211_TX2_N]
set_property PACKAGE_PIN AR39 [get_ports 211_RX2_P]
set_property PACKAGE_PIN AR40 [get_ports 211_RX2_N]
set_property PACKAGE_PIN AV41 [get_ports 211_TX1_P]
set_property PACKAGE_PIN AV42 [get_ports 211_TX1_N]
set_property PACKAGE_PIN AU39 [get_ports 211_RX1_P]
set_property PACKAGE_PIN AU40 [get_ports 211_RX1_N]
set_property PACKAGE_PIN AW43 [get_ports 211_TX0_P]
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set_property PACKAGE_PIN AW44 [get_ports 211_TX0_N]
set_property PACKAGE_PIN AV37 [get_ports 211_RX0_P]
set_property PACKAGE_PIN AV38 [get_ports 211_RX0_N]
set_property PACKAGE_PIN AL35 [get_ports 212_REFCLK0_P]
set_property PACKAGE_PIN AL36 [get_ports 212_REFCLK0_N]
set_property PACKAGE_PIN AN35 [get_ports 212_REFCLK1_P]
set_property PACKAGE_PIN AN36 [get_ports 212_REFCLK1_N]
set_property PACKAGE_PIN AL43 [get_ports 212_TX3_P]
set_property PACKAGE_PIN AL44 [get_ports 212_TX3_N]
set_property PACKAGE_PIN AL39 [get_ports 212_RX3_P]
set_property PACKAGE_PIN AL40 [get_ports 212_RX3_N]
set_property PACKAGE_PIN AN43 [get_ports 212_TX2_P]
set_property PACKAGE_PIN AN44 [get_ports 212_TX2_N]
set_property PACKAGE_PIN AM37 [get_ports 212_RX2_P]
set_property PACKAGE_PIN AM38 [get_ports 212_RX2_N]
set_property PACKAGE_PIN AP41 [get_ports 212_TX1_P]
set_property PACKAGE_PIN AP42 [get_ports 212_TX1_N]
set_property PACKAGE_PIN AM41 [get_ports 212_RX1_P]
set_property PACKAGE_PIN AM42 [get_ports 212_RX1_N]
set_property PACKAGE_PIN AR43 [get_ports 212_TX0_P]
set_property PACKAGE_PIN AR44 [get_ports 212_TX0_N]
set_property PACKAGE_PIN AN39 [get_ports 212_RX0_P]
set_property PACKAGE_PIN AN40 [get_ports 212_RX0_N]
set_property PACKAGE_PIN AF37 [get_ports 213_REFCLK0_P]
set_property PACKAGE_PIN AH38 [get_ports 213_REFCLK1_N]
set_property PACKAGE_PIN AF38 [get_ports 213_REFCLK0_N]
set_property PACKAGE_PIN AH37 [get_ports 213_REFCLK1_P]
set_property PACKAGE_PIN AG43 [get_ports 213_TX3_P]
set_property PACKAGE_PIN AG44 [get_ports 213_TX3_N]
set_property PACKAGE_PIN AE39 [get_ports 213_RX3_P]
set_property PACKAGE_PIN AE40 [get_ports 213_RX3_N]
set_property PACKAGE_PIN AH41 [get_ports 213_TX2_P]
set_property PACKAGE_PIN AH42 [get_ports 213_TX2_N]
set_property PACKAGE_PIN AG39 [get_ports 213_RX2_P]
set_property PACKAGE_PIN AG40 [get_ports 213_RX2_N]
set_property PACKAGE_PIN AJ43 [get_ports 213_TX1_P]
set_property PACKAGE_PIN AJ44 [get_ports 213_TX1_N]
set_property PACKAGE_PIN AJ39 [get_ports 213_RX1_P]
set_property PACKAGE_PIN AJ40 [get_ports 213_RX1_N]
set_property PACKAGE_PIN AK41 [get_ports 213_TX0_P]
set_property PACKAGE_PIN AK42 [get_ports 213_TX0_N]
set_property PACKAGE_PIN AK37 [get_ports 213_RX0_P]
set_property PACKAGE_PIN AK38 [get_ports 213_RX0_N]
set_property PACKAGE_PIN AA35 [get_ports 214_REFCLK0_P]
set_property PACKAGE_PIN AA36 [get_ports 214_REFCLK0_N]
set_property PACKAGE_PIN AB37 [get_ports 214_REFCLK1_P]
set_property PACKAGE_PIN AB38 [get_ports 214_REFCLK1_N]
set_property PACKAGE_PIN AC43 [get_ports 214_TX3_P]
set_property PACKAGE_PIN AC44 [get_ports 214_TX3_N]
set_property PACKAGE_PIN Y37 [get_ports 214_RX3_P]
set_property PACKAGE_PIN Y38 [get_ports 214_RX3_N]
set_property PACKAGE_PIN AD41 [get_ports 214_TX2_P]
set_property PACKAGE_PIN AD42 [get_ports 214_TX2_N]
set_property PACKAGE_PIN AA39 [get_ports 214_RX2_P]
set_property PACKAGE_PIN AA40 [get_ports 214_RX2_N]
set_property PACKAGE_PIN AE43 [get_ports 214_TX1_P]
set_property PACKAGE_PIN AE44 [get_ports 214_TX1_N]
set_property PACKAGE_PIN AC39 [get_ports 214_RX1_P]
set_property PACKAGE_PIN AC40 [get_ports 214_RX1_N]
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set_property PACKAGE_PIN AF41 [get_ports 214_TX0_P]
set_property PACKAGE_PIN AF42 [get_ports 214_TX0_N]
set_property PACKAGE_PIN AD37 [get_ports 214_RX0_P]
set_property PACKAGE_PIN AD38 [get_ports 214_RX0_N]
set_property PACKAGE_PIN U35 [get_ports 215_REFCLK0_P]
set_property PACKAGE_PIN U36 [get_ports 215_REFCLK0_N]
set_property PACKAGE_PIN W35 [get_ports 215_REFCLK1_P]
set_property PACKAGE_PIN W36 [get_ports 215_REFCLK1_N]
set_property PACKAGE_PIN W43 [get_ports 215_TX3_P]
set_property PACKAGE_PIN W44 [get_ports 215_TX3_N]
set_property PACKAGE_PIN T37 [get_ports 215_RX3_P]
set_property PACKAGE_PIN T38 [get_ports 215_RX3_N]
set_property PACKAGE_PIN Y41 [get_ports 215_TX2_P]
set_property PACKAGE_PIN Y42 [get_ports 215_TX2_N]
set_property PACKAGE_PIN U39 [get_ports 215_RX2_P]
set_property PACKAGE_PIN U40 [get_ports 215_RX2_N]
set_property PACKAGE_PIN AA43 [get_ports 215_TX1_P]
set_property PACKAGE_PIN AA44 [get_ports 215_TX1_N]
set_property PACKAGE_PIN V37 [get_ports 215_RX1_P]
set_property PACKAGE_PIN V38 [get_ports 215_RX1_N]
set_property PACKAGE_PIN AB41 [get_ports 215_TX0_P]
set_property PACKAGE_PIN AB42 [get_ports 215_TX0_N]
set_property PACKAGE_PIN W39 [get_ports 215_RX0_P]
set_property PACKAGE_PIN W40 [get_ports 215_RX0_N]
set_property PACKAGE_PIN N35 [get_ports 216_REFCLK0_P]
set_property PACKAGE_PIN N36 [get_ports 216_REFCLK0_N]
set_property PACKAGE_PIN R35 [get_ports 216_REFCLK1_P]
set_property PACKAGE_PIN R36 [get_ports 216_REFCLK1_N]
set_property PACKAGE_PIN R43 [get_ports 216_TX3_P]
set_property PACKAGE_PIN R44 [get_ports 216_TX3_N]
set_property PACKAGE_PIN M37 [get_ports 216_RX3_P]
set_property PACKAGE_PIN M38 [get_ports 216_RX3_N]
set_property PACKAGE_PIN T41 [get_ports 216_TX2_P]
set_property PACKAGE_PIN T42 [get_ports 216_TX2_N]
set_property PACKAGE_PIN N39 [get_ports 216_RX2_P]
set_property PACKAGE_PIN N40 [get_ports 216_RX2_N]
set_property PACKAGE_PIN U43 [get_ports 216_TX1_P]
set_property PACKAGE_PIN U44 [get_ports 216_TX1_N]
set_property PACKAGE_PIN P37 [get_ports 216_RX1_P]
set_property PACKAGE_PIN P38 [get_ports 216_RX1_N]
set_property PACKAGE_PIN V41 [get_ports 216_TX0_P]
set_property PACKAGE_PIN V42 [get_ports 216_TX0_N]
set_property PACKAGE_PIN R39 [get_ports 216_RX0_P]
set_property PACKAGE_PIN R40 [get_ports 216_RX0_N]
set_property PACKAGE_PIN J35 [get_ports 217_REFCLK0_P]
set_property PACKAGE_PIN J36 [get_ports 217_REFCLK0_N]
set_property PACKAGE_PIN L35 [get_ports 217_REFCLK1_P]
set_property PACKAGE_PIN L36 [get_ports 217_REFCLK1_N]
set_property PACKAGE_PIN L43 [get_ports 217_TX3_P]
set_property PACKAGE_PIN L44 [get_ports 217_TX3_N]
set_property PACKAGE_PIN H37 [get_ports 217_RX3_P]
set_property PACKAGE_PIN H38 [get_ports 217_RX3_N]
set_property PACKAGE_PIN M41 [get_ports 217_TX2_P]
set_property PACKAGE_PIN M42 [get_ports 217_TX2_N]
set_property PACKAGE_PIN J39 [get_ports 217_RX2_P]
set_property PACKAGE_PIN J40 [get_ports 217_RX2_N]
set_property PACKAGE_PIN N43 [get_ports 217_TX1_P]
set_property PACKAGE_PIN N44 [get_ports 217_TX1_N]
set_property PACKAGE_PIN K37 [get_ports 217_RX1_P]
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set_property PACKAGE_PIN K38 [get_ports 217_RX1_N]
set_property PACKAGE_PIN P41 [get_ports 217_TX0_P]
set_property PACKAGE_PIN P42 [get_ports 217_TX0_N]
set_property PACKAGE_PIN L39 [get_ports 217_RX0_P]
set_property PACKAGE_PIN L40 [get_ports 217_RX0_N]
set_property PACKAGE_PIN E35 [get_ports 218_REFCLK0_P]
set_property PACKAGE_PIN E36 [get_ports 218_REFCLK0_N]
set_property PACKAGE_PIN G35 [get_ports 218_REFCLK1_P]
set_property PACKAGE_PIN G36 [get_ports 218_REFCLK1_N]
set_property PACKAGE_PIN G43 [get_ports 218_TX3_P]
set_property PACKAGE_PIN G44 [get_ports 218_TX3_N]
set_property PACKAGE_PIN D37 [get_ports 218_RX3_P]
set_property PACKAGE_PIN D38 [get_ports 218_RX3_N]
set_property PACKAGE_PIN H41 [get_ports 218_TX2_P]
set_property PACKAGE_PIN H42 [get_ports 218_TX2_N]
set_property PACKAGE_PIN E39 [get_ports 218_RX2_P]
set_property PACKAGE_PIN E40 [get_ports 218_RX2_N]
set_property PACKAGE_PIN J43 [get_ports 218_TX1_P]
set_property PACKAGE_PIN J44 [get_ports 218_TX1_N]
set_property PACKAGE_PIN F37 [get_ports 218_RX1_P]
set_property PACKAGE_PIN F38 [get_ports 218_RX1_N]
set_property PACKAGE_PIN K41 [get_ports 218_TX0_P]
set_property PACKAGE_PIN K42 [get_ports 218_TX0_N]
set_property PACKAGE_PIN G39 [get_ports 218_RX0_P]
set_property PACKAGE_PIN G40 [get_ports 218_RX0_N]
set_property PACKAGE_PIN A35 [get_ports 219_REFCLK0_P]
set_property PACKAGE_PIN A36 [get_ports 219_REFCLK0_N]
set_property PACKAGE_PIN C35 [get_ports 219_REFCLK1_P]
set_property PACKAGE_PIN C36 [get_ports 219_REFCLK1_N]
set_property PACKAGE_PIN B41 [get_ports 219_TX3_P]
set_property PACKAGE_PIN B42 [get_ports 219_TX3_N]
set_property PACKAGE_PIN A39 [get_ports 219_RX3_P]
set_property PACKAGE_PIN A40 [get_ports 219_RX3_N]
set_property PACKAGE_PIN C43 [get_ports 219_TX2_P]
set_property PACKAGE_PIN C44 [get_ports 219_TX2_N]
set_property PACKAGE_PIN B37 [get_ports 219_RX2_P]
set_property PACKAGE_PIN B38 [get_ports 219_RX2_N]
set_property PACKAGE_PIN E43 [get_ports 219_TX1_P]
set_property PACKAGE_PIN E44 [get_ports 219_TX1_N]
set_property PACKAGE_PIN C39 [get_ports 219_RX1_P]
set_property PACKAGE_PIN C40 [get_ports 219_RX1_N]
set_property PACKAGE_PIN F41 [get_ports 219_TX0_P]
set_property PACKAGE_PIN F42 [get_ports 219_TX0_N]
set_property PACKAGE_PIN D41 [get_ports 219_RX0_P]
set_property PACKAGE_PIN D42 [get_ports 219_RX0_N]
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Appendix D

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx Support website.

For continual updates, add the Answer Record to your myAlerts.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

The most up to date information related to the VC7215 board and its documentation is available on these websites:

Virtex-7 FPGA VC7215 Characterization Kit

Virtex-7 FPGA VC7215 Characterization Kit documentation

Virtex-7 FPGA VC7215 Characterization Kit Master Answer Record (AR 55180)

These documents and websites provide supplemental material useful with this guide:

1. *7 Series FPGAs and Zynq-7000 All Programmable SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter User Guide* (UG480)
2. Information about the power system components used by the VC7215 board is available from the Texas Instruments digital power website at:

   www.ti.com/ww/en/analog/digital-power/index.html
3. Information about the 7 series GTX/GTH power supply modules included with the VC7215 Characterization Kit is available from General Electric:

   go.ge-energy.com/FPGA_2014_XiLinx_Download.html
4. *7 Series FPGAs Overview* (DS180)
5. *Vivado Design Suite User Guide: Using Constraints* (UG903)
6. *Virtex-7 T and XT FPGAs Data Sheet: DC and AC Switching Characteristics* (DS183)
7. *7 Series FPGAs Configuration User Guide* (UG470)
8. *7 Series FPGAs SelectIO Resources User Guide* (UG471)
9. *7 Series FPGAs Clocking Resources User Guide* (UG472)
10. *7 Series FPGAs Configurable Logic Block User Guide* (UG474)

11. *7 Series FPGAs Packaging and Pinout User Guide* (UG475)
12. *7 Series FPGAs GTX/GTH Transceivers User Guide* (UG476)
13. *7 Series FPGAs Integrated Block for PCI Express Product Guide for Vivado Design Suite* (PG054)
14. *HW-CLK-101-SCLK2 SuperClock-2 Module User Guide* (UG770)

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Appendix E

Regulatory and Compliance Information

This product is designed and tested to conform to the European Union directives and standards described in this section.

Declaration of Conformity

See the Virtex-7 FPGA VC7215 Declaration of Conformity.

Directives

2006/95/EC, *Low Voltage Directive (LVD)*

2004/108/EC, *Electromagnetic Compatibility (EMC) Directive*

Standards

EN standards are maintained by the European Committee for Electrotechnical Standardization (CENELEC). IEC standards are maintained by the International Electrotechnical Commission (IEC).

Electromagnetic Compatibility

EN 55022:2010, *Information Technology Equipment Radio Disturbance Characteristics – Limits and Methods of Measurement*

EN 55024:2010, *Information Technology Equipment Immunity Characteristics – Limits and Methods of Measurement*

This is a Class A product and can cause radio interference. In a domestic environment, the user might be required to take adequate corrective measures.

Safety

IEC 60950-1:2005, *Information technology equipment – Safety, Part 1: General requirements*

EN 60950-1:2006, *Information technology equipment – Safety, Part 1: General requirements*

Markings

This product complies with Directive 2002/96/EC on waste electrical and electronic equipment (WEEE). The affixed product label indicates that the user must not discard this electrical or electronic product in domestic household waste.

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

This product complies with CE Directives 2006/95/EC, *Low Voltage Directive (LVD)* and 2004/108/EC, *Electromagnetic Compatibility (EMC) Directive.*

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