Triple Buck Regulator Integrated Power Solution

Data Sheet

ADP5056

FEATURES

- Wide input voltage range: 2.75 V to 18 V
- Bias input voltage range: 4.5 V to 18 V
- Operation up to 150°C junction temperature
- −0.62% to +0.69% feedback voltage accuracy (−40°C to +125°C junction temperature)
- Channel 1 and Channel 2: 7 A synchronous buck regulator (9.4 A minimum valley current limit)
- Channel 1 and Channel 2: 14 A output in parallel operation
- Channel 3: 3 A synchronous buck regulator (4.2 A minimum valley current limit)
- 250 kHz to 2500 kHz adjustable switching frequency
- External compensation for fast load transient response
- Precision enable pin with 0.615 V accurate reference voltage
- Programmable power-up and power-down sequence
- Selective FPWM/PSM mode selection
- Frequency synchronization input or output
- Power-good flag for three channels
- Active output discharge switch
- UVLO, overcurrent protection, and TSD protection
- 43-terminal, 5 mm × 5.5 mm LGA package

APPLICATIONS

- Small cell base stations
- Field programmable gate array (FPGA) and processor applications
- Security and surveillance
- Medical applications

TYPICAL APPLICATION CIRCUIT

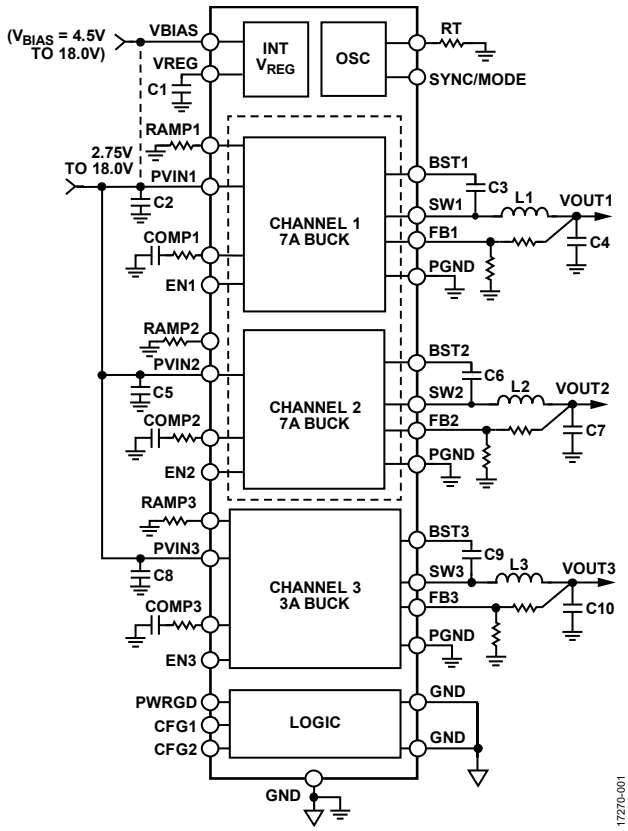

Figure 1.

GENERAL DESCRIPTION

The ADP5056 combines three high performance buck regulators in a 43-terminal land grid array (LGA) package that meets the demanding performance and board space requirements. The device enables direct connection to high input voltages up to 18 V with no preregulators.

All channels integrate both high-side and low-side power metal-oxide semiconductor field effect transistors (MOSFETs) to achieve an efficiency optimized solution. Channel 1 and Channel 2 deliver a programmable output current of 3.5 A or 7 A, or provide a single output with up to 14 A of current in parallel operation. Channel 3 delivers a programmable output current of 1.5 A or 3 A.

The switching frequency of the ADP5056 can be programmed or synchronized to an external clock. The ADP5056 contains an enable pin (ENx) on each channel for easy power-up sequencing or adjustable undervoltage lockout (UVLO) threshold.

The ADP5056 integrates start-up/shutdown sequence control, forced pulse-width modulation/power saving mode (FPWM/PSM) selection, an output discharge switch, and a power-good signal.

The ADP5056 is rated at −40°C to +150°C junction temperature.

Note that throughout this data sheet, multifunction pins, such as SYNC/MODE, are referred to either by the entire pin name or by a single function of the pin, for example, SYNC, when only that function is relevant.

Rev. 0 Document Feedback

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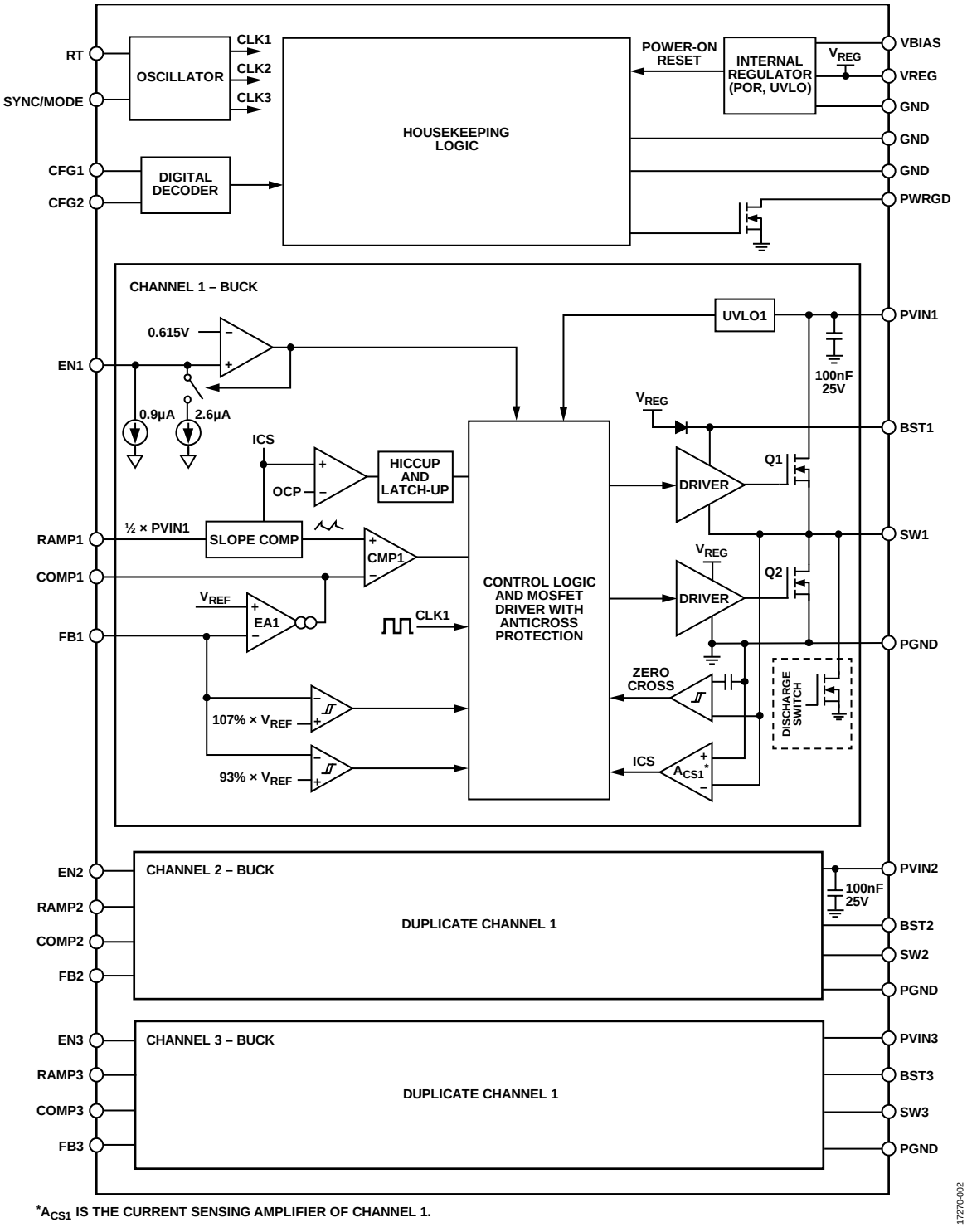
REVISION HISTORY

5/2020—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM



*A_{CS1} IS THE CURRENT SENSING AMPLIFIER OF CHANNEL 1.

Figure 2.

SPECIFICATIONS

Input voltage (V_{IN}) = bias input voltage (V_{BIAS}) = 12 V, VREG voltage (V_{REG}) = 4.8 V, T_J = −40°C to +150°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
WIDE INPUT VOLTAGE RANGE	V_{IN}	2.75		18	V	PVIN1 pin, PVIN2 pin, PVIN3 pin
BIAS INPUT VOLTAGE RANGE	V_{BIAS}	4.5		18	V	VBIAS pin
QUIESCENT CURRENT						VBIAS pin
Operating Quiescent Current	$I_{Q(3\text{-}BUCKS)}$		6.2	7.5	mA	No switching, all ENx pins high
Shutdown Current of Three Channels	$I_{SHDN(3\text{-}BUCKS)}$		42	80	µA	All ENx pins low
UNDERVOLTAGE LOCKOUT						
Power Input	$UVLO_{PVINx}$					PVIN1 pin, PVIN2 pin, PVIN3 pin
Rising Threshold	$V_{UVLO1\text{-}RISING}$		2.5	2.75	V	
Falling Threshold	$V_{UVLO1\text{-}FALLING}$		2.22		V	
Hysteresis	V_{HYS1}		0.30		V	
Bias Input Voltage	$UVLO_{VBIAS}$					VBIAS pin
Rising Threshold	$V_{UVLO2\text{-}RISING}$		4.20	4.50	V	
Falling Threshold	$V_{UVLO2\text{-}FALLING}$	3.60	3.80		V	
Hysteresis	V_{HYS2}		0.40		V	
OSCILLATOR CIRCUIT						
Switching Frequency	f_{SW}	530	600	630	kHz	R_T = 280 kΩ
		1140	1200	1250	kHz	R_T = 140 kΩ
		1700	1800	1900	kHz	R_T = 94.2 kΩ
Switching Frequency Range		250		2500	kHz	
Synchronization Input						
Input Clock Range	f_{SYNC}	250		2700	kHz	
Input Clock Pulse Width						
Minimum On Time	$t_{SYNC\_MIN\_ON}$	100			ns	
Minimum Off Time	$t_{SYNC\_MIN\_OFF}$	100			ns	
Input Clock High Voltage	$V_{H(SYNC)}$	2.65			V	
Input Clock Low Voltage	$V_{L(SYNC)}$			1.2	V	
Synchronization Output						
Clock Frequency	f_{CLK}		f_{SW}		kHz	
Positive Pulse Duty Cycle	$t_{CLK\_PULSE\_DUTY}$		50		%	
Rise or Fall Time	$t_{CLK\_RISE\_FALL}$		2		ns	
High Level Voltage	$V_{H(SYNC\_OUT)}$		V_{REG}		V	
PRECISION ENABLING						EN1 pin, EN2 pin, EN3 pin
Enable Voltage Range	V_{EN_RANGE}	0		18	V	
High Level Threshold	$V_{TH\_H(EN)}$		0.615	0.67	V	
Low Level Threshold	$V_{TH\_L(EN)}$	0.52	0.575		V	
Source Current (High Level)	$I_{TH\_H(EN)}$	0.48	0.9	1.55	µA	Above the rising threshold
Source Current (Low Level)	$I_{TH\_L(EN)}$	2.0	3.5	6.0	µA	Below the falling threshold
POWER GOOD						
Rising High Threshold	$V_{PWRGD(RISE\_H)}$		105		%	
Rising Low Threshold	$V_{PWRGD(RISE\_L)}$		95		%	
Falling High Threshold	$V_{PWRGD(FALL\_H)}$		107		%	
Falling Low Threshold	$V_{PWRGD(FALL\_L)}$		93		%	
Internal Power-Good Hysteresis	$V_{PWRGD(HYS)}$		2		%	
Falling Delay for PWRGD Pin	$t_{PWRGD\_FALL\_DLY}$		4 × switching period (t_{SW})		ms	
Rising Delay for PWRGD Pin[1]	$t_{PWRGD\_RISE\_DLY}$		0 or t_{SET}		ms	t_{SET} = 2.6 ms when the resistor value on the CFG2 pin (R_{CFG2}) = 0 Ω

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Leakage Current for PWRGD Pin	$I_{PWRGD\_LEAKAGE}$		0.1	1	µA	
Output Low Voltage for PWRGD Pin	V_{PWRGD_LOW}		10	150	mV	PWRGD pin current (I_{PWRGD}) = 1 mA
THERMAL SHUTDOWN (TSD)						
Thermal Shutdown Threshold	T_{SHDN}		175		°C	
Thermal Shutdown Hysteresis	T_{HYS}		15		°C	

[1] t_{SET} is the setting time programmed by CFG2.

BUCK REGULATOR SPECIFICATIONS

V_{IN} = 12 V, V_{REG} = 4.8 V, f_{SW} = 600 kHz for all channels, T_J = −40°C to +150°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
CHANNEL 1 BUCK REGULATOR						
Continuous Output Current	I_O		7			Determined by CFG1 pin configuration (see Table 6), CFG1 resistor (R_{CFG1}) = 0 Ω
			3.5			Determined by CFG1 pin configuration (see Table 6), R_{CFG1} = open
FB1 Pin						
Feedback Voltage			600		mV	
Feedback Voltage Accuracy	$V_{FB1\_DEFAULT}$	−0.25		+0.25	%	T_J = 25°C
Feedback Reference Voltage of Channel 1 (V_{FB1}) = 600 mV Default		−0.62		+0.69	%	−40°C ≤ T_J ≤ +125°C
		−0.62		+0.83	%	−40°C ≤ T_J ≤ +150°C
Feedback Bias Current	I_{FB1}			0.1	µA	Adjustable voltage
SW1 Pin						
High-Side Power Field Effect Transistor (FET) On Resistance	$R_{DSON\_HS(1)}$		25		mΩ	Pin to pin measurement
Low-Side Power FET On Resistance	$R_{DSON\_LS(1)}$		12		mΩ	Pin to pin measurement
Valley Current-Limit Threshold	$I_{TH(ILIM1)}$	9.4			A	Current limit of Channel 1 (I_{LIM1}) = 7 A, T_J = 25°C
		4.4			A	I_{LIM1} = 3.5 A, T_J = 25°C
Negative Current-Limit Threshold	$I_{TH(ILIM1-NEG)}$		−5.0		A	
Minimum On Time	t_{MIN_ON1}		35	55	ns	f_{SW} = 250 kHz to 2500 kHz
Minimum Off Time	t_{MIN_OFF1}		120	150	ns	f_{SW} = 250 kHz to 2500 kHz
Error Amplifier (EA), COMP1 Pin						
EA Transconductance	g_{m1}	330	350	365	µS	
Soft Start						
Soft Start Time	t_{SS1}		0.83 × t_{SET}		ms	t_{SET} = 2.6 ms when R_{CFG2} = 0 Ω
Hiccup Time	$t_{HICCUP1}$		7 × t_{SET}		ms	
Output Capacitor (C_{OUT}) Discharge Switch On Resistance	R_{DIS1}		85		Ω	
CHANNEL 2 BUCK REGULATOR						
Continuous Output Current	I_O		7			Determined by CFG1 pin configuration (see Table 6), R_{CFG1} = 0 Ω
			3.5			Determined by CFG1 pin configuration (see Table 6), R_{CFG1} = open
FB2 Pin						
Feedback Voltage			600		mV	
Feedback Voltage Accuracy	$V_{FB2\_DEFAULT}$	−0.25		+0.25	%	T_J = 25°C
Feedback Reference Voltage of Channel 2 (V_{FB2}) = 600 mV Default		−0.62		+0.69	%	−40°C ≤ T_J ≤ +125°C
		−0.62		+0.83	%	−40°C ≤ T_J ≤ +150°C
Feedback Bias Current	I_{FB2}			0.1	µA	Adjustable voltage

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SW2 Pin						
High-Side Power FET On Resistance	$R_{DSON\_HS(2)}$		25		mΩ	Pin to pin measurement
Low-Side Power FET On Resistance	$R_{DSON\_LS(2)}$		12		mΩ	Pin to pin measurement
Valley Current-Limit Threshold	$I_{TH(ILIM2)}$	9.4			A	Current limit of Channel 2 (I_{LIM2}) = 7 A, T_J = 25°C
		4.4			A	I_{LIM2} = 3.5 A, T_J = 25°C
Negative Current-Limit Threshold	$I_{TH(ILIM2-NEG)}$		−5.0		A	
Minimum On Time	t_{MIN_ON2}		35	55	ns	f_{SW} = 250 kHz to 2500 kHz
Minimum Off Time	t_{MIN_OFF2}		120	150	ns	f_{SW} = 250 kHz to 2500 kHz
EA, COMP2 Pin						
EA Transconductance	g_{m2}	330	350	365	µS	
Soft Start						
Soft Start Time	t_{SS2}		0.83 × t_{SET}		ms	t_{SET} = 2.6 ms when the R_{CFG2} = 0 Ω
Hiccup Time	$t_{HICCUP2}$		7 × t_{SET}		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS2}		85		Ω	
CHANNEL 1 AND CHANNEL 2 IN PARALLEL OPERATION						
Continuous Output Current	I_O		14			Determined by CFG1 pin configuration (see Table 6), R_{CFG1} = 23.7 kΩ
CHANNEL 3 BUCK REGULATOR						
Continuous Output Current	I_O		3			Determined by CFG1 pin configuration (see Table 6), R_{CFG1} = 0 Ω
			1.5			Determined by CFG1 pin configuration (see Table 6) R_{CFG1} = open
FB3 Pin						
Feedback Voltage			600		mV	
Feedback Voltage Accuracy	$V_{FB3\_DEFAULT}$	−0.25		+0.25	%	T_J = 25°C
Feedback Reference Voltage of Channel 3 (V_{FB3}) = 600 mV Default		−0.62		+0.69	%	−40°C ≤ T_J ≤ +125°C
		−0.62		+0.83	%	−40°C ≤ T_J ≤ +150°C
Feedback Bias Current	I_{FB3}			0.1	µA	Adjustable voltage
SW3 Pin						
High-Side Power FET On Resistance	$R_{DSON\_HS(3)}$		85		mΩ	Pin-to-pin measurement
Low-Side Power FET On Resistance	$R_{DSON\_LS(3)}$		45		mΩ	Pin-to-pin measurement
Valley Current-Limit Threshold	$I_{TH(ILIM3)}$	4.2			A	Current Limit of Channel 3 (I_{LIM3}) = 3 A, T_J = 25°C
		2.1			A	I_{LIM3} = 1.5 A, T_J = 25°C
Negative Current-Limit Threshold	$I_{TH(ILIM3-NEG)}$		−2.5		A	
Minimum On Time	t_{MIN_ON3}		35	55	ns	f_{SW} = 250 kHz to 2500 kHz
Minimum Off Time	t_{MIN_OFF3}		120	150	ns	f_{SW} = 250 kHz to 2500 kHz
EA, COMP3 Pin						
EA Transconductance	g_{m3}	330	350	365	µS	
Soft Start						
Soft Start Time	t_{SS3}		0.83 × t_{SET}		ms	t_{SET} = 2.6 ms when the R_{CFG2} = 0 Ω
Hiccup Time	$t_{HICCUP3}$		7 × t_{SET}		ms	
C_{OUT} Discharge Switch On Resistance	R_{DIS3}		85		Ω	

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VBIAS to GND	−0.3 V to +21 V
PVINx to PGND	−0.3 V to +21 V
SWx to PGND	−0.3 V to +21 V
RAMPx to GND	−0.3 V to +21 V
PGND to GND	−0.3 V to +0.3 V
BST1 to SW1	−0.3 V to +6.5 V
BST2 to SW2	−0.3 V to +6.5 V
BST3 to SW3	−0.3 V to +6.5 V
CFG1 and CFG2 to GND	−0.3 V to +6.5 V
ENx to GND	−0.3 V to +21 V
VREG to GND	−0.3 V to +6.5 V
SYNC/MODE to GND	−0.3 V to +6.5 V
RT to GND	−0.3 V to +6.5 V
PWRGD to GND	−0.3 V to +6.5 V
FB1, FB2, and FB3 to GND	−0.3 V to +6.5 V
COMPx to GND	−0.3 V to +6.5 V
Storage Temperature Range	−65°C to +150°C
Operational Junction Temperature Range	−40°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Thermal resistance values specified in Table 4 are simulated based on JEDEC specs (unless specified otherwise) and are used in compliance with JESD51-12. Using enhanced heat removal (PCB, heat sink, airflow) technique improves thermal resistance values.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}[1]	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
CC-43-1	26.0	14.3	9.3	0.2	9.0	(°C/W)

[1] For θ_{JC} test, 100 µm thermal interface material (TIM) is used. TIM is assumed to have 3.6 W/mK.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

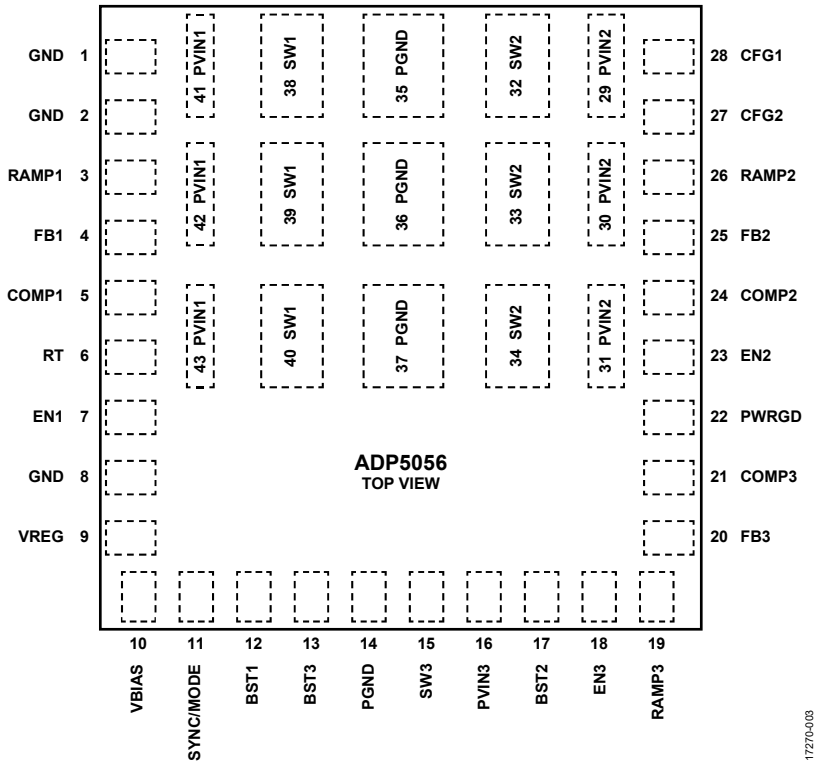


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	This pin is for internal test purposes. Connect this pin to ground.
2	GND	This pin is for internal test purposes. Connect this pin to ground.
3	RAMP1	Slope Compensation Setting for Channel 1. Connect a resistor from RAMP1 to ground to set the slope compensation.
4	FB1	Feedback Sensing Input for Channel 1.
5	COMP1	Error Amplifier Output for Channel 1. Connect a resistance and capacitor (RC) network from this pin to ground.
6	RT	Frequency Setting. Connect a resistor from RT to ground to program the switching frequency.
7	EN1	Enable Input for Channel 1.
8	GND	Analog Ground.
9	VREG	Output of the Internal 4.8 V Regulator. The control circuitry is powered from this voltage on this pin. Place a 4.7 µF ceramic capacitor (X7R or X5R) between this pin to GND.
10	VBIAS	Bias Input Voltage Pin to Supply Internal Regulator.
11	SYNC/MODE	Synchronization Input/Output (SYNC). To synchronize the switching frequency of the device to an external clock, connect this pin to an external clock with a frequency from 250 kHz to 2700 kHz. This pin can also be configured as a synchronization output via the CFG1 pin configuration. FPWM or Automatic PWM/PSM Selection Pin (MODE). When this pin is logic high, each channel works in FPWM mode. When this pin is logic low, all channels operate in automatic PWM/PSM mode.
12	BST1	Supply Rail for the High-Side Gate Drive in Channel 1. Place a 0.1 µF capacitor (X7R or X5R) between SW1 and BST1.
13	BST3	Supply Rail for the High-Side Gate Drive in Channel 3. Place a 0.1 µF capacitor (X7R or X5R) between SW3 and BST3.
14	PGND	Power Ground for all Channels.
15	SW3	Switching Node Output for Channel 3.
16	PVIN3	Power Input for Channel 3.
17	BST2	Supply Rail for the High-Side Gate Drive in Channel 2. Place a 0.1 µF capacitor (X7R or X5R) between SW2 and BST2.
18	EN3	Enable Input for Channel 3.
19	RAMP3	Slope Compensation Setting for Channel 3. Connect a resistor from RAMP3 to ground to set the slope compensation.
20	FB3	Feedback Sensing Input for Channel 3.
21	COMP3	Error Amplifier Output for Channel 3. Connect an RC network from this pin to ground.

Pin No.	Mnemonic	Description
22	PWRGD	Power Good Output for Selective Channels.
23	EN2	Enable Input for Channel 2.
24	COMP2	Error Amplifier Output for Channel 2. Connect an RC network from this pin to ground.
25	FB2	Feedback Sensing Input for Channel 2.
26	RAMP2	Slope Compensation Setting for Channel 2. Connect a resistor from RAMP2 to ground to set the slope compensation.
27	CFG2	System Configuration Pin 2. Connect one resistor from this pin to ground to program the t_{SET} timer, fast transient mode, and sequence mode.
28	CFG1	System Configuration Pin 1. Connect one resistor from this pin to ground to program the current limit, parallel operation, and clock output settings.
29	PVIN2	Power Input for Channel 2.
30	PVIN2	Power Input for Channel 2.
31	PVIN2	Power Input for Channel 2.
32	SW2	Switching Node Output for Channel 2.
33	SW2	Switching Node Output for Channel 2.
34	SW2	Switching Node Output for Channel 2.
35	PGND	Power Ground for all Channels.
36	PGND	Power Ground for all Channels.
37	PGND	Power Ground for all Channels.
38	SW1	Switching Node Output for Channel 1.
39	SW1	Switching Node Output for Channel 1.
40	SW1	Switching Node Output for Channel 1.
41	PVIN1	Power Input for Channel 1.
42	PVIN1	Power Input for Channel 1.
43	PVIN1	Power Input for Channel 1.

TYPICAL PERFORMANCE CHARACTERISTICS

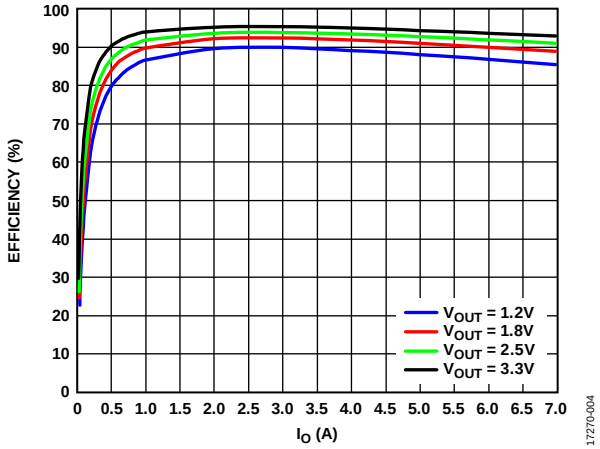


Figure 4. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 5 V, f_{SW} = 600 kHz, FPWM Mode

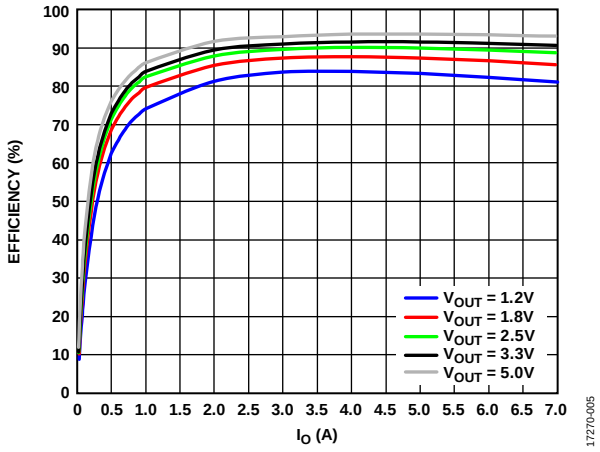


Figure 5. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM Mode

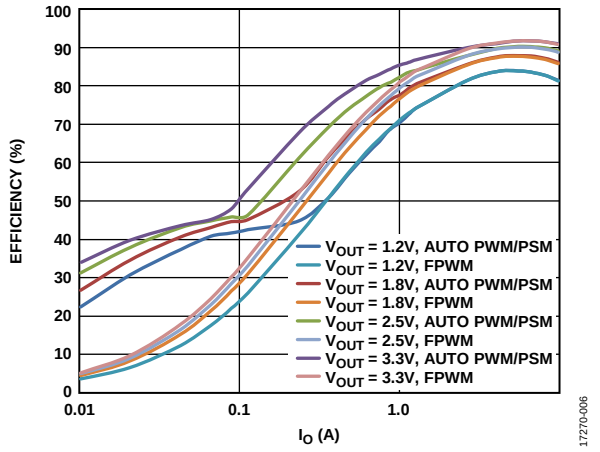


Figure 6. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM and Automatic PWM/PSM Modes

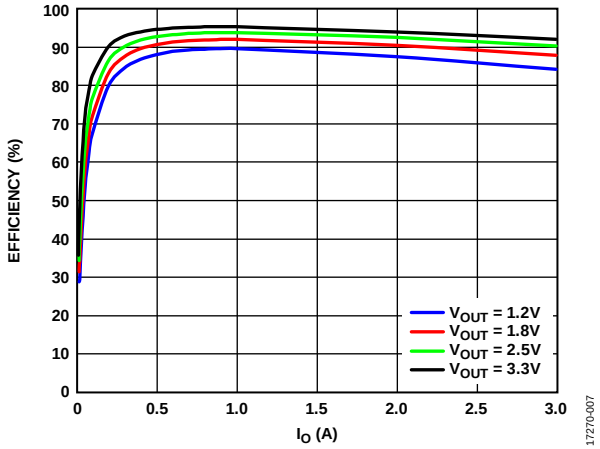


Figure 7. Channel 3 Efficiency Curve, V_{IN} = 5 V, f_{SW} = 600 kHz, FPWM Mode

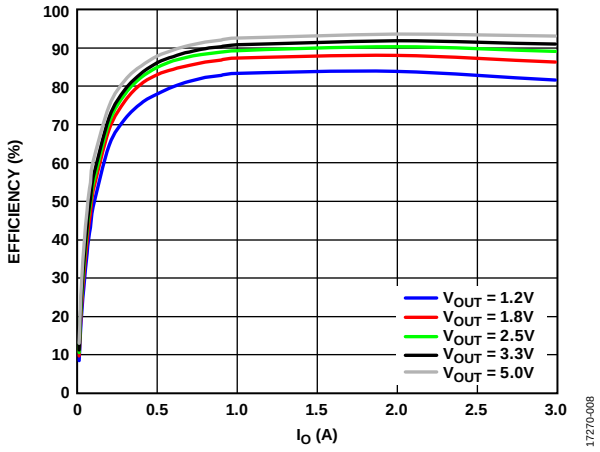


Figure 8. Channel 3 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM Mode

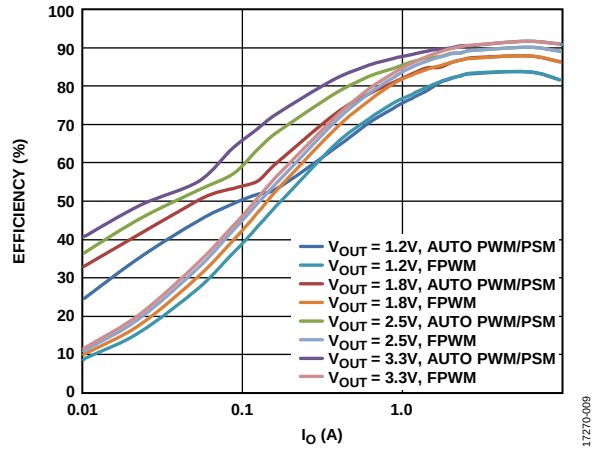


Figure 9. Channel 3 Efficiency Curve, V_{IN} = 12 V, f_{SW} = 600 kHz, FPWM Mode and Automatic PWM/PSM Modes

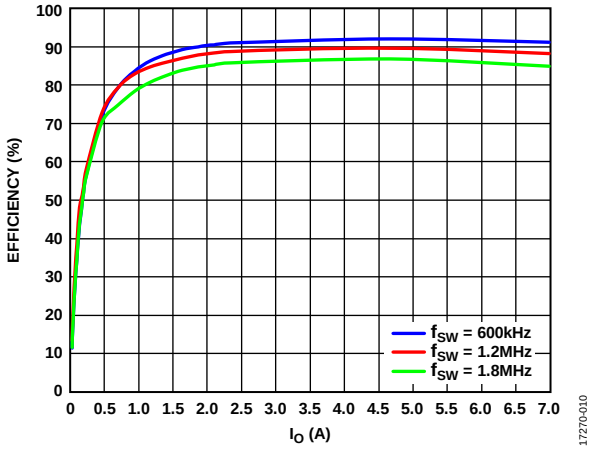


Figure 10. Channel 1/Channel 2 Efficiency Curve, V_{IN} = 12 V, Output Voltage (V_{OUT}) = 3.3 V, FPWM Mode (600 kHz, 1.2 MHz, 1.8 MHz)

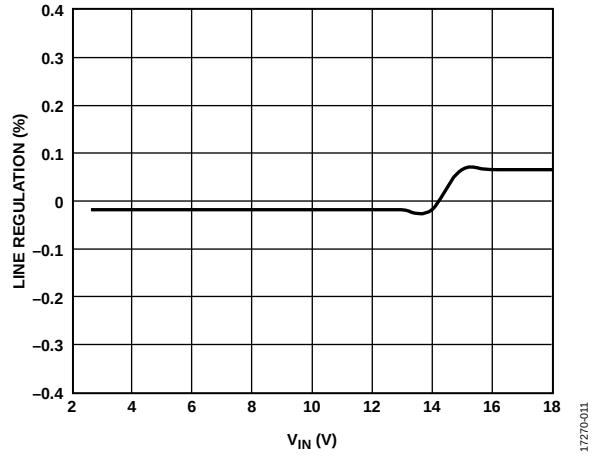


Figure 11. Channel 1/Channel 2 Line Regulation, V_{OUT} = 1.2 V, I_{OUT} = 7 A, f_{SW} = 600 kHz, FPWM Mode

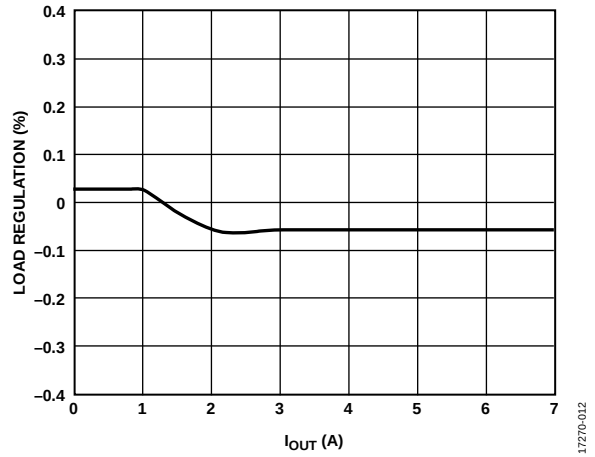


Figure 12. Channel 1/Channel 2 Load Regulation, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, FPWM Mode

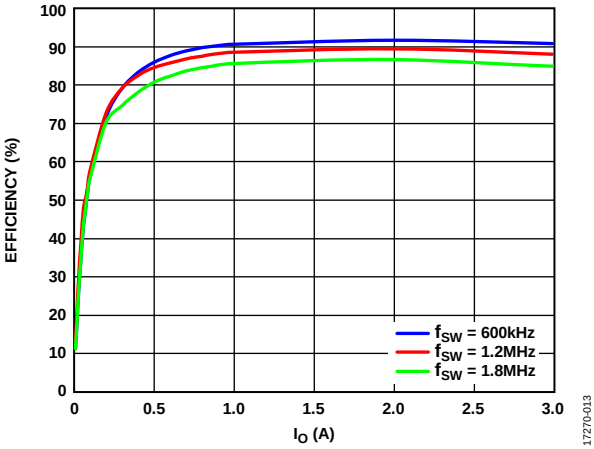


Figure 13. Channel 3 Efficiency Curve, V_{IN} = 12 V, V_{OUT} = 3.3 V, FPWM Mode (600 kHz, 1.2 MHz, 1.8 MHz)

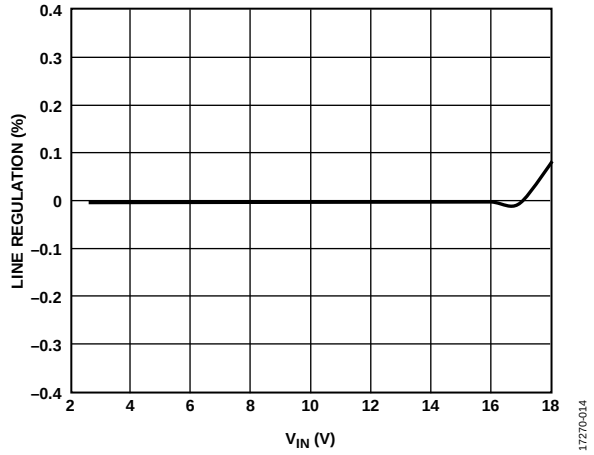


Figure 14. Channel 3 Line Regulation, V_{OUT} = 1.2 V, I_{OUT} = 3 A, f_{SW} = 600 kHz, FPWM Mode

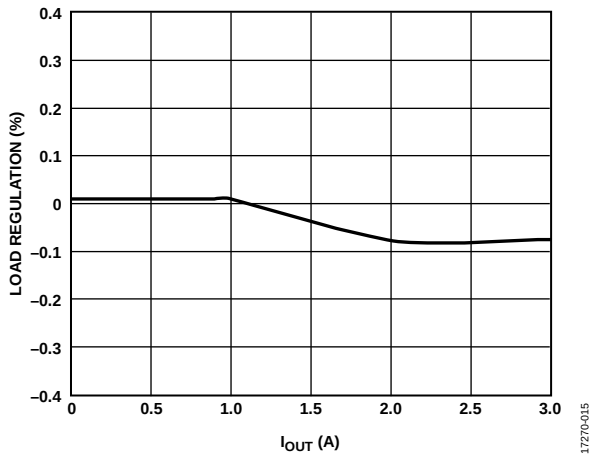


Figure 15. Channel 3 Load Regulation, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, FPWM Mode

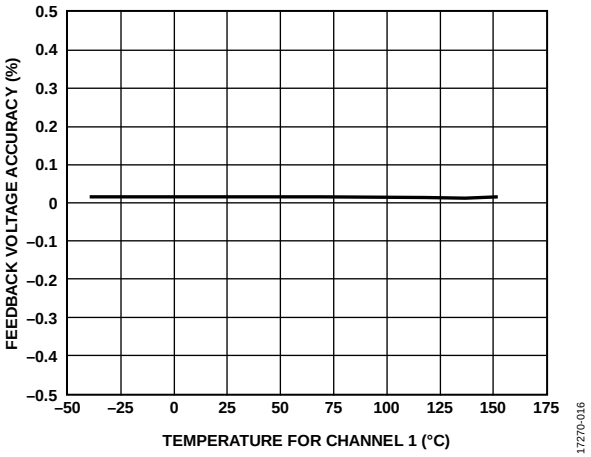


Figure 16. Feedback Voltage Accuracy vs. Temperature for Channel 1

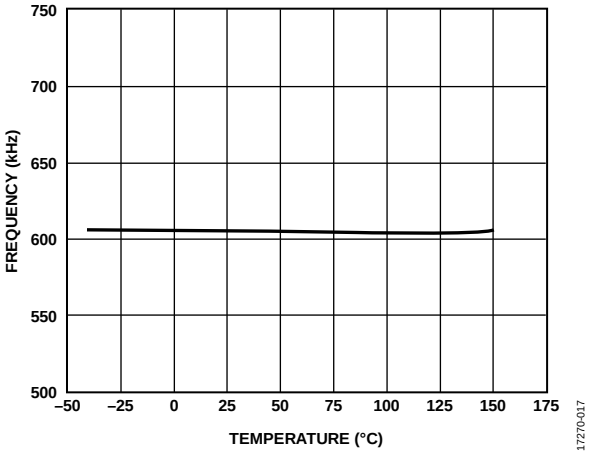


Figure 17. Frequency vs. Temperature, V_{IN} = 12 V

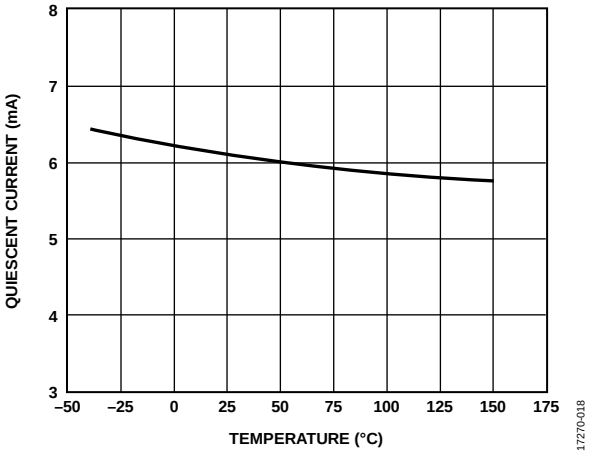


Figure 18. Quiescent Current vs. Temperature (Includes PVIN1, PVIN2, and PVIN3)

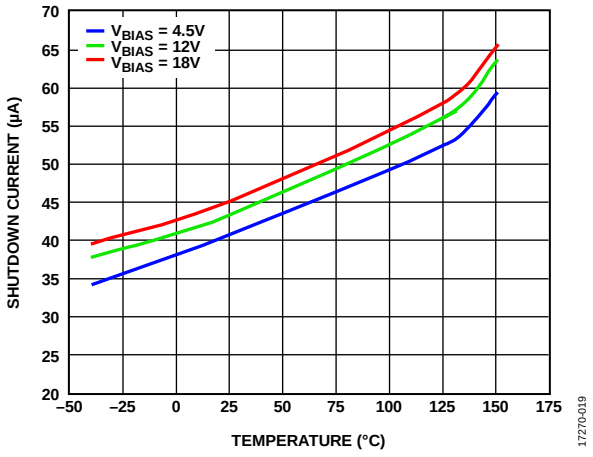


Figure 19. Shutdown Current vs. Temperature (EN1, EN2, and EN3 Low)

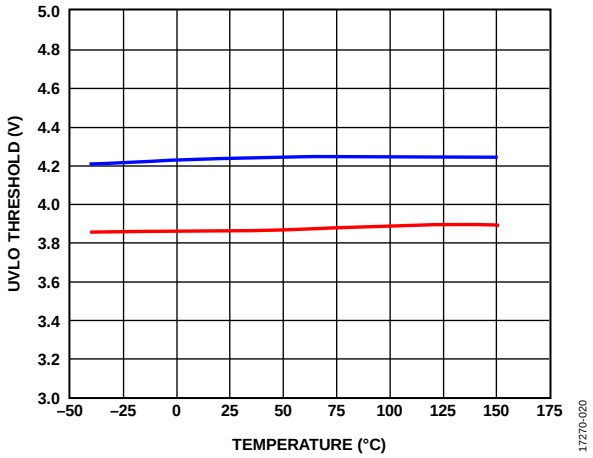


Figure 20. UVLO Threshold vs. Temperature

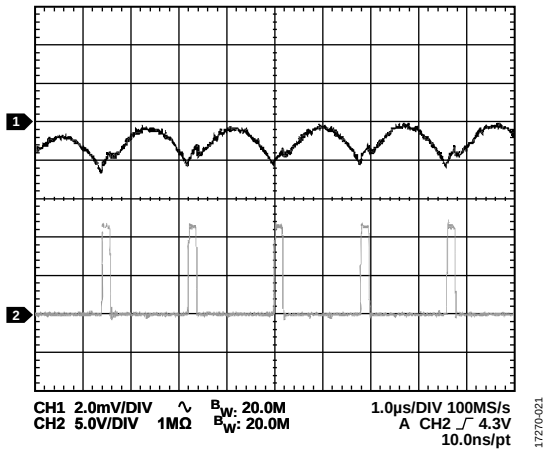


Figure 21. Channel 1/Channel 2 Steady State Waveform, V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 7 A, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 6, FPWM Mode, Channel 1 = V_{OUT}, Channel 2 = Switching Point (SW)

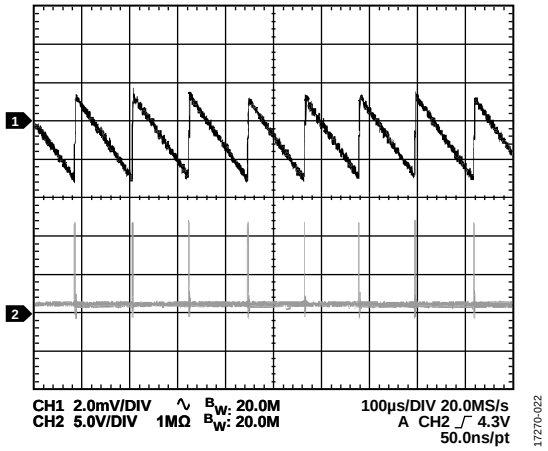


Figure 22. Channel 1/Channel 2 Steady State Waveform, V_{IN} = 12 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 6, Automatic PWM/PSM, Channel 1 = V_{OUT}, Channel 2 = SW

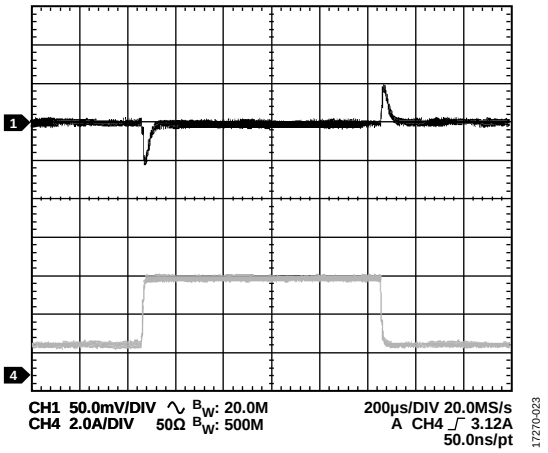


Figure 23. Load Transient, Channel 1/Channel 2 from 1.5 A to 5 A, V_{IN} = 12 V, V_{OUT} = 3.3 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 6, 1 A/µs, Channel 1 = V_{OUT}, Channel 4 = I_{OUT}

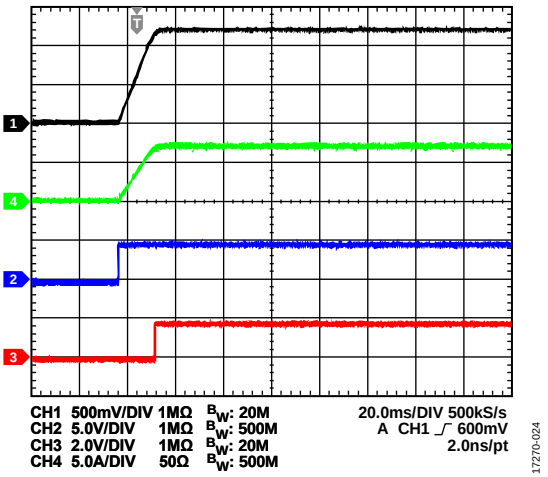


Figure 24. Channel 1/Channel 2 Soft Start with 7 A Resistance Load, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 6, Channel 1 = V_{OUT}, Channel 2 = EN, Channel 3 = PWRGD, Channel 4 = I_{OUT}

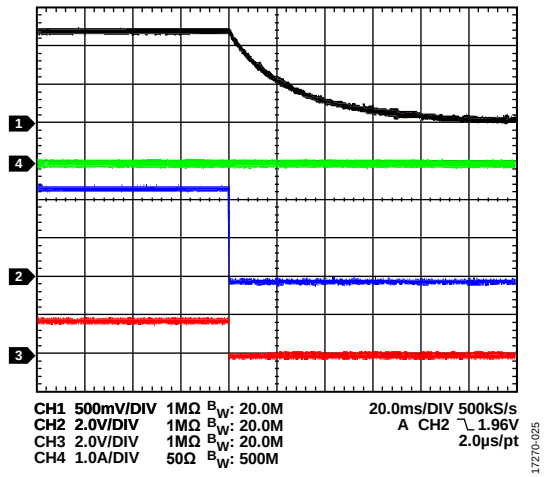


Figure 25. Channel 1/Channel 2 Shutdown with Active Output Discharge, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 6, Channel 1 = V_{OUT}, Channel 2 = EN, Channel 3 = PWRGD, Channel 4 = I_{OUT}

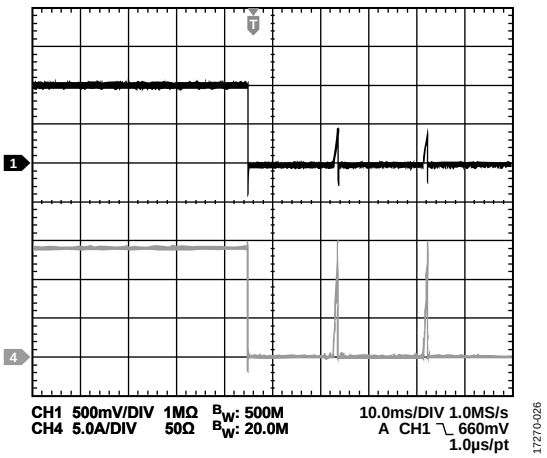


Figure 26. Channel 1/Channel 2 Short-Circuit Protection Entry, V_{IN} = 12 V, V_{OUT} = 1.0 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 6, Channel 1 = V_{OUT}, Channel 4 = I_{OUT}

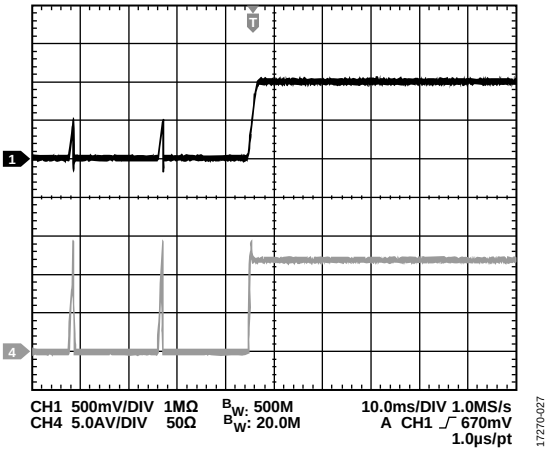


Figure 27. Channel 1/Channel 2 Short-Circuit Protection Recovery, V_{IN} = 12 V, V_{OUT} = 1.0 V, f_{SW} = 600 kHz, L = 1 µH, C_{OUT} = 47 µF × 6, Channel 1= V_{OUT}, Channel 4 = I_{OUT}

THEORY OF OPERATION

The ADP5056 is a power management unit that combines three high performance buck regulators in a 43-terminal LGA package to meet demanding performance and board space requirements. The device enables direct connection to high input voltages up to 18 V with no preregulators to make applications simpler and more efficient.

BUCK REGULATOR OPERATIONAL MODES

PWM Mode

In PWM mode, the buck regulators in the ADP5056 operate at a fixed frequency. An internal oscillator programmed by the RT pin sets this frequency. The ADP5056 uses the low-side MOSFET current for the PWM control, as shown in Figure 28. The valley current information is captured at the end of the off period and combines with the slope ramp to form the emulated current ramp voltage. The resistor from the RAMPx pin to ground controls the slope ramp voltage. At the start of each oscillator cycle, the high-side MOSFET turns on, and the inductor current increases until the emulated current ramp voltage crosses the COMPx voltage. When the current ramp voltage crosses the COMPx voltage, it turns off the high-side MOSFET and turns on the low-side MOSFET, which in turn places a negative voltage across the inductor, causing a reduction in the inductor current. The low-side MOSFET stays on for the remainder of the cycle.

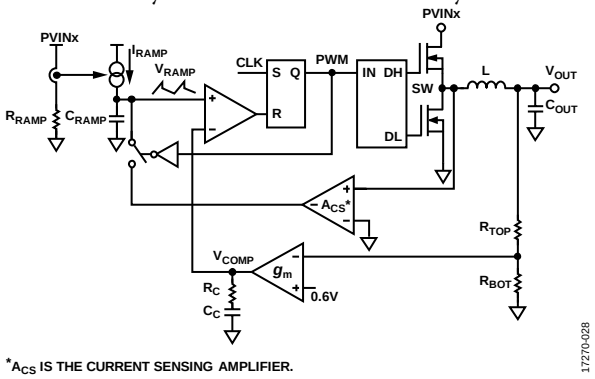


Figure 28. FlexMode™ PWM Control Architecture

PSM Mode

To achieve higher efficiency at light loads, the buck regulators in the ADP5056 smoothly transition to variable frequency PSM operation when the output load falls below the PSM current threshold. When the output voltage (V_{OUT}) falls below regulation, the buck regulator enters PWM mode for a few oscillator cycles until the voltage increases to within regulation. During the idle time between bursts, the MOSFET turns off, and the output capacitor supplies all the output current.

The PSM comparator monitors the internal compensation node, which represents the peak inductor current information. The average PSM current threshold depends on the V_{IN}, the V_{OUT}, the inductor, and the output capacitor. Because the output voltage occasionally falls below regulation and then recovers, the output voltage ripple in PSM operation is larger than the ripple in the FPWM mode of operation under light load conditions.

FPWM and Automatic PWM/PSM Modes

The buck regulators can be configured to always operate in FPWM mode using the SYNC/MODE pin. In FPWM mode, the regulator continues to operate at a fixed frequency even when the output current is below the PWM/PSM threshold. In FPWM mode, efficiency is lower compared to PSM mode under light load conditions. The low-side MOSFET remains on when the inductor current falls to less than 0 A, causing the ADP5056 to enter continuous conduction mode (CCM).

The buck regulators can be configured to operate in automatic PWM/PSM mode using the SYNC/MODE pin. In automatic PWM/PSM mode, the buck regulators operate in either PWM mode or PSM mode, depending on the output current. When the average output current falls below the PWM/PSM threshold, the buck regulator enters PSM mode operation. In PSM mode, the regulator operates with a reduced switching frequency to maintain high efficiency. The low-side MOSFET turns off when the inductor current reaches 0 A, causing the regulator to operate in discontinuous mode (DCM).

The user can alternate between FPWM mode and automatic PWM/PSM mode during operation. The flexible configuration capability during operation of the device enables efficient power management.

When a logic low level is applied to the SYNC/MODE pin, the operational mode of all three buck regulators is automatic PWM/PSM mode. When a logic high level is applied to the SYNC/MODE pin, the operational mode of all three buck regulators is FPWM mode.

ADJUSTABLE OUTPUT VOLTAGES

The ADP5056 provides an adjustable output voltage via an external resistor divider. For the adjustable output settings, use an external resistor divider to set the desired output voltage via the feedback reference voltage. The default reference voltage on each feedback pin is 600 mV for each channel.

INTERNAL REGULATORS (VREG)

The internal VREG regulator in the ADP5056 provides a stable 4.8 V power supply for the internal circuitry. Connect a 4.7 µF (X5R or X7R) ceramic capacitor between VREG and ground. The internal VREG regulator is always active as long as the VBIAS voltage is available.

SEPARATE SUPPLY APPLICATIONS

The ADP5056 supports separate input voltages for the three buck regulators, meaning that the input voltages for the three buck regulators can connect to different supply voltages. The ADP5056 integrates 100 nF, 25 V, X8L ceramic capacitors to provide local decoupling from PVIN1 and PVIN2 to power ground in Channel 1 and Channel 2.

The VBIAS voltage provides the power supply for the internal regulators and the control circuitry. Therefore, if the user plans

to use separate supply voltages for the buck regulators, the VBIAS voltage must be greater than the UVLO threshold before the other channels begin to operate.

Precision enabling can monitor the voltages of the PVIN1 pin, the PVIN2 pin, and the PVIN3 pin and to delay the startup of the outputs to ensure that the voltages of the PVIN1 pin, the PVIN2 pin, and the PVIN3 pin are high enough to support the outputs in regulation. For more information, see the Precision Enabling section.

The ADP5056 supports cascading supply operation for the three buck regulators. As shown in Figure 29, PVIN2 and PVIN3 are powered from the Channel 1 output. In this configuration, the Channel 1 output voltage must be higher than the UVLO threshold for PVIN2 and PVIN3.

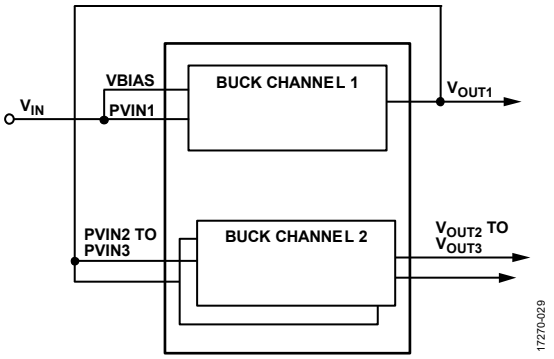


Figure 29. Cascading Supply Application

BOOTSTRAP CIRCUITRY

Each buck regulator in the ADP5056 has an integrated bootstrap regulator. The bootstrap regulator requires a 0.1 µF ceramic capacitor (X5R or X7R) between the BSTx pins and SWx pins to provide the gate drive voltage for the high-side MOSFET.

ACTIVE OUTPUT DISCHARGE SWITCH

Each buck regulator in the ADP5056 integrates a discharge switch from the switching node to ground. This switch is turned on when the associated regulator is disabled, which helps to discharge the output capacitor quickly. The typical value of the discharge switch is 85 Ω for Channel 1 to Channel 3.

PRECISION ENABLING

The ADP5056 has an enable control pin for each regulator. The enable control pin (ENx) features a precision enable circuit with a 0.615 V reference voltage. When the voltage at the ENx pin is greater than 0.615 V (typical high level threshold), the regulator is enabled. When the ENx pin voltage falls below 0.575 V (typical low level threshold), the regulator is disabled. The ADP5056 turns off the low-side MOSFET only after the inductor current reaches zero.

The precision enable pin has an internal pull-down current source (3.5 µA) that provides a default turn-off when the enable pin is left open. When the enable pin exceeds 0.615 V (typical), the regulator is enabled and the internal pull-down current source at the enable pin decreases to 0.9 µA. The precision enabling uses the ratio of the external resistor divider to program the UVLO threshold to monitor either input voltage or output voltage, while using the absolute value of the external resistor divider to program the hysteresis window. For more information, see the Programming the UVLO Input section.

To force the regulator to automatically start up when input power is applied, connect the enable pin to the VREG pin.

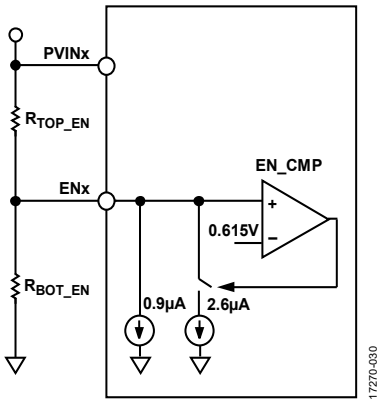


Figure 30. Precision Enable Diagram for One Channel

SEQUENCE MODE

The ADP5056 integrates the sequence control on each channel. When the ENx signal goes high, each channel controlled by the sequencer begins a soft start after the delay time (t_{EN_DLYx}) specified by the CFG2 pin setting (see Table 7). Similarly, when the ENx signal goes low, the channel turns off after the delay timer (t_{DIS_DLYx}). The turn on and turn off delay timer for all channels is designed in an opposite manner to meet typical system sequence requirements. The turn-on delay step is $3 \times t_{SET}$ timer, and the turn-off delay step is $6 \times t_{SET}$ timer, which provides the output with extra discharge time. The t_{SET} timer can be set to 2.6 ms or 20.8 ms by the CFG2 pin configuration. For example, when the CFG2 pin connects to 14.3 kΩ, the start-up sequence is set as Channel 1, Channel 2, and Channel 3. The enable delay of Channel 1, Channel 2, and Channel 3 are 0 ms, 7.8 ms, and 15.6 ms. The shutdown sequence is set as Channel 3, Channel 2, and Channel 1. The disable delay of Channel 1, Channel 2, and Channel 3 are 31.2 ms, 15.6 ms, and 0 ms. Figure 31 shows the logical states of each channel controlled by the grouped ENx signal, and it does not show soft start and output discharge ramps.

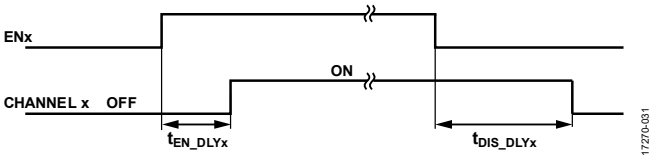


Figure 31. Sequencer Mode

OSCILLATOR

By connecting a resistor from the RT pin to ground, the f_{SW} of the ADP5056 can be set to a value between 250 kHz and 2500 kHz. Calculate the R_T resistor value in kΩ as follows:

$$R_T = \frac{167,305}{f_{SW}^{0.998}}$$

Figure 32 shows the typical relationship between the f_{SW} and the R_T resistor. The adjustable frequency allows users to make decisions based on the trade-off between efficiency and solution size.

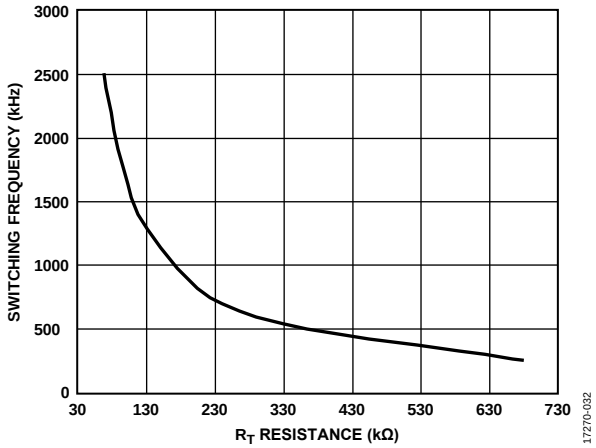


Figure 32. Switching Frequency vs. R_T Resistance

Out-Of-Phase Operation

By default, the phase shift between Channel 1, Channel 2, and Channel 3 is 120°. This value provides the benefits of out-of-phase operation by reducing the input ripple current and lowering the ground noise.

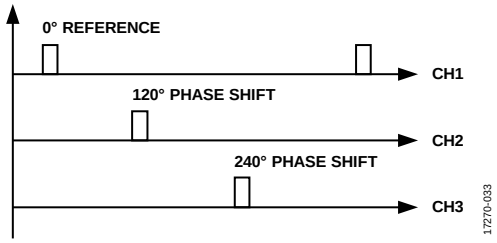


Figure 33. Phase Shift Diagram, Three Buck Regulators

In the in phase parallel operation configuration of Channel 1 and Channel 2, both channels operate in the same phase of Channel 1.

In the interleaved parallel operation configuration of Channel 1 and Channel 2, the phase shift between Channel 1, Channel 2, and Channel 3 is 0°, 180°, and 240°.

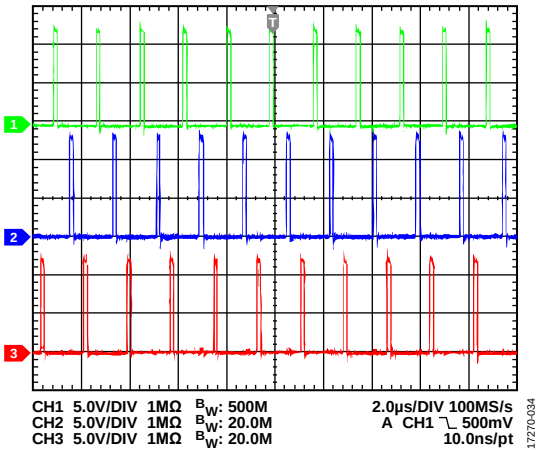


Figure 34. 120° Phase Shift Waveforms, Three Buck Regulators: Channel 1 = SW1, Channel 2 = SW2, Channel 3 = SW3

SYNCHRONIZATION INPUT/OUTPUT

The switching frequency of the ADP5056 can be synchronized to an external clock with a frequency range from 250 kHz to 2700 kHz. The ADP5056 automatically detects the presence of an external clock applied to the SYNC/MODE pin, and the switching frequency transitions smoothly to the frequency of the external clock. When the external clock signal stops, the device automatically switches back to the internal clock and continues to operate.

Note that the internal switching frequency set by the RT pin must be programmed to a value that is close to the external clock value for successful synchronization. The suggested frequency difference is less than ±15% in typical applications.

The SYNC/MODE pin can be configured as a synchronization clock output by the CFG1 pin (refer to Table 6). A positive clock pulse with a 50% duty cycle and VREG voltage level is generated at the SYNC/MODE pin with a frequency equal to the internal switching frequency set by the RT pin.

Figure 35 shows two ADP5056 devices configured for frequency synchronization mode. One ADP5056 device is configured as the clock output to synchronize another ADP5056 device.

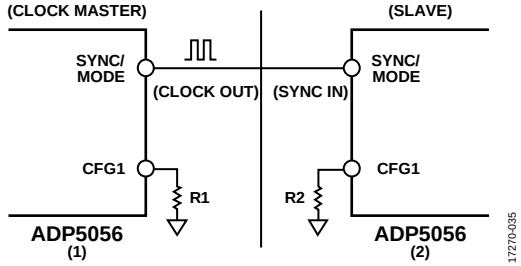


Figure 35. Two ADP5056 Devices Configured for Synchronization Mode

In the configuration shown in Figure 35, the phase shift between Channel 1 of the first ADP5056 device and Channel 1 of the second ADP5056 device is 0° (see Figure 36).

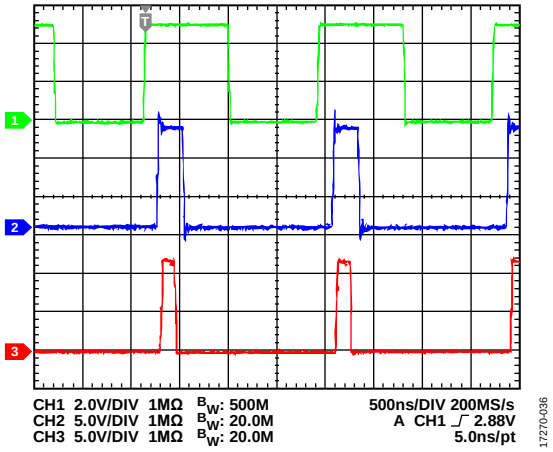


Figure 36. Waveforms of Two ADP5056 Devices Operating in Synchronization Mode, Channel 1 = Synchronization Clock Output of First ADP5056 Device, Channel 2 = SW1 of First ADP5056 Device, Channel 3 = SW1 of Second ADP5056 Device

SOFT START

The buck regulators in the ADP5056 include soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current. The soft start time for all channels is fixed at 0.83 × t_{SET} timer (2.2 ms or 17.3 ms, depending on R_{CFG2} value).

FUNCTION CONFIGURATIONS (CFG1 AND CFG2)

The ADP5056 includes the CFG1 pin and CFG2 pin to decode the function configurations for all channels. The logic statuses of each pin is decoded by connecting one resistor to ground. It is recommended to use ±1% resistor tolerance to achieve accurate decoding.

This decoder circuitry only works in the initiation stage of the ADP5056 when VBIAS passes the power-on reset (POR) threshold. Therefore, those configurations are latched into internal registers and cannot be changed in operation.

The CFG1 pin can be used to program the SYNC/MODE pin or CLKOUT, the load output capability, and parallel operation for all channels. Table 6 provides the values of R_{CFG1} needed to set different functionality in the CFG1 pin.

The CFG2 pin can be used to program the t_{SET} timer (2.6 ms or 20.8 ms), fast transient functionality, and sequence for the three channels. Table 7 provides the values of R_{CFG2} needed to set different functionality in the CFG2 pin.

Table 6. Configuration by the CFG1 Pin

R_{CFG1} (kΩ), ±1%	GPIO	Output Capability		
		Channel 1	Channel 2	Channel 3
0 (GND)	SYNC/MODE	7 A	7 A	3 A
14.3	SYNC/MODE	7 A	7 A	1.5 A
16.9	SYNC/MODE	7 A	3.5 A	3 A
20.0	SYNC/MODE	7 A	3.5 A	1.5 A
23.7	SYNC/MODE	Interleaved parallel (14 A)	Interleaved parallel (14 A)	3 A
Open	SYNC/MODE	3.5 A	3.5 A	1.5 A
32.4	SYNC/MODE	In phase parallel (14 A)	In phase parallel (14 A)	3 A
39.2	Clock output	7 A	7 A	3 A
47.5	Clock output	7 A	7 A	1.5 A
57.6	Clock output	7 A	3.5 A	3 A
71.5	Clock output	7 A	3.5 A	1.5 A
90.9	Clock output	3.5 A	7 A	3 A
127	Clock output	Interleaved parallel (14 A)	Interleaved parallel (14 A)	3 A
200	Clock output	3.5 A	3.5 A	1.5 A
511	Clock output	In phase parallel (14 A)	In phase parallel (14 A)	3 A

Table 7. Configuration by the CFG2 Pin

R_{CFG2} (kΩ), ±1%	t_{SET} timer (ms)	Fast Transient	Start-Up Sequence
0 (GND)	2.6	Disable	No delay
14.3	2.6	Disable	Channel 1, Channel 2, Channel 3
16.9	2.6	Disable	Channel 2, Channel 1, Channel 3
20	2.6	Disable	Channel 3, Channel 1, Channel 2
23.7	2.6	Enable	No delay
32.4	2.6	Enable	Channel 1, Channel 2, Channel 3
39.2	2.6	Enable	Channel 3, Channel 1, Channel 2
Open	20.8	Disable	No delay
47.5	20.8	Disable	Channel 1, Channel 2, Channel 3
57.6	20.8	Disable	Channel 2, Channel 1, Channel 3
71.5	20.8	Disable	Channel 3, Channel 1, Channel 2
90.9	20.8	Enable	No delay
127	20.8	Enable	Channel 1, Channel 2, Channel 3
200	20.8	Enable	Channel 2, Channel 1, Channel 3
511	20.8	Enable	Channel 3, Channel 1, Channel 2

PARALLEL OPERATION

The ADP5056 supports 2-phase parallel operation of Channel 1 and Channel 2 to provide a single output with up to 14 A of current. The ADP5056 includes two different parallel operation modes via the CFG1 pin configuration: in phase parallel operation and interleaved parallel operation.

In Phase Parallel Operation

In phase parallel operation parallels internal MOSFETs and driver circuitry between Channel 1 and Channel 2. In phase parallel operation treats Channel 1 as the control master, and the Channel 2 control stage is ignored. The in phase parallel operation mode uses a single inductor for external components and space saving. To configure Channel 1 and Channel 2 for in phase parallel single output operation, do the following (see Figure 37):

- Use the CFG1 pin to select in phase parallel operation, as specified in Table 6.
- Use the COMP1 pin as the compensation network.
- Use the FB1 pin to set the output voltage.
- Use the EN1 pin to enable the channel.
- Connect the FB2 pin to ground (FB2 is ignored).
- Leave the COMP2 pin open (COMP2 is ignored).
- Leave the RAMP2 pin open (RAMP2 is ignored).
- Connect the EN2 pin to ground (EN2 is ignored).

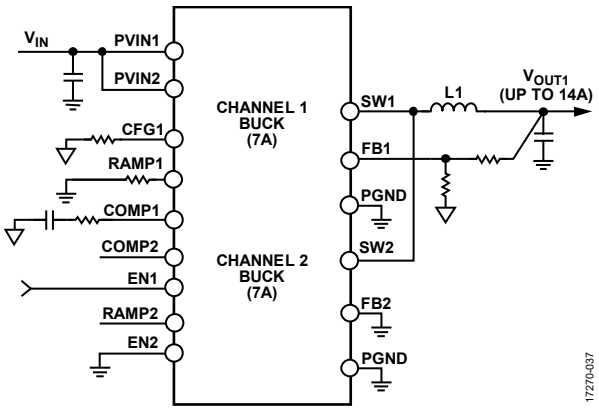


Figure 37. In Phase Parallel Operation for Channel 1 and Channel 2

Interleaved Parallel Operation

The ADP5056 supports 2-phase interleaved parallel operation of Channel 1 and Channel 2 to provide a single output with up to 14 A of current. In this mode, two channels operate in 180° out of phase operation and rely on an individual control loop to achieve current balance between the two channels. The interleaved parallel operation mode uses two inductors with the advantages of ripple current cancellation and higher equivalent switching frequency.

To configure a two-phase interleaved parallel operation, do the following (see Figure 38):

- Use the CFG1 pin to select interleaved parallel operation, as specified in Table 6.
- Use the COMP1 pin as the compensation network.
- Use the same RAMP1 and RAMP2 resistors.
- Use the FB1 pin to set the output voltage.
- Use the EN1 pin to enable the channel.
- Connect the FB2 pin to ground (FB2 is ignored).
- Leave the COMP2 pin open (COMP2 is ignored).
- Connect the EN2 pin to ground (EN2 is ignored).

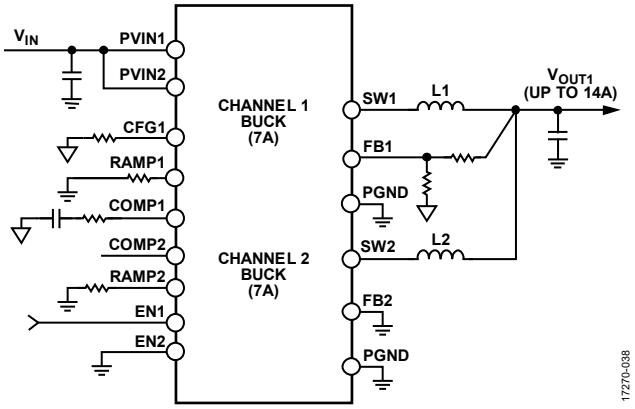


Figure 38. Interleaved Parallel Operation for Channel 1 and Channel 2

The current balance in parallel configuration is well balanced by careful designs of symmetrical printed circuit board (PCB) layout and circuitry designs. Figure 39 and Figure 40 show the typical current balance matching in the parallel output configuration.

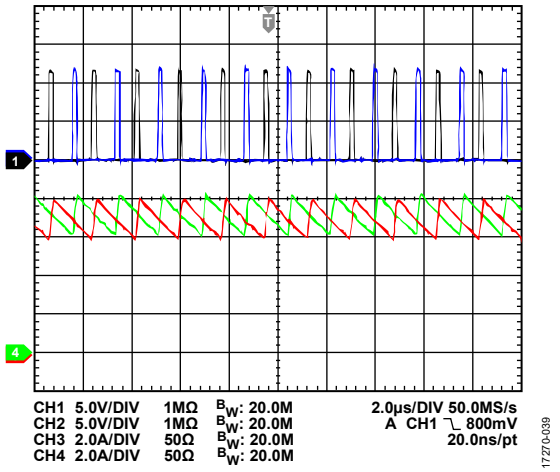


Figure 39. Steady State Waveform in Interleaved Parallel Output Configuration, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, FPWM Mode, Channel 1 = SW1, Channel 2 = SW2, Channel 3 = Current of Inductor L1, Channel 4 = Current of Inductor L2

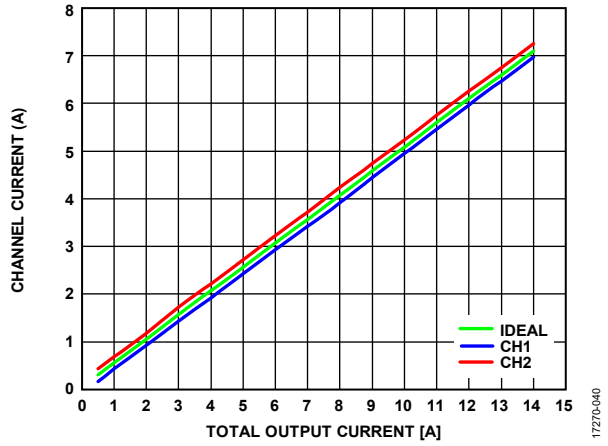


Figure 40. Current Balance in Interleaved Parallel Output Configuration, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, FPWM Mode

FAST TRANSIENT MODE

The ADP5056 includes fast transient response for large load step conditions. The ADP5056 feedback pin senses the output voltage to determine if a load step has occurred. When the output voltage falls below the specific threshold, the internal loop gain gradually increases to improve the load transient response speed. The fast enhanced transient threshold is at −2.5% × V_{OUT} with five times of nominal g_M, where g_M = 350 µA/V.

The CFG2 pin needs be programmable to turn on the fast transient mode.

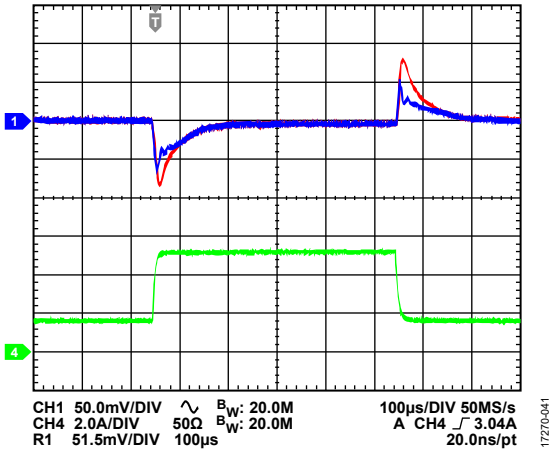


Figure 41. Enable or Disable Fast Transient Mode, Load Transient Comparison, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, FPWM Mode, Channel 1 = V_{OUT} with Fast Transient Mode Enable, Channel 3 = V_{OUT} with Fast Transient Mode Enable, Channel 4 = I_{OUT}

STARTUP WITH PRECHARGED OUTPUT

The buck regulators in the ADP5056 include a precharged start-up feature to protect the low-side FETs from damage during startup. If the output voltage is precharged before the regulator is turned on, the regulator prevents reverse inductor current (which discharges the output capacitor) until the internal soft start reference voltage exceeds the precharged voltage on the feedback (FBx) pin.

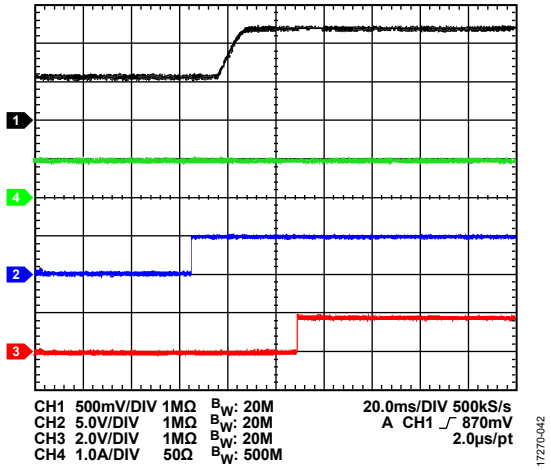


Figure 42. Channel 1 Startup with Precharged Ouput, V_{IN} = 12 V, V_{OUT} = 1.2 V, f_{SW} = 600 kHz, FPWM Mode, Channel 1 = V_{OUT}, Channel 2 = EN, Channel 3 = PWRGD, Channel 4 = I_{OUT}

CURRENT-LIMIT PROTECTION

The ADP5056 uses the emulated current ramp voltage for cycle by cycle current-limit protection to prevent current runaway. When the emulated current ramp voltage reaches the valley current-limit threshold plus the ramp voltage, the high-side MOSFET turns off and the low-side MOSFET turns on until the next cycle. If the overcurrent counter reaches 20, the device enters hiccup mode, and the ADP5056 turns off the low-side MOSFET only after the inductor current reaches zero. During hiccup mode, the high-side MOSFET and low-side MOSFET are both turned off. The device remains in this mode for seven soft start cycles and then attempts to restart with soft start. If the current-limit fault is cleared, the device resumes normal operation. Otherwise, the device re-enters hiccup mode.

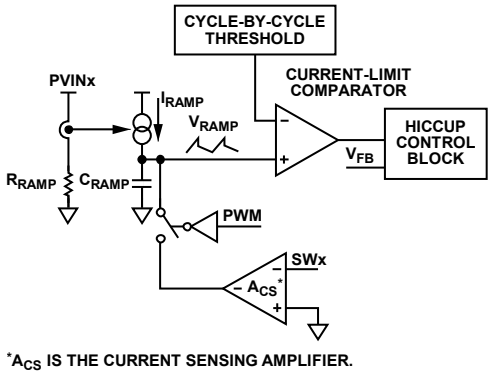


Figure 43. Current-Limit Circuitry

The buck regulators in the ADP5056 include negative current-limit protection circuitry to limit certain amounts of negative current flowing through the low-side MOSFET switch and high-side MOSFET body diode.

UVLO

Undervoltage lockout circuitry monitors both bias input voltage (VBIAS pin) and power input voltage level (PVINx pin) of each buck regulator in the ADP5056. If the power input voltage falls below 2.22 V (typical falling threshold), the corresponding channel is turned off. After the input voltage rises above 2.5 V (typical rising threshold), the soft start period initiates, and the corresponding channel enables when the ENx pin is high.

If the bias voltage falls below 3.8 V (typical falling threshold), all channels turn off. After the bias voltage rises above 4.2 V (typical rising threshold), a soft start initiates for each enabled channel.

POWER-GOOD FUNCTION

The ADP5056 includes an open-drain, power-good output (PWRGD pin) that becomes active high when the three buck regulators are operating normally. The PWRGD pin monitors the output voltage on three channels.

A logic high of the PWRGD signal indicates that the regulated output voltage of the buck regulator is above 95% (typical) and below 105% (typical) of the nominal output. When the regulated output voltage of the buck regulator falls below 93% (typical) or rises above 107% (typical) of the nominal output for a deglitched time greater than approximately four switching cycles, the PWRGD pin is set to 0.

The output of the PWRGD pin is the logical AND of the internal PWRGD signals on all channels. The output of the PWRGD pin becomes high after the t_{SET} delay and is 2.6 ms when the CFG2 pin is connected to ground. The t_{SET} timer can be increased by 8× using the CFG2 pin configuration. If one internal PWRGD signal fails, the PWRGD pin goes low with no delay.

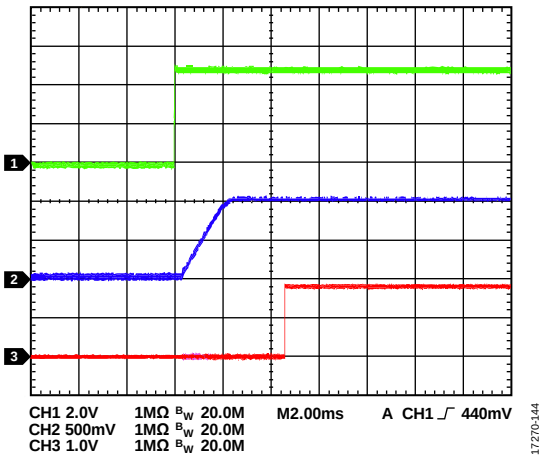


Figure 44. Power-Good Delay, V_{IN} = 12 V, V_{OUT} = 1.0 V, f_{SW} = 600 kHz, FPWM Mode, Channel 1 = EN, Channel 2 = V_{OUT}, Channel 3 = PWRGD

POWER-UP AT HIGH TEMPERATURE

Although the maximum operating junction temperature is 150°C, the ADP5056 has a lower temperature protection limit of 125°C by which the device must be powered up. This 125°C limit protects the internal nonvolatile memory, which is read on this initial power-up. Power-up is the condition of V_{BIAS} rising above $UVLO_{VBIAS}$. If power-up is attempted above 125°C, the devices does not allow operation until the temperature drops below 125°C. When this temperature is achieved and stored in the volatile memory, the device is ready for normal operation without the 125°C limit.

THERMAL SHUTDOWN

If the ADP5056 junction temperature exceeds 175°C, the thermal shutdown circuit turns off the IC, except for the internal linear regulators. The ADP5056 turns off the low-side MOSFET only after the inductor current reaches zero. Extreme junction temperatures can be the result of high current operation, poor circuit board design, or high ambient temperature. A 15°C hysteresis is included so that the ADP5056 does not return to operation after thermal shutdown until the on-chip temperature falls below 160°C. When the device exits thermal shutdown, a soft start is initiated for each enabled channel.

APPLICATIONS INFORMATION

PROGRAMMING THE ADJUSTABLE OUTPUT VOLTAGE

The output voltage of the ADP5056 is externally set by a resistive voltage divider from the output voltage to the FBx pin. To limit the degradation of the output voltage accuracy due to feedback bias current, ensure that the bottom resistor in the divider is not too large. A value of less than 50 kΩ is recommended.

The equation for the output voltage setting is

$$V_{OUT} = V_{REF} \times (1 + (R_{TOP}/R_{BOT}))$$

where:
V_{OUT} is the output voltage.
V_{REF} is the feedback reference voltage, 0.6 V for Channel 1 to Channel 3.
R_{TOP} is the feedback resistor from V_{OUT} to FBx.
R_{BOT} is the feedback resistor from FBx to ground.

VOLTAGE CONVERSION LIMITATIONS

For a given input voltage, upper and lower limitations on the output voltage exist due to the minimum on time and the minimum off time.

The minimum on time limits the output voltage for a given input voltage and switching frequency. The minimum on time for Channel 1 to Channel 3 is 50 ns (maximum).

In FPWM mode, Channel 1 and Channel 2 can skip the switching pulses to maintain the output regulation when the minimum on time limit is exceeded. Careful selection of switching frequency is required to avoid this condition.

To calculate the minimum output voltage in CCM for a given input voltage and switching frequency, use the following equation:

$$V_{OUT\_MIN} = V_{IN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT\_MIN} \times t_{MIN\_ON} \times f_{SW} - (R_{DSON\_LS} + R_L) \times I_{OUT\_MIN} \quad (1)$$

where:
V_{OUT_MIN} is the minimum output voltage.
V_{IN} is the input voltage.
t_{MIN_ON} is the minimum on time.
f_{SW} is the switching frequency.
R_{DSON_HS} is the on resistance of the high-side MOSFET.
R_{DSON_LS} is the on resistance of the low-side MOSFET.
I_{OUT_MIN} is the minimum output current.
R_L is the resistance of the output inductor.

The maximum output voltage for a given input voltage and switching frequency is limited by the minimum off time and the maximum duty cycle.

The maximum output voltage for a given input voltage and switching frequency can be calculated using the following equation:

$$V_{OUT\_MAX} = V_{IN} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_HS} - R_{DSON\_LS}) \times I_{OUT\_MAX} \times (1 - t_{MIN\_OFF} \times f_{SW}) - (R_{DSON\_LS} + R_L) \times I_{OUT\_MAX} \quad (2)$$

where:
t_{MIN_OFF} is the minimum off time.
I_{OUT_MAX} is the maximum output current.

As shown in Equation 1 and Equation 2, reducing the switching frequency eases the minimum on time and off time limitations.

CURRENT-LIMIT SETTING

The ADP5056 has two selectable current-limit thresholds for Channel 1, Channel 2, and Channel 3. Ensure that the selected current-limit value is larger than the peak current of the inductor (I_{PEAK}) for the current-limit configuration for all channels.

SOFT START SETTING

The buck regulators in the ADP5056 include soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current. To set the soft start time to a value of 2.2 ms or 17.3 ms, connect a resistor from the CFG2 pin to ground (see the Soft Start section).

INDUCTOR SELECTION

The inductor value is determined by the switching frequency, input voltage, output voltage, and inductor ripple current. Using a small inductor value yields faster transient response but may degrade efficiency due to the larger inductor ripple current. Using a large inductor value yields a smaller ripple current and improved efficiency but results in slower transient response. Thus, a trade-off must be made between transient response and efficiency. As a guideline, the inductor peak-to-peak ripple current, ΔI_L, is typically set to a value from 30% to 40% of the maximum load current. Use the following equation to calculate the inductor value:

$$L = ((V_{IN} - V_{OUT}) \times D)/(\Delta I_L \times f_{SW})$$

where:
V_{OUT} is the output voltage.
D is the duty cycle ($D = V_{OUT}/V_{IN}$).
ΔI_L is the inductor ripple current.

The ADP5056 has internal slope compensation in the current loop to prevent subharmonic oscillations when the duty cycle is greater than 50%.

Use the following equation to calculate the peak inductor current:

$$I_{PEAK} = I_{OUT} + (\Delta I_L/2)$$

The saturation current of the inductor must be larger than the peak inductor current. For ferrite core inductors with a fast saturation characteristic, ensure that the saturation current rating

of the inductor is higher than the current-limit threshold of the buck regulator to prevent the inductor from becoming saturated.

To avoid overheating and poor efficiency, an inductor must be chosen with an rms current rating that is greater than the calculated maximum rms current. Calculate the rms current of the inductor by using the following equation:

$$I_{RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}}$$

Shielded ferrite core materials are recommended for low core loss and low electromagnetic interference (EMI). Table 8 lists recommended inductors.

Table 8. Recommended Inductors

Vendor	Series[1]
Coilcraft	XAL5030, XEL5030
Toko	FDUE0650
Wurth	WE-HCI, WE-XHMI

[1] Visit the Coilcraft, Toko, and Wurth manufacturer websites for more information about the recommended series inductors.

OUTPUT CAPACITOR SELECTION

The selected output capacitor affects both the output voltage ripple and the loop dynamics of the regulator. For example, during load step transients on the output, when the load is suddenly increased, the output capacitor supplies the load until the control loop can ramp up the inductor current, causing an undershoot of the output voltage.

To calculate the output capacitance required to meet the undershoot (voltage droop) requirement, use the following equation:

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT\_UV}}$$

where:
K_{UV} is a factor (typically set to 2).
ΔI_{STEP} is the load step.
ΔV_{OUT_UV} is the allowable undershoot on the output voltage.

Another example of the effect of the output capacitor on the loop dynamics of the regulator is when the load is suddenly removed from the output and the energy stored in the inductor rushes into the output capacitor, causing an overshoot of the output voltage.

To calculate the output capacitance required to meet the overshoot requirement, use the following equation:

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}^2 \times L}{(V_{OUT} + \Delta V_{OUT\_OV})^2 - V_{OUT}^2}$$

where:
K_{OV} is a factor (typically set to 2).
ΔI_{STEP} is the load step.
ΔV_{OUT_OV} is the allowable overshoot on the output voltage.

The effective series resistance (ESR) of the output capacitor and the capacitance value of the output capacitor determine the output voltage ripple. Use the following equations to select output capacitors that can meet the output ripple requirements:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

where:
ΔI_L is the inductor ripple current.
ΔV_{OUT_RIPPLE} is the allowable output voltage ripple.
R_{ESR} is the equivalent series resistance of the output capacitor.

Select the largest output capacitance given by C_{OUT_UV}, C_{OUT_OV}, and C_{OUT_RIPPLE} to meet both load transient and output ripple requirements.

Ceramic capacitors have very low ESR and provide optimal ripple performance. For recommended starting values, see the Typical Application Circuits section. Use X5R or X7R type capacitors to achieve low output ripple and small output deviation during transient response. Transient performance can be improved with a higher value output capacitor and the addition of a feedforward capacitor placed between VOUTx and FBx. Increasing the output capacitance also decreases the output voltage ripple. A lower value output capacitor can be used to save space and cost, but transient performance suffers and may cause loop instability. See the Typical Application Circuits section for suggested capacitor values.

When choosing a capacitor, calculate the effective capacitance under the relevant operating conditions of voltage bias and temperature. A physically larger capacitor or a capacitor with a higher voltage rating may be required.

INPUT CAPACITOR SELECTION

The input decoupling capacitor attenuates high frequency noise on the input and acts as an energy reservoir. Use a ceramic capacitor and place it near to the PVINx pin. The loop composed of the input capacitor, the high-side MOSFET, and the low-side MOSFET must be kept as small as possible. The voltage rating of the input capacitor must be greater than the maximum input voltage. Ensure that the rms current rating of the input capacitor is larger than the following equation:

$$I_{C_{IN}\_rms} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

PROGRAMMING THE UVLO INPUT

The precision enable input can program the UVLO threshold of the input voltage, as shown in Figure 30.

The precision turn on threshold is 0.615 V, and the turn off threshold is 0.575 V. Use the following equations to calculate the resistive voltage divider for the programmable V_{IN} turn on voltage and the V_{IN} turn off voltage:

$$V_{IN\_RISING} = (3.5\ \mu A + 0.615\ V/R_{BOT\_EN}) \times R_{TOP\_EN} + 0.615\ V$$

$$V_{IN\_FALLING} = (0.9\ \mu A + 0.575\ V/R_{BOT\_EN}) \times R_{TOP\_EN} + 0.575\ V$$

where:
V_{IN_RISING} is the V_{IN} turn on voltage.
$V_{IN\_FALLING}$ is the V_{IN} turn off voltage.
R_{BOT_EN} is the resistor from ENx to ground.
R_{TOP_EN} is the resistor from V_{IN} to ENx.

SLOPE COMPENSATION SETTING

The slope compensation is necessary in a current mode control architecture to prevent subharmonic oscillation and to maintain a stable output. The ADP5056 uses the emulated current mode, and the slope compensation is implemented by connecting a resistor (R_{RAMPx}) from the RAMPx pin to ground.

Theoretically, an extra slope of $V_{OUT}/(2 \times L)$ is enough to stabilize the system. To guarantee that any noise is decimated in one cycle and the system is stable from subharmonic oscillation, the ADP5056 uses an extra slope of V_{OUT}/L.

Calculate the ramp resistor values, R_{RAMPx}, in kΩ, by using the following equations:

$$R_{RAMP1} = L1 \times 500$$

$$R_{RAMP2} = L2 \times 500$$

$$R_{RAMP3} = L3 \times 226$$

where $L1$, $L2$, and $L3$ are the inductor values in each channel, in µH.

COMPENSATION COMPONENTS DESIGN

For current mode control, the power stage can be simplified as a voltage controlled current source that supplies current to the output capacitor and load resistor. The simplified loop is composed of one domain pole and a zero contributed by the output capacitor ESR. The control-to-output transfer function is shown in the following equations:

$$G_{vd}(s) = \frac{V_{OUT}(s)}{V_{COMP}(s)} = A_{VI} \times R \times \frac{\left(1 + \frac{s}{2 \times \pi \times f_z}\right)}{\left(1 + \frac{s}{2 \times \pi \times f_p}\right)}$$

where:
s is the domain in the control to output transfer function.
A_{VI} = 12.5 A/V for Channel 1 and Channel 2, 5 A/V for Channel 3.
R is the load resistance.
f_z is the zero frequency.
f_p is the pole frequency.

$$f_z = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}}$$

$$f_p = \frac{1}{2 \times \pi \times (R + R_{ESR}) \times C_{OUT}}$$

where C_{OUT} is the output capacitance.

The ADP5056 uses a transconductance amplifier as the error amplifier to compensate the system. Figure 45 shows the simplified peak current mode control small signal circuit.

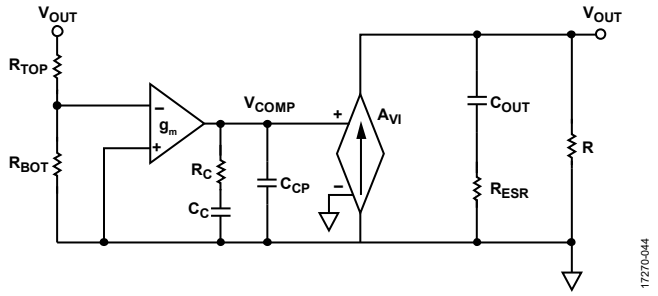


Figure 45. Simplified Peak Current Mode Control Small Signal Circuit

The compensation components, R_C and C_C, contribute a zero. R_C and the optional C_{CP} contribute an optional pole.

The closed-loop transfer equation is as follows:

$$T_V(s) = \frac{R_{BOT}}{R_{BOT} + R_{TOP}} \times \frac{-g_m}{C_C + C_{CP}} \times \frac{1 + R_C \times C_C \times s}{s \times \left(1 + \frac{R_C \times C_C \times C_{CP}}{C_C + C_{CP}} \times s\right)} \times G_{vd}(s)$$

The following guidelines show how to select the compensation components—R_C, C_C, and C_{CP}—for ceramic output capacitor applications.

1. Determine the cross frequency (f_C). Generally, f_C is between $f_{SW}/12$ and $f_{SW}/6$.
2. Calculate R_C using the following equation:

$$R_C = \frac{2 \times \pi \times V_{OUT} \times C_{OUT} \times f_C}{0.6 \times g_m \times A_{VI}}$$

3. Place the compensation zero at the domain pole (f_P). Calculate C_C using the following equation:

$$C_C = \frac{(R + R_{ESR}) \times C_{OUT}}{R_C}$$

4. C_{CP} is optional. C_{CP} can be used to cancel the zero caused by the ESR of the output capacitor. Calculate C_{CP} using the following equation:

$$C_{CP} = \frac{R_{ESR} \times C_{OUT}}{R_C}$$

POWER DISSIPATION

The total power dissipation in the ADP5056 simplifies to

$$P_D = P_{BUCK1} + P_{BUCK2} + P_{BUCK3}$$

where:
P_D is the power dissipation in the package.
P_{BUCK1} is the power dissipation of Channel 1.
P_{BUCK2} is the power dissipation of Channel 2.
P_{BUCK3} is the power dissipation of Channel 3.

Buck Regulator Power Dissipation

The power dissipation (P_{LOSS}) for each buck regulator includes power switch conduction losses (P_{COND}), switching losses (P_{SW}), and transition losses (P_{TRAN}). Other sources of power dissipation exist, but these sources are generally less significant at the high output currents of the application thermal limit.

Use the following equation to estimate the power dissipation of the buck regulator:

$$P_{LOSS} = P_{COND} + P_{SW} + P_{TRAN}$$

Power Switch Conduction Loss (P_{COND})

Power switch conduction losses are caused by the flow of output current through both the high-side and low-side power switches. Each of these switches has internal on resistance (R_{DSON}).

Use the following equation to estimate the power switch conduction loss:

$$P_{COND} = (R_{DSON\_HS} \times D + R_{DSON\_LS} \times (1 - D)) \times I_{OUT}^2$$

where:
R_{DSON_HS} is the on resistance of the high-side MOSFET.
R_{DSON_LS} is the on resistance of the low-side MOSFET.

Switching Loss (P_{SW})

Switching losses are associated with the current drawn by the driver to turn the power devices on and off at the switching frequency. Each time a power device gate is turned on or off, the driver transfers a charge from the input supply to the gate, and then from the gate to ground. Use the following equation to estimate the switching loss:

$$P_{SW} = (C_{GATE\_HS} + C_{GATE\_LS}) \times V_{IN}^2 \times f_{SW}$$

where:
C_{GATE_HS} is the gate capacitance of the high-side MOSFET.
C_{GATE_LS} is the gate capacitance of the low-side MOSFET.

Transition Loss (P_{TRAN})

Transition losses occur because the high-side MOSFET cannot turn on or off instantaneously. During a switch node transition, the MOSFET provides all the inductor current. The source to drain voltage of the MOSFET is half the input voltage, resulting in power loss. Transition losses increase with both load and input voltage and occur twice for each switching cycle. Use the following equation to estimate the transition loss:

$$P_{TRAN} = 0.5 \times V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}$$

where:
t_R is the rise time of the switch node.
t_F is the fall time of the switch node.

JUNCTION TEMPERATURE

The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to power dissipation, as shown in the following equation:

$$T_J = T_A + T_R$$

where:
T_J is the junction temperature.
T_A is the ambient temperature.
T_R is the rise in temperature of the package due to power dissipation.

The rise in temperature of the package is directly proportional to the power dissipation in the package. The proportionality constant for this relationship is the thermal resistance from the junction of the die to the ambient temperature, as shown in the following equation:

$$T_R = \theta_{JA} \times P_D$$

where:
θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature of the package (see Table 4).

An important factor to consider is that the thermal resistance value is based on a 4-layer, 4 inch × 3 inch PCB with 2.5 oz. of copper, as specified in the JEDEC standard, whereas real-world applications may use PCBs with different dimensions and a different number of layers.

It is important to maximize the amount of copper used to remove heat from the device. Copper exposed to air dissipates heat better than copper used in the inner layers. Connect Pin 35, Pin 36, and Pin 37 to the ground plane with the maximum number of vias.

TYPICAL APPLICATION CIRCUITS

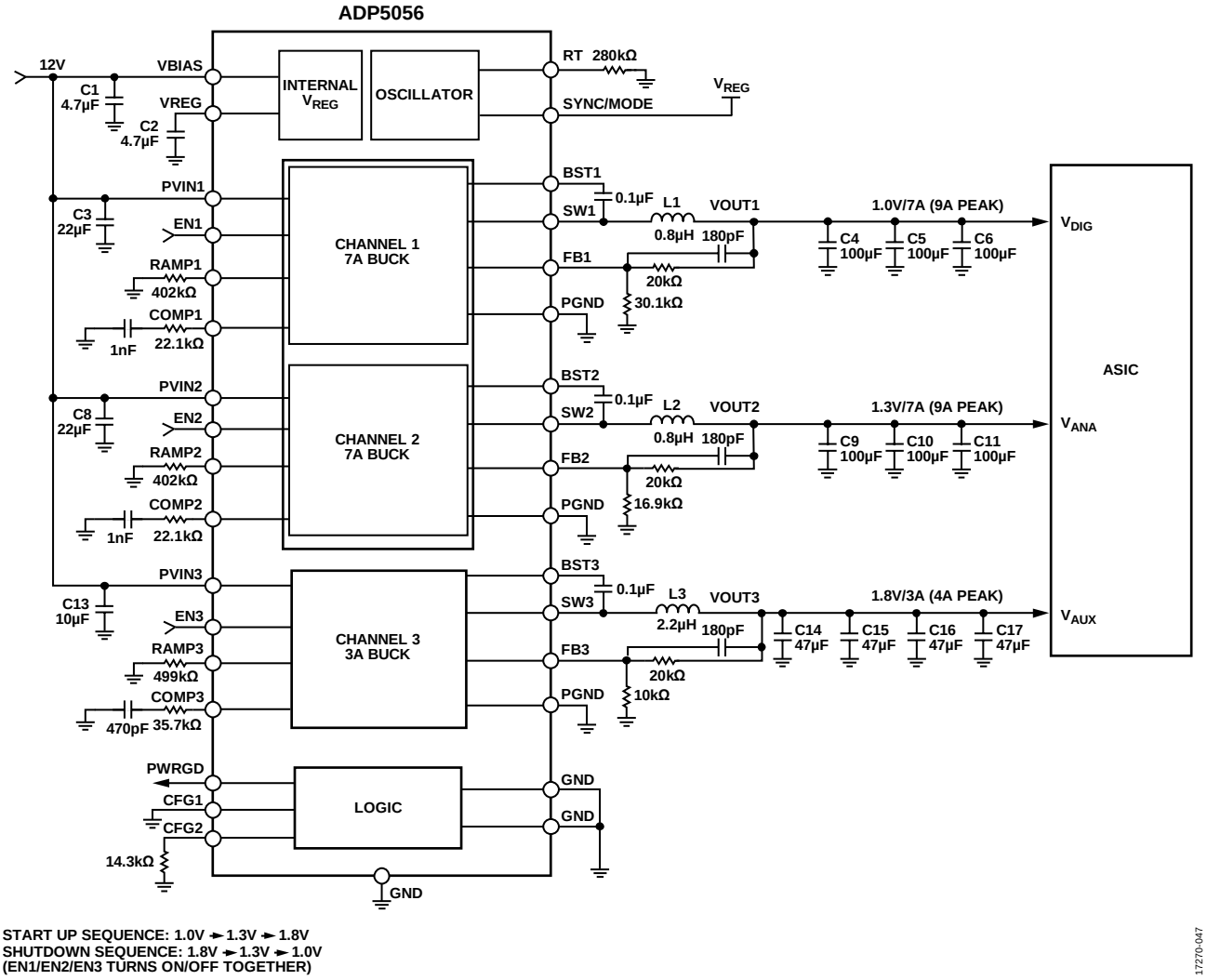


Figure 46. Typical Application, 12 V Input, f_{SW} = 600 kHz, V_{OUT1} = 1.0 V, V_{OUT2} = 1.3 V, V_{OUT3} = 1.8 V, Sequence Mode

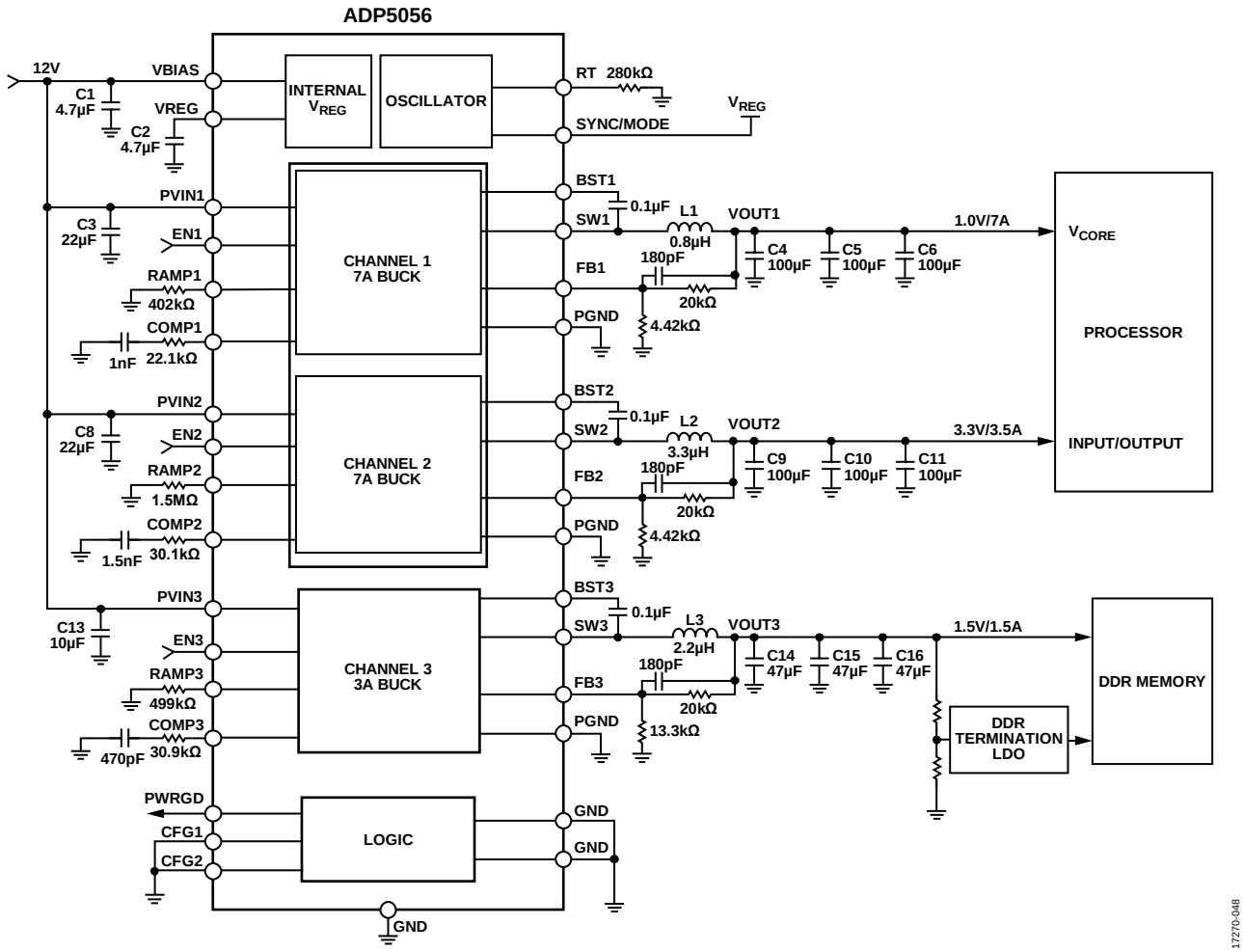


Figure 47. Typical Application, 12 V Input, f_{SW} = 600 kHz, V_{OUT1} = 1.0 V, V_{OUT2} = 3.3 V, V_{OUT3} = 1.5 V

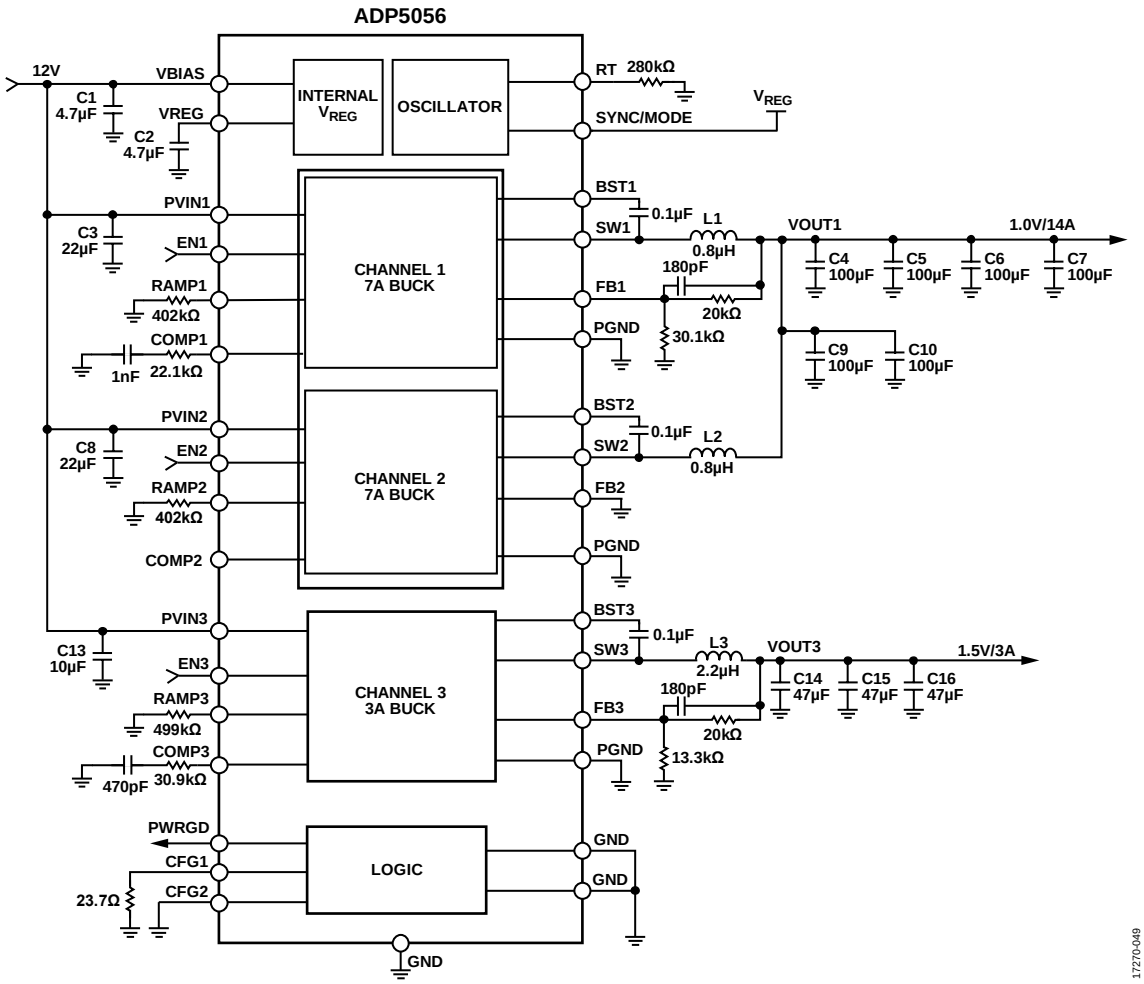


Figure 48. Typical Channel 1/Channel 2 Interleaved Parallel Application, 12 V Input, f_{SW} = 600 kHz, V_{OUT1} = 1.0 V, V_{OUT3} = 1.5 V

DESIGN EXAMPLE

This section provides an example of the step by step design procedures and the external components required for Channel 1. Table 9 lists the design requirements for this example.

Table 9. Example Design Requirements for Channel 1

Parameter	Specification
Input Voltage	V_{PVIN1} = 12 V ± 5%
Output Voltage	V_{OUT1} = 1.2 V
Output Current	I_{OUT1} = 7 A
Output Ripple	ΔV_{OUT1_RIPPLE} = 12 mV in CCM mode
Load Transient	±5% at 25% to 75% load transient, 1 A/µs

Although this example shows step by step design procedures for Channel 1, the procedures apply to all other buck regulator channels (Channel 1 to Channel 3).

SETTING THE SWITCHING FREQUENCY

The first step is to determine the switching frequency for the ADP5056 design. In general, higher switching frequencies produce a smaller solution size due to the lower component values required, whereas lower switching frequencies result in higher conversion efficiency due to lower switching losses.

The switching frequency of the ADP5056 can be set to a value from 250 kHz to 2500 kHz by connecting a resistor from the RT pin to ground. The selected resistor allows the user to make decisions based on the trade-off between efficiency and solution size.

However, the highest supported switching frequency must be assessed by checking the voltage conversion limitations enforced by the minimum on time and the minimum off time (see the Voltage Conversion Limitations section).

In this design example, a switching frequency of 600 kHz is used to achieve an optimal combination of small solution size and high conversion efficiency. To set the switching frequency to 600 kHz and calculate the value of the resistor from the RT pin to ground, R_T, use the following equations:

$$R_T(\text{k}\Omega) = \frac{167{,}305}{f_{SW}(\text{kHz})^{0.998}}$$

$$R_T(\text{k}\Omega) = \frac{167{,}305}{600^{0.998}} = 280\ \text{k}\Omega$$

Therefore, select the closest standard 1% resistor value for R_T = 280 kΩ.

SETTING THE OUTPUT VOLTAGE

Select a 10 kΩ bottom resistor (R_{BOT}) and then calculate the top feedback resistor by using the following equation:

$$R_{BOT} = R_{TOP} \times (V_{REF}/(V_{OUT} - V_{REF}))$$

where V_{REF} is 0.6 V for Channel 1.

To set the output voltage to 1.2 V, choose the following resistor values: R_{TOP} = 10 kΩ, R_{BOT} = 10 kΩ.

SETTING THE CONFIGURATIONS (CFG1 AND CFG2)

The CFG1 pin can program the load output capability and parallel operation for all channels. For this example, choose R_{CFG1} = 0 Ω (see Table 6).

The CFG2 pin can program the t_{SET} timer (2.6 ms or 20.8 ms), fast transient functionality, and sequence for the ADP5056. For this example, choose R_{CFG2} = 0 Ω (see Table 7).

SELECTING THE INDUCTOR

The peak-to-peak ΔI_L is set to 35% of the maximum output current. Use the following equation to estimate the value of the inductor:

$$L = ((V_{IN} - V_{OUT}) \times D)/(\Delta I_L \times f_{SW})$$

where:
V_{IN} = 12 V.
V_{OUT} = 1.2 V.
D is the duty cycle ($D = V_{OUT}/V_{IN}$ = 0.1).
ΔI_L = 35% × 7 A = 2.45 A.
f_{SW} = 600 kHz.

The resulting value for L is 0.73 µH. The closest standard inductor value is 0.8 µH. Therefore, ΔI_L is 2.25 A.

Calculate the peak inductor current by using the following equation:

$$I_{PEAK} = I_{OUT} + (\Delta I_L/2)$$

The calculated peak current for the inductor is 8.125 A.

Use the following equation to calculate the rms current of the inductor:

$$I_{RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I_L^2}{12}}$$

The rms current of the inductor is approximately 7.03 A.

Therefore, an inductor with a minimum rms current rating of 7.03 A and a minimum saturation current rating of 8.125 A is required. However, to prevent the inductor from reaching the saturation point in current-limit conditions, it is recommended that the inductor saturation current be higher than the maximum peak current limit, typically 11.65 A, for reliable operation.

Based on these requirements and recommendations, the XAL5030-801ME, with a dc resistance of 5.14 mΩ, was selected for this design.

SELECTING THE OUTPUT CAPACITOR

The output capacitor must meet the output voltage ripple and load transient requirements. To meet the output voltage ripple requirement, use the following equations to calculate the ESR and capacitance:

$$C_{OUT\_RIPPLE} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT\_RIPPLE}}$$

$$R_{ESR} = \frac{\Delta V_{OUT\_RIPPLE}}{\Delta I_L}$$

The calculated capacitance, C_{OUT_RIPPLE}, is 39 µF, and the calculated R_{ESR} is 5.3 mΩ.

To meet the ±5% overshoot and undershoot requirements, use the following equations to calculate the capacitance:

$$C_{OUT\_UV} = \frac{K_{UV} \times \Delta I_{STEP}{}^2 \times L}{2 \times \left(V_{IN} - V_{OUT}\right) \times \Delta V_{OUT\_UV}}$$

$$C_{OUT\_OV} = \frac{K_{OV} \times \Delta I_{STEP}{}^2 \times L}{\left(V_{OUT} + \Delta V_{OUT\_OV}\right)^2 - V_{OUT}{}^2}$$

For estimation purposes, use $K_{OV} = K_{UV} = 2$. Therefore, $C_{OUT\_OV} = 133$ µF and $C_{OUT\_UV} = 15.1$ µF.

The ESR of the output capacitor must be less than 5.3 mΩ, and the output capacitance must be greater than 133 µF. It is recommended that three ceramic capacitors be used (47 µF, X5R, and 6.3 V), such as the GRM21BR60J476ME15 from Murata with an ESR of 2 mΩ.

DESIGNING THE COMPENSATION NETWORK

For improved load transient and stability performance, set the f_C to $f_{SW}/10$. In this example, f_{SW} is set to 600 kHz. Therefore, f_C is set to 60 kHz.

For the 1.2 V output rail, the 47 µF ceramic output capacitor has a derated value of 40 µF.

Choose standard components: $R_C = 24.9$ kΩ and $C_C = 1$ nF. C_{CP} is optional.

Figure 49 shows the Bode plot for the 1.2 V output rail. The cross frequency is 58 kHz, and the phase margin is 63°.

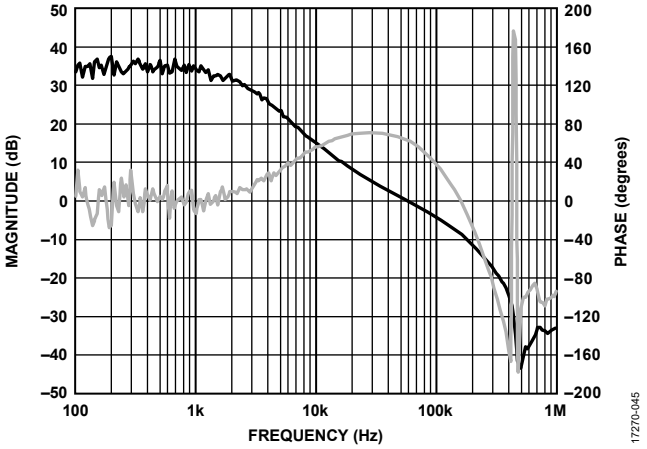


Figure 49. Bode Plot for 1.2 V Output

SELECTING THE INPUT CAPACITOR

For the input capacitor, select a ceramic capacitor with a minimum value of 10 µF. Place the input capacitor near to the PVIN1 pin. In this example, one 10 µF, X5R, 25 V ceramic capacitor is recommended.

CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Optimal circuit board layout is essential to obtain the best performance from the ADP5056 (see Figure 50). Poor layout can affect the regulation and stability of the device, as well as the EMI and electromagnetic compatibility (EMC) performance. Refer to the following guidelines for an optimal PCB layout:

- Place the input capacitor, inductor, output capacitor, and bootstrap capacitor near to the IC.
- Use short, thick traces to connect the input capacitors to the PVINx pins, and use dedicated power ground to connect the input and output capacitor grounds to minimize the connection length.
- Use several high current vias, if required, to connect PVINx and PGND to other power planes.
- Use short, thick traces to connect the inductors to the SWx pins and the output capacitors.
- Ensure that the high current loop traces are as short and wide as possible.
- Maximize the amount of ground metal connecting Pin 35, Pin 36, and Pin 37, and use as many vias as possible on the component side to improve thermal dissipation.
- Use a ground plane with several vias connecting to the component side ground to further reduce noise interference on sensitive circuit nodes.
- Place the decoupling capacitors near to the VREG pin and VBIAS pin.
- Place the frequency setting resistor near to the RT pin.
- Place the feedback resistor divider near to the FBx pin. In addition, keep the FBx traces away from the high current traces and the switch node to avoid noise pickup.
- Use size 0402 or 0603 resistors and capacitors to achieve the smallest possible footprint solution on boards where space is limited.

For recommended PCB assembly and manufacturing procedures, visit the µModule® design and manufacturing resources page.

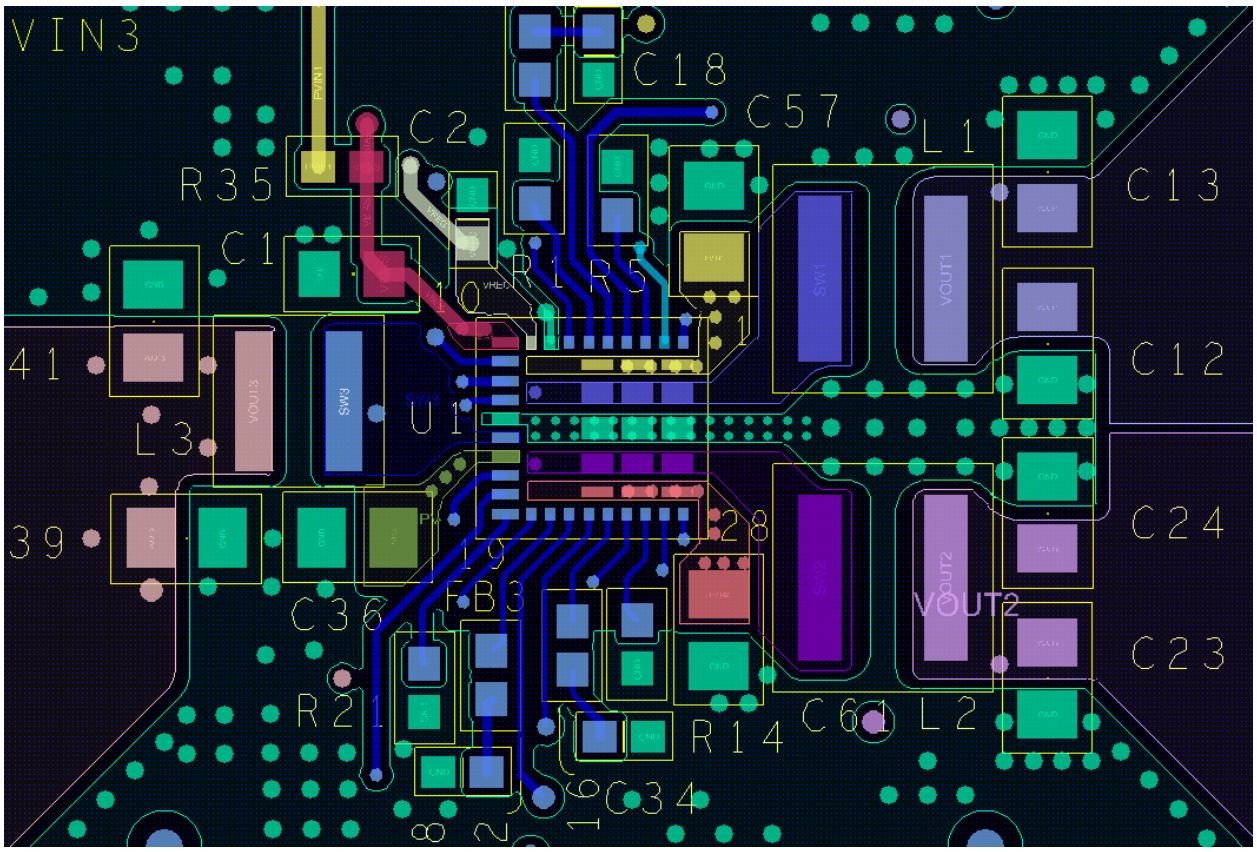


Figure 50. Typical PCB Layout for the ADP5056

OUTLINE DIMENSIONS

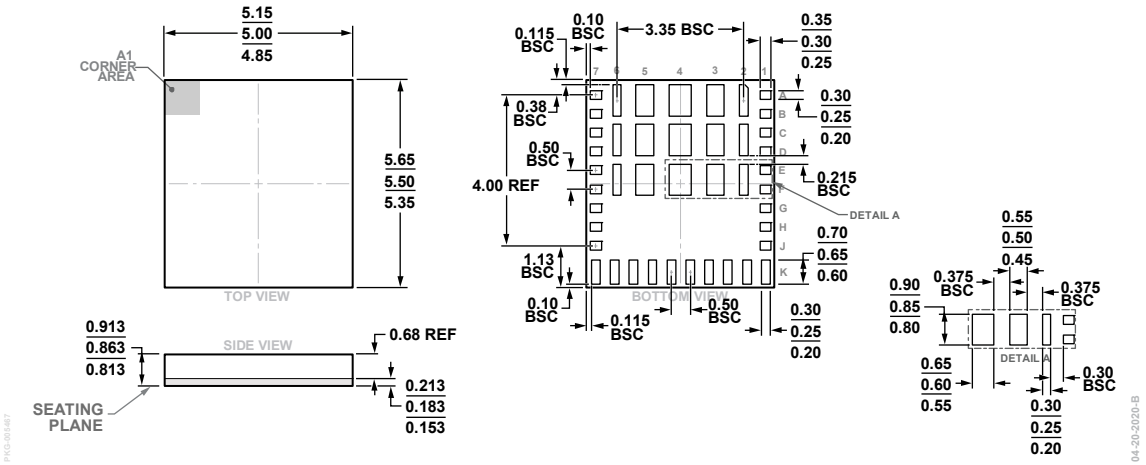


Figure 51. 43-Terminal Land Grid Array [LGA]
(CC-43-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADP5056ACCZ-R7	−40°C to +150°C	43-Terminal Land Grid Array [LGA]	CC-43-1
ADP5056-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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Analog Devices Inc.:

ADP5056ACCZ-R7 ADP5056-EVALZ