K Band Quadrature Demodulator with Integrated Fractional-N PLL and VCO

FEATURES

- Fractional-N synthesizer with low phase noise VCO
- K band quadrature demodulator
- Programmable via 4-wire SPI
- RF operating frequency range: 17 GHz to 22 GHz
- LO internal frequency range: 17 GHz to 21.5 GHz
- Double sideband noise figure: 5 dB at maximum conversion gain
- Output integrated phase noise, 1 kHz to 10 MHz: <1°
- Maximum conversion gain of >50 dB
- Conversion gain control range of >50 dB
- IM3 of −54 dBc at −30 dBm composite input level, Δf_{RF} = 1 MHz
- 3 baseband, SPI-selectable LPFs with corner frequencies of: 125 MHz, 250 MHz, and 500 MHz on each baseband path

APPLICATIONS

- Satellite communications

FUNCTIONAL BLOCK DIAGRAM

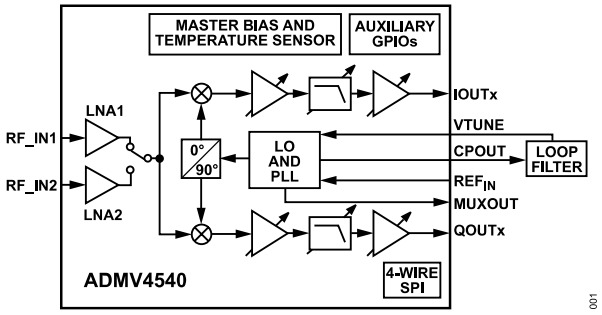

Figure 1.

GENERAL DESCRIPTION

The ADMV4540 is a highly integrated quadrature demodulator with integrated synthesizer ideally suited for next generation K band satellite communication.

The RF front end of the ADMV4540 consists of two low noise amplifier (LNA) paths, each with an optimal cascaded, 5 dB, double sideband noise figure at maximum gain, while minimizing external components. The dual paths allow support for antenna polarization. Selection of the LNA path can be done through the SPI.

The LNA output is then downconverted to baseband using an inphase and quadrature (I/Q) mixer. The I/Q mixer output is then fed into fully differential low noise and low distortion programmable filters and variable gain amplifiers (VGAs). Each channel is capable of rejecting large, out of band interferers while reliably boosting the wanted signal, thus reducing the bandwidth and resolution requirements on the analog-to-digital converters (ADCs) of the system. The excellent matching between channels and their high spurious-free dynamic range (SFDR) over all gain and bandwidth settings make the ADMV4540 ideal for satellite communication systems with dense constellations, multiple carriers, and nearby interferers.

The three filter corners of 125 MHz, 250 MHz, and 500 MHz are all programmable via a serial peripheral interface (SPI). The filters provide a sixth-order Butterworth response with −3 dB corner frequencies of 141 MHz, 282 MHz, and 565 MHz. For operation beyond 565 MHz, the filter can be disabled and completely bypassed, thereby extending the −3 dB bandwidth up to 900 MHz.

The high dynamic range baseband output amplifiers of the ADMV4540 provide an overall nominal conversion gain of 57 dB. The three baseband voltage variable attenuator (VVA) pins (VCTRL_BBVVAx) of the ADMV4540 can be used for automatic gain control (AGC), giving the ADMV4540 a wide RF input dynamic range.

This feature rich device contains an integrated fractional-N phase-locked loop (PLL) and a low phase noise voltage controlled oscillator (VCO) that generates the necessary on-chip local oscillator (LO) signal for the two double balanced I/Q mixers, eliminating the need for external frequency synthesis. The VCO utilizes an internal automatic calibration routine that allows the PLL to select the necessary settings and lock.

The reference input (REF_{IN}) to the PLL of the ADMV4540 employs a differentially excited crystal oscillator at 50 MHz. Alternatively, the REF_{IN} can be driven by an external single-ended frequency reference up to 100 MHz. The phase frequency detector (PFD) comparison frequency operates up to 100 MHz, which allows for continuous LO coverage from 17 GHz to 21.5 GHz in extremely fine steps.

The ADMV4540 operates on a 3.3 V supply with less than 3.2 W of total power dissipation. It is available in a 48-terminal, RoHS compliant, 7 mm × 7 mm LGA package with an exposed paddle. The ADMV4540 can operate over the −40°C to +85°C temperature range on a + 3.3 V power supply.

TABLE OF CONTENTS

TABLE OF CONTENTS

REVISION HISTORY

10/2021—Revision 0: Initial Version

SPECIFICATIONS

Supply voltage (V_{CC}) = 3.3 V, and T_A = 25°C, unless otherwise noted.

A 50 Ω source input impedance with a single-ended input drive was used, and the evaluation board RF traces were deembedded until the RF_INx pin.

The performance metrics were per the I channel and Q channel, the evaluation board I channel and Q channel traces were deembedded until the I channel and Q channel pins, the I channel and Q channel outputs were ac-coupled with a 1 µF capacitor on each channel output, the I channel and Q channel positive and negative outputs were combined with a 180° balun, and BB_AMP1_GAIN_x = 0, unless otherwise stated.

PLL filter bandwidth = 220 kHz with 60° of phase margin, reference frequency (f_{REF}) = 50 MHz, DOUBLER_EN = 1, PFD frequency (f_{PFD}) = 100 MHz, and the external reference power is set to 3 dBm for the single-ended external reference, unless otherwise stated.

VCTRL_BBVVA1 = 3.3 V, VCTRL_BBVVA2 and VCTRL_BBVA3 are used for automatic gain control (AGC), and the total output power for the I channel and Q channel is set to be −10 dBm each, unless otherwise stated.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT INTERFACE	RF_IN1 and RF_IN2				
Operating Frequency		17		22	GHz
Return Loss	Single-ended input drive		12		dB
Nominal Input Impedance	Single-ended input drive		50		Ω
Composite Carrier Input Power					
Minimum	Input carrier bandwidth of 250 MHz		−66		dBm
Maximum	Input carrier bandwidth of 1 GHz		−30		dBm
RF1 to RF 2 Isolation			>25		dB
SYNTHESIZER					
LO Internal Frequency		17		21.5	GHz
PFD Frequency (f_{PFD})				100	MHz
VCO Tuning Sensitivity (K_{VCO})			190		MHz/V
VTUNE		1	1.5	2	V
MUXOUT		0		V_{CC}	V
Charge Pump Current (I_{CP})		0.3		4.8	mA
CLOSED-LOOP PHASE NOISE	f_{REF} = 50 MHz, f_{PFD} = 100 MHz, CP_CURRENT = 4, BICP = 4, PLL filter bandwidth = 220 kHz with 58° of phase margin, and f_{REF} = 50 MHz, see Loop Filter section				
1 kHz Offset			−84		dBc/Hz
10 kHz Offset			−96		dBc/Hz
100 kHz Offset			−98		dBc/Hz
1 MHz Offset			−115		dBc/Hz
10 MHz Offset			−128		dBc/Hz
Output Integrated Phase Noise	Integrated from 1 kHz and 10 MHz		0.8		°RMS
BASEBAND I/Q INTERFACE					
I/Q Output Voltage	Differential on I and Q		200		mV p-p
I/Q Output Impedance	Differential on I and Q		100		Ω
I/Q Amplitude Imbalance			±0.5		dB
I/Q Phase Imbalance			1.6		Degrees
Return Loss	Differential return loss on I and Q		10		dB
BASEBAND LOW-PASS FILTERS (LPFs)					
125 MHz SPI-Selectable LPF	Register 0x13C = 0x00				
3 dB Filter Bandwidth			140		MHz
2 × 3 dB Bandwidth Rejection			35		dB
Group Delay Variation			1.6		ns
3 dB Bandwidth Tolerance			±10		%

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
250 MHz SPI-Selectable LPF	Register 0x13C = 0x05				
3 dB Filter Bandwidth			285		MHz
2 × 3 dB Bandwidth Rejection			35		dB
Group Delay Variation			1.4		ns
3 dB Bandwidth Tolerance			±10		%
500 MHz SPI-Selectable LPF	Register 0x13C = 0x0A				
3 dB Filter Bandwidth			565		MHz
2 × 3 dB Bandwidth Rejection			35		dB
Group Delay Variation			1		ns
3 dB Bandwidth Tolerance			±10		%
Bypass SPI-Selectable LPF	Register 0x13C = 0x0F				
3dB Filter Bandwidth			900		MHz
2 × 3 dB Bandwidth Rejection			35		dB
Group Delay Variation			0.2		ns
I/Q DEMODULATOR PERFORMANCE					
Maximum Conversion Gain		50	57		dB
Conversion Gain Control Range	Gain control at baseband amplifiers using VCTRL_BBVVA2 and VCTRL_BBVA3		55		dB
	Gain control at baseband amplifiers using all VCTRL_BBVVAx		70		dB
Input Third-Order Intercept (IIP3)	At −30 dBm composite input level, delta RF frequency (Δf_{RF}) = 1 MHz		−3		dBm
Third-Order Intermodulation Level (IM3)	At −30 dBm composite input level, Δf_{RF} = 1 MHz		−54		dBc
Input 1 dB Compression Point (IP1dB)	At maximum attenuation		−19		dBm
Image Rejection	Uncalibrated		30		dBc
Double Sideband Noise Figure	At maximum conversion gain		5		dB
	At maximum attenuation		8		dB
Input Second-Order Intercept Point (IIP2)	At −30 dBm composite input level, Δf_{RF} = 12 MHz		28		dBm
In Band Output Spurious			−50		dBc
Output Fractional Spurs			−60		dBc
LO to RF Leakage (dBm)			−60		dBm
DC Offset Error	25°C		7.5		mV
	85°C		7.8		mV
	−40°C		8		mV
PLL REF_{IN} INTERFACE					
REF_{IN} Frequency	Single-ended mode, DOUBLER_EN = 0		50	100	MHz
	Single-ended mode, DOUBLER_EN = 1			50	MHz
	Crystal mode		50		MHz
Power Level REF_{IN}	Single-ended mode	−5	+3	+5	dBm
VCTRL_BBVVAx INTERFACE					
AGC Voltage	On each VCTRL_BBVVAx pin	0		3.3	V
Impedance	On each VCTRL_BBVVAx pin		6.2		kΩ
Gain Slope	VCTRL_BBVVA1 = 3.3 V, AGC using VCTRL_BBVVA2 and VCTRL_BBVA3, series resistance of 5 kΩ on each VCTRL_BBVVAx, AGC from 1.1 V to 2.6 V		35		dB/V
	AGC using VCTRL_BBVVAx, series resistance of 5 kΩ on each VCTRL_BBVVAx, AGC from 1.1 V to 2.8 V		45		dB/V

SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS					
Input Voltage Range					
High, V_{INH}		1.5		3.3	V
Low, V_{INL}		0		0.4	V
Input High and Low Current, I_{INH}/I_{INL}			100		µA
LOGIC OUTPUTS					
Output Voltage Range					
High, V_{OH}		1.5		3.3	V
Low, V_{OL}		0		0.4	V
Output High Current, I_{OH}			100		µA
POWER INTERFACE					
V_{CC}		3.135	3.3	3.465	V
Supply Current (I_{CC})			980		mA
Total Power Consumption			3.2		W
	Power down, PD = logic high		600		mW
	Power down, Register 0x100, Register 0x120, Register 0x130, Register 0x131, and Register 0x132 = 0x00.[1]		300		mW

[1] For further optimization of power-down power consumption, contact Analog Devices, Inc., sales.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Maximum RF Power	0 dBm
Single-Ended External Reference Power	8 dBm
V_{CC}	4 V
Maximum Power Dissipation	4 W
VCTRL_BBVVAx	3.7 V
Digital Logic	–0.4 V to V_{CC} + 0.4 V
AGPIO	3.7 V
VCM_BBx	3.7 V
Source and Sink Current (MUXOUT)	300 µA
Temperature	
Storage Range (T_{STG})	–50°C to +125°C
Operating Ambient (T_A) Range	–40°C to +85°C
Maximum Junction (T_J)	125°C
Lifetime at Maximum T_J	1×10^6 hours
Peak	
Reflow Soldering	260°C
Time	40 secs
Moisture Sensitivity Level (MSL)[1]	MSL3

[1] Based on IPC/JEDEC J-STD-20 MSL classifications.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient thermal resistance, and θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
CC-48-5	24.5	10	°C/W

[1] Thermal resistance values specified are simulated based on JEDEC specifications in compliance with JESD-51.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADMV4540

Table 4. ADMV4540, 48-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	±500	1B
FICDM	±500	C2A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

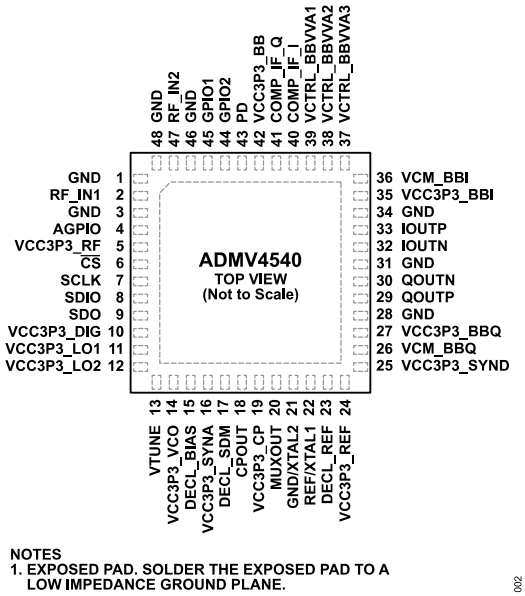

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground.
2	RF_IN1	RF Input 1. The RF_IN1 pin has a 50 Ω input impedance. DC-coupled to ground. Ensure that no dc voltage is present on the RF_IN1 pin.
3	GND	Ground.
4	AGPIO	Analog General-Purpose Input and Output. Refer to the Temperature Sensor Configuration section to configure the temperature sensor output to the AGPIO pin. Refer to the ADC Configuration section to use the AGPIO pin as an input.
5	VCC3P3_RF	3.3 V Supply for the RF Path. Place a 0.01 µF capacitor close to the VCC3P3_RF pin.
6	$\overline{CS}$	Digital Logic Pin for SPI Chip Select (Negative Polarity, 3.3 V Logic). Place a series 33 Ω resistor for optimum performance. Serial communication is enabled when $\overline{CS}$ is set to logic low. When $\overline{CS}$ is set to logic high at the end of the serial data command, the data written into the register address is given in the command.
7	SCLK	Digital Logic Pin for SPI Clock (3.3 V Logic). Place a series 33 Ω resistor for optimum performance. In write mode, data is sampled on the rising edge of SCLK. During a read cycle, output data changes at the falling edge of SCLK.
8	SDIO	Digital Logic Pin for SPI Data Input and Output in 3-Wire Mode. SPI data input in 4-wire mode (3.3 V logic). Place a series 33 Ω resistor for optimum performance.
9	SDO	Digital Logic Pin. In 4-wire SPI mode, SDO is a serial data output (3.3 V logic), digital logic pin. In 3-wire SPI mode, SDO is unused and can be connected to ground. Place a series 33 Ω resistor for optimum performance.
10	VCC3P3_DIG	SPI and Digital Supply. Place a 0.01 µF capacitor close to the VCC3P3_DIG pin.
11	VCC3P3_LO1	LO Path 3.3 V Supply 1. Place a 0.01 µF capacitor close to the VCC3P3_LO1 pin.
12	VCC3P3_LO2	LO Path 3.3 V Supply 2. Place a 0.01 µF capacitor close to the VCC3P3_LO2 pin.
13	VTUNE	VCO Tune Input (1 V to 2 V). The VTUNE pin is driven by the output of the loop filter.
14	VCC3P3_VCO	VCO 3.3 V Supply. Place a 0.01 µF capacitor close to the VCC3P3_VCO pin.
15	DECL_BIAS	VCO Core Bias Decouple Pin. Place a 1 µF capacitor close to the DECL_BIAS pin.
16	VCC3P3_SYNA	Synthesizer Analog 3.3 V Supply. Place a 0.01 µF capacitor close to the VCC3P3_SYNA pin.
17	DECL_SDM	Σ-Δ Modulator Low Dropout (LDO) Regulator Decouple Pin. Place a 1 µF capacitor close to the DECL_SDM pin.
18	CPOUT	Synthesizer Charge Pump Output. Connect the CPOUT pin to VTUNE (Pin 13) through the loop filter. Place the loop filter component, C1, as close as possible to the CPOUT pin.
19	VCC3P3_CP	Charge Pump 3.3 V Supply. Place a 0.01 µF capacitor close to the VCC3P3_CP pin.
20	MUXOUT	PLL Multiplexer Output. Refer to the EVAL-ADMV4540 for connection options.
21	GND/XTAL2	Second Reference Clock Input for Differential Reference or Ground from Single-Ended Reference. See Crystal Oscillator section and Reference Input section for configuration options.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
22	REF/XTAL1	Reference Clock Input. Single ended external reference input. For more information, see the Reference Input section for configuration options.
23	DECL_REF	Reference 1.8 V LDO Regulator Decouple Pin. Place a 1 µF capacitor close to the DECL_REF pin.
24	VCC3P3_REF	Reference Input Buffer 3.3 V Supply. Place a 0.01 µF capacitor close to the VCC3P3_REF pin.
25	VCC3P3_SYND	Synthesizer Digital 3.3 V Supply. Place a 0.01 µF capacitor close to the VCC3P3_SYND pin.
26	VCM_BBQ	Baseband Q Channel Output Common-Mode Level Input. Leave the VCM_BBQ pin floating.
27	VCC3P3_BBQ	Baseband Q Channel 3.3 V Supply. Place a 0.01 µF capacitor close to the VCC3P3_BBQ pin.
28	GND	Ground.
29, 30	QOUTP, QOUTN	Baseband Q Channel Positive and Negative Outputs. These 100 Ω differential impedance outputs can be ac-coupled with an ac coupling capacitor. The default common-mode output voltage is 1.65 V.
31	GND	Ground.
32, 33	IOUTN, IOUTP	Baseband I Channel Negative and Positive Outputs. These 100 Ω differential impedance outputs can be ac-coupled with an ac coupling capacitor. The default common-mode output voltage is 1.65 V.
34	GND	Ground.
35	VCC3P3_BBI	Baseband I Channel 3.3 V Supply. Place a 0.01 µF capacitor close to the VCC3P3_BBI pin.
36	VCM_BBI	Baseband I Channel Output Common-Mode Level Input. Leave this pin floating.
37	VCTRL_BBVVA3	Baseband VVA Control Voltage 3. Place a series resistor of 5 kΩ.
38	VCTRL_BBVVA2	Baseband VVA Control Voltage 2. Place a series resistor of 5 kΩ.
39	VCTRL_BBVVA1	Baseband VVA Control Voltage 1. Place a series resistor of 5 kΩ.
40	COMP_IF_I	Baseband I Channel Offset Cancellation Compensation Capacitor. Place a 1 µF capacitor close to the COMP_IF_I pin.
41	COMP_IF_Q	Baseband Q Channel Offset Cancellation Compensation Capacitor. Place a 1 µF capacitor close to the COMP_IF_Q pin.
42	VCC3P3_BB	Baseband 3.3 V Supply. Place a 0.01 µF capacitor close to the VCC3P3_BB pin.
43	PD	Digital Logic Power-Down Pin. Set to logic low (0 V) for normal operation. Set to logic high (3.3 V) to power down the ADMV4540 while keeping the synthesizer locked. Refer to the Power Down section for more information.
44	GPIO1	Digital Logic General-Purpose Digital Input and Output Pin 1. Do not exceed the input voltage of 3.3 V. Refer to GPIOs section for more details.
45	GPIO2	Digital Logic General-Purpose Digital Input and Output Pin 2. Do not exceed the input voltage of 3.3 V. Refer to GPIOs section for more details.
46	GND	Ground.
47	RF_IN2	RF Input 2. The RF_IN2 has a 50 Ω input impedance. DC-coupled to ground. Ensure that no dc voltage is present on the RF_IN2 pin.
48	GND	Ground.
	EPAD	Exposed Pad. Solder the exposed pad to a low impedance ground plane. See the Heat Sink Selection section and the Recommended Land Pattern section for more information.

TYPICAL PERFORMANCE CHARACTERISTICS

RF BANDWIDTH PERFORMANCE CHARACTERISTIC

Baseband frequency (f_{BB}) = 36 MHz, V_{CC} = 3.3 V, and T_A = 25°C, unless otherwise noted. The evaluation board RF traces were deembedded until RF_INx, unless otherwise noted. The minimum input power was measured with BB_AMP1_GAIN_x = 0, RF_INx = −66 dBm, and VCTRL_BBVVAx = 3.3 V. The maximum input power measurements were made with RF_INx = −30 dBm, BB_AMP1_GAIN_x = 3, VCTRL_BBVVA1 = 3.3 V, AGC using VCTRL_BBVVA2 and VCTRL_BBVA3, and the total output power set to −10 dBm per I and Q through AGC. Performance metrics were per the I channel and Q channel, the evaluation board I channel and Q channel traces were deembedded until the I channel and Q channel pins. The I channel and Q channel outputs were ac-coupled with a 1 µF capacitor on each channel output, and the I channel and Q channel positive and negative outputs were combined with a 180° balun, unless otherwise noted. PLL filter bandwidth = 220 kHz with 60° of phase margin, f_{REF} = 50 MHz, DOUBLER_EN = 1, f_{PFD} = 100 MHz, and the external reference power was set to 3 dBm for the single-ended external reference, unless otherwise stated.

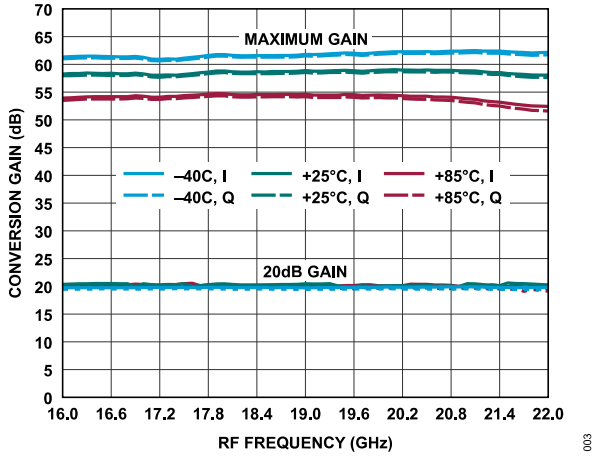

Figure 3. Conversion Gain vs. RF Frequency at Maximum Gain (Minimum Input Power) and 20 dB Gain (Maximum Input Power) at Various Temperatures and I and Q Channels

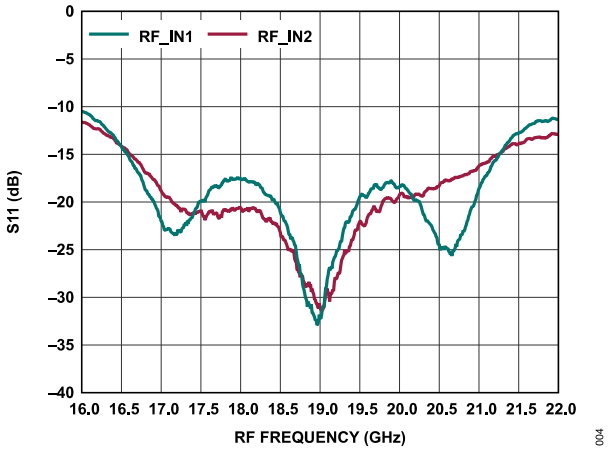

Figure 4. Input Return Loss (S11) vs. RF Frequency for RF_IN1 and RF_IN2

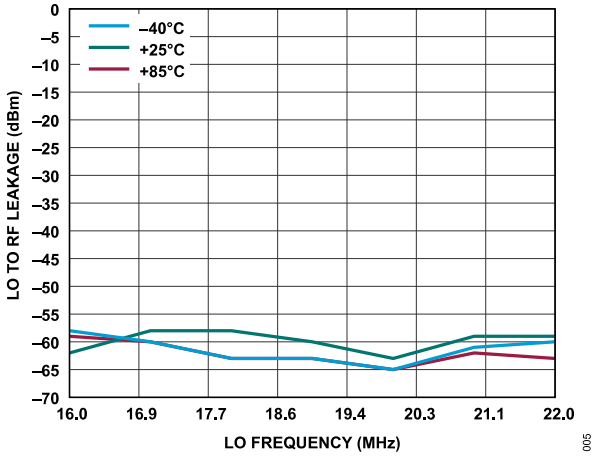

Figure 5. LO to RF Leakage vs. LO Frequency at Various Temperatures

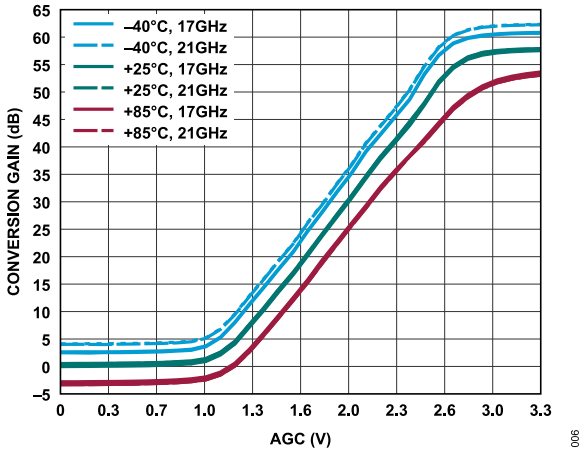

Figure 6. Conversion Gain vs. AGC for LO = 17 GHz and 21 GHz at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

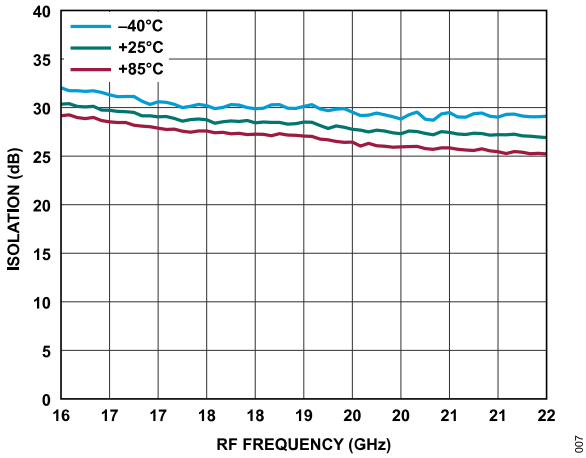

Figure 7. RF_IN1 to RF_IN2 Isolation vs. RF Frequency, 20 dB Gain (Maximum Input Power) at Various Temperatures

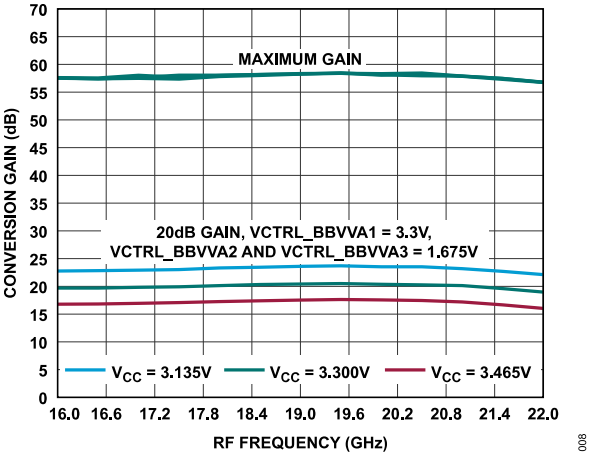

Figure 8. Conversion Gain vs. RF Frequency at Maximum Gain (Minimum Input Power) and 20 dB Gain (Maximum Input Power) at Various Supply Voltages (±5%)

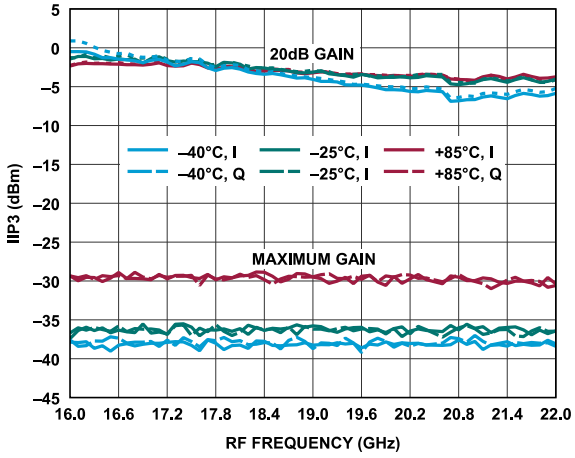

Figure 9. IIP3 vs. RF Frequency, Tone Spacing = 1 MHz, at Maximum Gain (Minimum Input Power) and 20 dB Gain (Maximum Input Power) at Various Temperatures and I and Q Channels

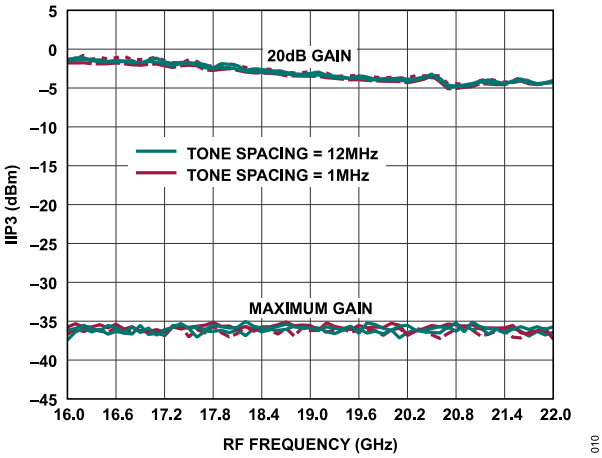

Figure 10. IIP3 vs. RF Frequency, Tone Spacing = 12 MHz and 1 MHz at Maximum Gain (Minimum Input Power) and 20 dB Gain (Maximum Input Power)

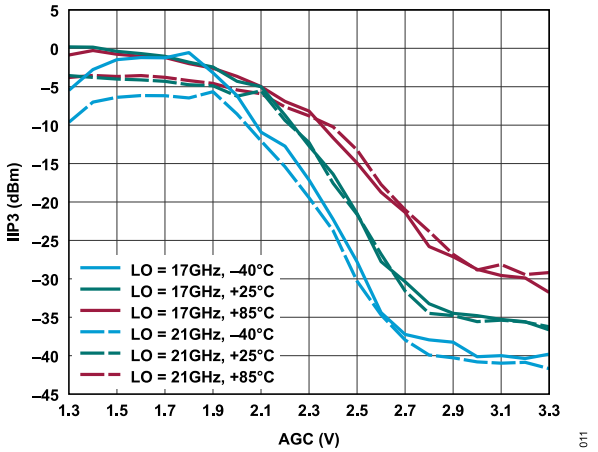

Figure 11. IIP3 vs. AGC, LO = 17 GHz and 21 GHz at Various Temperatures

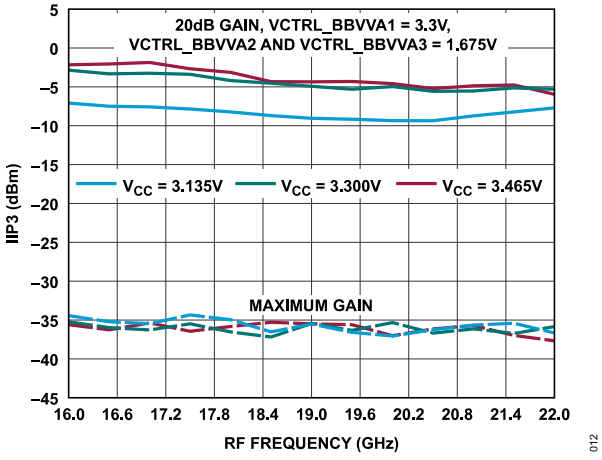

Figure 12. IIP3 vs. RF Frequency at Maximum Gain (Minimum Input Power) and 20 dB Gain (Maximum Input Power) at Various Supply Voltages (±5)

TYPICAL PERFORMANCE CHARACTERISTICS

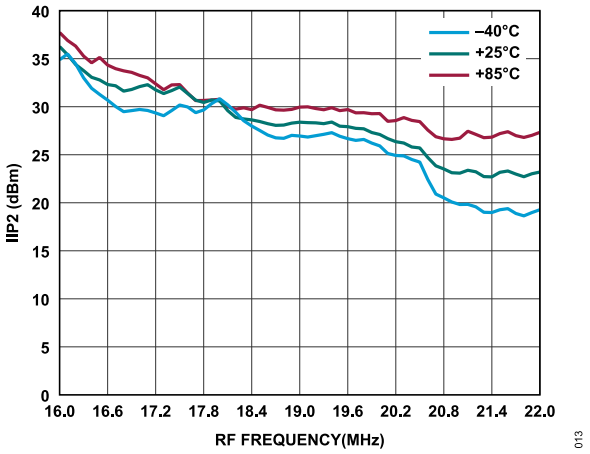

Figure 13. IIP2 vs. RF Frequency, Tone Spacing = 12 MHz at 20 dB Gain (Maximum Input Power) at Various Temperatures

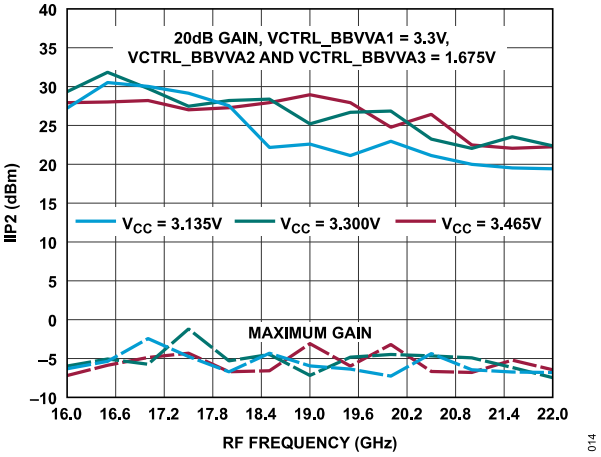

Figure 14. IIP2 vs. RF Frequency at Maximum Gain (Minimum Input Power) and 20 dB Gain (Maximum Input Power) at Various Supply Voltages (±5)

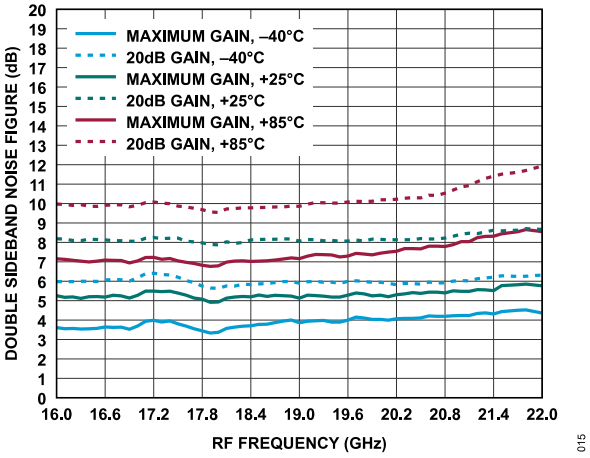

Figure 15. Double Sideband Noise Figure vs. RF Frequency at Maximum Gain (Minimum Input Power) and 20 dB Gain (Maximum Input Power) at Various Temperatures

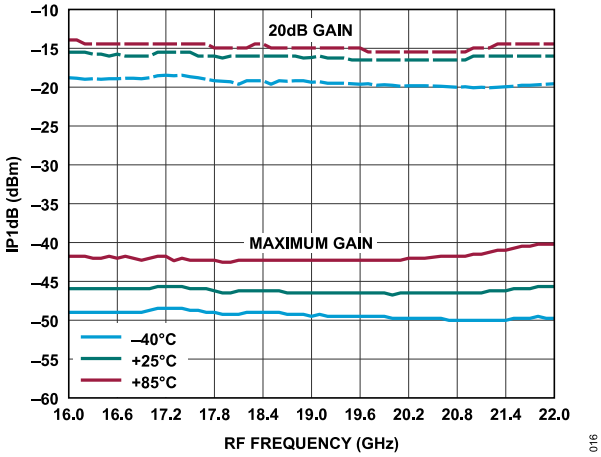

Figure 16. Input P1dB vs. RF Frequency, Maximum Gain (Minimum Input Power) and 20 dB Gain (Maximum Input Power) at Various Temperatures

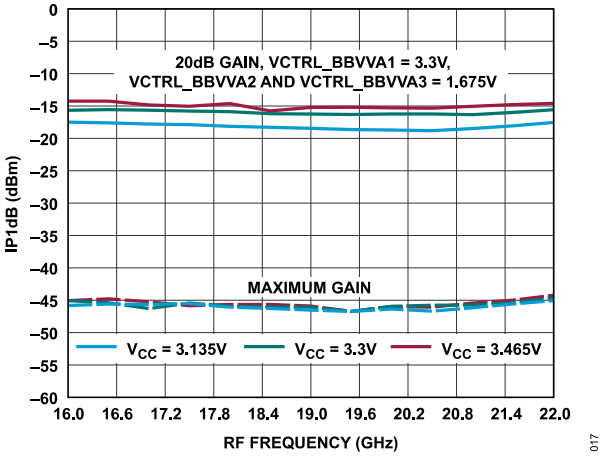

Figure 17. Input P1dB vs. RF Frequency at Maximum Gain (Minimum Input Power) and 20 dB Conversion Gain (Maximum Input Power) at Various Supply Voltages (±5%)

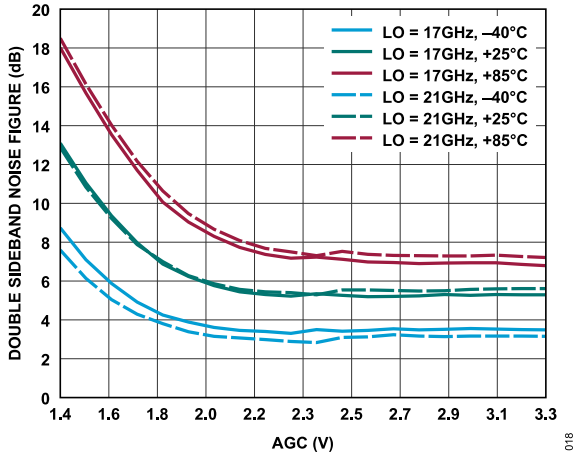

Figure 18. Double Sideband Noise Figure vs. AGC, LO = 17 GHz and 21 GHz at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

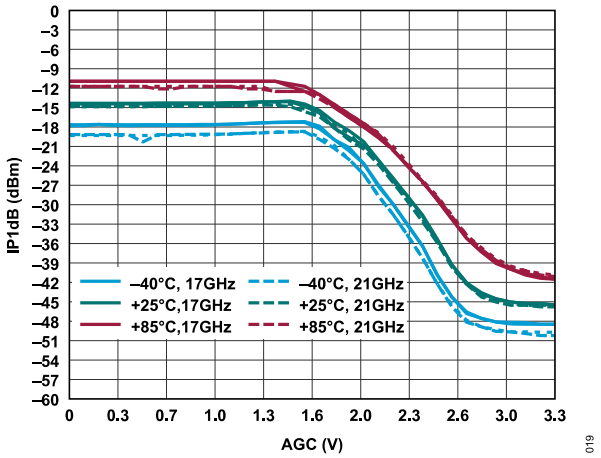

Figure 19. Input P1dB vs. AGC, LO = 17 GHz and 21 GHz at Various Temperatures

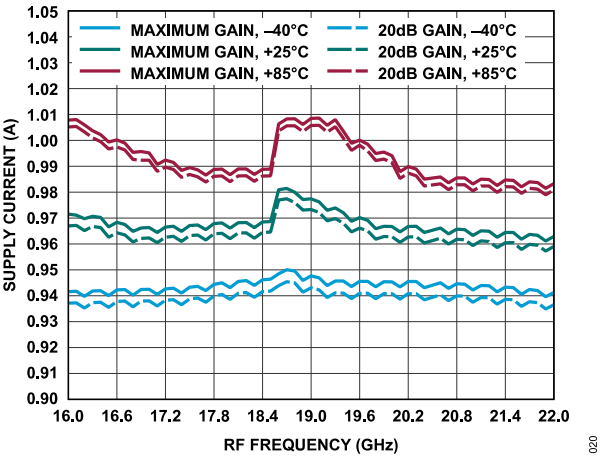

Figure 20. Supply Current vs. RF Frequency for Maximum Gain (Minimum Input Power) and 20 dB Gain (Maximum Input Power) at Various Temperatures

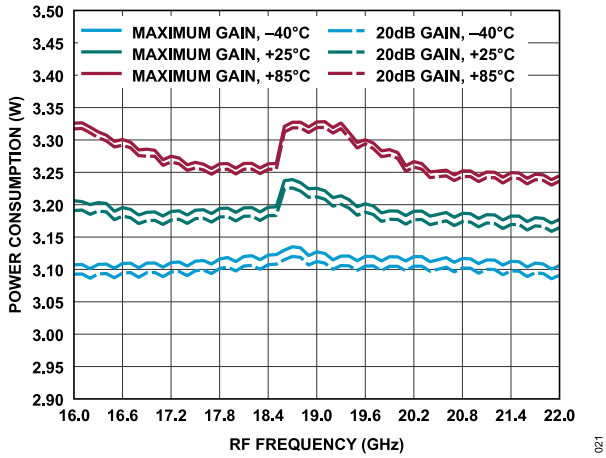

Figure 21. Power Consumption vs. RF Frequency for Maximum Gain (Minimum Input Power) and 20 dB Gain (Maximum Input Power) at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

BASEBAND BANDWIDTH PERFORMANCE CHARACTERISTIC

f_{BB} = 36 MHz, V_{CC} = 3.3 V, and T_A = 25°C, unless otherwise noted. The evaluation board RF traces were deembedded until RF_INx, unless otherwise noted. The minimum input power was measured with BB_AMP1_GAIN_x = 0, RF_INx= −66 dBm, and VCTRL_BBVVAx = 3.3 V. The maximum input power measurements were made with RF_INx = −30 dBm, BB_AMP1_GAIN_x = 0, VCTRL_BBVVA1 = 3.3 V, AGC using VCTRL_BBVVA2 and VCTRL_BBVA3, and the total output power set to −10 dBm per I and Q through AGC. Performance metrics were per the I channel and Q channel, the evaluation board I channel and Q channel traces were deembedded until the I channel and Q channel pins. The I channel and Q channel outputs were ac-coupled with a 1 µF capacitor on each channel output, and the I channel and Q channel positive and negative outputs were combined with a 180° balun, unless otherwise noted. PLL filter bandwidth = 220 kHz with 60° of phase margin, f_{REF} = 50 MHz, DOUBLER_EN = 1, f_{PFD} = 100 MHz, and the external reference power was set to 3 dBm for the single-ended external reference, unless otherwise stated.

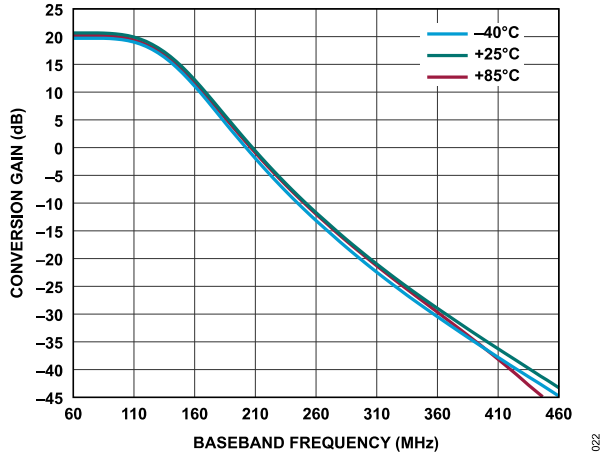

Figure 22. 125 MHz, SPI-Selectable Baseband LPF Frequency Response, Conversion Gain vs. Baseband Frequency at Various Temperature

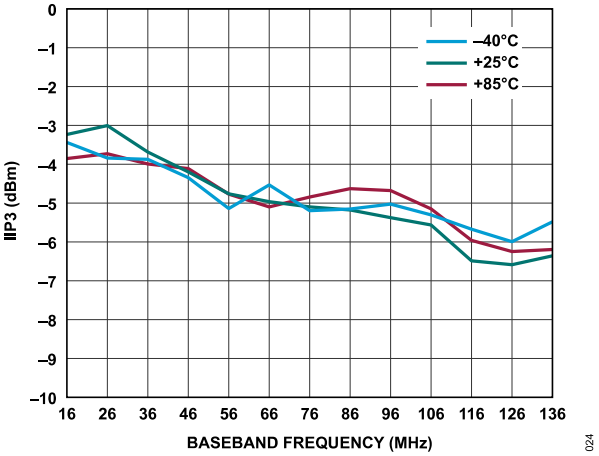

Figure 24. 125 MHz, SPI-Selectable Baseband LPF, IIP3 vs. Baseband Frequency at Various Temperatures at 20 dB Gain (Maximum Input Power)

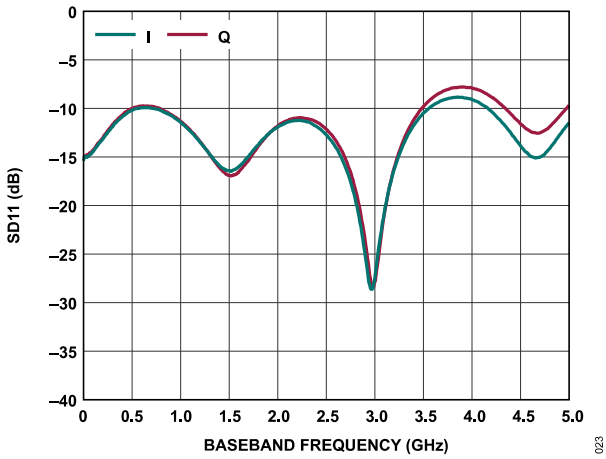

Figure 23. 125 MHz, SPI-Selectable Baseband LPF, I and Q Differential Return Loss (SD11) vs. Baseband Frequency

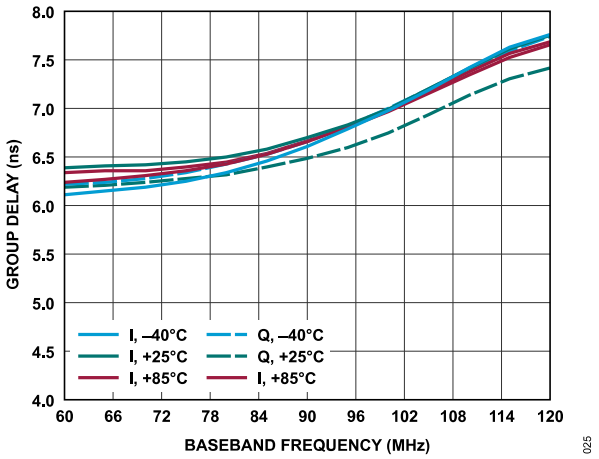

Figure 25. 125 MHz, SPI-Selectable Baseband LPF, Group Delay vs. Baseband Frequency at Various Temperatures and the I and Q Channels

TYPICAL PERFORMANCE CHARACTERISTICS

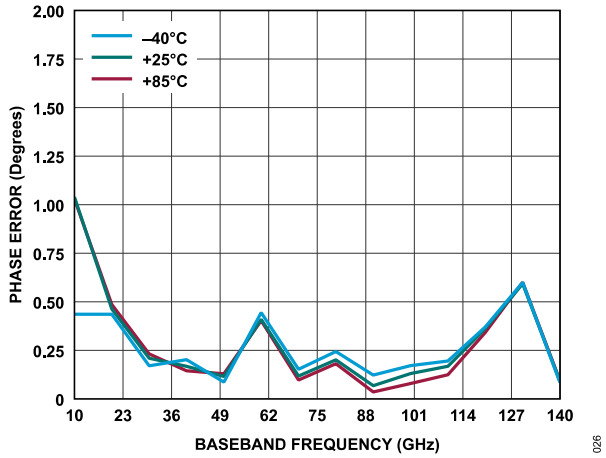

Figure 26. 125 MHz, SPI-Selectable Baseband LPF, Phase Error vs. Baseband Frequency at Various Temperatures

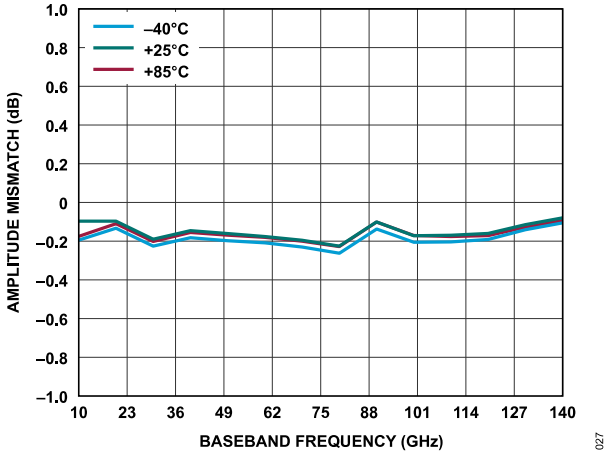

Figure 27. 125 MHz, SPI-Selectable Baseband LPF, Amplitude Mismatch vs. Baseband Frequency at Various Temperatures

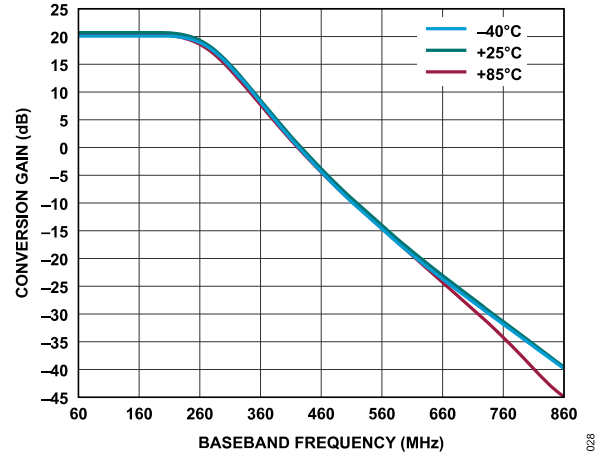

Figure 28. 250 MHz, SPI-Selectable Baseband LPF Frequency Response, Conversion Gain vs. Baseband Frequency at Various Temperatures

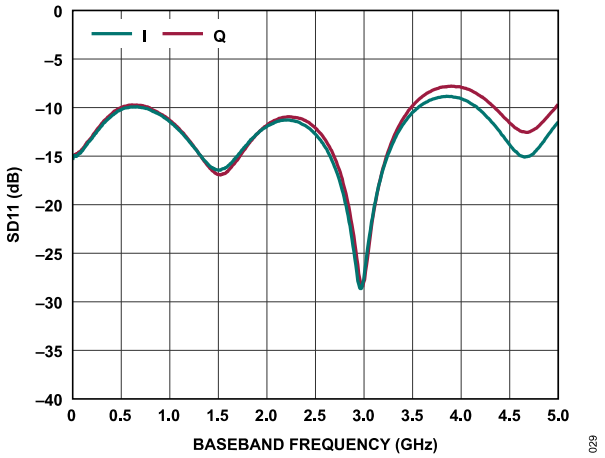

Figure 29. 250 MHz, SPI-Selectable Baseband LPF, I and Q SD11 vs. Baseband Frequency

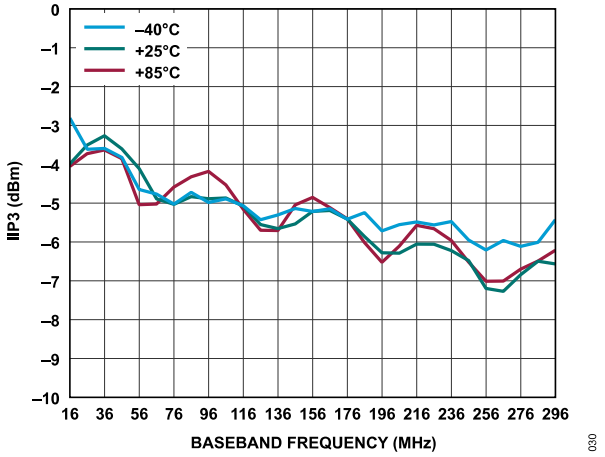

Figure 30. 250 MHz, SPI-Selectable Baseband LPF, IIP3 vs. Baseband Frequency at Various Temperatures at 20 dB Gain (Maximum Input Power)

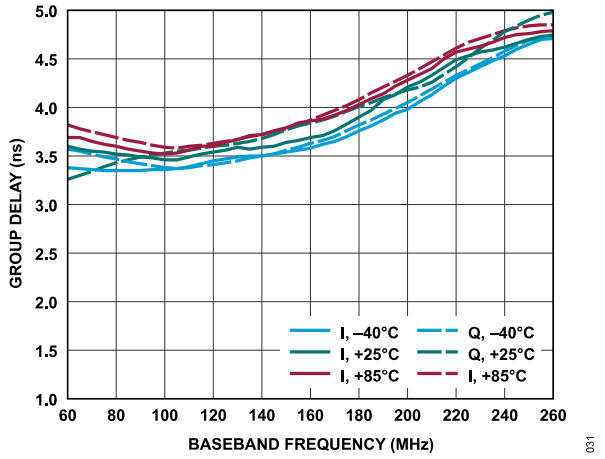

Figure 31. 250 MHz, SPI-Selectable Baseband LPF, Group Delay vs. Baseband Frequency at Various Temperatures and the I and Q Channels

TYPICAL PERFORMANCE CHARACTERISTICS

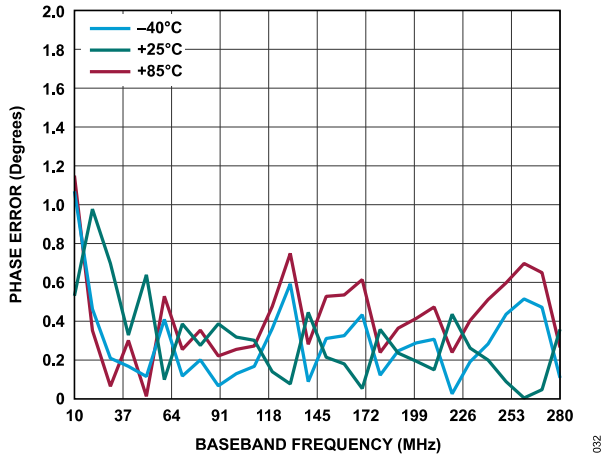

Figure 32. 250 MHz, SPI-Selectable Baseband LPF, Phase Error vs. Baseband Frequency at Various Temperatures

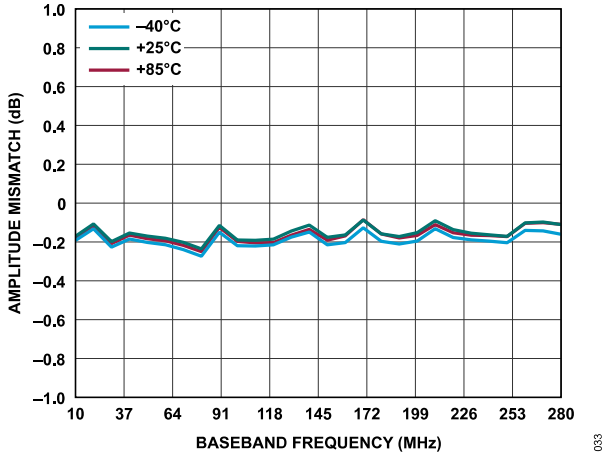

Figure 33. 250 MHz, SPI-Selectable Baseband LPF, Amplitude Mismatch vs. Baseband Frequency at Various Temperatures

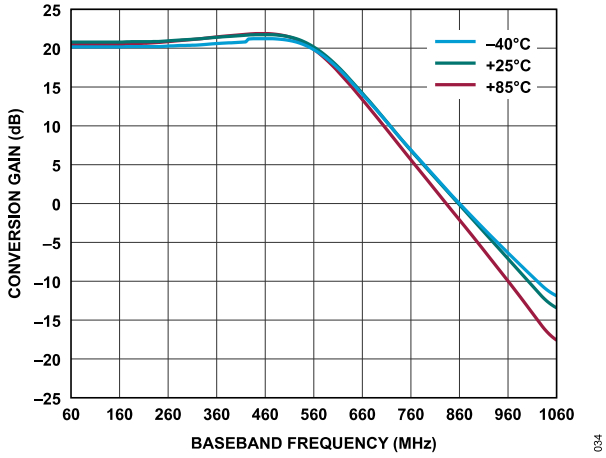

Figure 34. 500 MHz, SPI-Selectable LPF Frequency Response, Conversion Gain vs. Baseband Frequency at Various Temperatures

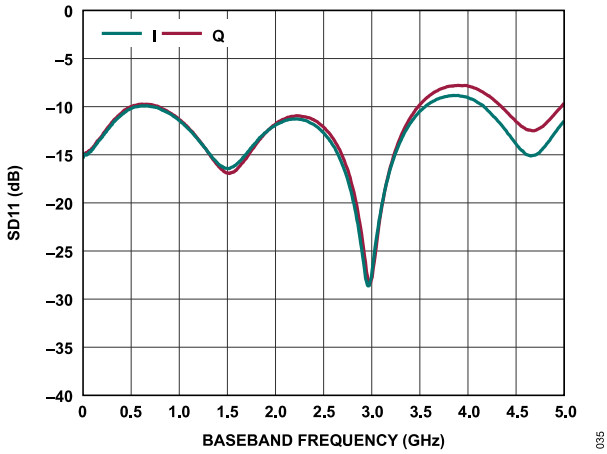

Figure 35. 500 MHz, SPI-Selectable LPF, I and Q SD11 vs. Baseband Frequency

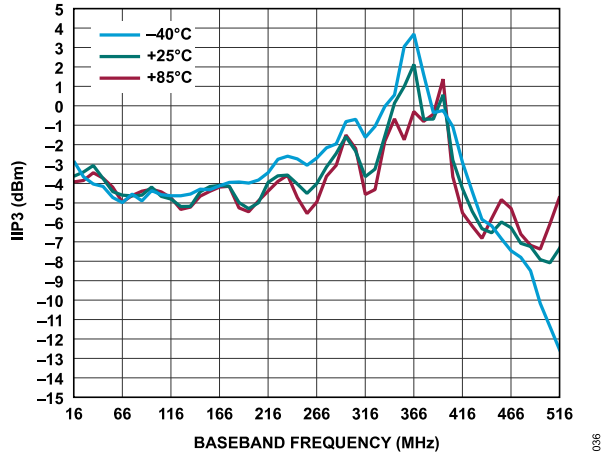

Figure 36. 500 MHz, SPI-Selectable LPF, IIP3 vs. Baseband Frequency at Various Temperatures at 20 dB Gain (Maximum Input Power)

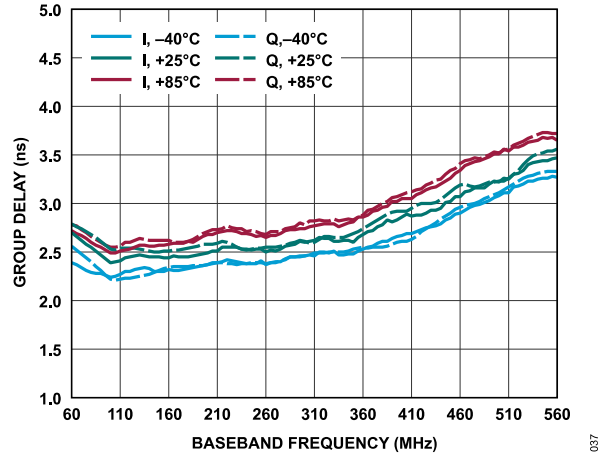

Figure 37. 500 MHz, SPI-Selectable LPF, Group Delay vs. Baseband Frequency at Various Temperatures and the I and Q Channels

TYPICAL PERFORMANCE CHARACTERISTICS

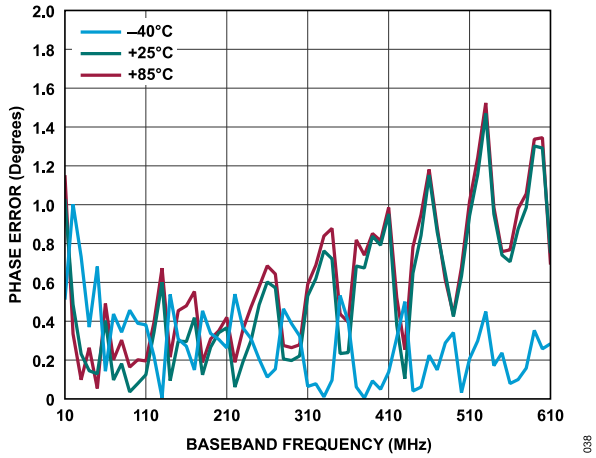

Figure 38. 500 MHz, SPI-Selectable LPF, Phase Error vs. Baseband Frequency at Various Temperatures

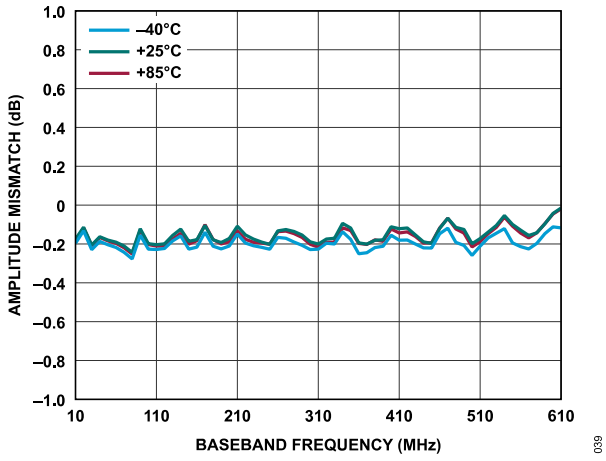

Figure 39. 500 MHz, SPI-Selectable LPF, Amplitude Mismatch vs. Baseband Frequency at Various Temperatures

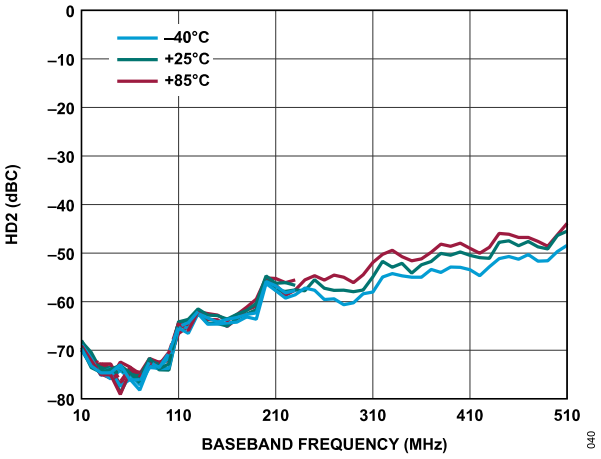

Figure 40. Harmonic Distortion 2 (HD2) vs. Baseband Frequency at 20 dB Gain (Maximum Input Power) and at Various Temperatures

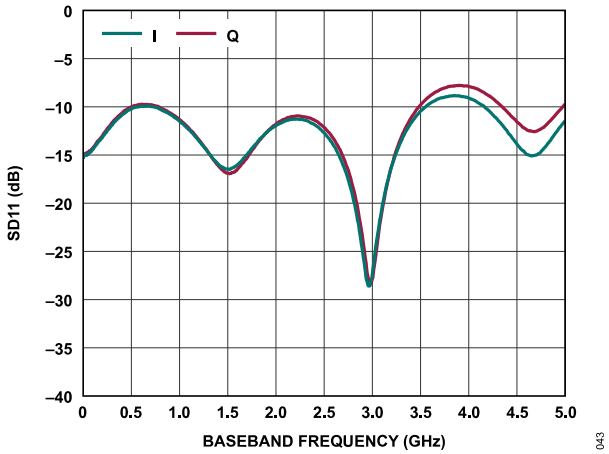

Figure 41. Bypass, SPI-Selectable LPFs, I and Q Differential SD11 vs. Baseband Frequency

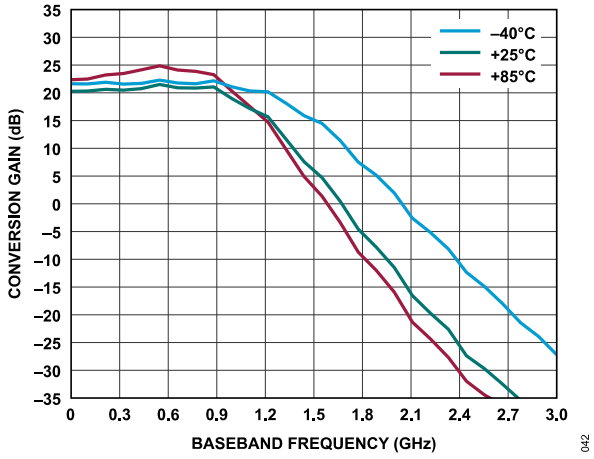

Figure 42. Bypass, SPI-Selectable LPFs, Conversion Gain vs. Baseband Frequency at Various Temperatures

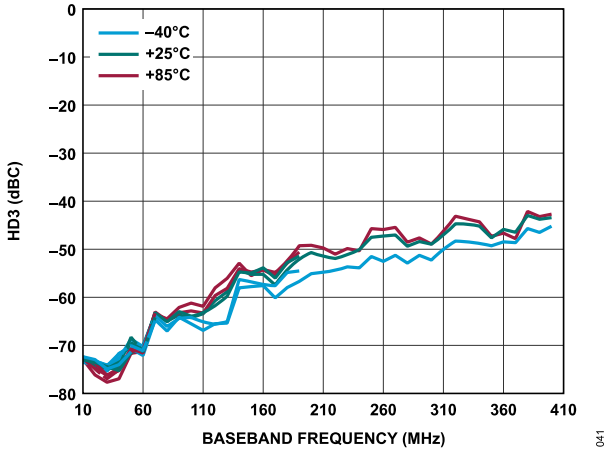

Figure 43. Harmonic Distortion 3 (HD3) vs. Baseband Frequency at 20 dB Gain (Maximum Input Power) and at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

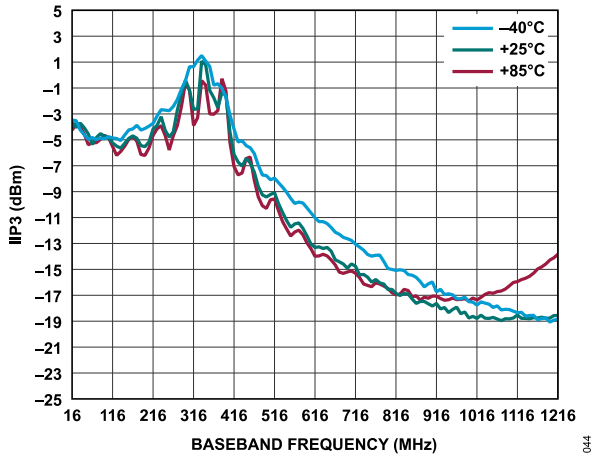

Figure 44. Bypass, SPI-Selectable LPFs, IIP3 vs. Baseband Frequency at Various Temperatures and at 20 dB Gain (Maximum Input Power)

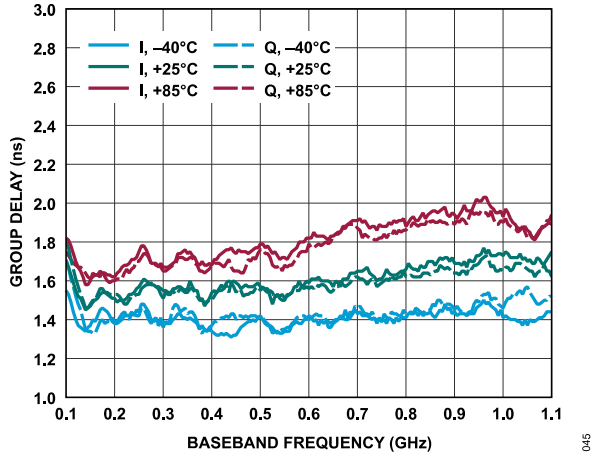

Figure 45. Bypass, SPI-Selectable LPFs, Group Delay vs. Baseband Frequency at Various Temperatures and the I and Q Channels

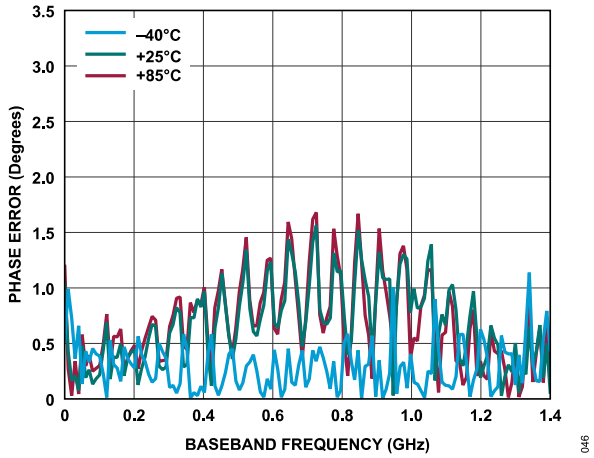

Figure 46. Bypass, SPI-Selectable LPFs, Phase Error vs. Baseband Frequency at Various Temperatures

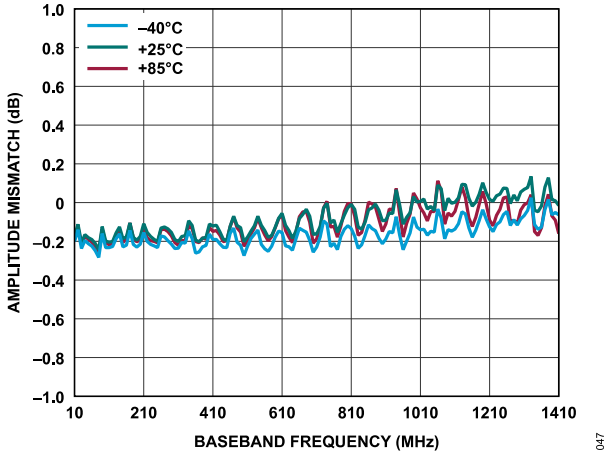

Figure 47. Bypass, SPI-Selectable LPFs, Amplitude Mismatch vs. Baseband Frequency at Various Temperatures

TYPICAL PERFORMANCE CHARACTERISTICS

TEMPERATURE SENSOR AND ADC

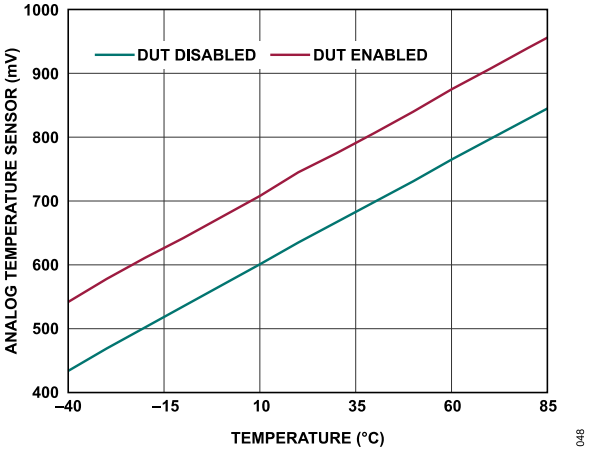

Figure 48. Analog Temperature Sensor at AGPIO Pin vs. Temperature with Device Under Test (DUT) Disabled and Enabled

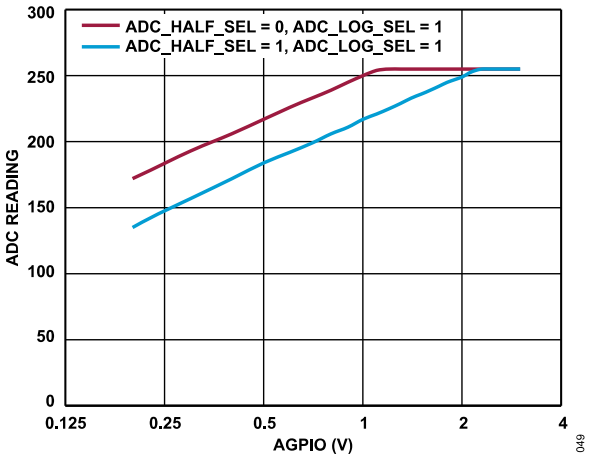

Figure 49. ADC Reading vs. AGPIO for ADC_LOG_SEL = 1

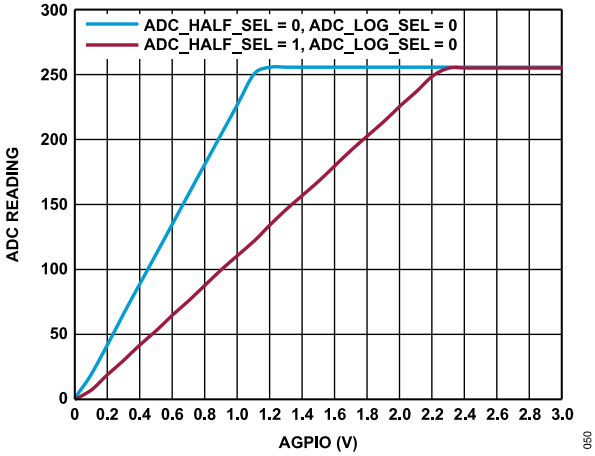

Figure 50. ADC Reading vs. AGPIO for ADC_LOG_SEL = 0

TYPICAL PERFORMANCE CHARACTERISTICS

PLL AND VCO PERFORMANCE CHARACTERISTIC

The I channel and Q channel outputs are ac-coupled with a 1 µF capacitor on each channel output, and the I channel and Q channel positive and negative outputs are combined with a 180° balun, unless otherwise noted. f_{BB} = 100 MHz, V_{CC} = 3.3 V, and T_A = 25°C, unless otherwise noted. PLL filter bandwidth = 220 kHz with 60° of phase margin, f_{REF} = 50 MHz, DOUBLER_EN = 1, f_{PFD} = 100 MHz, and the external reference power is set to 3 dBm for the single-ended external reference, unless otherwise stated.

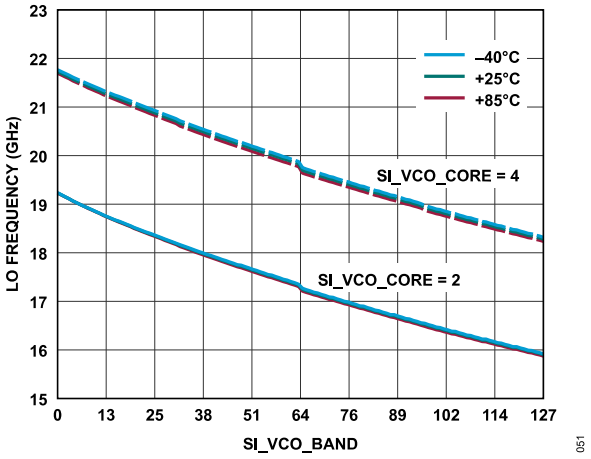

Figure 51. LO Frequency vs. SI_VCO_BAND, VTUNE = 1.5 V at Various Temperatures, Open Loop, SI_VCO_CORE = 1 and = 4

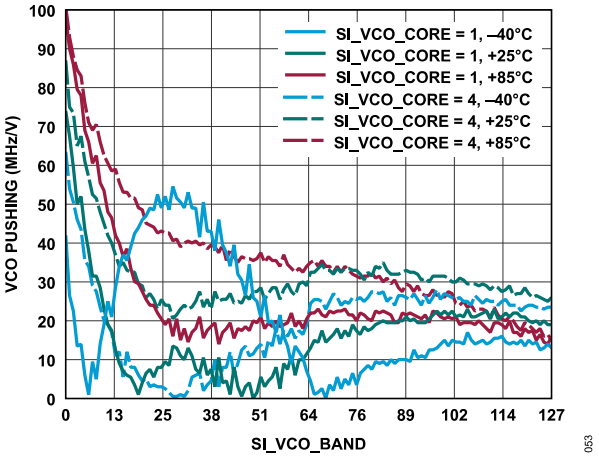

Figure 53. VCO Pushing vs. SI_VCO_BAND, Open Loop, VTUNE = 1.5 V, at Various Temperatures, SI_VCO_CORE = 1 and = 4

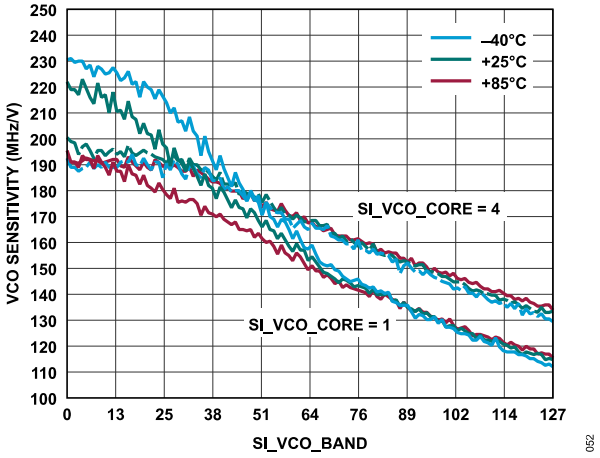

Figure 52. VCO Sensitivity vs. SI_VCO_BAND, VTUNE = 1.5 V, Open Loop at Various Temperatures, SI_VCO_CORE = 1 and = 4

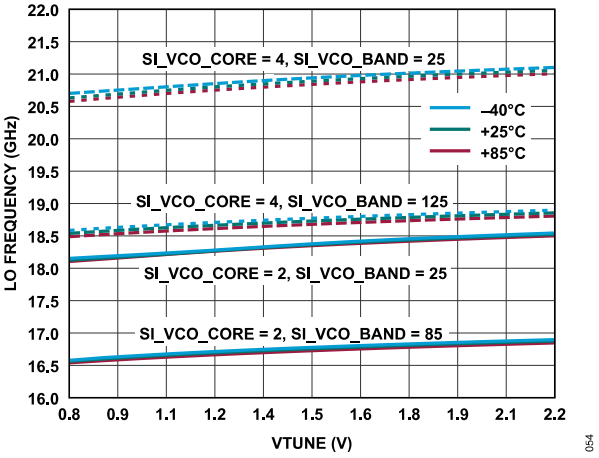

Figure 54. LO Frequency vs. VTUNE over Temperature, Four Bands (Two Bands for VCO Core 1 and Two Bands for VCO Core 2)

TYPICAL PERFORMANCE CHARACTERISTICS

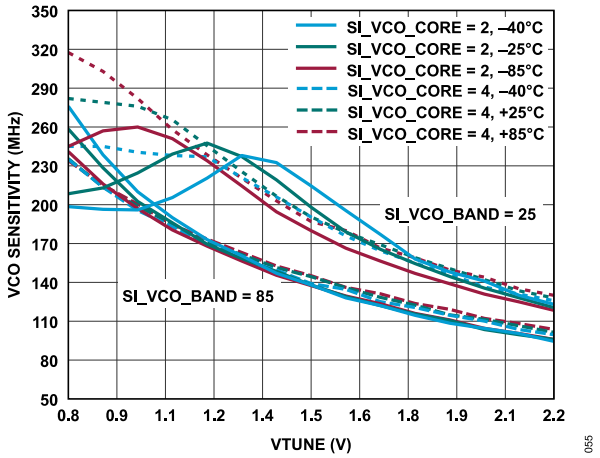

Figure 55. VCO Sensitivity vs. VTUNE at Various Temperatures, SI_VCO_CORE = 2 and = 4

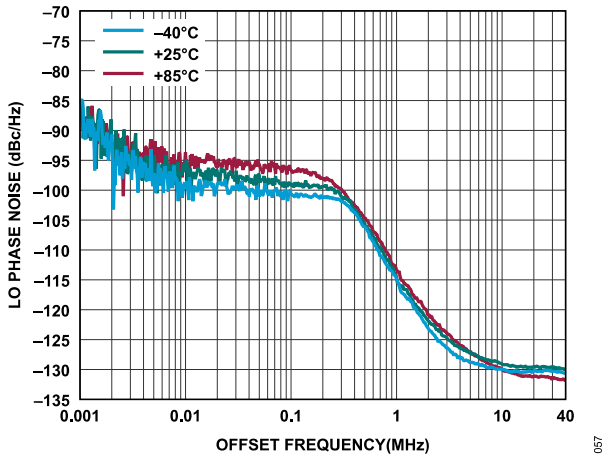

Figure 56. LO Phase Noise vs. Offset Frequency at 17.1 GHz and at Various Temperatures, CP_CURRENT = 4 and SI_VCO_CORE = 1

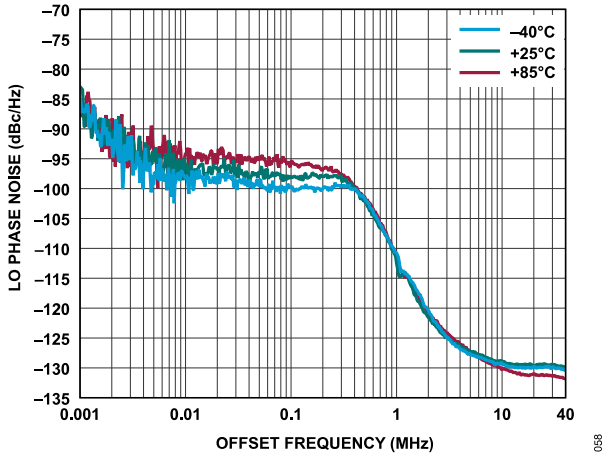

Figure 57. LO Phase Noise vs. Offset Frequency at 18.6 GHz and at Various Temperatures, CP_CURRENT = 4 and SI_VCO_CORE = 1

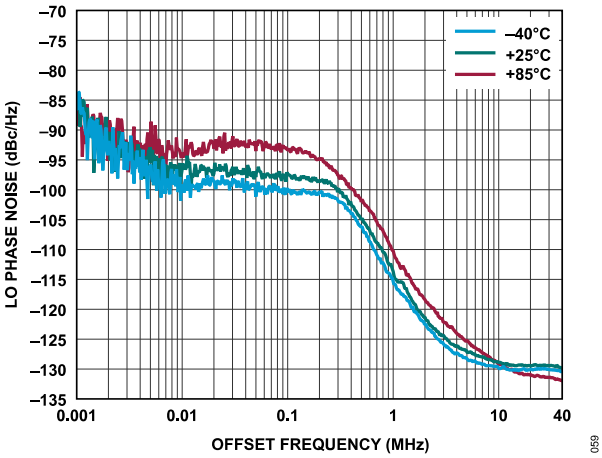

Figure 58. LO Phase Noise vs. Offset Frequency at 18.6 GHz and at Various Temperatures, CP_CURRENT = 4 and SI_VCO_CORE = 4

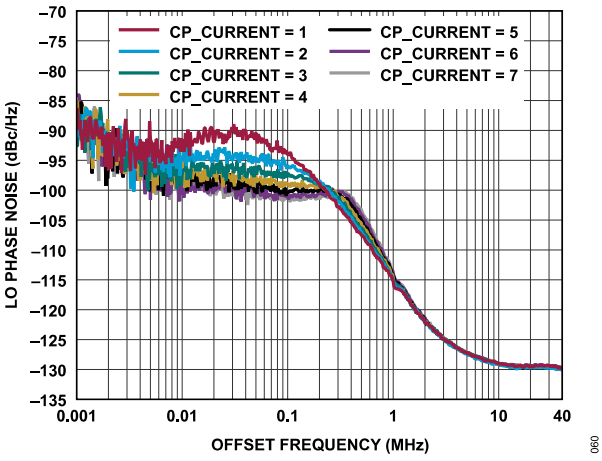

Figure 59. LO Phase Noise vs. Offset Frequency, CP_CURRENT = 1 to 7, LO = 17 GHz, and SI_VCO_CORE = 1

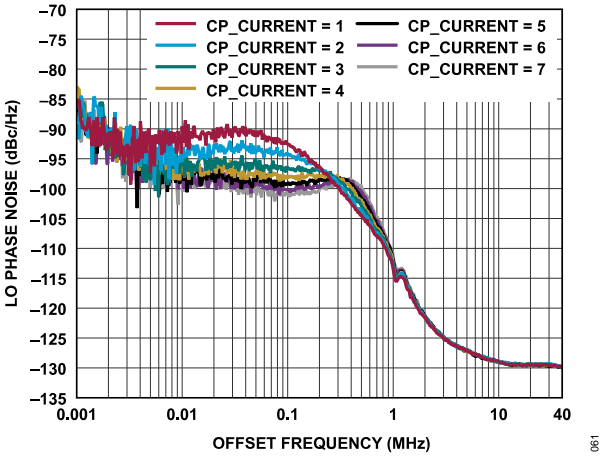

Figure 60. LO Phase Noise vs. Offset Frequency, CP_CURRENT = 1 to 7, LO = 18.5 GHz, and SI_VCO_CORE = 1

TYPICAL PERFORMANCE CHARACTERISTICS

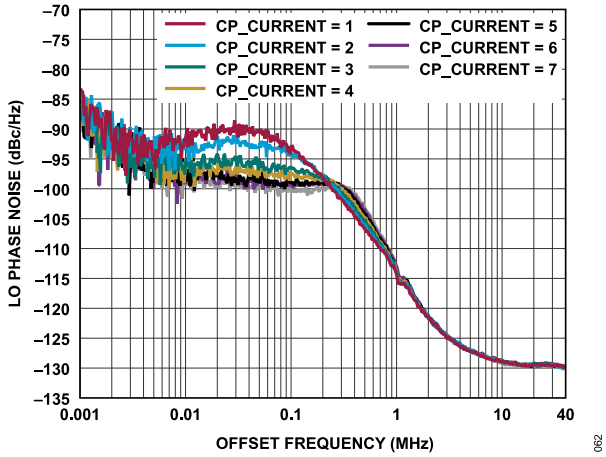

Figure 61. LO Phase Noise vs. Offset Frequency, CP_CURRENT = 1 to 7, LO = 19 GHz, and SI_VCO_CORE = 4

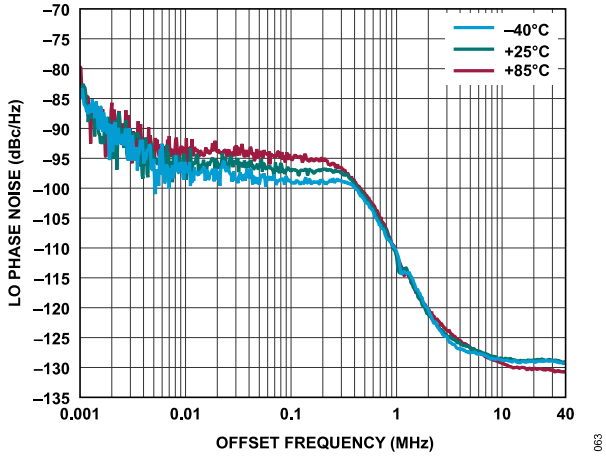

Figure 62. LO Phase Noise vs. Offset Frequency at 21 GHz and at Various Temperatures, CP_CURRENT = 4 and SI_VCO_CORE = 4

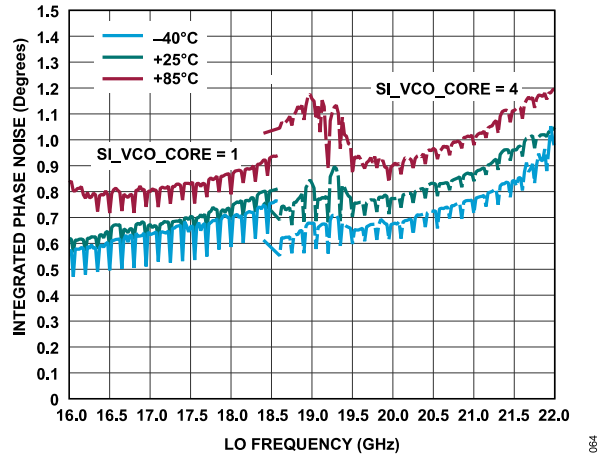

Figure 63. Integrated Phase Noise, 1 kHz to 10 MHz vs. LO Frequency and at Various Temperatures, CP_CURRENT = 4

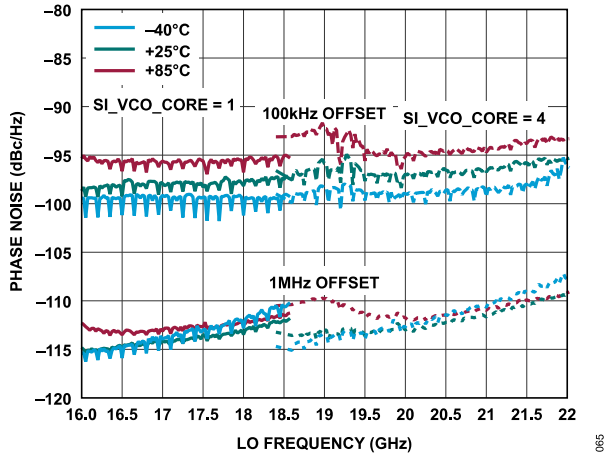

Figure 64. 100 kHz and 1 MHz Offset, Phase Noise vs. LO Frequency and at Various Temperatures, CP_CURRENT = 4

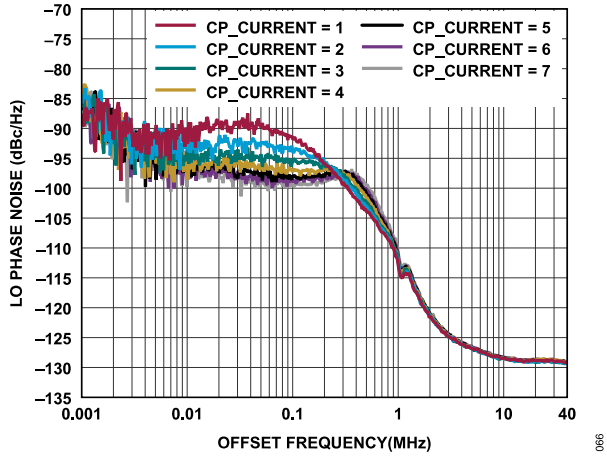

Figure 65. LO Phase Noise vs. Offset Frequency, CP_CURRENT = 1 to 7, LO = 21 GHz, and SI_VCO_CORE = 1

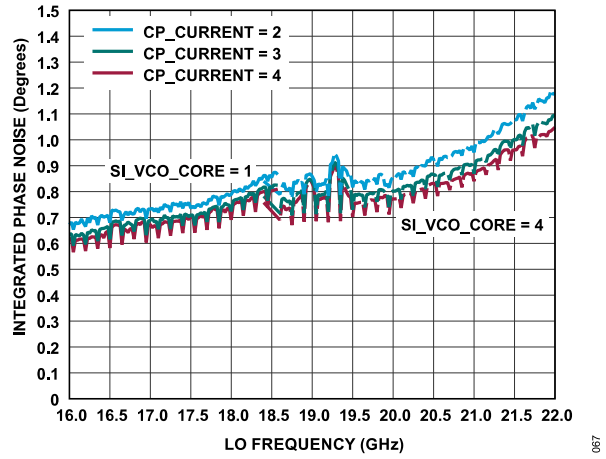

Figure 66. Integrated Phase Noise, 1 kHz to 10 MHz vs. LO Frequency, CP_CURRENT = 2, 3, and 4

TYPICAL PERFORMANCE CHARACTERISTICS

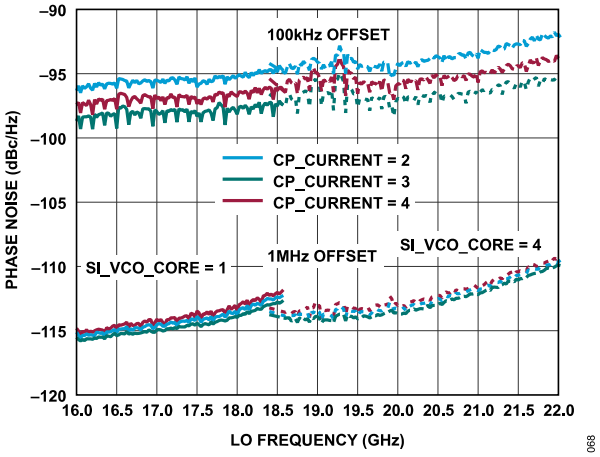

Figure 67. 100 kHz and 1 MHz Offset, Phase Noise vs. LO Frequency at Various Temperatures, CP _CURRENT = 2, 3, and 4

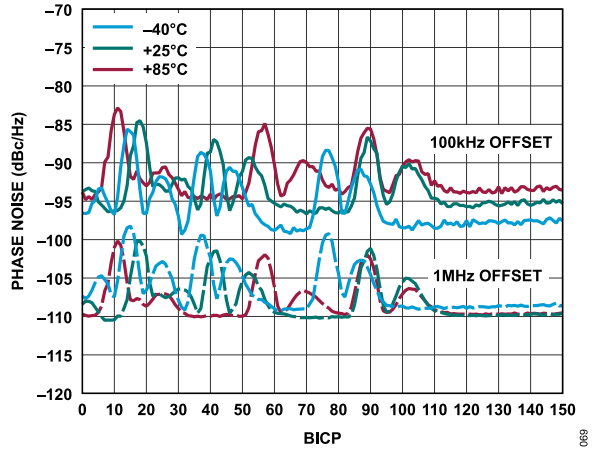

Figure 68. 1 MHz and 100 kHz Offset, Phase Noise vs. BICP at Various Temperatures, CP_CURRENT = 4, and LO = 21 GHz

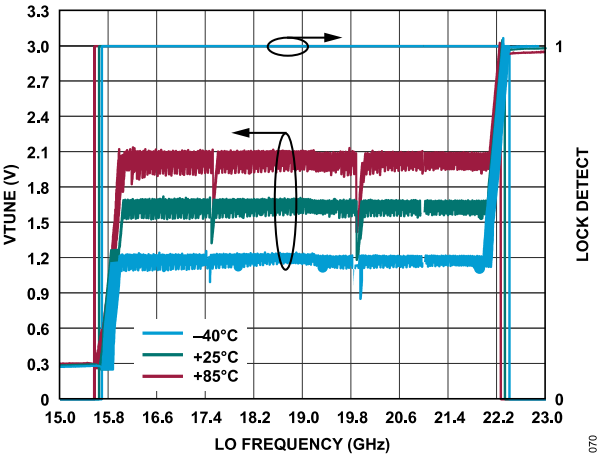

Figure 69. VTUNE and Lock Detect vs. LO Frequency at Various Temperatures

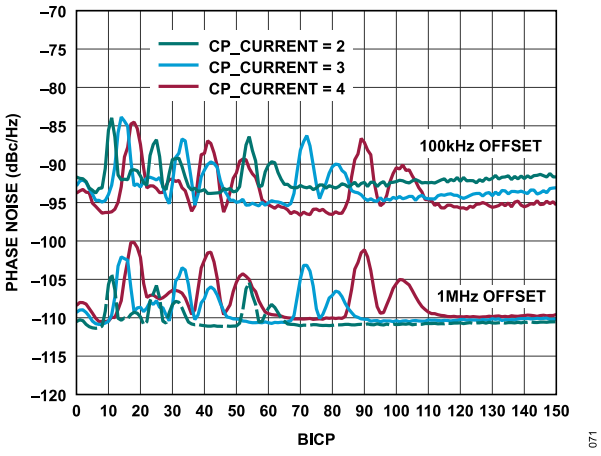

Figure 70. 100 kHz and 1 MHz Offset, Phase Noise vs. BICP, CP_CURRENT = 2, 3, and 4 and LO = 21 GHz

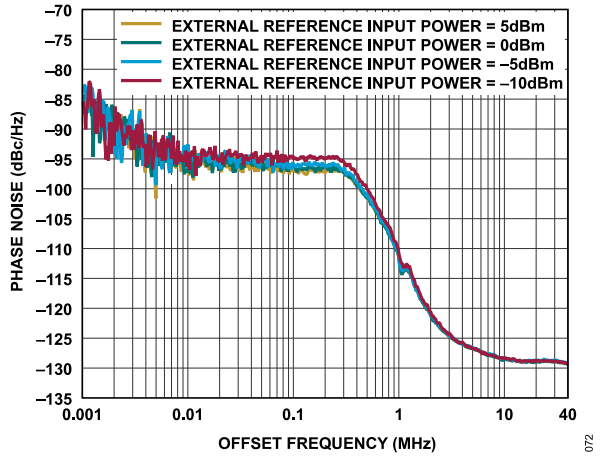

Figure 71. Phase Noise vs. Offset Frequency over the External Reference Input Power, LO = 21 GHz

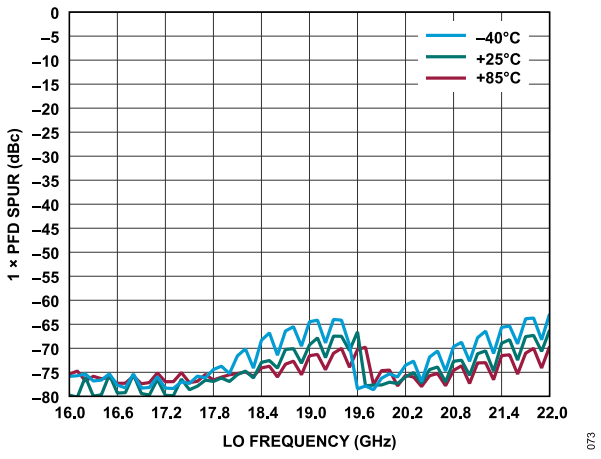

Figure 72. 1 × PFD Spur vs. LO Frequency at Various Temperatures, Spur Referred to the Main I Channel and Q Channel Output Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

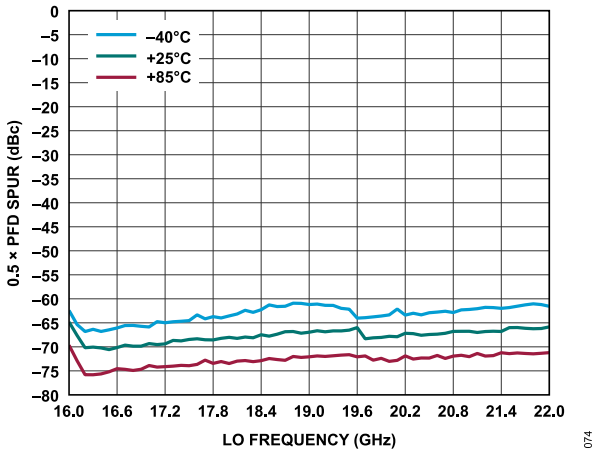

Figure 73. 0.5 × PFD Spur vs. LO Frequency at Various Temperatures, Spur Referred to the Main I Channel and Q Channel Output Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

PERFORMANCE WITH CONTROLLING VCTRL_BBVVA1, VCTRL_BBVVA2, AND VCTRL_BBVVA3 TOGETHER

f_{BB} = 36 MHz, V_{CC} = 3.3 V, and T_A = 25°C, unless otherwise noted. The evaluation board RF traces were deembedded until RF_INx, unless otherwise noted. The minimum input power was measured with RF_INx= −66 dBm and VCTRL_BBVVAx = 3.3 V. The maximum input power measurements were made with RF_INx = −30 dBm, AGC using VCTRL_BBVVAx, and the total output power set to −10 dBm per I and Q through AGC. Performance metrics were per the I channel and Q channel, the evaluation board I channel and Q channel traces were deembedded until the I channel and Q channel pins. The I channel and Q channel outputs were ac-coupled with a 1 µF capacitor on each channel output, and the I channel and Q channel positive and negative outputs were combined with a 180° balun, unless otherwise noted. PLL filter bandwidth = 220 kHz with 60° of phase margin, f_{REF} = 50 MHz, DOUBLER_EN = 1, f_{PFD} = 100 MHz, and the external reference power was set to 3 dBm for the single-ended external reference, unless otherwise stated.

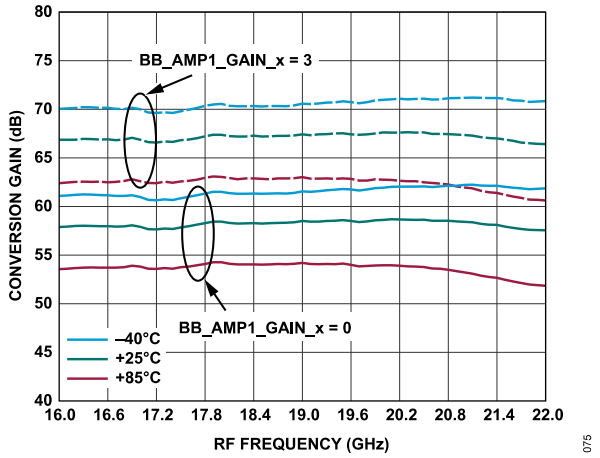

Figure 74. Conversion Gain vs. RF Frequency at Maximum Gain (Minimum Input Power) at Various Temperatures and Various BB_AMP1_GAIN_x Settings

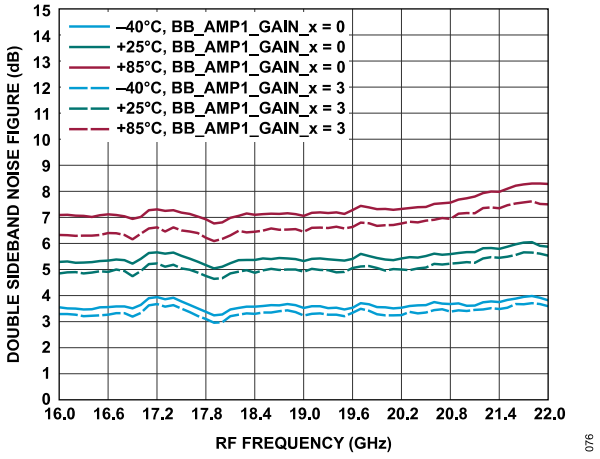

Figure 75. Double Sideband Noise Figure vs. RF Frequency at Maximum Gain (Minimum Input Power) at Various Temperatures and Various BB_AMP1_GAIN_x Settings

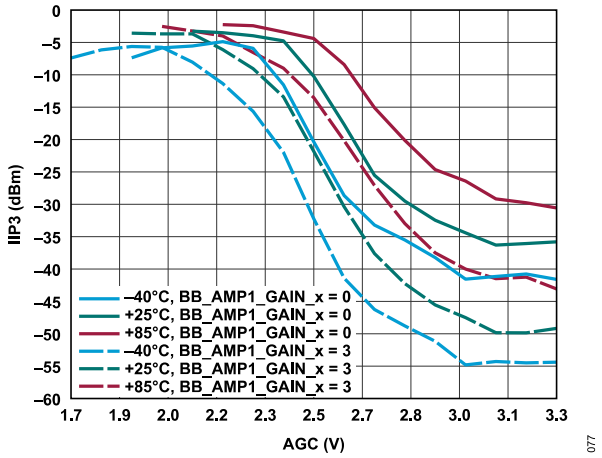

Figure 76. IIP3 vs. AGC, LO = 21 GHz at Maximum Gain (Minimum Input Power) at Various Temperatures and Various BB_AMP1_GAIN_x Settings

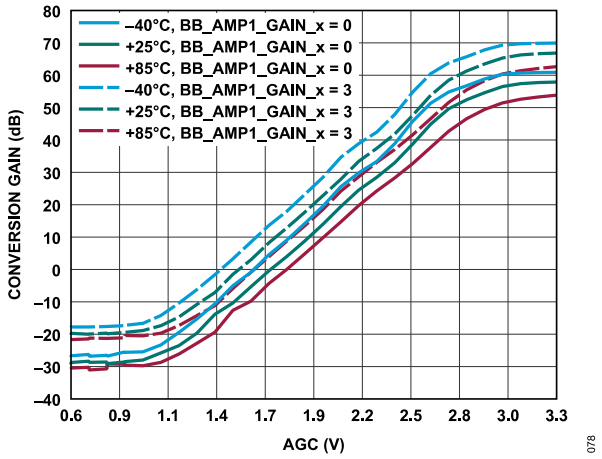

Figure 77. Conversion Gain vs. AGC, LO = 17 GHz, Maximum Gain (Minimum Input Power) at Various Temperatures and Various BB_AMP1_GAIN_x Settings

TYPICAL PERFORMANCE CHARACTERISTICS

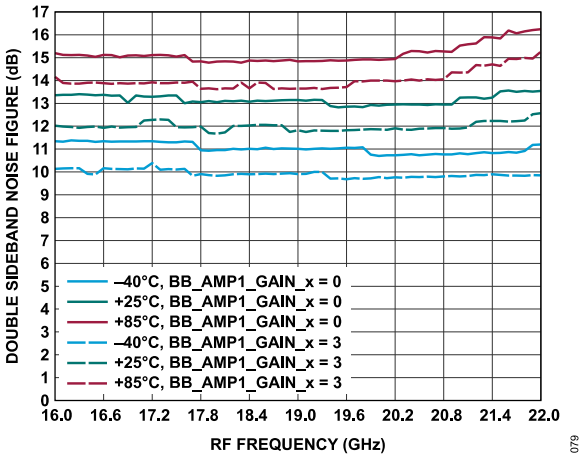

Figure 78. Double Sideband Noise Figure vs. RF Frequency 20 dB Gain (Minimum Input Power) at Various Temperatures and Various BB_AMP1_GAIN_x Settings

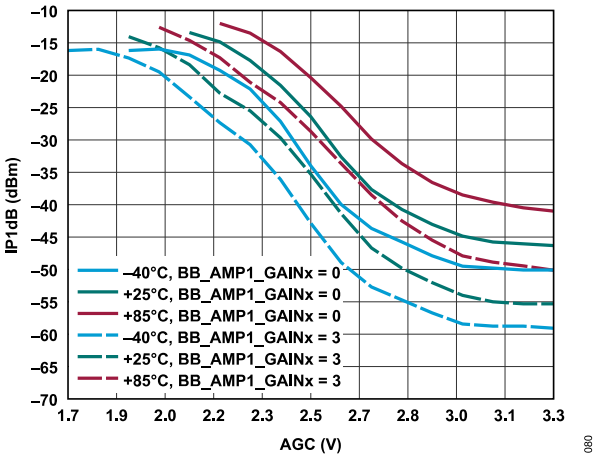

Figure 79. IP1dB vs. AGC, LO = 21 GHz Various Temperatures

THEORY OF OPERATION

The ADMV4540 is a highly integrated quadrature demodulator with integrated fractional-N PLL and LO ideally suited for next generation K band satellite communication. The fractional-N PLL locks the LO to a precise reference input signal for low noise operation. The LO signal is then amplified to generate the necessary LO level for the I/Q mixer. The I/Q mixer generates differential baseband outputs that are amplified using differential baseband amplifiers whose gain can be controlled using external control voltages. The differential baseband output is then filtered using three SPI-selectable LPFs or optionally bypassed.

SPI PROTOCOL

The SPI of the ADMV4540 allows the user to configure the device for specific operation using a 4-wire SPI (SCLK, SDIO, SDO, and $\overline{CS}$). The SPI is compatible with 3.3 V dc logic. See Table 6 for the digital lock timing.

The ADMV4540 protocol consists of a write or read bit, followed by 15 register address (A14 to A0) bits and 8 data bits (D7 to D0). The default for both the address and data fields are organized MSB first and end with the LSB when Register 0x000, Bit 6 is set to 0. For a write, set the first bit (MSB) to 0, and for a read, set this bit to 1. The $\overline{CS}$, SCLK, SDIO, and optional SDO are used to communicate with the ADMV4540. The rising edge of the SCLK is used to latch the data. Figure 80 shows a typical write sequence, and Figure 81 shows a typical 4-wire SPI read sequence.

Table 6. Digital Logic Timing

Parameter	Value	Unit	Description
f_{SCLK}	10	MHz	Maximum serial clock rate, $1/t_{SCLK}$, which is the SCLK time
t_{HI}	50	ns	Minimum period that SCLK is in logic high state
t_{LO}	50	ns	Minimum period that SCLK is in logic low state
t_{DS}	15	ns	Setup time between data and rising edge of SCLK
t_{DH}	10	ns	Hold time between data and rising edge of SCLK
t_{DV}	14	ns	Maximum time delay between the falling edge of SCLK and the output data valid for a read operation in 4-wire mode
t_H	10	ns	Hold time between the rising edge of $\overline{CS}$ and the last falling edge of SCLK
t_S	10	ns	Setup time between the falling edge of $\overline{CS}$ and the rising edge of SCLK
t_Z	12	ns	Maximum time delay between $\overline{CS}$ deactivation and SDIO bus return to high impedance
t_{ACCESS}	14	ns	Maximum time delay between the falling edge of SCLK and the output data valid for a read operation in 3-wire mode

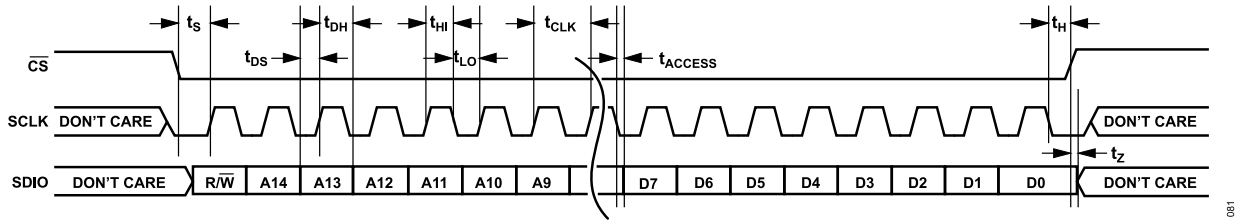

Figure 80. SPI Register Timing Diagram for Analog Devices, Inc., Standard SPI, MSB First

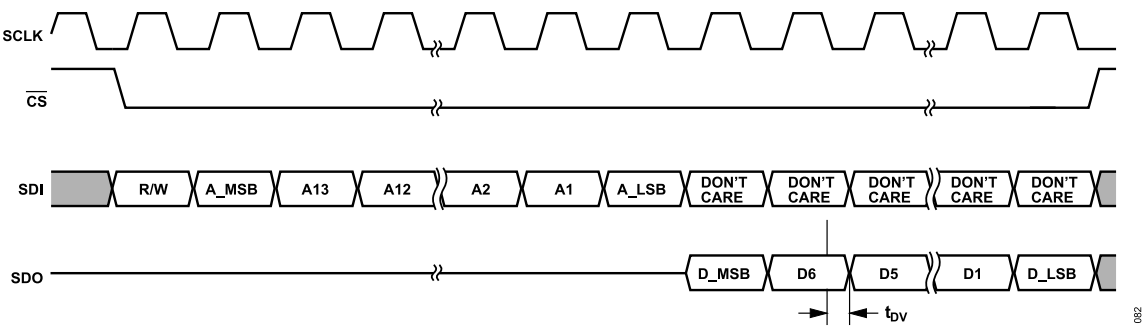

Figure 81. Timing Diagram for Analog Devices Standard SPI Register Read, 4-Wire Mode

THEORY OF OPERATION

SUPPLY SEQUENCING

The ADMV4540 is designed so that all supply pins can be turned on simultaneously. If the different supply pins cannot be turned on simultaneously, turn on VCC3P3_DIG at 3.3 V before all other supply pins. An arbitrary power supply sequence is not recommended. Contact Analog Devices Sales if additional guidance is needed.

SPI START-UP SEQUENCES

The ADMV4540 SPI settings require the SPI to be configured for the required mode of operation. On startup, the SPI mode must be selected along with the RF input port and baseband filter settings.

Soft Reset and 3-Wire and 4-Wire Mode

To set the soft reset in 3-wire mode, take the following steps:

1. Write 0x81 to Register 0x000.
2. Write 0x00 to Register 0x000.

To set the soft reset in 4-wire mode, take the following steps:

1. Write 0x81 to Register 0x000.
2. Write 0x18 to Register 0x000.

Baseband and Common-Mode Recommended Settings

Program the following registers to the recommended settings listed after performing a soft reset and choosing either 3-wire or 4-wire mode:

1. Write 0xCC to Register 0x133.
2. Write 0xFF to Register 0x134.
3. Write 0xFF to Register 0x135.
4. Write 0x4e to Register 0x10A.
5. Write 0x4e to Register 0x10B.

RF Input Port Selection

Either RF_IN1 or RF_IN2 must be selected at startup. Both inputs cannot be selected at the same time.

For the RF_IN1 input port, write 0x3E to Register 0x100, and for the RF_IN2 input port, write 0x3D to Register 0x100.

Baseband Filter Settings

One of the four filter settings must be selected at startup, which include the following:

- For the baseband filter 125 MHz setting, write 0x00 to Register 0x013C.
- For the baseband filter 250 MHz setting, write 0x05 to Register 0x013C.
- For the baseband filter 500 MHz setting, write 0x0A to Register 0x013C.
- For the baseband filter bypass setting, write 0x0F to Register 0x013C.

FREQUENCY UPDATE SEQUENCE

After the SPI start-up sequences (see the SPI Start-Up Sequences section) are performed, the output frequency can be updated by programming the registers as detailed in LO Lock Write Sequence When DOUBLER_EN = 0 section and the LO Lock Write Sequence for DOUBLER_EN = 1 section.

LO Synthesizer Calculations

The following are the LO synthesizer calculations required to calculate the register values when doing a frequency update as indicated in the LO Lock Write Sequence When DOUBLER_EN = 0 section and the LO Lock Write Sequence for DOUBLER_EN = 1 section:

$$Reference\ \ Multiplier = \frac{(1 + DOUBLER\_EN)}{((1 + REF\_DIV\_2) \times (R\_DIV))} \quad (1)$$

$$f_{PFD} = \text{Reference}\ \ \text{Multiplier} \times f_{REF} \quad (2)$$

$$VCO\ Frequency = \frac{LO\ Frequency}{1.5} \quad (3)$$

$$\text{N} = \frac{VCO\ Frequency}{f_{PFD}} \quad (4)$$

$$INT\_DIV = Integer\ \ Value\ \ of\ \ N \quad (5)$$

$$FRAC\,Value\ \ Required = \ \ N - \ \ INT\_DIV \quad (6)$$

$$FRAC1\ \ Required = \ \ FRAC\,Value\ \ Required \times MOD1 \quad (7)$$

$$FRAC1 = \ \ Integer\ \ Value\ \ of\ \ FRAC1\ \ Required \quad (8)$$

If FRAC1 is 0, SD_EN_OUT_OFF = 1, SD_EN_FRAC0 = 0, and BICP = 0.

If FRAC1 is not 0, SD_EN_OUT_OFF = 0, SD_EN_FRAC0 = 0, and BICP= 4 or 130.

$$FRAC1\ \ Remainder = \ \ FRAC1\ \ Required - FRAC \quad (9)$$

$$FRAC2 = FRAC1\ \ \ Remainder \times MOD2 \quad (10)$$

$$VCO\ Frequency = \frac{LO\ Frequency}{1.5} \quad (11)$$

where:
For DOUBLER_EN = 1, CP_CURRENT = 4.
For DOUBLER_EN = 0, CP_CURRENT = 8.
R_DIV = 1.
REF_DIV_2 = 0.
f_{REF} = 50 MHz.
MOD1 = is a 24-bit primary modulus with a fixed value of 2^{24} = 16777216.

THEORY OF OPERATION

MOD2 is a programmable, 14-bit auxiliary fractional modulus (2 to 16,383) with a recommended value = 3.

LO Lock Write Sequence When DOUBLER_EN = 0

Use the following write sequence to update the LO frequency when DOUBLER_EN = 0 and use the values calculated in LO Synthesizer Calculations section.

1. Write 0xA1 to Register 0x22D.
2. Write 0x02 to Register 0x240.
3. If the LO frequency is greater than 18.6 GHz, write 0x04 to Register 0x217, and if the LO frequency is less than or equal to 18.6 GHz, write 0x01 to Register 0x217.
4. Write the BICP value to Register 0x22F.
5. Write the CP_CURRENT value to Register 0x022E.
6. Write the R_DIV value to Register 0x20C.
7. Write 0x04 to Register 0x20E.
8. Write the SD_EN_OUT_OFF value and the SD_EN_FRAC0 value to Register 0x22A.
9. Write the MOD2 value to Register 0x208 to Register 0x209 from the highest to the lowest register.
10. Write the FRAC2 value to Register 0x233 and Register 0x234 from the highest to the lowest register.
11. Write 0x01 to Register 0x20B.
12. Write 0x0A to Register 0x22B.
13. Write the FRAC1 value to Register 0x202 to Register 0x204 from the highest to the lowest register.
14. Write the INT_DIV value to Register 0x200 and Register 0x201 from the highest to the lowest register.
15. Read Register 0x24D. If Register 0x24D data is 0x01, the synthesizer is locked.

LO Lock Write Sequence for DOUBLER_EN = 1

Use the following write sequence to update the LO frequency when DOUBLER_EN = 1 and use the values calculated in LO Synthesizer Calculations section. Note that, DOUBLER_EN = 1 is the recommended mode for optimal integrated phase noise performance.

1. Write 0x80 to Register 0x21F.
2. Lock the device with DOUBLER_EN = 0 based on the LO synthesizer calculations (see the LO Synthesizer Calculations section) and the procedure outlined in LO Lock Write Sequence When DOUBLER_EN = 0 section.
3. Verify that the synthesizer is locked by reading Register 0x24D. If the readback is 0x01, the synthesizer is locked.
4. Write 0xC0 to Register 0x21F.
5. Go through the LO synthesizer calculations (see the LO Synthesizer Calculations section) again based on DOUBLER_EN = 1. Make note of these values for the next steps.
6. Write 0xA1 to Register 0x022D.
7. Write 0x02 to Register 0x240.
8. If the LO frequency is greater than 18.6 GHz, write 0x04 to Register 0x217, and if the LO frequency is less than or equal to 18.6 GHz, write 0x01 to Register 0x217.
9. Write the BICP value to Register 0x22F.
10. Write the CP_CURRENT value to Register 0x022E. Program with half the value used in Step 2 to keep the loop gain constant.
11. Write the R_DIV value to Register 0x20C.
12. Write 0x0C to Register 0x20E.
13. Write the SD_EN_OUT_OFF value and the SD_EN_FRAC0 value to Register 0x22A.
14. Write the MOD2 value to Register 0x208 to Register 0x209 from the highest to the lowest register.
15. Write the FRAC2 value to Register 0x233 and Register 0x234 from the highest to the lowest register.
16. Write 0x01 to Register 0x20B.
17. Write 0x0A to Register 0x22B.
18. Write the FRAC1 value to Register 0x202 to Register 0x204 from the highest to the lowest register.
19. Write the INT_DIV value to Register 0x200 and Register 0x201 from the highest to the lowest register.
20. Read Register 0x24D. If Register 0x24D data is 0x01, the synthesizer is locked.
21. Write 0x80 to Register 0x21F.

N COUNTER

The N counter allows a division ratio in the PLL feedback path from the LO. Note that the signal from the N counter is multiplied by 1.5 to achieve the LO frequency at the input of the mixer. The division ratio is determined by using the Integer N (INT_DIV), fractional-N (FRAC1 and FRAC2), and modulus (MOD2) values that this counter comprises. The applicable registers for setting the INT_DIV, FRAC1, MOD2, and FRAC2 values are Register 0x200 to Register 0x204, Register 0x208 to Register 0x209 and Register 0x233 to Register 0x234.

THEORY OF OPERATION

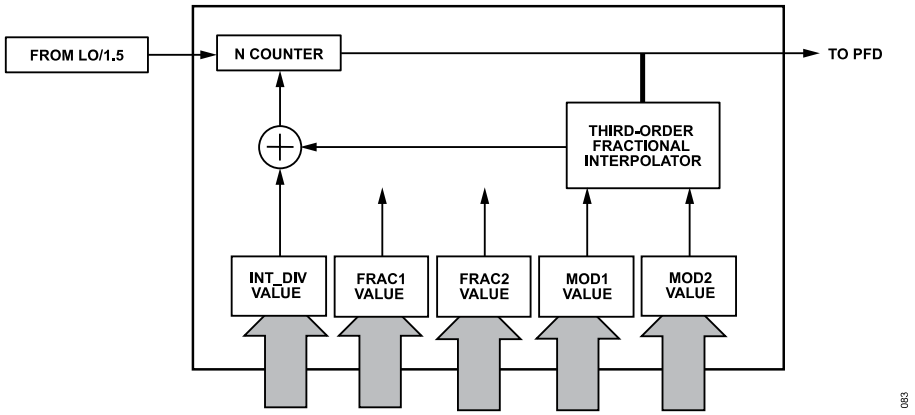

Figure 82. N Counter Functional Block Diagram

DOUBLE BUFFERED REGISTERS

The PLL inside the ADMV4540 contains several double buffered bit fields that take effect only after a write to the lower portion of the N counter integer value (Register 0x200). This register applies any changes to these double buffered bit fields and initiates the autocalibration routine. The following is a list of the double buffered bit fields and their corresponding registers:

- RDIV2_SEL (Register 0x20E)
- DOUBLER_EN (Register 0x20E)
- R_DIV (Register 0x20C)
- CP_CURRENT (Register 0x22E)
- FRAC2 (Register 0x233 and Register 0x234)
- FRAC1 (Register 0x202 through Register 0x204)
- MOD2 (Register 0x208 and Register 0x209)
- INT_DIV (Register 0x200 and Register 0x201)

LOOP FILTER

Figure 83 shows the loop filter configuration for the ADMV4540. Resistor and capacitor values must be within 1% tolerance. The loop filter is optimized for integrated phase noise and to operate from 17 GHz to 21.5 GHz. When the doubler is enabled, use a charge pump current setting of 4. When the doubler is disabled, use a charge pump setting of 8.

The loop filter, as implemented is a third-order passive filter (see Figure 83). The filter is designed with the following simulation input parameters: f_{PFD} = 50 MHz/100 MHz, K_{VCO} = 190 MHz/V, LO frequency = 21.2 GHz, and I_{CP} = 1.5 mA (CP_CURRENT = 4). The resulting loop filter bandwidth and phase margin are 220 kHz and 60°, respectively, for the following component values: C1 = 220 pF, C2 = 15 nF, C3 = 150 pF, R1 = 750 Ω, and R2 = 750 Ω. Ensure that C1 is placed as close as possible to CPOUT (Pin 18).

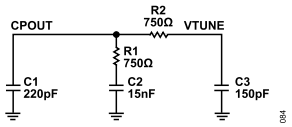

Figure 83. Loop Filter

REFERENCE INPUT

Figure 84 shows the reference input stage. There is an internal reference multiply by 2 block (×2 doubler) that allows generation of higher $f_{PFD.}$ A higher f_{PFD} is useful for improving overall system phase noise performance. Typically, doubling the f_{PFD} improves the in band phase noise performance by up to 3 dBc/Hz. Use the DOUBLER_EN bit (Register 0x20E, Bit 3) to enable the reference doubler. Following the reference doubler block, there are two frequency dividers: a 5-bit R counter (1 to 32 allowed) and a divide by 2 block. These dividers allow the REF_{IN} frequency to be divided down to produce lower f_{PFD}, which helps minimize the fractional-N integer boundary spurs at the output. Use the R_DIV bits (Bits[4:0]) in Register 0x20C to set the R counter. If R_DIV = 1, the R counter is bypassed. Additionally, R_DIV = 0 corresponds to a divide by 32 value for the R counter. To enable the reference divide by 2 block, use the RDIV2_SEL bit (Register 0x020E, Bit 0).

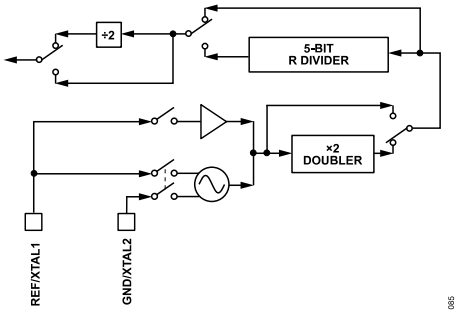

Figure 84. Reference Input Stage

The ADMV4540 has two options to input the reference signal into the device: a single-ended external reference and a differential crystal oscillator.

THEORY OF OPERATION

The schematic to configure for the single-ended external reference is shown in Figure 85.

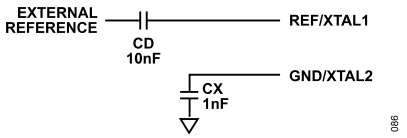

Figure 85. External Circuitry for Single-Ended Reference

To set the ADMV4540 single-ended external reference option, set the EN_XTAL_BUFMODE bit in Register 0x129 (Bit 1) to 1 and vice versa to disable this option.

See the Crystal Oscillator section for how to set the differential crystal oscillator option.

CRYSTAL OSCILLATOR

To set the ADMV4540 differential crystal oscillator option, set the EN_XTAL_BUFMODE bit in Register 0x129 (Bit 1) to 0 and vice versa to disable this option. The circuit for the crystal oscillator is shown in Figure 86.

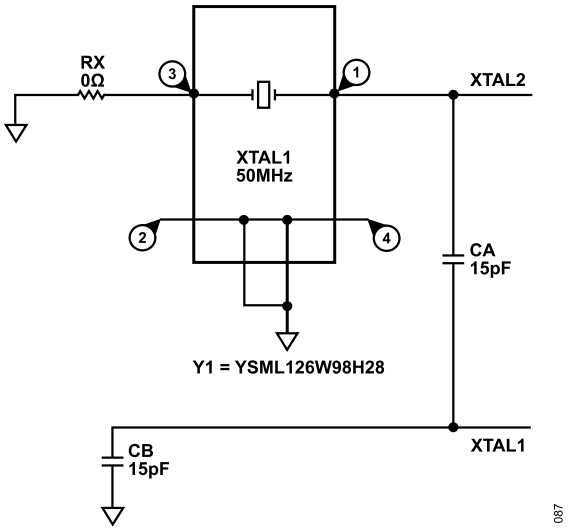

Figure 86. External Circuitry for Crystal Oscillator

CHARGE PUMP CURRENT SETUP

For a specifically designed loop filter, set the I_{CP} by adjusting the CP_CURRENT value in Bits[3:0], Register 0x22E. To calculate I_{CP}, use the following equation:

$$I_{CP} = (CP\_CURRENT + 1) \times 300\mu A \quad (12)$$

where *CP_CURRENT* is an integer value (0 to 15).

The recommended value for a 100 MHz f_{PFD} is CP_CURRENT = 4, which yields a current of 1.5 mA based on the recommended loop filter configuration. The applicable range is 0.30 mA to 4.8 mA, with 0.30 mA steps.

To change the f_{PFD}, if no change has been made to the existing loop filter components, it is recommended to scale I_{CP} by using the following equation:

$$I_{CP\ (NEW)} = \frac{I_{CP(DEFAULT)} \times f_{PFD(DEFAULT)}}{f_{PFD(NEW)}} \quad (13)$$

where:
$I_{CP\ (NEW)}$ is the new desired I_{CP}.
$I_{CP\ (DEFAULT)}$ is the default I_{CP}.
$f_{PFD\ (DEFAULT)}$ is the default f_{PFD}.
$f_{PFD\ (NEW)}$ is the new desired f_{PFD}.

When $I_{CP(NEW)}$ is obtained, the CP_CURRENT value in Register 0x22E can be updated using the round function,

$$CP\_CURRENT = ROUND\frac{\left(I_{CP(NEW)}\right)}{300\ \mu A} - 1 \quad (14)$$

where *ROUND* is the mathematical round function.

BLEED CURRENT (BICP) SETUP

The charge pump includes a binary scaled bleed current (I_{BLEED}) that is set by using the BICP value in Register 0x22F. The bleed current introduces a slight phase offset in the phase frequency detector to improve integer boundary spurs and phase noise when operating in fractional-N mode. To enable the bleed current for fractional-N mode, set BLEED_EN = 1 (Register 0x22D, Bit 0). For integer mode, BLEED_EN must be set to 0.

Generally, the optimum bleed current value is either 4 or 130, and this value provides optimal performance for most applications. However, there can be additional performance improvements by empirically determining the appropriate bleed current value from the actual measurements for the intended application. The applicable range is 0 µA to 956.25 µA, with 3.75 µA steps.

$$I_{BLEED} = BICP \times 3.75\mu A \quad (15)$$

where *BICP* is an integer value (0 to 255).

DIGITAL LOCK DETECT

A digital lock detect bit (LOCK_DETECT) is available in Bit 0 of Register 0x24D. A logic high indicates that the digital lock detect has declared the PLL is locked.

The digital lock detect function has some adjustable settings in Register 0x214. The LD_BIAS and LDP bits of Register 0x214 adjust an internal precision window. It is recommended to keep the settings listed in the register map.

The lock detect output is also available on the MUXOUT pin by selecting EN_MUXOUT (Register 0x120, Bit 7) to 1 and the MUX_SEL bit field (Register 0x24E, Bits[7:0]) to 1.

THEORY OF OPERATION

PFD AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter to produce an output that is proportional to the phase and frequency differences between these counters. This proportional information is then output to a charge pump circuit that generates current to drive an external loop filter that is then used to appropriately increase or decrease VTUNE.

Figure 87 shows a simplified schematic of the PFD and charge pump. Note that the PFD includes a fixed delay element that ensures that there is no dead zone in the PFD transfer function for consistent reference spur levels.

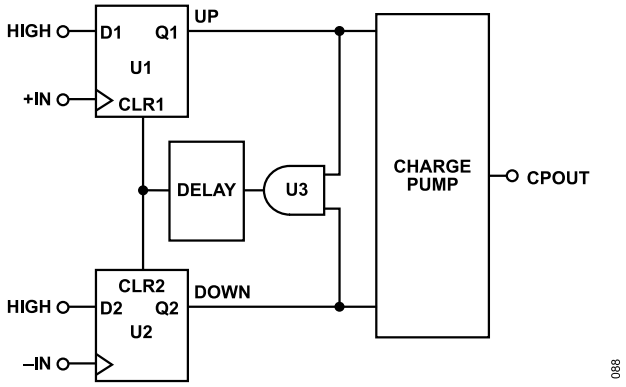

Figure 87. PFD and Charge Pump Simplified Schematic

VCO AUTOCALIBRATION

The internal VCO uses an internal autocalibration routine that optimizes the VCO settings for a particular frequency and allows the PLL to lock after the lower portion of the N counter integer value (Register 0x200) is programmed. For nominal applications, maintain the autocalibration default values in the register map unless suggested as in the LO Lock Write Sequence for DOUBLER_EN = 1 section for operation at higher PFD frequencies.

AUTOCALIBRATION LOCK TIME

The PLL lock time divides into a number of settings. The total lock time for changing frequencies is the sum of three separate times: synthesizer lock, VCO band selection, and PLL settling.

SYNTHESIZER LOCK TIMEOUT

The synthesizer lock timeout ensures that the VCO calibration digital-to-analog converter (DAC), which forces the VCO tune voltage (VTUNE), has settled to a steady value for the band select circuitry. The SYNTH_LOCK_TIMEOUT bits (Register 0x218) and the VCO_TIMEOUT bits (Register 0x21C and Register 0x21D) select the length of time the DAC is allowed to settle to the final voltage before the VCO calibration process continues to the next phase (VCO band selection). The PFD frequency is the clock for this logic, and the duration is set by using the following equation:

$$(SYNTH\_LOCK\_TIMEOUT \times 1024 + VCO\_TIMEOUT)/f_{PFD} \quad (16)$$

where:
SYNTH_LOCK_TIMEOUT is programmed in Bits[4:0], Register 0x218.
VCO_TIMEOUT is programmed in Bits[7:0], Register 0x21C and Bits[1:0], Register 0x21D.

The calculated time must be greater than or equal to 30 µs. For the SYNTH_LOCK_TIMEOUT bits, the minimum value is 2, and the maximum value is 31. For VCO_TIMEOUT, the minimum value is 2, and the maximum value is 1023.

VCO BAND SELECTION TIME

Use the VCO_BAND_DIV bits (Bits[7:0], Register 0x21E) and the f_{PFD} to generate the VCO band selection clock (f_{BSC}) as follows:

$$f_{BSC} = (f_{PFD}/VCO\_BAND\_DIV)$$

The calculated frequency must be less than 2.4 MHz.

Note that 16 clock cycles are required for one VCO core and band calibration step, and the total band selection process takes 11 steps, resulting in the following equation:

$$11 \times \left(\frac{16 \times VCO\_BAND\_DIV}{f_{PFD}}\right) \quad (17)$$

The minimum value for VCO_BAND_DIV is 1, and the maximum value is 255.

PLL SETTING TIME

The time taken for the loop to settle is inversely proportional to the loop filter bandwidth.

THEORY OF OPERATION

VCO CALIBRATION BAND READ BACK

To read back the VCO calibration band data, load the required registers, let the device lock using the procedures stated in LO Lock Write Sequence When DOUBLER_EN = 0 section and the LO Lock Write Sequence for DOUBLER_EN = 1 section, and read the VCO band for each frequency once the device is locked by reading Bit 1 in Register 0x24D. If Bit 0 of Register 0x24D is 1, the VCO band can be read back by reading SI_VCO_FSM_CAPS_RB in Register 0x248, Bits[7:1]. The ADMV4540 has two VCO cores with each VCO core comprising 128 bands.

TEMPERATURE SENSOR CONFIGURATION

The ADMV4540 has an on-chip temperature sensor. This temperature sensor output can be configured so that the temperature sensor value appears on the AGPIO pin (Pin 4) of the ADMV4540. Note that this pin must not be loaded down less than 1 kΩ to get an accurate measurement.

To configure the temperature sensor to read its outputs on the AGPIO pin, write 0x06 to Register 0x301.

The following equation relates the temperature sensor voltage reading from the AGPIO pin to the temperature at the temperature sensor:

$$Temperature\ \ on\ \ the\ \ Chip\ \ near\ \ the\ \ Temperature\ \ Sensor\ \ (℃)\ \ = APIO(V) \times 314 - 179 \quad (18)$$

The temperature sensor output can also be configured to be read from the on-chip ADC. To configure the temperature sensor to read its outputs from the on-chip ADC, write 0x0E to Register 301.

See the ADC Configuration section for how to read its outputs by the ADC.

ADC CONFIGURATION

The ADMV4540 has an 8-bit resolution on-chip ADC that can be used to either read the temperature sensor output or read a voltage between 0 V to 2.3 V from the AGPIO pin.

To configure the ADC to read from the AGPIO pin, write 0x0F to Register 0x301.

Take the following steps to read a voltage from the ADC from the temperature sensor:

1. Enable the ADC (ENABLE_ADC), Bit 0 on Register 0x302.
2. Set the ADC_START bit, Bit 1 on Register 0x302 to 0.
3. Set the ADC_START, Bit 1 on Register 0x302 to 1.
4. Keep reading Register 0x303 (ADC_STATUS) until the ADC_EOC bit (Bit 0) is 1 and the ADC_BUSY bit (Bit 1) is 0.
5. Read Register 0x304 (ADC_DATA) to get the ADC data.

The ADC range can be configured from 0 V to 1.2 V by setting the ADC_HALF_SEL bit, Bit 2 in Register 0x302, to 0.

The ADC range can be configured from 0 V to 2.3 V by setting the ADC_HALF_SEL bit, Bit 2 in Register 0x302, to 1.

The ADC range can be configured to be linear in volts by setting the ADC_LOG_SEL bit, Bit 3 in Register 0x302, to 0.

The ADC range can be configured to be logarithmic by setting the ADC_LOG_SEL bit, Bit 3 in Register 0x302, to 1.

The ADC clock (ADC_CLK) is generated from the f_{REF}.

$$ADC\_CLOCK = \frac{f_{REF}}{(2 \times SEL\_ADC\_CLKDIV)} \quad (19)$$

where *SEL_ADC_CLKDIV* is stored in Bits[7:4] of Register 0x302.

GAIN POLICY

The ADMV4540 has three baseband VCTRL pins: VCTRL_BBVVA1 (Pin 39), VCTRL_BBVVA2 (Pin 38), and VCTRL_BBVVA3 (Pin 37). The recommended gain policy to optimize noise figure over temperature at the maximum specified RF input power is as follows:

- Keep VCTRL_BBVVA1 (Pin 39) at 3.3 V.
- VCTRL_BBVA2 (Pin 38) and VCTRL_BBVVA3 (Pin 37) are swept together to attenuate the ADMV4540.

The three baseband VCTRL_BBVVAx pins can also be swept together. The RF performance for this condition is shown in the Performance with Controlling VCTRL_BBVVA1, VCTRL_BBVVA2, and VCTRL_BBVVA3 Together section.

POWER DOWN

The ADMV4540 has a power-down pin (PD, Pin 43) to reduce power dissipation while keeping the synthesizer locked. The rest of the analog circuitry, temperature sensor, and ADC are disabled when the ADMV4540 is in a power-down state. Set to a logic high of 3.3 V to power down the device with a power dissipation of approximately 0.6 W, and set to logic low to power up the device.

MUXOUT

The output multiplexer on the ADMV4540 allows the user to access various internal signals on the chip. The MUX_SEL bit field (Register 0x24E, Bits[7:0]) shown in MUXOUT register lists the available signals. When the EN_MUXOUT bit (Register 0x120, Bit 7) is set to 1, the MUXOUT signal is enabled. Otherwise, the MUXOUT signal is disabled.

THEORY OF OPERATION

GPIOS

The ADMV4540 has two GPIO pins that can be configured to be outputs or inputs. GPIO1 is Pin 44 and GPIO2 is Pin 45. To set both the GPIOx pins as outputs, set the EN_GPIO_OUT bits, Bits[5:4] in Register 0x307 (see the Control of GPIOx Pins section), to 0x3. To set both the GPIOx pins as outputs, set the EN_GPIO_OUT bits, Bits[5:4] in Register 0x307, to 0x0.

To set the GPIOx pins as 3.3 V logic, set the SEL_GPIO_LEVELS bits, Bits[2:1] in Register 0x307, to 0x3. To set the GPIOx pins as 1.8 V logic, set the SEL_GPIO_LEVELS bits, Bits[2:1] in Register 0x307, to 0x0.

When the GPIOx pins are set to output, the output values for the two GPIOx pins are set in the GPIO_WRITEVALS bits, Bits[2:1] in Register 0x305. Bit 1 sets the GPIO1 logic level, and Bit 2 sets the GPIO2 logic level (see the GPIOx Write Register section).

When the GPIOx pins are set to input, the input values for the two GPIOs pins are read in the GPIO_READVALS bits, Bits[2:1] in Register 0x306. Bit 1 sets the GPIO1 logic level, and Bit 2 sets the GPIOs2 logic level (see the GPIO Read Register section).

LNA SELECTION

The ADMV4540 has two RF input paths that are SPI selectable. Only use one path at a time. The SPI settings are used to turn on the specific LNA for each path as follows:

- To select RF_IN1 (Pin 2), write 0x3E to Register 0x0100.
- To select RF_IN1 (Pin 47), write 0x3D to Register 0x0100.

BASEBAND FILTER SELECTION

The ADMV4540 features three 6th -order Butterworth LPF configurations on the I channel and the Q channel that can be digitally selected and a fourth digitally selectable configuration that can bypass all of the filters. These three LPFs are approximately 125 MHz, 250 MHz, and 500 MHz bandwidth on each I channel and Q channel. To select one of these four configurations, take the following steps:

- To select the baseband filter 125 MHz settings, write 0x00 to Register 0x013C.
- To select the baseband filter 250 MHz settings, write 0x05 to Register 0x013C.
- To select the baseband filter 500 MHz settings, write 0x0A to Register 0x013C.
- To select the baseband filter bypass settings, write 0x0F to Register 0x013C.

IMAGE REJECT OPTIMIZATION

The ADMV4540 provides an uncalibrated 35 dBc of image rejection. The image rejection can be further optimized by tuning the phase bits (LO_PHASE_I, Register 0x128, Bits[2:0], and LO_PHASE_Q,
Register 0x128, Bits[5:3]), which have up to 6° of phase range and approximately 0.4° resolution, and by tuning the 0.1 dB DSA bits (SEL_BB_ATT_I, Register 0x140, Bits[3:0], and SEL_BB_ATT_Q, Register 0x140, Bits[7:4]) with up to a 1.5 dB range.

DC OFFSET CORRECTION LOOP

The ADMV4540 has a dc offset correction loop in the I path and Q path, respectively. The dc offset correction loop is enabled by default (EN_BB_OFS_LOOP_I, Bit 4 in Register 0x130 and EN_BB_OFS_LOOP_Q, Bit 4 in Register 0x131). Keep the dc offset correction loop enabled; otherwise, the dc offset saturates the baseband amplifiers clipping the output signal.

APPLICATIONS INFORMATION

The ADMV4540 is intended to be used in receiver terrestrial satellite communication systems. The ADMV4540 integrates a low noise downconverter, fractional-N PLL and synthesizer, baseband amplifiers, and low-pass baseband filters. The integrated solution can directly interface with the receiver ADC and supports the DVB-S2X standard and is backwards compatible with earlier standards. Figure 88 shows a simplified system block diagram of the ADMV4540.

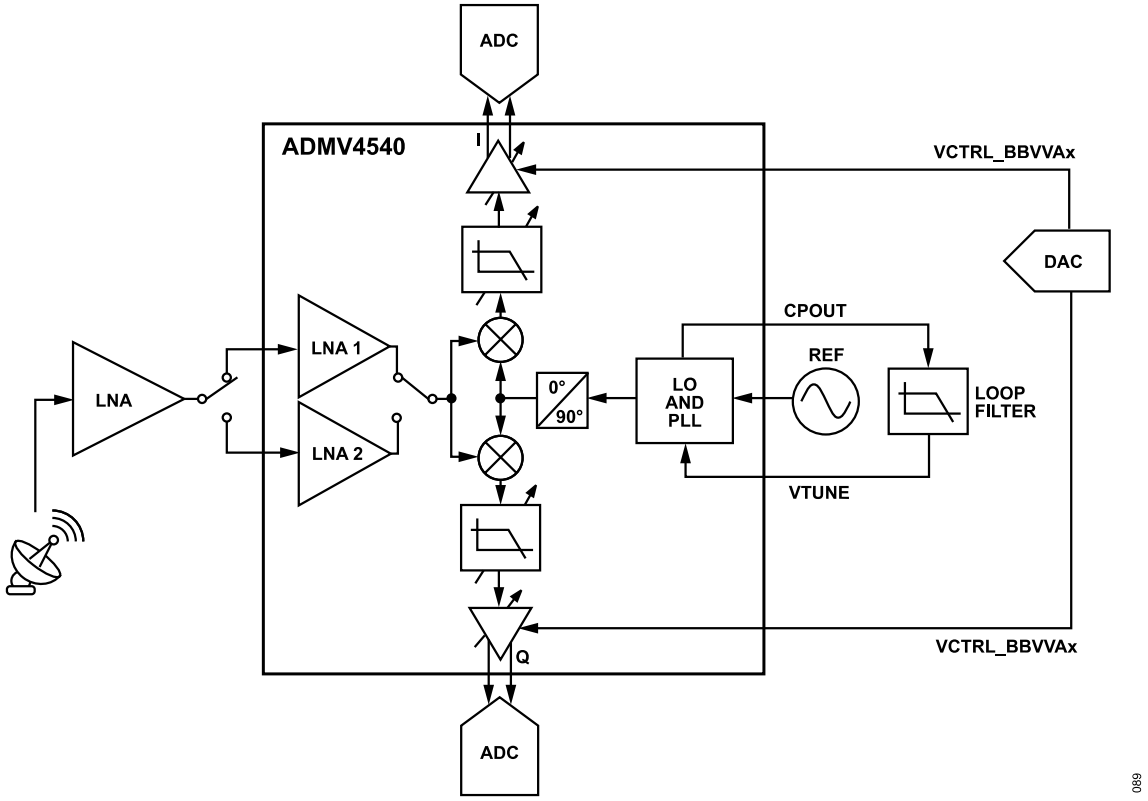

Figure 88. System Block Diagram of the ADMV4540

APPLICATIONS INFORMATION

POWERING THE ADMV4540

The ADMV4540 has two power supply domains where low noise LDO regulators of 3.3 V each are recommended, such as the ADM7172, which is shown in the ADMV4540-EVALZ user guide, for optimum phase noise and noise figure performance:

- VCC3P3_VCO (Pin 14)
- VCC3P3_BBI (Pin 35), VCC3P3_BBQ (Pin 27), and VCC3P3_BB (Pin 42)

All other supply lines can be connected to a single low noise 3.3 V supply voltage to ensure low noise power delivery.

All supplies require 0.01 µF decoupling capacitors placed as close as possible to the supply pins.

Ensure that the three baseband supply pins have their own power plane for minimal voltage drop from the low noise LDO regulator to each of the baseband supply pins.

HEAT SINK SELECTION

The ADMV4540 requires a bottom side heat sink for efficient heat transfer. The bottom side heat sink requires a large, exposed copper area on the PCB bottom layer under the device. Ensure that the exposed pad is filled with thermal vias for efficient heat transfer from the top of the PCB, where the ADMV4540 is attached to the bottom, where the heat sink is placed. Connect the thermal vias to a ground plane on each layer that the vias cross. Make sure that the vias are plated shut and sit flush with the top and bottom ground plane. A heat sink with embedded copper is recommended for more efficient heat transfer. Place a thin thermal interface material (TIM) with high conductivity between the PCB bottom layer and bottom side heat sink for efficient heat transfer.

The exposed pad requires a solder coverage of more than 90% for optimum heat transfer between the bottom of the ADMV4540 and the exposed pad. Ensure that there are no solder voids. Solder voids underneath the ADMV4540 degrade the RF performance of the ADMV4540.

RECOMMENDED LAND PATTERN

Solder the exposed pad on the underside of the ADMV4540 to a low thermal and electrical impedance ground plane. This pad is typically soldered to an exposed opening in the solder mask on the ADMV4540-EVALZ evaluation board. Connect these ground vias to all other ground layers on the ADMV4540-EVALZ evaluation board to maximize heat transfer from the device package. See the ADMV4540-EVALZ gerber files on the recommended solder mask for the ADMV4540. See the Heat Sink Selection section for more information on the solder coverage of the exposed pad.

LAYOUT CONSIDERATIONS

All measurements in this data sheet are measured on the ADMV4540-EVALZ. The design of the ADMV4540-EVALZ serves as a layout recommendation for ADMV4540 application. See the ADMV4540-EVALZ user guide for more information on using the evaluation board.

RF Trace Routing

The two RF inputs of the ADMV4540 require 50 Ω traces. These traces must use optimal RF transmission line layout techniques and can be either coplanar waveguide (CPWG) or stripline traces. These traces must also use tight via fences with a typical via to via spacing of 1/8 the minimum wavelength or less up to the ground pin next to these pins. Ensure that these via fences also cover the RF_INx pins (Pin 2 and Pin 47) for further isolation.

External Reference and Crystal Oscillator Routing

It is recommended that the reference traces to REF/XTAL1 (Pin 22) and GND/XTAL2 (Pin 21) are 50 Ω. Route these traces mostly on the bottom layer, or a layer different from where the I and Q traces and the traces of the loop filter are located. This routing is recommended for maximizing reference spur rejection at the I and Q outputs of the ADMV4540.

Baseband Trace Routing

The IOUTP and IOUTN traces require 100 Ω differential and 50 Ω single-ended traces. Similarly, the QOUTP and QOUTN require 100 Ω differential and 50 Ω single-ended traces. Ensure that there is sufficient isolation between the IOUTx and QOUTx traces using tight via fences with typical via to via spacing of 1/8 the minimum wavelength or less.

REGISTER SUMMARY

Table 7. Register Summary

Register	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x000	ADI_SPI_CONFIG	[7:0]	SOFT RESET_	LSB_ FIRST_	ENDIAN_	SDO ACTIVE_	SDO ACTIVE	ENDIAN	LSB_ FIRST	SOFT RESET	0x00	R/W
0x004	PRODUCT_ID_L	[7:0]	PRODUCT_ID_L								0x4A	R
0x005	PRODUCT_ID_H	[7:0]	PRODUCT_ID_H								0x00	R
0x00B	SPI_REV	[7:0]	SPI_REV								0x01	R
0x100	RF_CKT_ENABLES	[7:0]	RESERVED	ENABLE_ RF_ MIXER_ BIAS	EN_ RFAMP_Q	EN_ RFAMP_I	EN_ LNA_Q	EN_ LNA_I	EN_ LNA_1	EN_ LNA_2	0x3D	R/W
0x10A	COMMON_MODE_I	[7:0]	RESERVED					COMMON_MODE_I			0x4A	R/W
0x10B	COMMON_MODE_Q	[7:0]	RESERVED					COMMON_MODE_Q			0x4A	R/W
0x120	LO_CKT_ENABLES	[7:0]	EN_ MUXOUT	EN_ SYNTH	EN_VCO_ QUADBUF	EN_LO_ BUF_Q	EN_LO_ BUF_I	EN_LO_ PPF DRIVER	EN_LO_ MULT	EN_LO_ DIVIDER	0xFF	R/W
0x128	LO_PHASE_IMR	[7:0]	RESERVED		LO_PHASE_Q			LO_PHASE_I			0x00	R/W
0x129	XTAL_OSC	[7:0]	RESERVED						EN_XTAL_ BUFMODE	EN_XTAL_ OSC	0x0F	R/W
0x130	BB_CKT_ENABLES_I	[7:0]	ENABLE_ BBAMP3_I	EN_BB_ DC_ SWCH_I	ENABLE_ BBAMP2_I	EN_BB_ OFS_ LOOP_I	EN_BB_ OFS_ OTRIM_I	ENABLE_ BB_ OFS_I	ENABLE_ BB_FLT_I	ENABLE_ BBAMP1_I	0xBF	R/W
0x131	BB_CKT_ENABLES_Q	[7:0]	ENABLE_ BBAMP3_ Q	EN_BB_ DC_ SWCH_Q	ENABLE_ BBAMP2_ Q	EN_BB_ OFS_ LOOP_Q	EN_BB_ OFS_ OTRIM_Q	ENABLE_ BB_OFS_ Q	ENABLE_ BB_FLT_Q	ENABLE_ BBAMP1_ Q	0xBF	R/W
0x132	BB_CKT_ENABLES_COMMON	[7:0]	RESERVED							EN_BB_ COMMON	0x01	R/W
0x133	BB_AMP1_SEL_IQ	[7:0]	RESERVED		BB_AMP1_ GAIN_Q		RESERVED		BB_AMP1_GAIN_I		0xEE	R/W
0x134	BB_AMP2_SEL_IQ	[7:0]	RESERVED		BB_AMP2_ GAIN_Q		RESERVED		BB_AMP2_GAIN_I		0xEE	R/W
0x135	BB_AMP3_SEL_IQ	[7:0]	RESERVED		BB_AMP3_ GAIN_Q		RESERVED		BB_AMP3_GAIN_I		0xEE	R/W
0x13C	BB_FLT_SEL_IQ	[7:0]	RESERVED				SEL_BB_FLT_FC_Q		SEL_BB_FLT_FC_I		0x0A	R/W
0x140	BB_DSA_IQ	[7:0]	SEL_BB_ATT_Q					SEL_BB_ATT_I			0x77	R/W
0x200	INT_L	[7:0]	INT_DIV[7:0]								0x89	R/W
0x201	INT_H	[7:0]	INT_DIV[15:8]								0x01	R/W
0x202	FRAC1_L	[7:0]	FRAC1[7:0]								0x00	R/W
0x203	FRAC1_M	[7:0]	FRAC1[15:8]								0x00	R/W
0x204	FRAC1_H	[7:0]	FRAC1[23:16]								0x00	R/W
0x208	MOD_L	[7:0]	MOD2[7:0]								0x00	R/W
0x209	MOD_H	[7:0]	RESERVED		MOD2[13:8]						0x00	R/W
0x20B	SYNTH	[7:0]	RESERVED						PRE_SEL	EN_FBDIV	0x01	R/W
0x20C	R_DIV	[7:0]	RESERVED			R_DIV					0x03	R/W
0x20E	SYNTH_0	[7:0]	RESERVED				DOUBLER_EN	RESERVED		RDIV2_SEL	0x04	R/W

REGISTER SUMMARY

Table 7. Register Summary

Register	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x214	MULTI_FUNC_ SYNTH_ CTRL_0214	[7:0]	LD_BIAS		LDP			RESERVED			0x48	R/W
0x215	SI_BAND_0	[7:0]	SI_VCO_BAND								0x00	R/W
0x217	SI_VCO_CORE	[7:0]	RESERVED				SI_VCO_CORE				0x00	R/W
0x218	SYNTH_ LOCK_ TIMEOUT	[7:0]	RESERVED			SYNTH_LOCK_TIMEOUT					0x1F	R/W
0x21C	VCO_TIMEOUT_L	[7:0]	VCO_TIMEOUT[7:0]								0x20	R/W
0x21D	VCO_TIMEOUT_H	[7:0]	RESERVED						VCO_TIMEOUT[9:8]		0x00	R/W
0x21E	VCO_BAND_DIV	[7:0]	VCO_BAND_DIV								0x14	R/W
0x21F	ALC_SELECT	[7:0]	RESERVED	DISABLE _CAL	RESERVED						0x80	R/W
0x22A	SD_CTRL	[7:0]	RESERVED		SD_EN_ FRAC0	SD_EN_ OUT_OFF	RESERVED				0x02	R/W
0x22B	MULTI_FUNC_ SYNTH_ CTRL_022B	[7:0]	RESERVED						RF_PBS		0x09	R/W
0x22C	MULTI_FUNC_ SYNTH_ CTRL_022C	[7:0]	RESERVED						CP_HIZ		0x03	R/W
0x22D	MULTI_FUNC_ SYNTH_ CTRL_022D	[7:0]	RESERVED		SEL_PFD_ POLARITY	RESERVED				BLEED_ EN	0x81	R/W
0x22E	CP_CURR	[7:0]	RESERVED				CP_CURRENT				0x0F	R/W
0x22F	BICP	[7:0]	BICP								0x08	R/W
0x233	FRAC2_L	[7:0]	FRAC2[7:0]								0x00	R/W
0x234	FRAC2_H	[7:0]	RESERVED		FRAC2[13:8]						0x00	R/W
0x240	VCO_FORCE	[7:0]	RESERVED						FORCE_ VCO_ CORE	FORCE_ VCO_ BAND	0x00	R/W
0x248	VCO_FSM_ CAPS_RB	[7:0]	SI_VCO_FSM_CAPS_RB							RESERVED	0x00	R
0x24D	LOCK_DETECT	[7:0]	RESERVED							LOCK_ DETECT	0x00	R
0x24E	MUXOUT	[7:0]	MUX_SEL								0x00	R/W
0x300	PLLMUXOUT_ CONTROL	[7:0]	RESERVED							SEL_ MUXOUT_ LEVEL	0x01	R/W
0x301	AGPIO_CONTROL	[7:0]	RESERVED				SEL_ AGPIO	SEL_AMUX			0x00	R/W
0x302	ADC_CONTROL	[7:0]	SEL_ADC_CLKDIV				ADC_ LOG_ SEL	ADC_ HALF_ SEL	ADC_ START	ENABLE_ ADC	0xCA	R/W
0x303	ADC_STATUS	[7:0]	RESERVED					ADC_ LATCH DATA	ADC_ BUSY	ADC_EOC	0x00	R
0x304	ADC_DATA	[7:0]	ADC_DATA								0x00	R
0x305	GPIO_WRITEVALS	[7:0]	RESERVED					GPIO_ WRITEVALS		RESERVED	0x00	R/W

REGISTER SUMMARY

Table 7. Register Summary

Register	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	R/W
0x306	GPIO_READVALS	[7:0]	RESERVED					GPIO_READVALS		RESERVED	0x00	R
0x307	GPIO_CONTROL	[7:0]	RESERVED		EN_GPIO_OUT		RESERVED	SEL_GPIO_LEVELS		RESERVED	0x00	R/W
0x600	SPARE_READREG1	[7:0]	SPARE_READBITS1								0x00	R
0x601	SPARE_READREG2	[7:0]	SPARE_READBITS2								0xFF	R
0x602	SPARE_READREG3	[7:0]	SPARE_READBITS3								0x00	R
0x603	SPARE_WRITEREG1	[7:0]	SPARE_WRITEBITS1								0x00	R/W
0x604	SPARE_WRITEREG2	[7:0]	SPARE_WRITEBITS2								0xFF	R/W
0x605	SPARE_WRITEREG3	[7:0]	SPARE_WRITEBITS3								0x00	R/W

REGISTER DETAILS

ANALOG DEVICES SPI STANDARD REGISTER

Address: 0x000, Reset: 0x00, Name: ADI_SPI_CONFIG

Table 8. Bit Descriptions for ADI_SPI_CONFIG

Bits	Bit Name	Description	Reset	Access
7	SOFTRESET_	Soft Reset. 0: reset asserted. 1: reset not asserted.	0x0	R/W
6	LSB_FIRST_	LSB First. 0: LSB first. 1: MSB first.	0x0	R/W
5	ENDIAN_	Endian. 0: Little Endian. 1: Big Endian.	0x0	R/W
4	SDOACTIVE_	SDO Active. 0: SDO inactive. 1: SDO active.	0x0	R/W
3	SDOACTIVE	SDO Active. 0: SDO inactive. 1: SDO active.	0x0	R/W
2	ENDIAN	Endian. 0: Little Endian. 1: Big Endian.	0x0	R/W
1	LSB_FIRST	LSB First. 0: LSB first. 1: MSB first.	0x0	R/W
0	SOFTRESET	Soft Reset. 0: reset asserted. 1: reset not asserted.	0x0	R/W

PRODUCT ID (LOWER 8 BITS OF THE 16 BITS) REGISTER

Address: 0x004, Reset: 0x4A, Name: PRODUCT_ID_L

Table 9. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID_L	PRODUCT_ID_L, Lower 8 Bits.	0x4A	R

PRODUCT ID (UPPER 8 BITS OF THE 16 BITS) REGISTER

Address: 0x005, Reset: 0x00, Name: PRODUCT_ID_H

Table 10. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID_H	PRODUCT_ID_H, Higher 8 Bits.	0x0	R

REGISTER DETAILS

REVISION NUMBER FOR ANALOG DEVICES SPI DEFINITION REGISTER

Address: 0x00B, Reset: 0x01, Name: SPI_REV

Table 11. Bit Descriptions for SPI_REV

Bits	Bit Name	Description	Reset	Access
[7:0]	SPI_REV	SPI Register Map Revision.	0x1	R

RF SIGNAL CHAIN ENABLES REGISTER

Address: 0x100, Reset: 0x3D, Name: RF_CKT_ENABLES

Table 12. Bit Descriptions for RF_CKT_ENABLES

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
6	ENABLE_RF_MIXER_BIAS	1: enable mixer subblock bias.	0x0	R/W
5	EN_RFAMP_Q	1: enable Q path RF amplifier	0x1	R/W
4	EN_RFAMP_I	1: enable I path RF amplifier	0x1	R/W
3	EN_LNA_Q	1: enable Q path LNA	0x1	R/W
2	EN_LNA_I	1: enable I path LNA	0x1	R/W
1	EN_LNA_1	1: enable LNA2.	0x0	R/W
0	EN_LNA_2	1: enable LNA1.	0x1	R/W

I PATH COMMON-MODE REGISTER

Address: 0x10A, Reset: 0x4A, Name: COMMON_MODE_I

Table 13. Bit Descriptions for COMMON_MODE_I

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x9	R/W
[2:0]	COMMON_MODE_I	I path DAC common-mode level.	0x2	R/W

Q PATH COMMON-MODE REGISTER

Address: 0x10B, Reset: 0x4A, Name: COMMON_MODE_Q

Table 14. Bit Descriptions for COMMON_MODE_Q

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x9	R/W
[2:0]	COMMON_MODE_Q	Q path DAC common-mode level.	0x2	R/W

LO SIGNAL CHAIN ENABLES REGISTER

Address: 0x120, Reset: 0xFF, Name: LO_CKT_ENABLES

Table 15. Bit Descriptions for LO_CKT_ENABLES

Bits	Bit Name	Description	Reset	Access
7	EN_MUXOUT	1: Enable MUXOUT pin for PLL test signals.	0x1	R/W
6	EN_SYNTH	1: enable synthesizer.	0x1	R/W
5	EN_VCO_QUADBUF	1: enable LO multiplier driver (quad buffer).	0x1	R/W
4	EN_LO_BUF_Q	1: enable LO Q path 20 GHz buffer.	0x1	R/W
3	EN_LO_BUF_I	1: enable LO I path 20 GHz buffer.	0x1	R/W
2	EN_LO_PPFDRIVER	1: enable LO Polyphase® filter driver.	0x1	R/W

REGISTER DETAILS

Table 15. Bit Descriptions for LO_CKT_ENABLES

Bits	Bit Name	Description	Reset	Access
1	EN_LO_MULT	1: enable LO multiplier.	0x1	R/W
0	EN_LO_DIVIDER	1: enable LO frequency divider.	0x1	R/W

LO PHASE ADJUST REGISTER

Address: 0x128, Reset: 0x00, Name: LO_PHASE_IMR

Table 16. Bit Descriptions for LO_PHASE_IMR

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:3]	LO_PHASE_Q	LO Q channel phase adjust.	0x0	R/W
[2:0]	LO_PHASE_I	LO I channel phase adjust.	0x0	R/W

CRYSTAL OSCILLATOR BITS REGISTER

Address: 0x129, Reset: 0x0F, Name: XTAL_OSC

Table 17. Bit Descriptions for XTAL_OSC

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:2]	RESERVED	Reserved	0x3	R/W
1	EN_XTAL_BUFMODE	1: enable reference buffer mode.	0x1	R/W
0	EN_XTAL_OSC	1: enable crystal oscillator.	0x1	R/W

BASEBAND I PATH CIRCUIT ENABLES REGISTER

Address: 0x130, Reset: 0xBF, Name: BB_CKT_ENABLES_I

Table 18. Bit Descriptions for BB_CKT_ENABLES_I

Bits	Bit Name	Description	Reset	Access
7	ENABLE_BBAMP3_I	1: enable baseband I path Amplifier 3.	0x1	R/W
6	EN_BB_DC_SWCH_I	1: enable baseband I path dc offset monitoring circuit.	0x0	R/W
5	ENABLE_BBAMP2_I	1: enable baseband I path Amplifier 2.	0x1	R/W
4	EN_BB_OFS_LOOP_I	1: enable I path offset correction.	0x1	R/W
3	EN_BB_OFS_OTRIM_I	1: enable I path offset currents.	0x1	R/W
2	ENABLE_BB_OFS_I	1: enable I path baseband offset loop op amp.	0x1	R/W
1	ENABLE_BB_FLT_I	1: enable baseband I path filter.	0x1	R/W
0	ENABLE_BBAMP1_I	1: enable baseband I path Amplifier 1.	0x1	R/W

BASEBAND Q PATH CIRCUIT ENABLES REGISTER

Address: 0x131, Reset: 0xBF, Name: BB_CKT_ENABLES_Q

Table 19. Bit Descriptions for BB_CKT_ENABLES_Q

Bits	Bit Name	Description	Reset	Access
7	ENABLE_BBAMP3_Q	1: enable baseband Q path Amplifier 3.	0x1	R/W
6	EN_BB_DC_SWCH_Q	1: enable baseband Q path dc offset monitoring circuit.	0x0	R/W
5	ENABLE_BBAMP2_Q	1: enable baseband Q path Amplifier 2.	0x1	R/W
4	EN_BB_OFS_LOOP_Q	1: enable Q path offset correction.	0x1	R/W
3	EN_BB_OFS_OTRIM_Q	1: enable Q path offset currents.	0x1	R/W

REGISTER DETAILS

Table 19. Bit Descriptions for BB_CKT_ENABLES_Q

Bits	Bit Name	Description	Reset	Access
2	ENABLE_BB_OFS_Q	1: enable Q path baseband offset loop op amp.	0x1	R/W
1	ENABLE_BB_FLT_Q	1: enable baseband Q path filter.	0x1	R/W
0	ENABLE_BBAMP1_Q	1: enable baseband Q path Amplifier 1.	0x1	R/W

BASEBAND COMMON BLOCKS ENABLES REGISTER

Address: 0x132, Reset: 0x01, Name: BB_CKT_ENABLES_COMMON

Table 20. Bit Descriptions for BB_CKT_ENABLES_COMMON

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	EN_BB_COMMON	1: enable shared bias blocks; attenuation controls and bias.	0x1	R/W

BASEBAND SELECT AMPLIFIER 1 IQ GAIN AND BIAS REGISTER

Address: 0x133, Reset: 0xEE, Name: BB_AMP1_SEL_IQ

Table 21. Bit Descriptions for BB_AMP1_SEL_IQ

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x3	R/W
[5:4]	BB_AMP1_GAIN_Q	Select baseband Q path Amplifier 1 gain mode.	0x2	R/W
[3:2]	RESERVED	Reserved.	0x3	R/W
[1:0]	BB_AMP1_GAIN_I	Select baseband I path Amplifier 1 gain mode.	0x2	R/W

BASEBAND SELECT AMPLIFIER 2 IQ GAIN AND BIAS REGISTER

Address: 0x134, Reset: 0xEE, Name: BB_AMP2_SEL_IQ

Table 22. Bit Descriptions for BB_AMP2_SEL_IQ

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x3	R/W
[5:4]	BB_AMP2_GAIN_Q	Select baseband Q path Amplifier 2 gain mode.	0x2	R/W
[3:2]	RESERVED	Reserved.	0x3	R/W
[1:0]	BB_AMP2_GAIN_I	Select baseband I path Amplifier 2 gain mode.	0x2	R/W

BASEBAND SELECT AMPLIFIER 3 IQ GAIN AND BIAS REGISTER

Address: 0x135, Reset: 0xEE, Name: BB_AMP3_SEL_IQ

Table 23. Bit Descriptions for BB_AMP3_SEL_IQ

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x3	R/W
[5:4]	BB_AMP3_GAIN_Q	Select baseband Q path Amplifier 3 gain mode.	0x2	R/W
[3:2]	RESERVED	Reserved.	0x3	R/W
[1:0]	BB_AMP3_GAIN_I	Select baseband I path Amplifier 3 gain mode.	0x2	R/W

REGISTER DETAILS

BASEBAND IQ FILTERS BANDWIDTH SELECT REGISTER

Address: 0x13C, Reset: 0x0A, Name: BB_FLT_SEL_IQ

Table 24. Bit Descriptions for BB_FLT_SEL_IQ

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:2]	SEL_BB_FLT_FC_Q	Select baseband Q path filter bandwidth. 00: 125 MHz. 01: 250 MHz. 10: 500 MHz. 11: bypass.	0x2	R/W
[1:0]	SEL_BB_FLT_FC_I	Select baseband I path filter bandwidth. 00: 125 MHz. 01: 250 MHz. 10: 500 MHz. 11: bypass.	0x2	R/W

BASEBAND DIGITAL STEP ATTENUATION SETTING REGISTER

Address: 0x140, Reset: 0x77, Name: BB_DSA_IQ

Table 25. Bit Descriptions for BB_DSA_IQ

Bits	Bit Name	Description	Reset	Access
[7:4]	SEL_BB_ATT_Q	Select baseband Q path attenuator setting.	0x7	R/W
[3:0]	SEL_BB_ATT_I	Select baseband I path attenuator setting.	0x7	R/W

N DIVIDER INT LSB AND TRIGGER REGISTER

Address: 0x200, Reset: 0x89, Name: INT_L

Table 26. Bit Descriptions for INT_L

Bits	Bit Name	Description	Reset	Access
[7:0]	INT_DIV[7:0]	Integer-N Word—Double Buffered. Writing the LSB of the integer word normally causes an autocalibration event.	0x89	R/W

N DIVIDER INT MSB REGISTER

Address: 0x201, Reset: 0x01, Name: INT_H

Table 27. Bit Descriptions for INT_H

Bits	Bit Name	Description	Reset	Access
[7:0]	INT_DIV[15:8]	Integer-N Word—Double Buffered. Writing the LSB of the integer word normally causes an autocalibration event.	0x1	R/W

N DIVIDER FRAC1 LSB REGISTER

Address: 0x202, Reset: 0x00, Name: FRAC1_L

Table 28. Bit Descriptions for FRAC1_L

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC1[7:0]	Fractional-N Word—Double Buffered. Lower 8 bits of the 24-bit FRAC1 value.	0x0	R/W

REGISTER DETAILS

N DIVIDER FRAC1 MIDDLE REGISTER

Address: 0x203, Reset: 0x00, Name: FRAC1_M

Table 29. Bit Descriptions for FRAC1_M

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC1[15:8]	Fractional-N Word—Double Buffered. The middle 8 bits of the 24-bit FRAC1 value.	0x0	R/W

N DIVIDER FRAC1 MSB REGISTER

Address: 0x204, Reset: 0x00, Name: FRAC1_H

Table 30. Bit Descriptions for FRAC1_H

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC1[23:16]	FractionI-N Word—Double Buffered. The upper 8 bits of the 24-bit FRAC1 value.	0x0	R/W

AUXILIARY FRACTIONAL MODULUS LSB WHEN USING THE EXACT FREQUENCY MODE REGISTER

Address: 0x208, Reset: 0x00, Name: MOD_L

Table 31. Bit Descriptions for MOD_L

Bits	Bit Name	Description	Reset	Access
[7:0]	MOD2[7:0]	14-Bit Auxiliary Fractional Modulus. Recommended setting is 3.	0x0	R/W

AUXILIARY FRACTIONAL MODULUS MSB WHEN USING THE EXACT FREQUENCY MODE REGISTER

Address: 0x209, Reset: 0x00, Name: MOD_H

Table 32. Bit Descriptions for MOD_H

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	MOD2[13:8]	14-Bit Auxiliary Fractional Modulus. Recommended setting is 3.	0x0	R/W

N DIVIDER ENABLE AND MODE SELECT REGISTER

Address: 0x20B, Reset: 0x01, Name: SYNTH

Table 33. Bit Descriptions for SYNTH

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
1	PRE_SEL	Prescaler Select. 0: disable 2× prescalar. 1: enable 2× prescalar.	0x0	R/W
0	EN_FBDIV	Enable Feedback Divider.	0x1	R/W

R DIVIDER SETPOINT REGISTER

Address: 0x20C, Reset: 0x03, Name: R_DIV

Table 34. Bit Descriptions for R_DIV

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R

REGISTER DETAILS

Table 34. Bit Descriptions for R_DIV

Bits	Bit Name	Description	Reset	Access
[4:0]	R_DIV	R Divider Word. The 5-bit reference R divider word.	0x3	R/W

R DIVIDER CONTROLS REGISTER

Address: 0x20E, Reset: 0x04, Name: SYNTH_0

Table 35. Bit Descriptions for SYNTH_0

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	DOUBLER_EN	Reference Doubler enable - double-buffered.	0x0	R/W
2	RESERVED	Reserved.	0x1	R/W
1	RESERVED	Reserved.	0x0	R
0	RDIV2_SEL	Reference Divide by 2. Double buffered. 0: reference divide by 2 disabled. 1: reference divide by 2 enabled.	0x0	R/W

LOCK DETECT CONFIGURATION REGISTER

Address: 0x214, Reset: 0x48, Name: MULTI_FUNC_SYNTH_CTRL_0214

Table 36. Bit Descriptions for MULTI_FUNC_SYNTH_CTRL_0214

Bits	Bit Name	Description	Reset	Access
[7:6]	LD_BIAS	Lock Detect Bias. 00: 40 µA. 01: 30 µA. 10: 20 µA. 11: 10 µA.	0x1	R/W
[5:3]	LDP	Lock Detect Precision. 000: check 1024 consecutive PFD cycles for lock. 001: check 2048 consecutive PFD cycles. 010: check 4096 consecutive PFD cycles. 011: check 8192 consecutive PFD cycles.	0x1	R/W
[2:0]	RESERVED	Reserved.	0x0	R/W

SPI OVERRIDE VALUE FOR VCO BAND REGISTER

Address: 0x215, Reset: 0x00, Name: SI_BAND_0

Table 37. Bit Descriptions for SI_BAND_0

Bits	Bit Name	Description	Reset	Access
[7:0]	SI_VCO_BAND	Sets the VCO band if FORCE_VCO_BAND == 1.	0x0	R/W

SPI OVERRIDE VALUE FOR VCO SELECT REGISTER

Address: 0x217, Reset: 0x00, Name: SI_VCO_CORE

Table 38. Bit Descriptions for SI_VCO_CORE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	SI_VCO_CORE	Sets the VCO core if FORCE_VCO_CORE == 1.	0x0	R/W

REGISTER DETAILS

SYNTH_LOCK_TIMEOUT

Address: 0x218, Reset: 0x1F, Name: SYNTH_LOCK_TIMEOUT

Table 39. Bit Descriptions for SYNTH_LOCK_TIMEOUT

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:0]	SYNTH_LOCK_TIMEOUT	Synthesizer Lock Timeout. Recommended values for the SYNTH_LOCK_TIMEOUT are approximately 30 µs.	0x1F	R/W

VCO CALIBRATION TIMEOUT LSB REGISTER

Address: 0x21C, Reset: 0x20, Name: VCO_TIMEOUT_L

Table 40. Bit Descriptions for VCO_TIMEOUT_L

Bits	Bit Name	Description	Reset	Access
[7:0]	VCO_TIMEOUT[7:0]	Main VCO Calibration Timeout.	0x20	R/W

VCO CALIBRATION TIMEOUT MSB REGISTER

Address: 0x21D, Reset: 0x00, Name: VCO_TIMEOUT_H

Table 41. Bit Descriptions for VCO_TIMEOUT_H

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	VCO_TIMEOUT[9:8]	Main VCO Calibration Timeout.	0x0	R/W

AUTOMATIC FREQUENCY CALIBRATION (AFC) MEASUREMENT RESOLUTION REGISTER

Address: 0x21E, Reset: 0x14, Name: VCO_BAND_DIV

Table 42. Bit Descriptions for VCO_BAND_DIV

Bits	Bit Name	Description	Reset	Access
[7:0]	VCO_BAND_DIV	Value sets how long a single AFC measurement cycle lasts. The AFC measurement lasts 16 × VCO_BAND_DIV. It is required that users program this value, depending on the PFD rate of the user, to represent approximately 10 µs. A longer value than necessary leads to longer automatic calibration times, and shorter values may risk autocalibration accuracy due to insufficient frequency measurement resolution.	0x14	R/W

ALC_SELECT REGISTER

Address: 0x21F, Reset: 0x80, Name: ALC_SELECT

Table 43. Bit Descriptions for ALC_SELECT

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x1	R/W
6	DISABLE_CAL	Disable VCO calibration.	0x0	R/W
[5:0]	RESERVED	Reserved	0x0	R/W

MISCELLANEOUS CONTROL REGISTER 1

Address: 0x22A, Reset: 0x02, Name: SD_CTRL

Table 44. Bit Descriptions for SD_CTRL

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R/W
5	SD_EN_FRAC0	Σ-Δ Enabled with FRAC = 0.	0x0	R/W

REGISTER DETAILS

Table 44. Bit Descriptions for SD_CTRL

Bits	Bit Name	Description	Reset	Access
4	SD_EN_OUT_OFF	Σ-Δ Enabled, Output Off.	0x0	R/W
[3:0]	RESERVED	Reserved.	0x2	R

MISCELLANEOUS CONTROL REGISTER 2

Address: 0x22B, Reset: 0x09, Name: MULTI_FUNC_SYNTH_CTRL_022B

Table 45. Bit Descriptions for MULTI_FUNC_SYNTH_CTRL_022B

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x2	R
[1:0]	RF_PBS	Prescaler Bias Option.	0x1	R/W

CHARGE PUMP HIGH-Z REGISTER

Address: 0x22C, Reset: 0x03, Name: MULTI_FUNC_SYNTH_CTRL_022C

Table 46. Bit Descriptions for MULTI_FUNC_SYNTH_CTRL_022C

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
[1:0]	CP_HIZ	Charge Pump Tristate. 0: Charge Pump Tristate Mode 0. 1: Charge Pump Tristate Mode 1. 2: Charge Pump Tristate Mode 2. 3: Charge Pump Tristate Mode 3.	0x3	R/W

CHARGE PUMP CONTROL REGISTER

Address: 0x22D, Reset: 0x81, Name: MULTI_FUNC_SYNTH_CTRL_022D

Table 47. Bit Descriptions for MULTI_FUNC_SYNTH_CTRL_022D

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x2	R/W
5	SEL_PFD_POLARITY	Selects the PFD Polarity.	0x0	R/W
[4:1]	RESERVED	Reserved.	0x0	R
0	BLEED_EN	Bleed Enable.	0x1	R/W

CHARGE PUMP CURRENT REGISTER

Address: 0x22E, Reset: 0x0F, Name: CP_CURR

Table 48. Bit Descriptions for CP_CURR

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CP_CURRENT	Main Charge Pump Current.	0xF	R/W

CHARGE PUMP BLEED CURRENT REGISTER

Address: 0x22F, Reset: 0x08, Name: BICP

Table 49. Bit Descriptions for BICP

Bits	Bit Name	Description	Reset	Access
[7:0]	BICP	Binary Scaled Bleed Current.	0x8	R/W

REGISTER DETAILS

FRAC2 LSB REGISTER

Address: 0x233, Reset: 0x00, Name: FRAC2_L

Table 50. Bit Descriptions for FRAC2_L

Bits	Bit Name	Description	Reset	Access
[7:0]	FRAC2[7:0]	Frac2 Word for Exact Frequency Mode—Double Buffered.	0x0	R/W

FRAC2 MSB REGISTER

Address: 0x234, Reset: 0x00, Name: FRAC2_H

Table 51. Bit Descriptions for FRAC2_H

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	FRAC2[13:8]	Frac2 Word for Exact Frequency Mode—Double Buffered.	0x0	R/W

VCO AND BAND SELECTION ADJUSTMENT REGISTER

Address: 0x240, Reset: 0x00, Name: VCO_FORCE

Table 52. Bit Descriptions for VCO_FORCE

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
1	FORCE_VCO_CORE	Override VCO core calibration.	0x0	R/W
0	FORCE_VCO_BAND	Override VCO band calibration.	0x0	R/W

VCO CALIBRATION FSM REGISTER

Address: 0x248, Reset: 0x00, Name: VCO_FSM_CAPS_RB

Table 53. Bit Descriptions for VCO_FSM_CAPS_RB

Bits	Bit Name	Description	Reset	Access
[7:1]	SI_VCO_FSM_CAPS_RB	Use the SI_VCO_FSM_CAPS_RB bits to read back the VCO calibration band as outlined in VCO Calibration Band Read Back	0x0	R
0	RESERVED	Reserved	0x0	R

LOCK DETECT READBACK REGISTER

Address: 0x24D, Reset: 0x00, Name: LOCK_DETECT

Table 54. Bit Descriptions for LOCK_DETECT

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	LOCK_DETECT	State of the Lock Detect Signal.	0x0	R

REGISTER DETAILS

MUXOUT

Address: 0x24E, Reset: 0x00, Name: MUXOUT

Table 55. Bit Descriptions for MUXOUT

Bits	Bit Name	Description	Reset	Access
[7:0]	MUX_SEL	Selection of Which Signal to Output from the MUXOUT Pin. 0 = Logic 0. 1 = lock detect. 2 = up. 3 = down. 4 = RDIV/2. 5 = NDIV/2. 8 = Logic 1.	0x0	R/W

PLL MUXOUT LEVEL CONTROL REGISTER

Address: 0x300, Reset: 0x01, Name: PLLMUXOUT_CONTROL

Table 56. Bit Descriptions for PLLMUXOUT_CONTROL

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	SEL_MUXOUT_LEVEL	1: 3.3 V. 0: 1.8 V.	0x1	R/W

AGPIO MUX AND PIN CONTROL REGISTER

Address: 0x301, Reset: 0x00, Name: AGPIO_CONTROL

Table 57. Bit Descriptions for AGPIO_CONTROL

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	SEL_AGPIO	Select AGPIO. 0: AMUX to AGPIO output.	0x0	R/W
		1: AGPIO input to ADC.		
[2:0]	SEL_AMUX	Select AMUX Input to ADC (Must also Assert SEL_AGPIO). 6: temperature sensor. 7: AGPIO input.	0x0	R/W

ADC CONTROL BITS REGISTER

Address: 0x302, Reset: 0xCA, Name: ADC_CONTROL

Table 58. Bit Descriptions for ADC_CONTROL

Bits	Bit Name	Description	Reset	Access
[7:4]	SEL_ADC_CLKDIV	ADC Clock = REFCLK/(2 × SEL_ADC_CLKDIV).	0xC	R/W
3	ADC_LOG_SEL	Select ADC Log Scale. 0: not scaled. 1: ADC output log scaled.	0x1	R/W
2	ADC_HALF_SEL	Select ADC. 0: 1× input to ADC. 1: divide by 2 input to ADC.	0x0	R/W

REGISTER DETAILS

Table 58. Bit Descriptions for ADC_CONTROL

Bits	Bit Name	Description	Reset	Access
1	ADC_START	Transition. Toggling the ADC_START from 0 to 1 starts ADC conversion.	0x1	R/W
0	ENABLE_ADC	Enable or Disable the ADC. 0: ADC disabled. 1: ADC enabled.	0x0	R/W

ADC STATUS BITS REGISTER

Address: 0x303, Reset: 0x00, Name: ADC_STATUS

Table 59. Bit Descriptions for ADC_STATUS

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
2	ADC_LATCHDATA	ADC Latch Data. 1: indicates that the ADC data is ready to be read from SPI.	0x0	R
1	ADC_BUSY	ADC Busy Indicator. 1: indicates that the ADC is busy.	0x0	R
0	ADC_EOC	ADC End of Conversion. 1: indicates that the ADC conversion is complete.	0x0	R

ADC RESULT REGISTER

Address: 0x304, Reset: 0x00, Name: ADC_DATA

Table 60. Bit Descriptions for ADC_DATA

Bits	Bit Name	Description	Reset	Access
[7:0]	ADC_DATA	ADC Output Data (8 Bits).	0x0	R

GPIOX WRITE REGISTER

Address: 0x305, Reset: 0x00, Name: GPIO_WRITEVALS

Table 61. Bit Descriptions for GPIO_WRITEVALS

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:1]	GPIO_WRITEVALS	Values for Writing Out to the GPIOx Pins.	0x0	R/W
0	RESERVED	Reserved.	0x0	R

GPIO READ REGISTER

Address: 0x306, Reset: 0x00, Name: GPIO_READVALS

Table 62. Bit Descriptions for GPIO_READVALS

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved.	0x0	R
[2:1]	GPIO_READVALS	Values Read from GPIOx Pins.	0x0	R
0	RESERVED	Reserved.	0x0	R

REGISTER DETAILS

CONTROL OF GPIOX PINS

Address: 0x307, Reset: 0x00, Name: GPIO_CONTROL

Table 63. Bit Descriptions for GPIO_CONTROL

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:4]	EN_GPIO_OUT	Enable GPIO as an Input or an Output. 0: GPIO is input. 1: GPIO is output.	0x0	R/W
3	RESERVED	Reserved.	0x0	R
[2:1]	SEL_GPIO_LEVELS	GPIO Output Voltage Levels. 0: 3.3 V. 1: 1.8 V.	0x0	R/W
0	RESERVED	Reserved.	0x0	R

SPARE READ REGISTER 1

Address: 0x600, Reset: 0x00, Name: SPARE_READREG1

Table 64. Bit Descriptions for SPARE_READREG1

Bits	Bit Name	Description	Reset	Access
[7:0]	SPARE_READBITS1	Spare Read Register (8 Bits).	0x0	R

SPARE READ REGISTER 2

Address: 0x601, Reset: 0xFF, Name: SPARE_READREG2

Table 65. Bit Descriptions for SPARE_READREG2

Bits	Bit Name	Description	Reset	Access
[7:0]	SPARE_READBITS2	Spare Read Register (8 Bits).	0xFF	R

SPARE READ REGISTER 3

Address: 0x602, Reset: 0x00, Name: SPARE_READREG3

Table 66. Bit Descriptions for SPARE_READREG3

Bits	Bit Name	Description	Reset	Access
[7:0]	SPARE_READBITS3	Spare Read Register (8 Bits).	0x0	R

SPARE WRITE REGISTER 1

Address: 0x603, Reset: 0x00, Name: SPARE_WRITEREG1

Table 67. Bit Descriptions for SPARE_WRITEREG1

Bits	Bit Name	Description	Reset	Access
[7:0]	SPARE_WRITEBITS1	Spare Write Register (8 Bits).	0x0	R/W

SPARE WRITE REGISTER 2

Address: 0x604, Reset: 0xFF, Name: SPARE_WRITEREG2

Table 68. Bit Descriptions for SPARE_WRITEREG2

Bits	Bit Name	Description	Reset	Access
[7:0]	SPARE_WRITEBITS2	Spare Write Register (8 Bits).	0xFF	R/W

REGISTER DETAILS

SPARE WRITE REGISTER 3

Address: 0x605, Reset: 0x00, Name: SPARE_WRITEREG3

Table 69. Bit Descriptions for SPARE_WRITEREG3

Bits	Bit Name	Description	Reset	Access
[7:0]	SPARE_WRITEBITS3	Spare Write Register (8 Bits).	0x0	R/W

OUTLINE DIMENSIONS

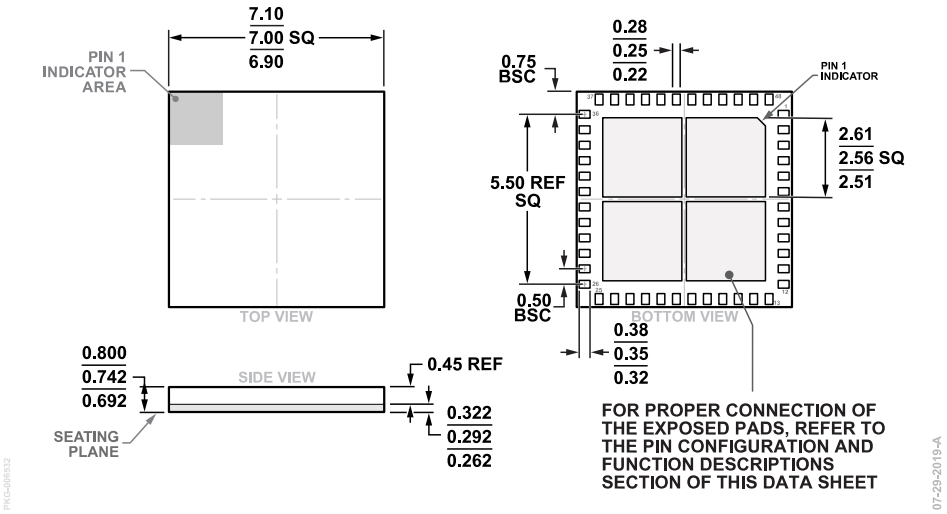

Figure 89. 48-Terminal Land Grid Array [LGA]
(CC-48-5)
Dimensions Shown in Millimeters

Updated: October 21, 2021

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADMV4540ACCZ	–40°C to +85°C	48-Terminal Land Grid Array [LGA]	Reel, 0	CC-48-5
ADMV4540ACCZ-RL7	–40°C to +85°C	48-Terminal Land Grid Array [LGA]	Reel, 750	CC-48-5

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model	Description
ADMV4540-EVALZ	Evaluation Board

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

ADMV4540ACCZ ADMV4540ACCZ-RL7