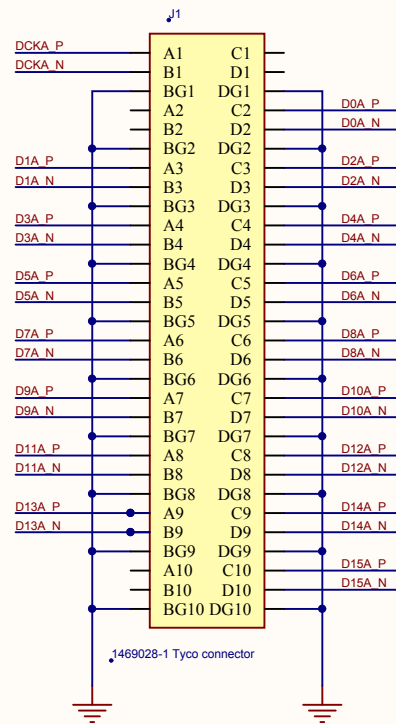


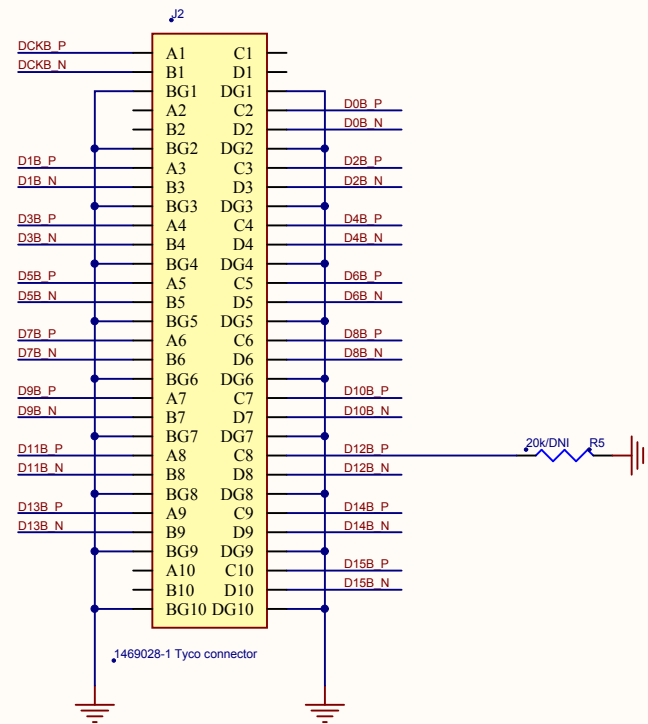
R15	IO_L10N_2
R16	IO_L10P_2
W17	IO_L11N_2
V17	IO_L11P_2
U13	IO_L12N_D2_MISO3_2
U14	IO_L12P_D1_MISO2_2
V15	IO_L13N_D10_2
U15	IO_L13P_M1_2
AB18	IO_L14N_D12_2
AA18	IO_L14P_D11_2
AB17	IO_L15N_2
Y17	IO_L15P_2
AB14	IO_L16N_VREF_2
AA14	IO_L16P_2
W15	IO_L17N_2
Y16	IO_L17P_2
W13	IO_L18N_2
V13	IO_L18P_2
AB16	IO_L19N_2
AA16	IO_L19P_2
AA22	IO_L1N_M0_CMPMISO_2
Y14	IO_L20N_2
W14	IO_L20P_2
AB15	IO_L21N_2
Y15	IO_L21P_2
U12	IO_L22N_2
T12	IO_L22P_2
R13	IO_L23N_2
T14	IO_L23P_2
Y12	IO_L29N_GCLK2_2
W12	IO_L29P_GCLK3_2
AB21	IO_L2N_CMPMOSI_2
AA21	IO_L2P_CMPCLK_2
AB13	IO_L30N_GCLK0_USERCCLK_2
Y13	IO_L30P_GCLK1_D13_2
AB12	IO_L31N_GCLK30_D15_2
AA12	IO_L31P_GCLK31_D14_2
AB11	IO_L32N_GCLK28_2
Y11	IO_L32P_GCLK29_2
AB20	IO_L3N_MOSI_CSI_B_MISO0_2
T11	IO_L40N_2
R11	IO_L40P_2
AB10	IO_L41N_VREF_2
AA10	IO_L41P_2
W11	IO_L42N_2
V11	IO_L42P_2
AB9	IO_L43N_2
Y9	IO_L43P_2
Y10	IO_L44N_2
W10	IO_L44P_2
AB8	IO_L45N_2
AA8	IO_L45P_2
V7	IO_L46N_2
W8	IO_L46P_2
Y8	IO_L47N_2
W9	IO_L47P_2
AB7	IO_L48N_RDWR_B_VREF_2
Y7	IO_L48P_D7_2
AB6	IO_L49N_D4_2
AA6	IO_L49P_D3_2
T17	IO_L4N_VREF_2
T18	IO_L4P_2
V9	IO_L50N_2
U9	IO_L50P_2
U8	IO_L51N_2
T8	IO_L51P_2
U10	IO_L52N_2
T10	IO_L52P_2
Y6	IO_L53N_2
W6	IO_L53P_2
AB5	IO_L54N_2
Y5	IO_L54P_2
AB4	IO_L55N_2
AA4	IO_L55P_2
AA3	IO_L57P_2
AB3	IO_L58N_2
Y3	IO_L58P_2
R8	IO_L59N_2
R9	IO_L59P_2
AB19	IO_L5N_2
Y19	IO_L5P_2
R7	IO_L5P_2
T7	IO_L60N_2
T7	IO_L60P_2
Y4	IO_L62N_D6_2
W4	IO_L62P_D5_2
V5	IO_L63N_2
U6	IO_L63P_2
AB2	IO_L64N_D9_2
AA2	IO_L64P_D8_2
T5	IO_L65N_CSO_B_2
Y18	IO_L6N_2
W18	IO_L6P_2
T15	IO_L7N_2
T16	IO_L7P_2
U16	IO_L8N_2
U17	IO_L8P_2
V18	IO_L9N_2
V19	IO_L9P_2
Y20	CMPCS_B_2

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INPUT A CONNECTOR
NOTE: DIFFERENTIAL PAIRS ROUTED AT 1% LENGTH, 100-OHM DIFFERENTIAL



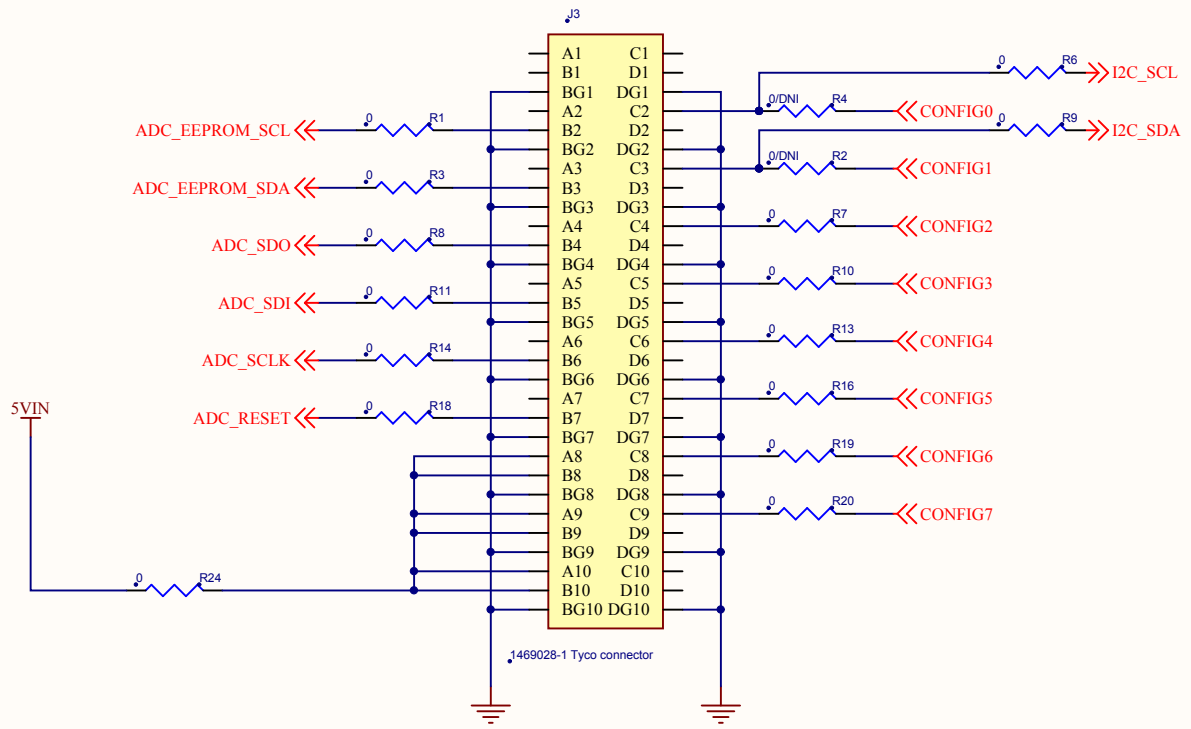
INPUT B CONNECTOR
NOTE: DIFFERENTIAL PAIRS ROUTED AT 1% LENGTH, 100-OHM DIFFERENTIAL



NOTE: D8A_P AND D8A_N ARE EXPECTED TO BE USED FOR LVDS OVERRRANGE SIGNAL

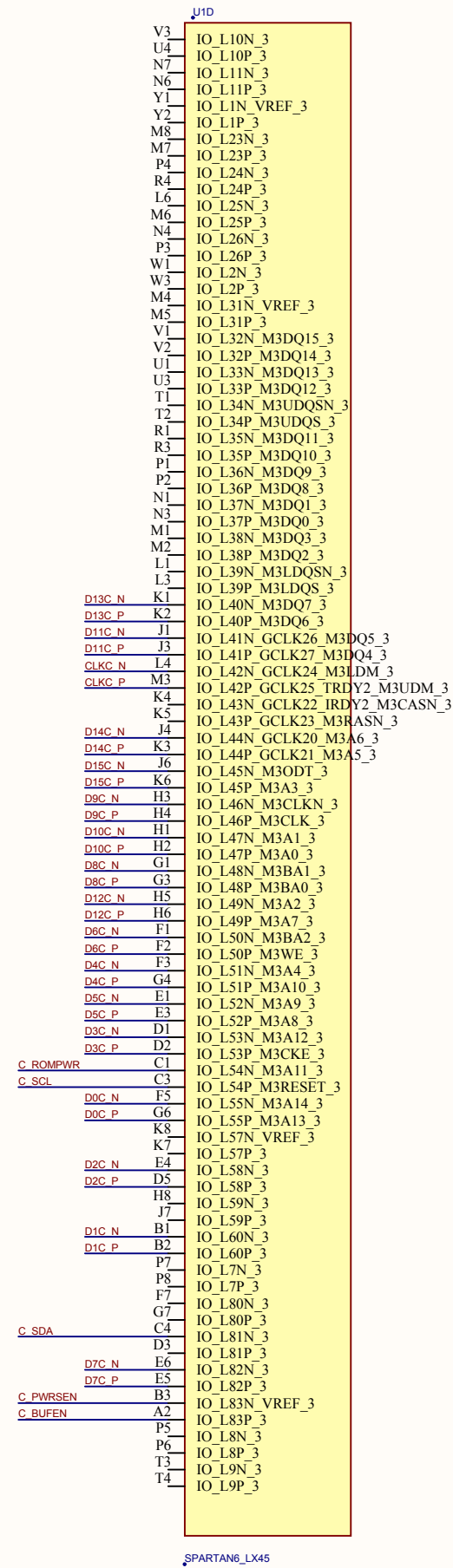
NOTE: CONFIG[0:15] IS RESERVED FOR FUTURE USE, ROUTED SINGLE-ENDED

CONFIGURATION CONNECTOR



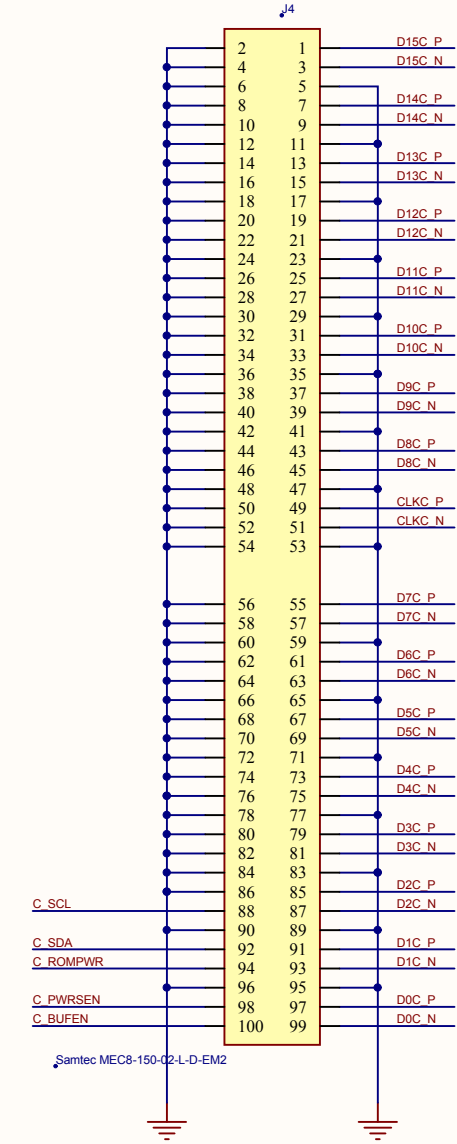
NOTE: CONFIG INTERFACE PIN A1 SHOULD BE 38mm FROM INPUT A PIN A1 WHICH SHOULD BE 32mm FROM INPUT B PIN A1. (CENTER OF PINS)

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NOTE: DIFFERENTIAL PAIRS ROUTED AT 14 LENGTH, 100-OHM DIFFERENTIAL

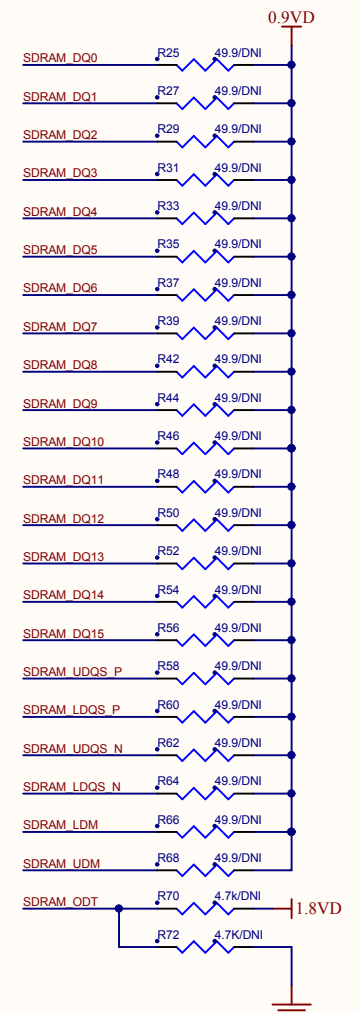
INPUT C CONNECTOR



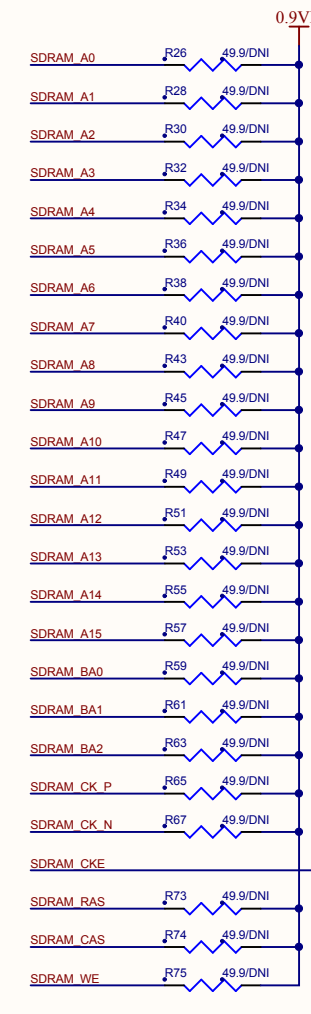
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SDRAM Pin	FPGA Pin	FPGA Pin Name
SDRAM DQ0	N20	IO_M1DQ0_1
SDRAM DQ1	N22	IO_M1DQ1_1
SDRAM DQ2	M21	IO_M1DQ2_1
SDRAM DQ3	M22	IO_M1DQ3_1
SDRAM DQ4	J20	IO_M1DQ4_1
SDRAM DQ5	J22	IO_M1DQ5_1
SDRAM DQ6	K21	IO_M1DQ6_1
SDRAM DQ7	K22	IO_M1DQ7_1
SDRAM DQ8	P21	IO_M1DQ8_1
SDRAM DQ9	P22	IO_M1DQ9_1
SDRAM DQ10	R20	IO_M1DQ10_1
SDRAM DQ11	R22	IO_M1DQ11_1
SDRAM DQ12	U20	IO_M1DQ12_1
SDRAM DQ13	U22	IO_M1DQ13_1
SDRAM DQ14	V21	IO_M1DQ14_1
SDRAM DQ15	V22	IO_M1DQ15_1
SDRAM A0	F21	IO_M1A0_1
SDRAM A1	F22	IO_M1A1_1
SDRAM A2	E22	IO_M1A2_1
SDRAM A3	G20	IO_M1A3_1
SDRAM A4	F20	IO_M1A4_1
SDRAM A5	K20	IO_M1A5_1
SDRAM A6	K19	IO_M1A6_1
SDRAM A7	E20	IO_M1A7_1
SDRAM A8	C20	IO_M1A8_1
SDRAM A9	C22	IO_M1A9_1
SDRAM A10	G19	IO_M1A10_1
SDRAM A11	F19	IO_M1A11_1
SDRAM A12	D22	IO_M1A12_1
SDRAM A13	D19	IO_M1A13_1
SDRAM A14	D20	IO_M1A14_1
SDRAM BA0	J17	IO_M1BA0_1
SDRAM BA1	K17	IO_M1BA1_1
SDRAM BA2	H18	IO_M1BA2_1
SDRAM CK P	J19	IO_M1CKLN_1
SDRAM CK N	H20	IO_M1CKLN_1
SDRAM ODT	G22	IO_M1ODT_1
SDRAM CAS	H22	IO_M1CASN_1
SDRAM RAS	H21	IO_M1IRASN_1
SDRAM LDM	L19	IO_M1LDM_1
SDRAM UDM	M20	IO_M1UDM_1
SDRAM LDQS P	L20	IO_M1LDQS_1
SDRAM LDQS N	L22	IO_M1LDQSN_1
SDRAM UDQS P	T21	IO_M1UDQS_1
SDRAM UDQS N	T22	IO_M1UDQSN_1
SDRAM WE	H19	IO_M1WE_1
SDRAM CKE	D21	IO_M1WE_1
	F18	IO_M1CKE_1
	F17	IO_M1RESET_1
	F16	IO_L10N_1
	B22	IO_L10P_1
	B21	IO_L19N_1
	C19	IO_L19P_1
	A21	IO_L1P_A25_1
	A20	IO_L20N_1
	J16	IO_L20P_1
	K16	IO_L21N_1
	H16	IO_L21P_1
	M19	IO_L28P_1
	L15	IO_L53P_1
	M16	IO_L58N_1
	P20	IO_L58P_1
	P19	IO_L59N_1
	W22	IO_L59P_1
	W20	IO_L60N_1
	K18	IO_L60P_1
	L17	IO_L61N_1
	V20	IO_L61P_1
	U19	IO_L70N_1
	M18	IO_L70P_1
	M17	IO_L71N_1
	N16	IO_L71P_1
	P17	IO_L72N_1
	R19	IO_L72P_1
	P18	IO_L73N_1
	T20	IO_L73P_1
	T19	IO_L74N_DOUT_BUSY_1
	G17	IO_L74P_AWAKE_1
	G16	IO_L9N_1
	B20	IO_L9P_1
	H17	IO_L1N_A24_VREF_1
	N19	IO_L28N_VREF_1
		IO_L53N_VREF_1

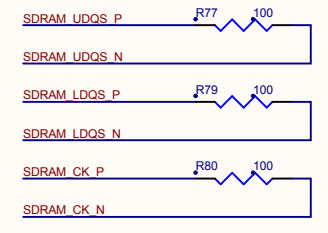
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NOTE: PLACE TERMINATION AT LOAD



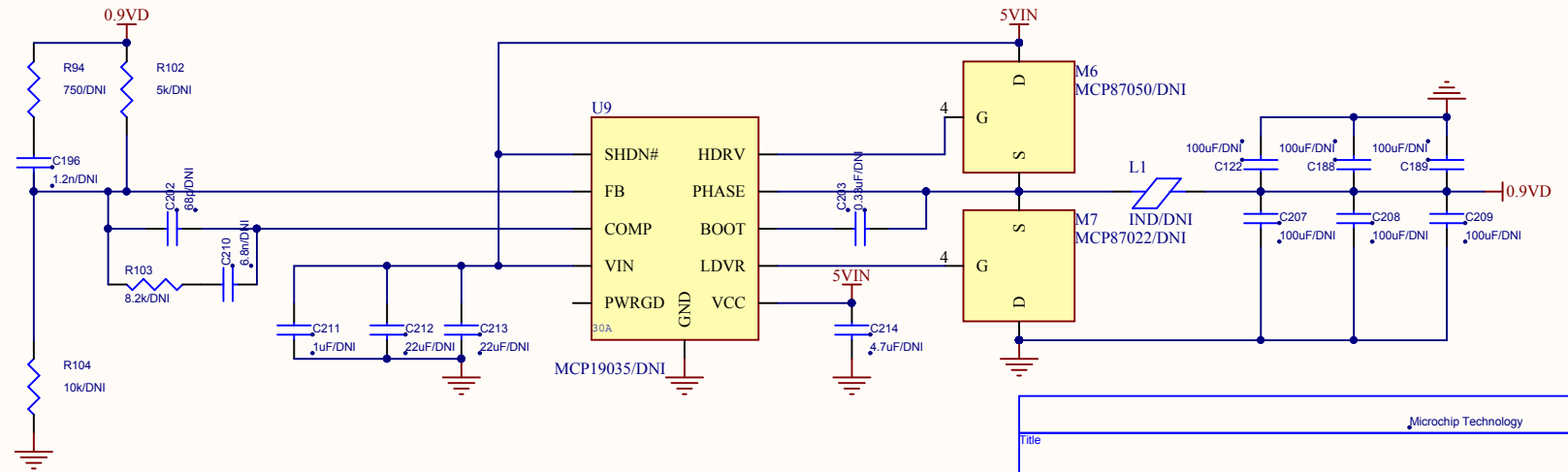
NOTE: PLACE TERMINATION AT LOAD

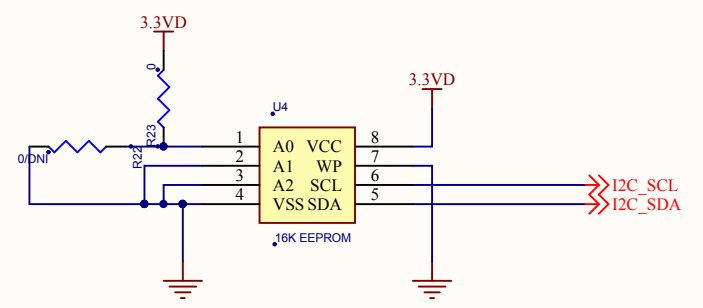
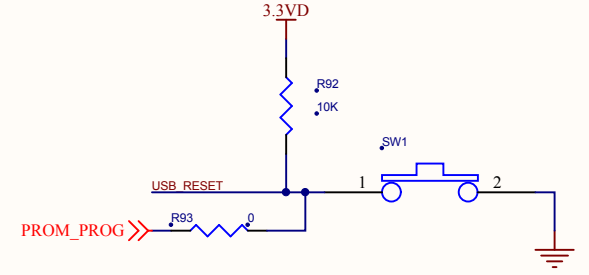
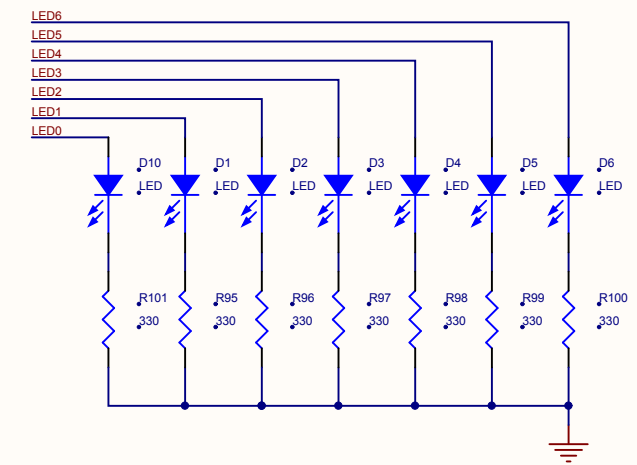
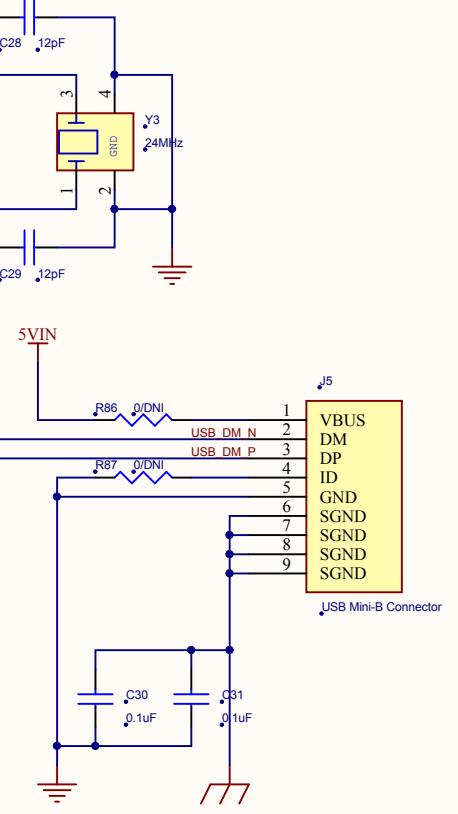
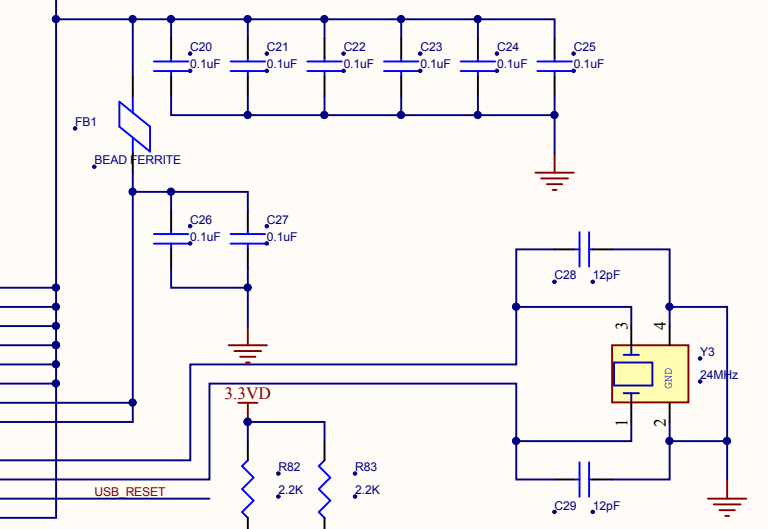
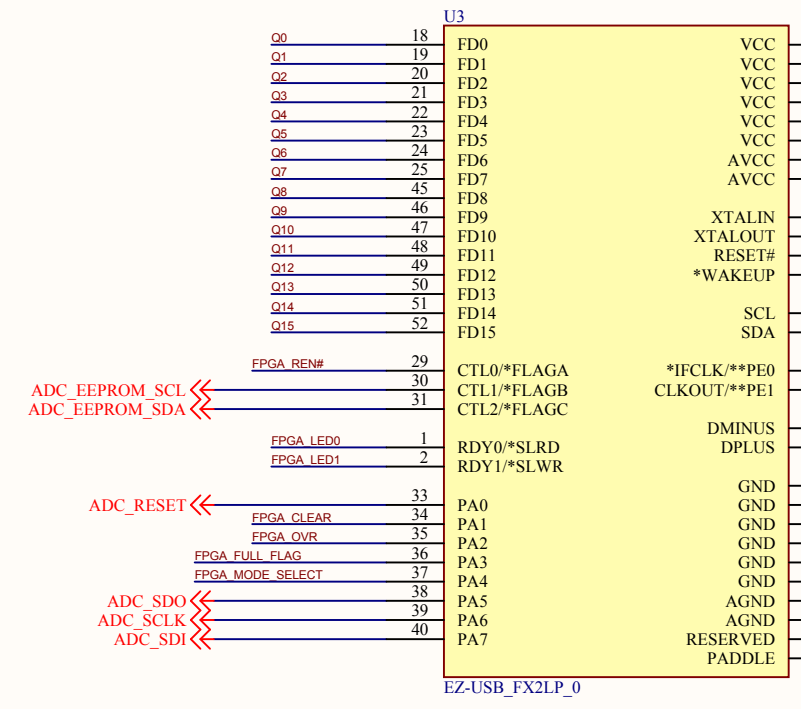
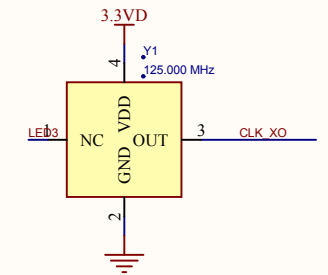
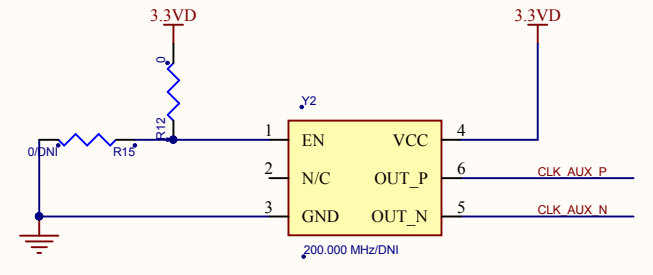
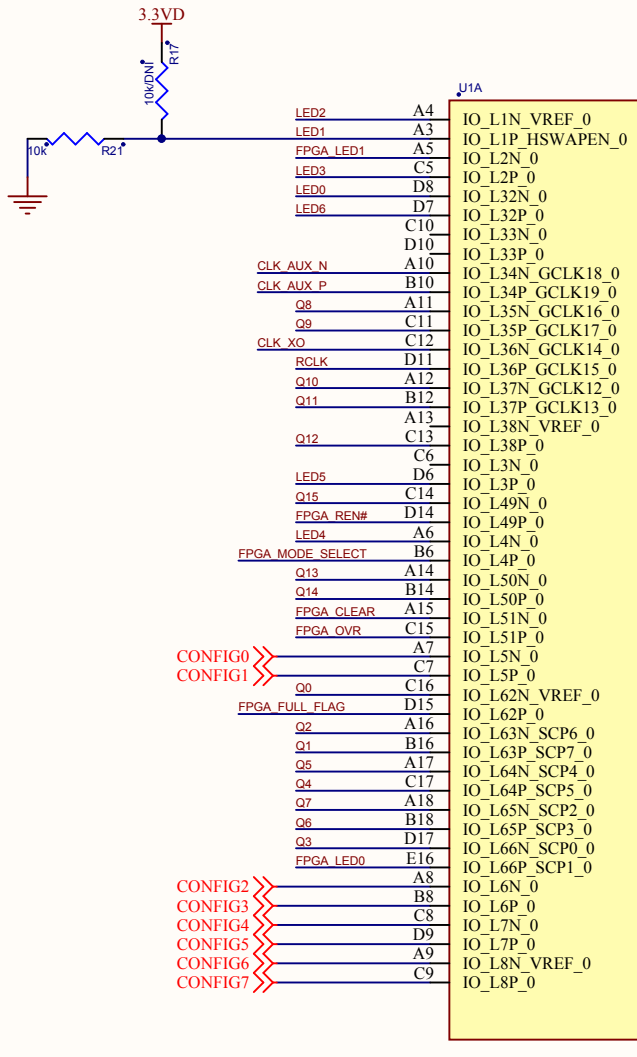


NOTE: PLACE TERMINATION AT LOAD

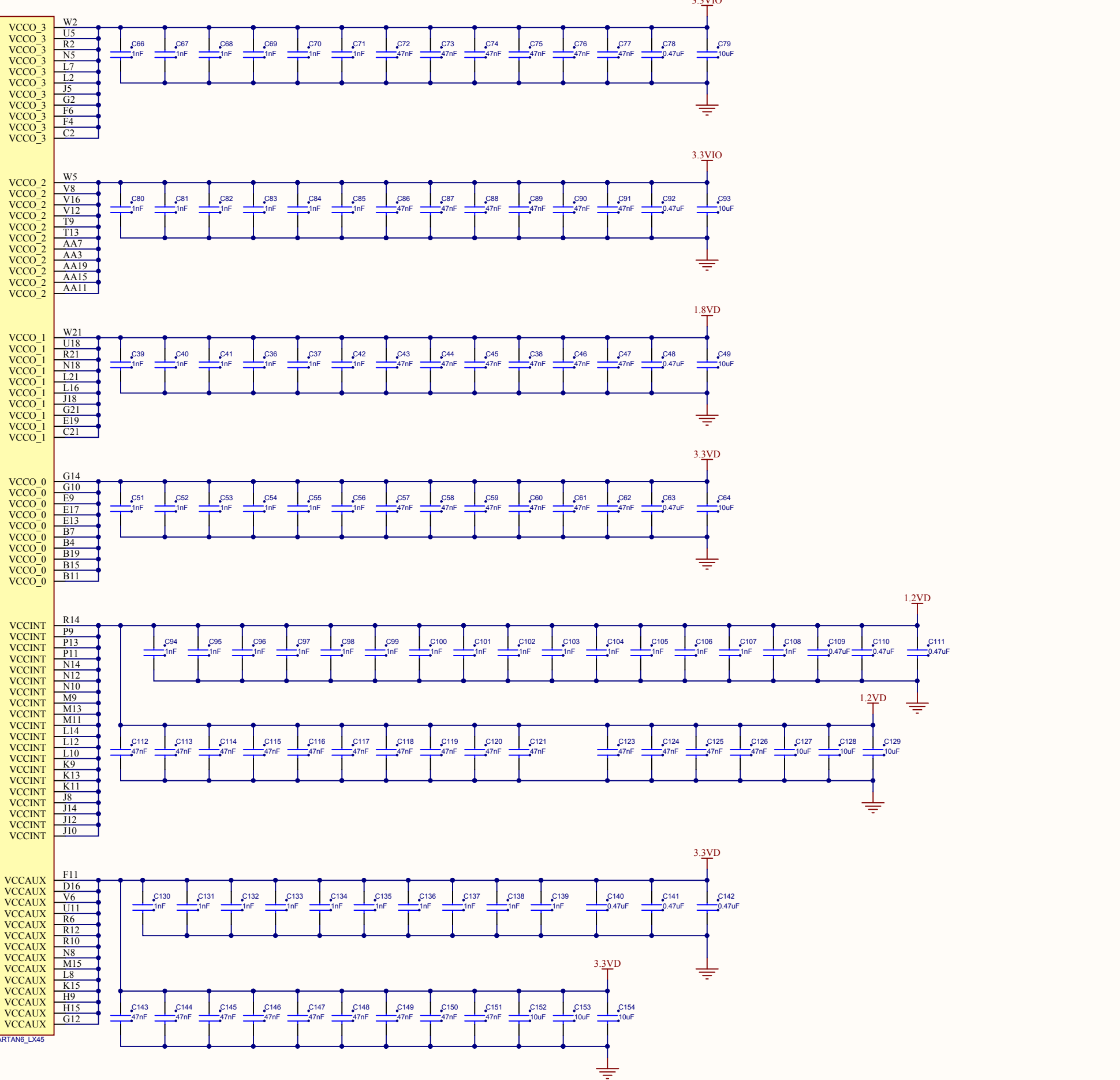
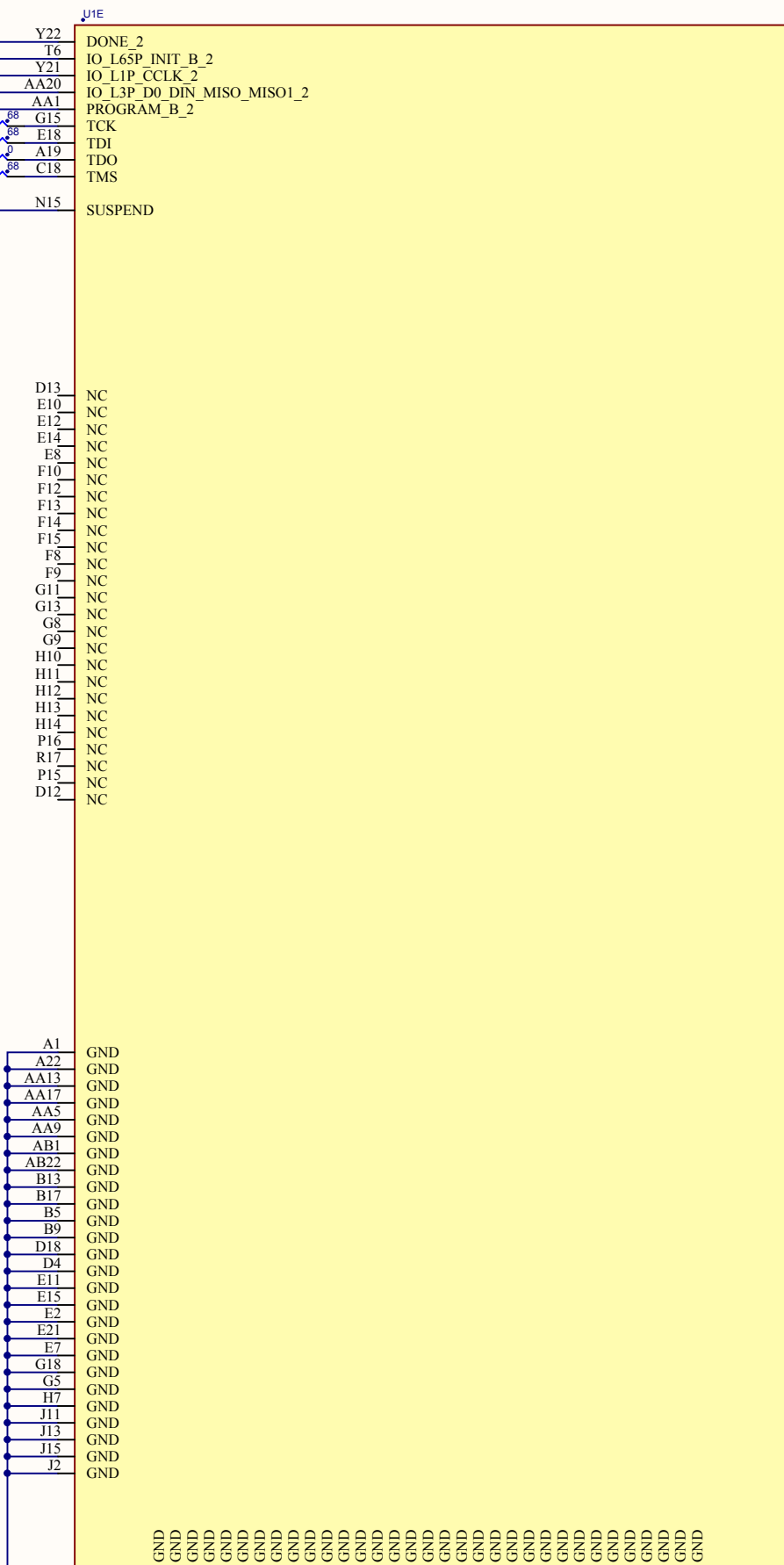
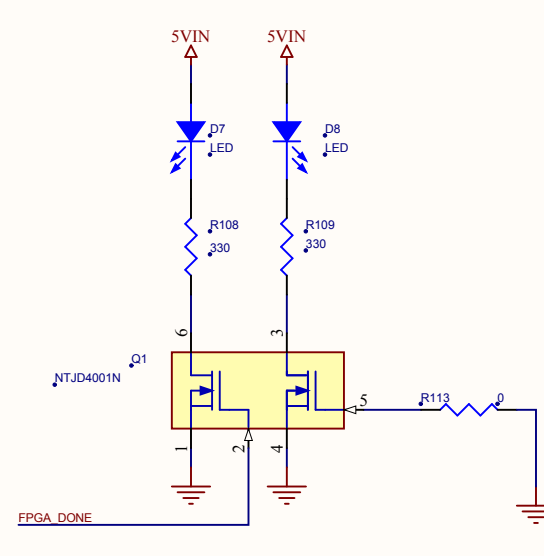
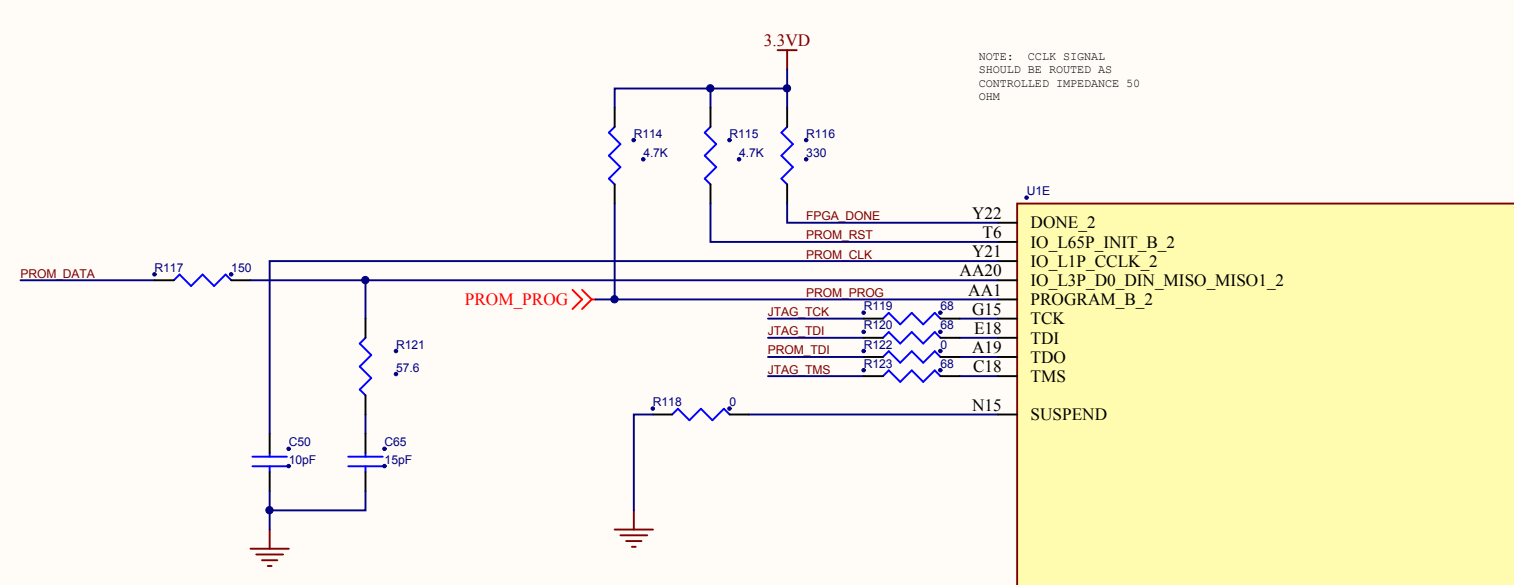
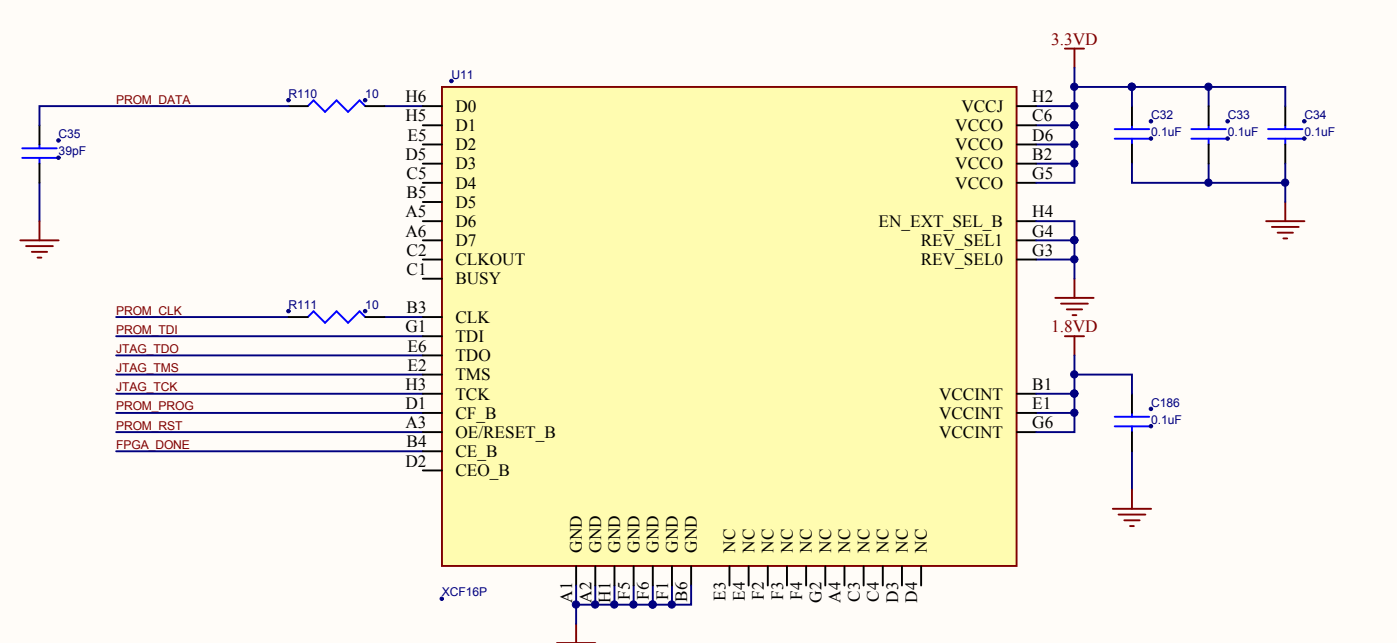
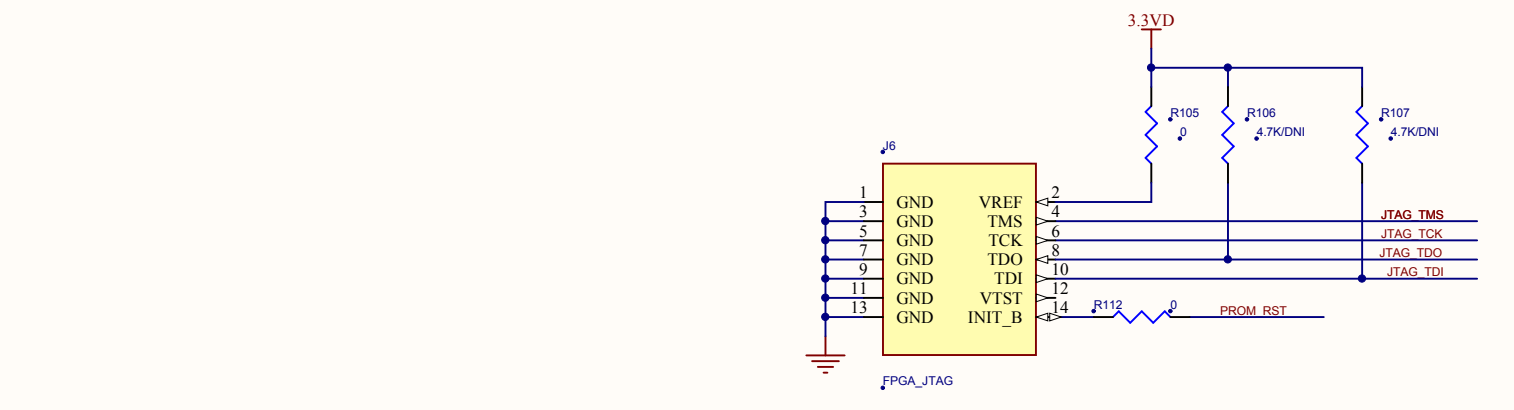
NOTE: ALL TRACES ROUTED AT 50 OHM SINGLE-ENDED, ALL DIFFERENTIAL TRACES ROUTED AT 100 OHM DIFFERENTIAL. TRACE LENGTHS SHOULD BE MATCHED TO KEEP PROPAGATION DELAY BETWEEN ANY TWO TRACES TO LESS THAN 25ps.

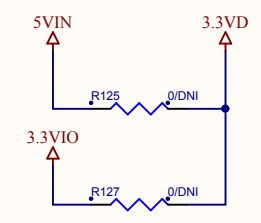
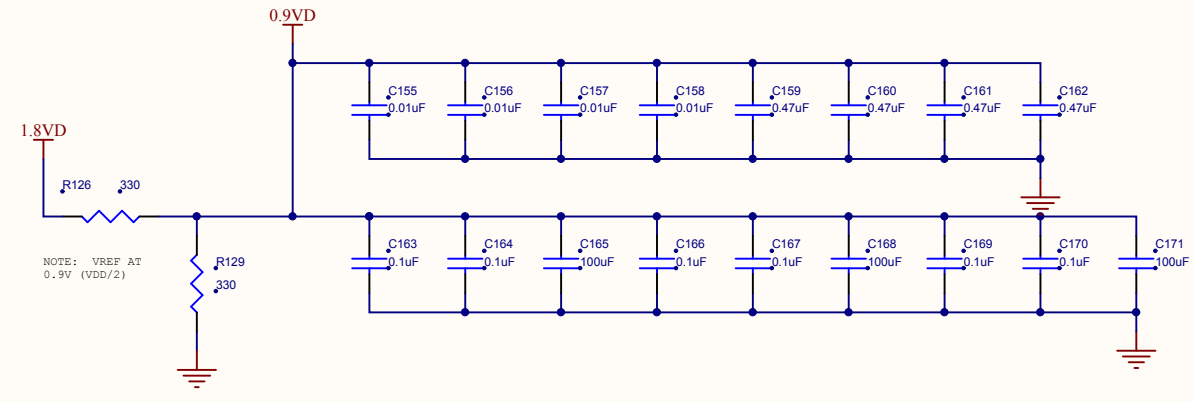
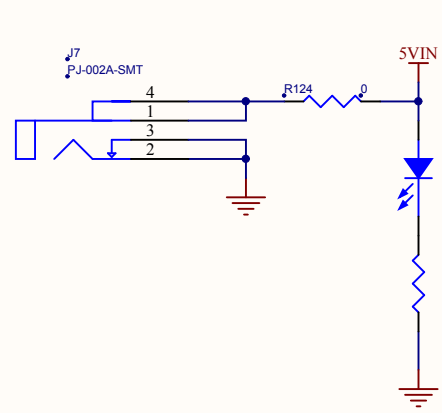
NOTE: SDRAM_LOOP PINS SHOULD BE ROUTED THE FULL DISTANCE TO THE SDRAM AND BACK TO FPGA JUST LIKE ALL OTHER SDRAM PINS TO SERVE AS TIMING ADJUSTMENT CONTROL FOR THE FPGA. IE, DO NOT CONNECT THEM AT THE FPGA. SIGNAL SHOULD BE ROUTED IN THE MIDDLE OF THE GROUP OF DQ ROUTES.



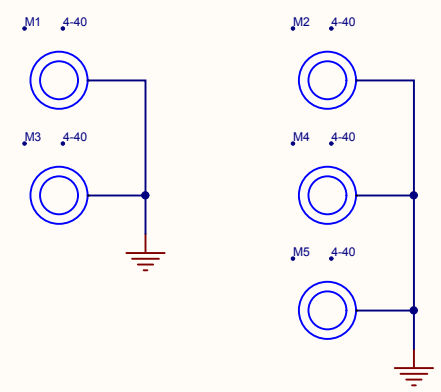


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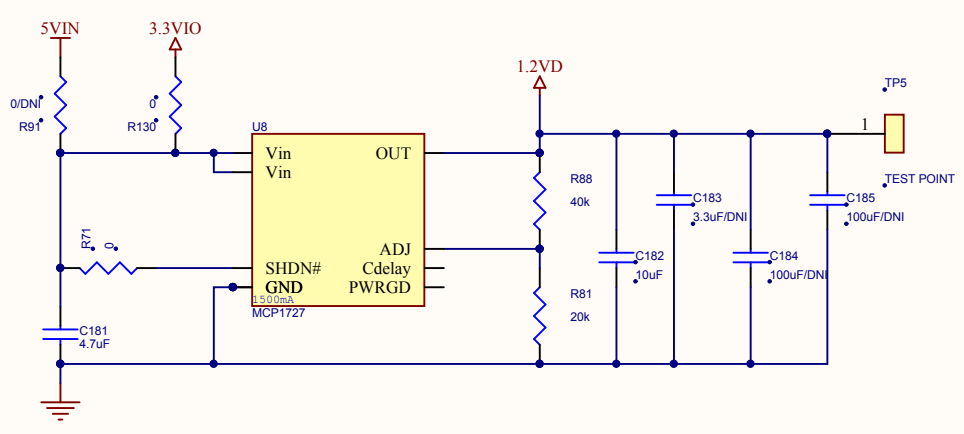
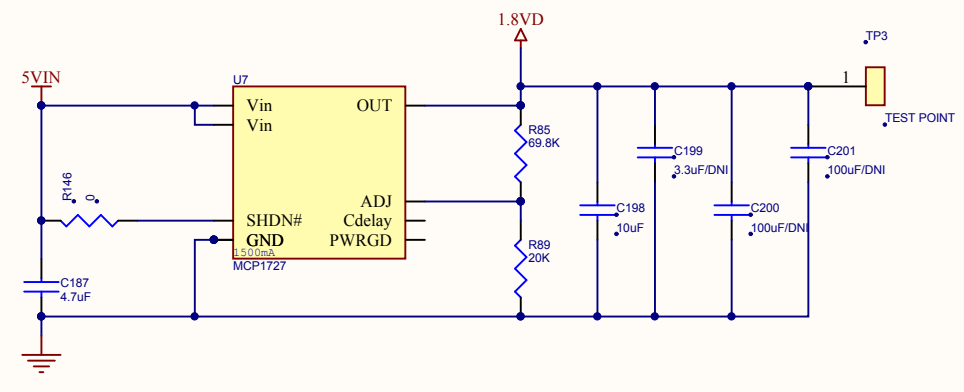
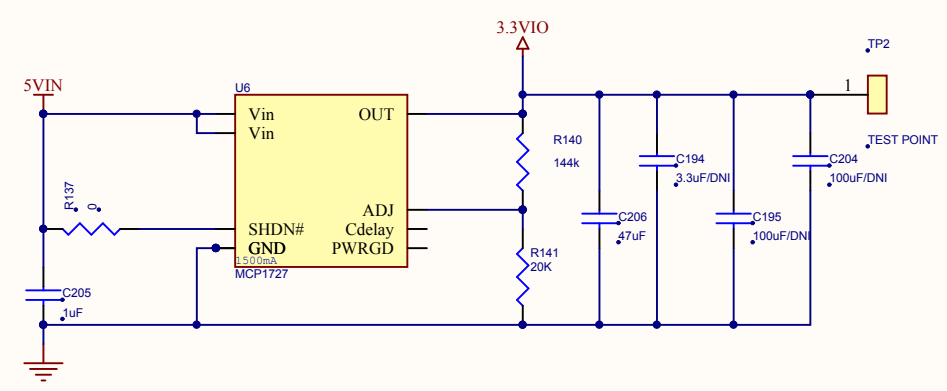
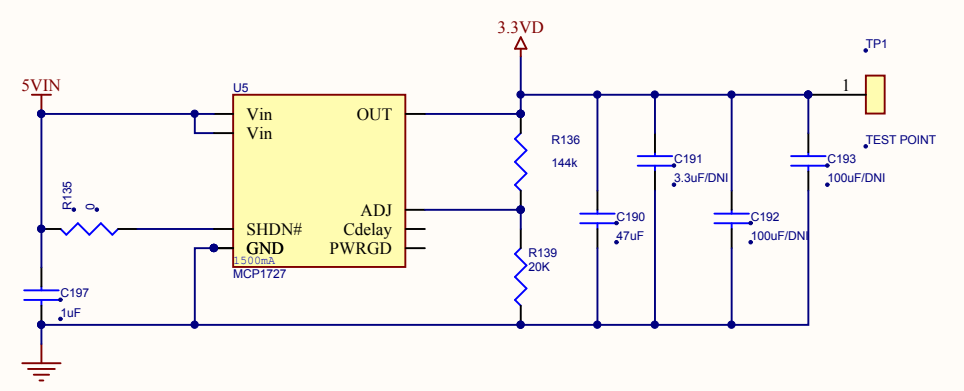
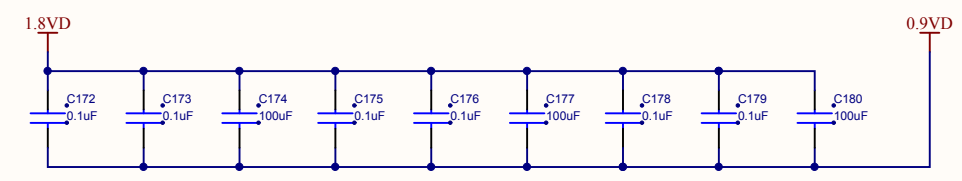




NOTE: PLACE MOUNTING HOLES AT CORNERS OF PCB



NOTE: USE IF SUPPLYING 3.3V TO EXTERNAL POWER CONNECTOR. MUST ALSO REMOVE OR SHUTDOWN 3.3V REGULATOR.



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