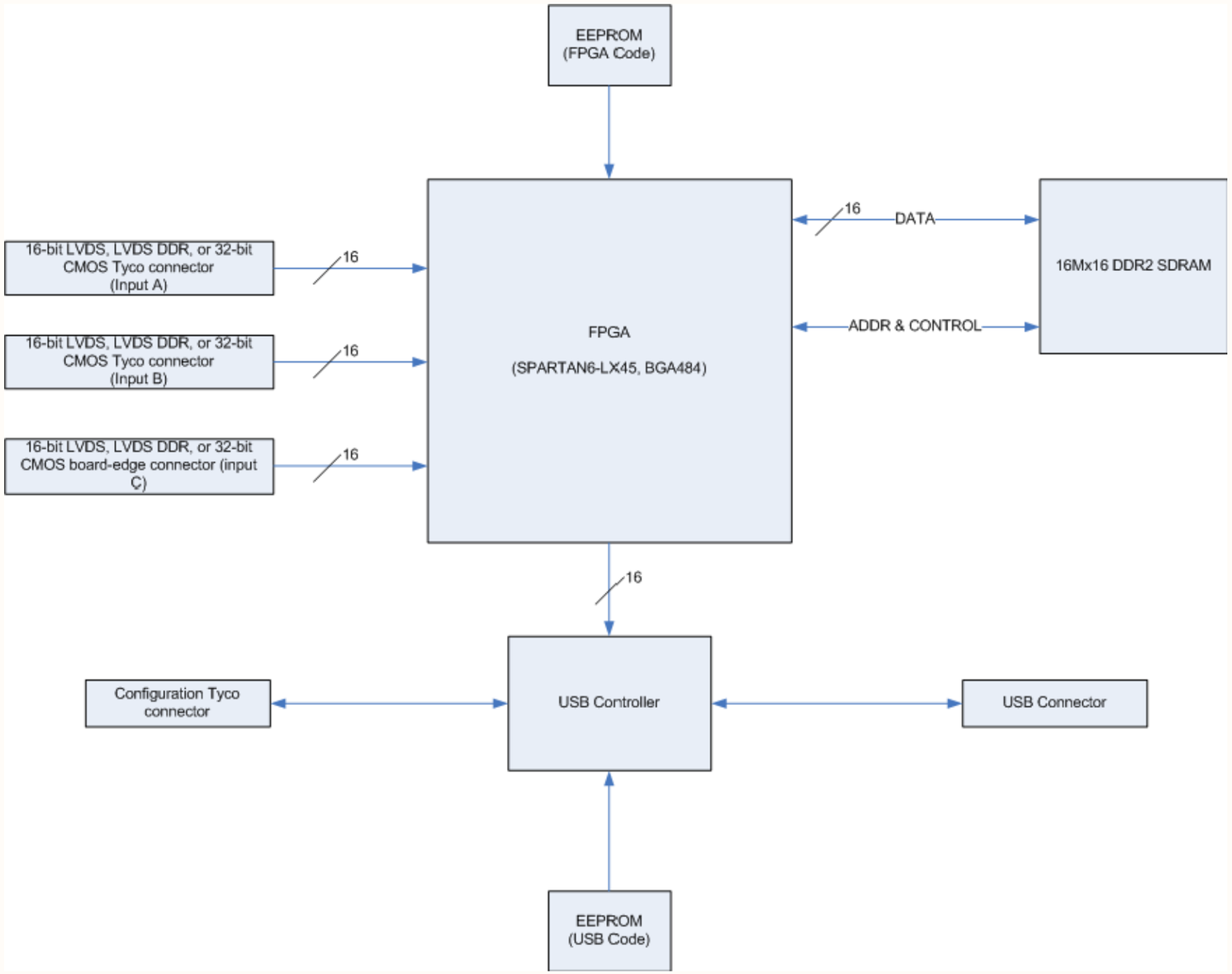

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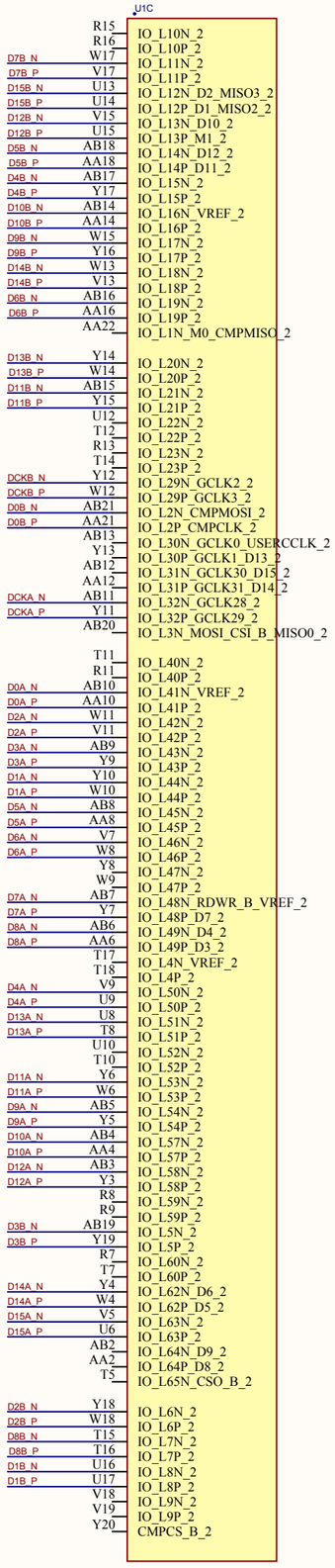
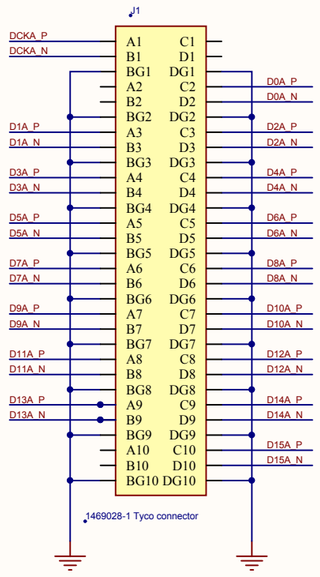


INPUT A CONNECTOR

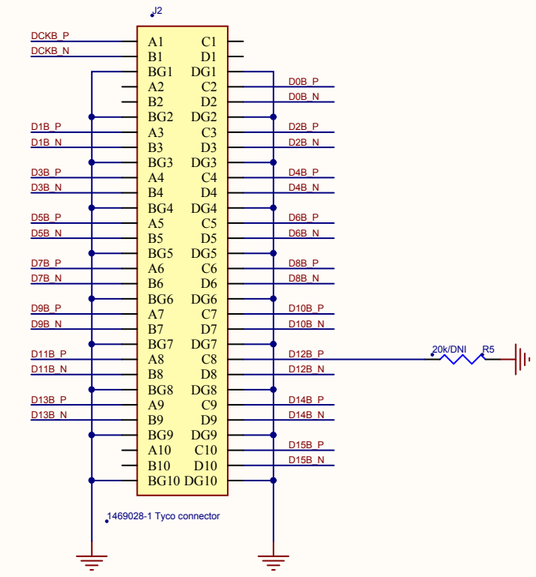
NOTE:DIFFERENTIAL PAIRS ROUTED AT 1% LENGTH, 100-OHM DIFFERENTIAL



NOTE: D8A_P AND D8A_N ARE EXPECTED TO BE USED FOR LVDS OVERRANGE SIGNAL

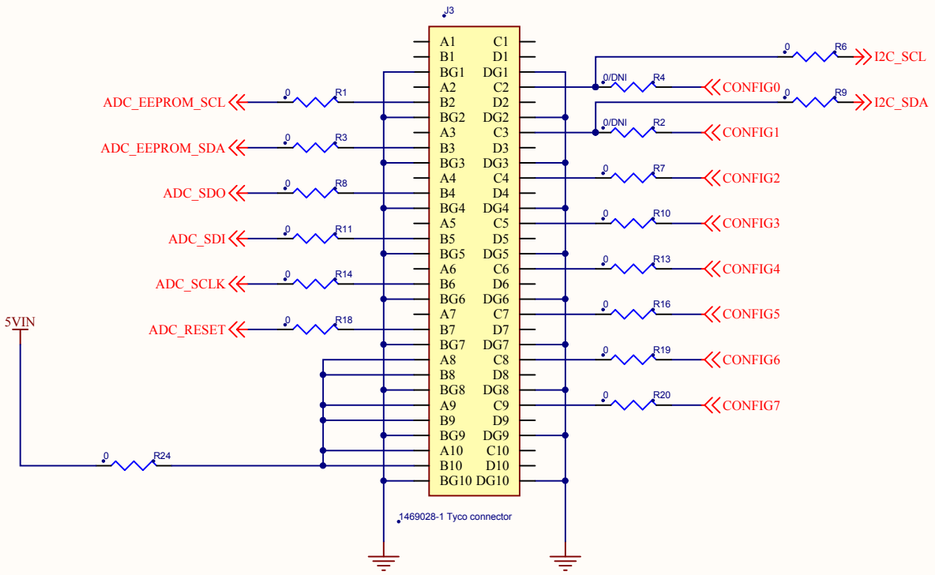
INPUT B CONNECTOR

NOTE:DIFFERENTIAL PAIRS ROUTED AT 1% LENGTH, 100-OHM DIFFERENTIAL



NOTE: CONFIG[0:15] IS RESERVED FOR FUTURE USE, ROUTED SINGLE-ENDED

CONFIGURATION CONNECTOR



NOTE: CONFIG INTERFACE PIN A1 SHOULD BE 38mm FROM INPUT A PIN A1 WHICH SHOULD BE 32mm FROM INPUT B PIN A1. (CENTER OF PINS)

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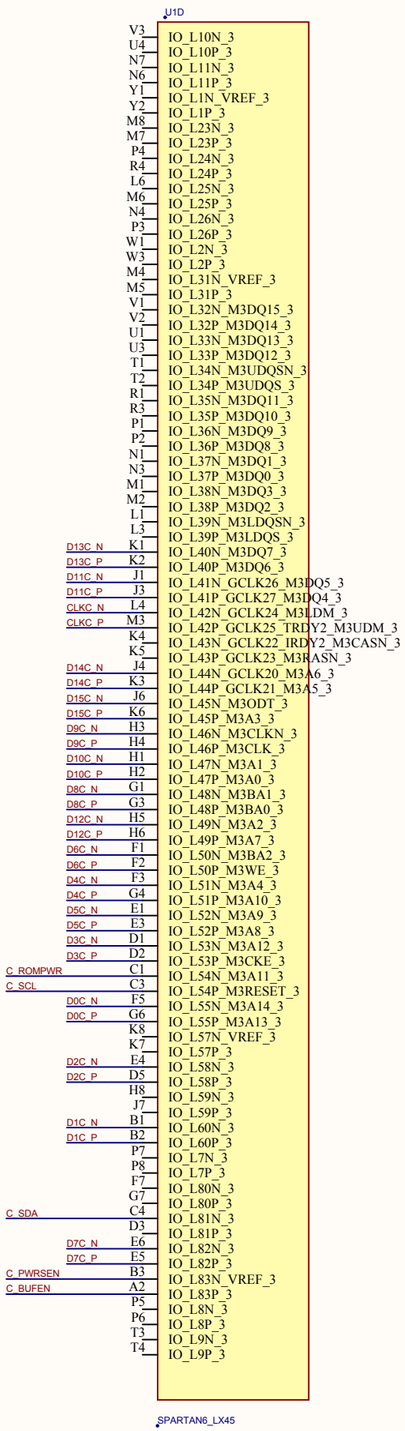
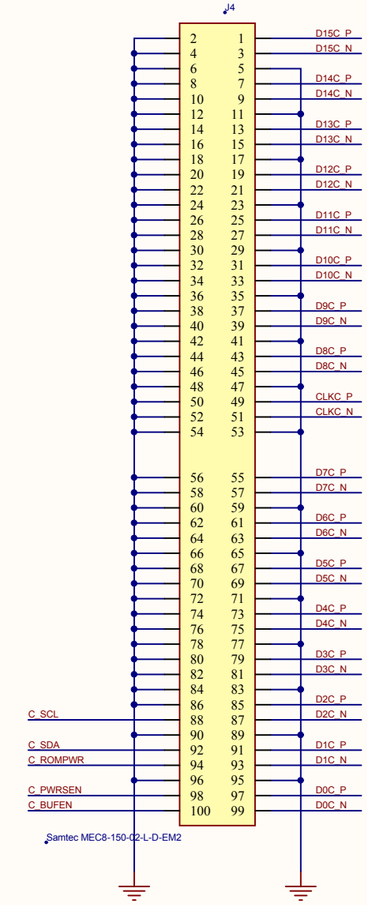


NOTE:DIFFERENTIAL PAIRS ROUTED AT 1% LENGTH, 100-OHM DIFFERENTIAL

INPUT C CONNECTOR



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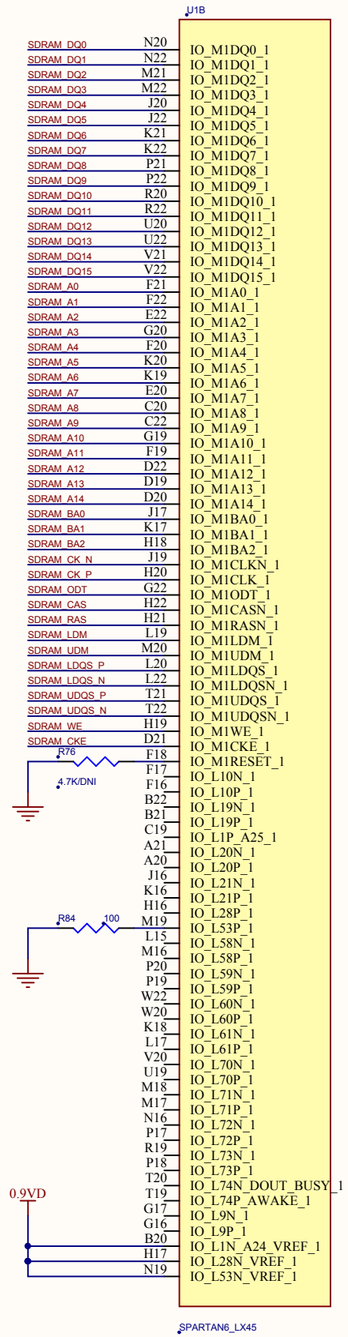
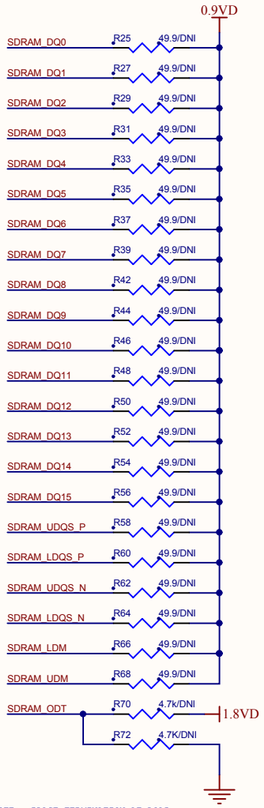
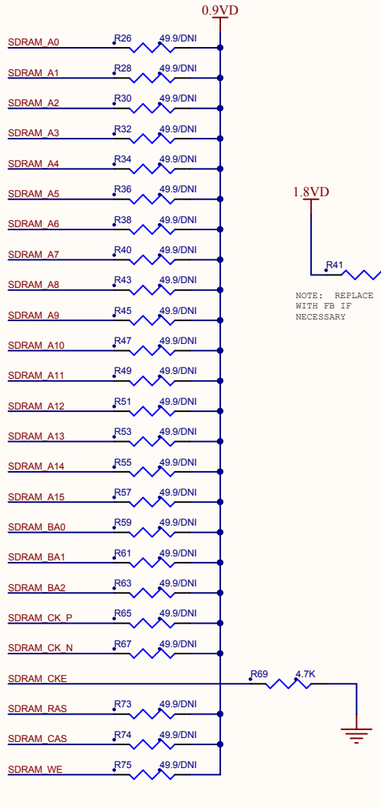
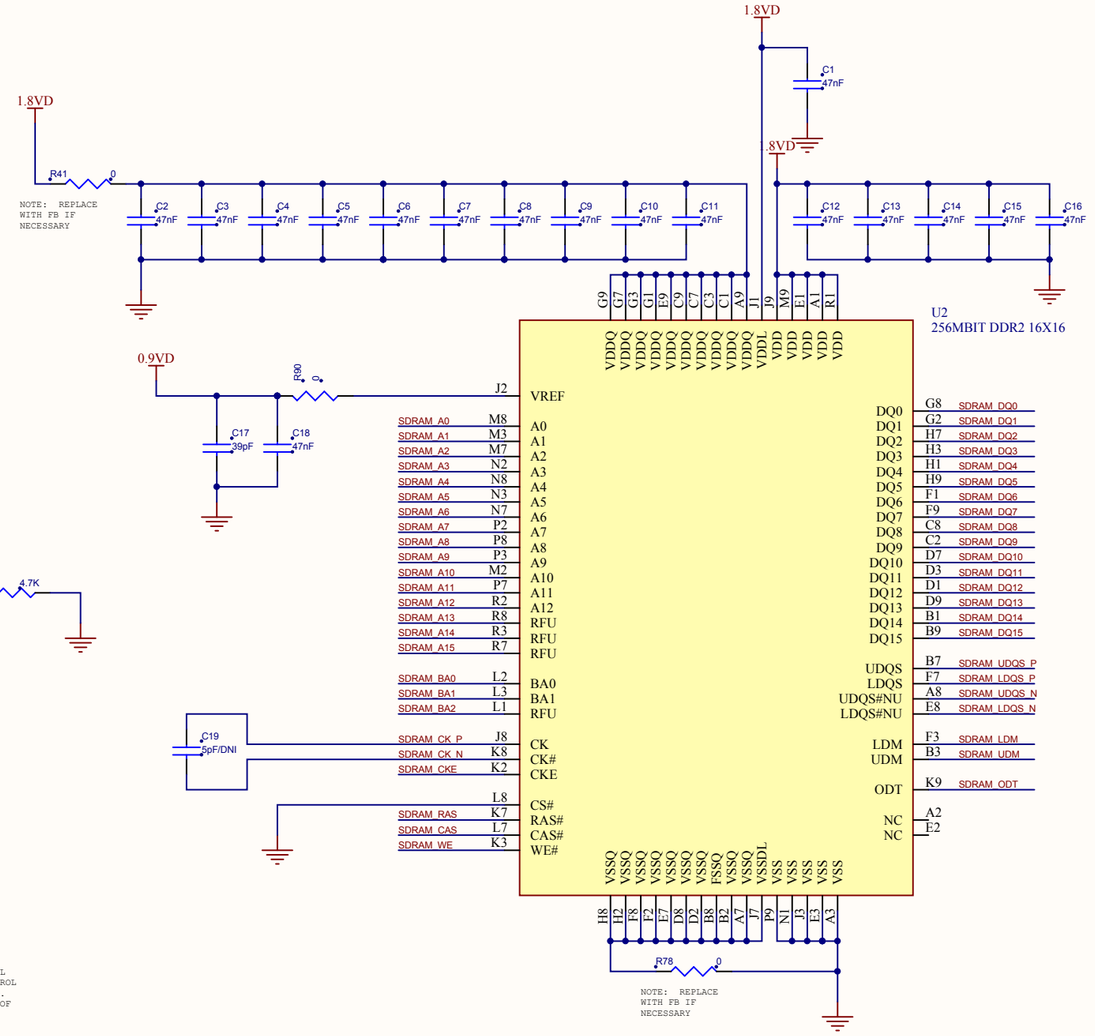
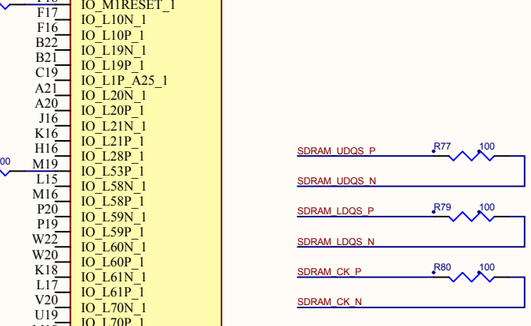




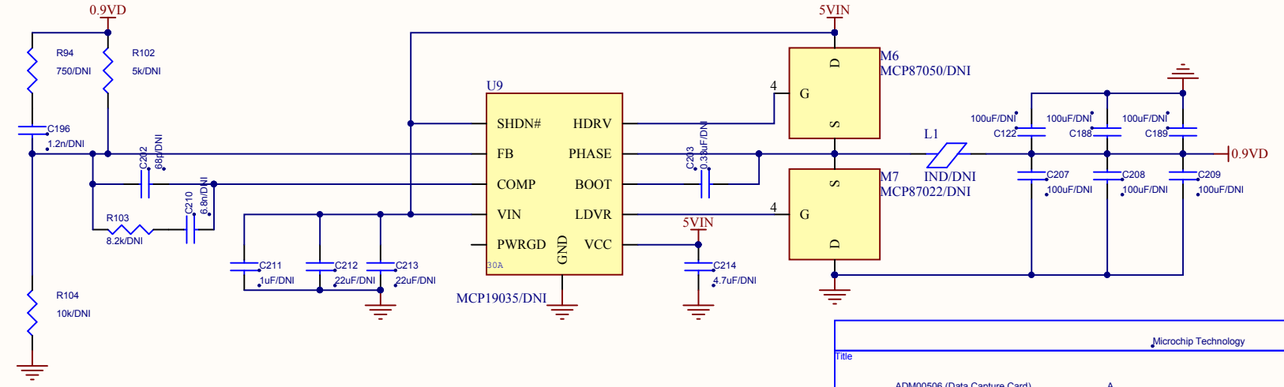






NOTE: ALL TRACES ROUTED AT 50 OHM SINGLE-ENDED, ALL DIFFERENTIAL TRACES ROUTED AT 100 OHM DIFFERENTIAL. TRACE LENGTHS SHOULD BE MATCHED TO KEEP PROPOGATION DELAY BETWEEN ANY TWO TRACES TO LESS THAN 25pS.

NOTE: SDRAM_LOOP PINS SHOULD BE ROUTED THE FULL DISTANCE TO THE SDRAM AND BACK TO FPGA JUST LIKE ALL OTHER SDRAM PINS TO SERVE AS TIMING ADJUSTMENT CONTROL FOR THE FPGA. IE. DO NOT CONNECT THEM AT THE FPGA. SIGNAL SHOULD BE ROUTED IN THE MIDDLE OF THE GROUP OF DQ ROUTES.



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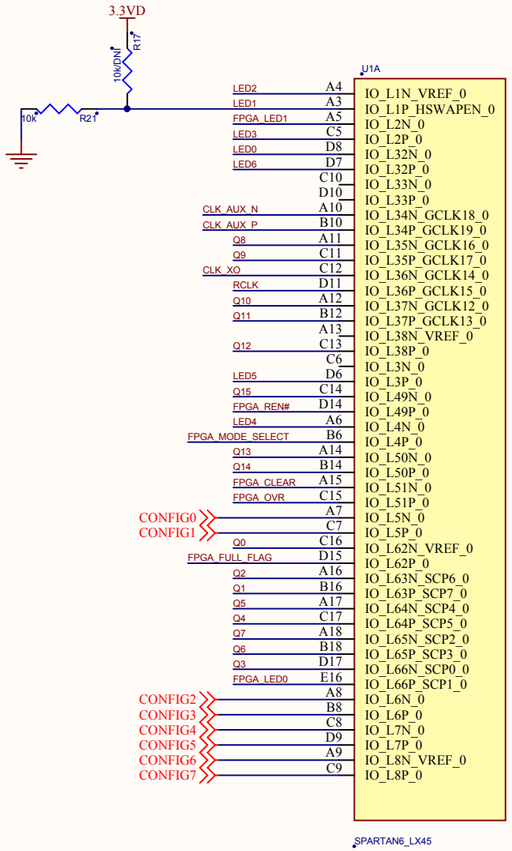

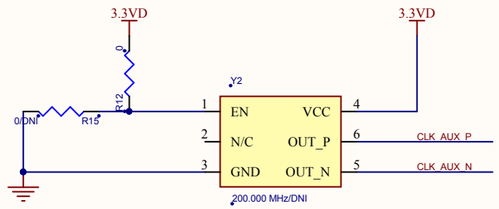

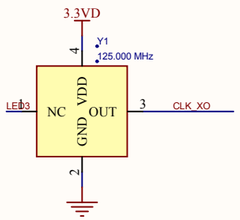

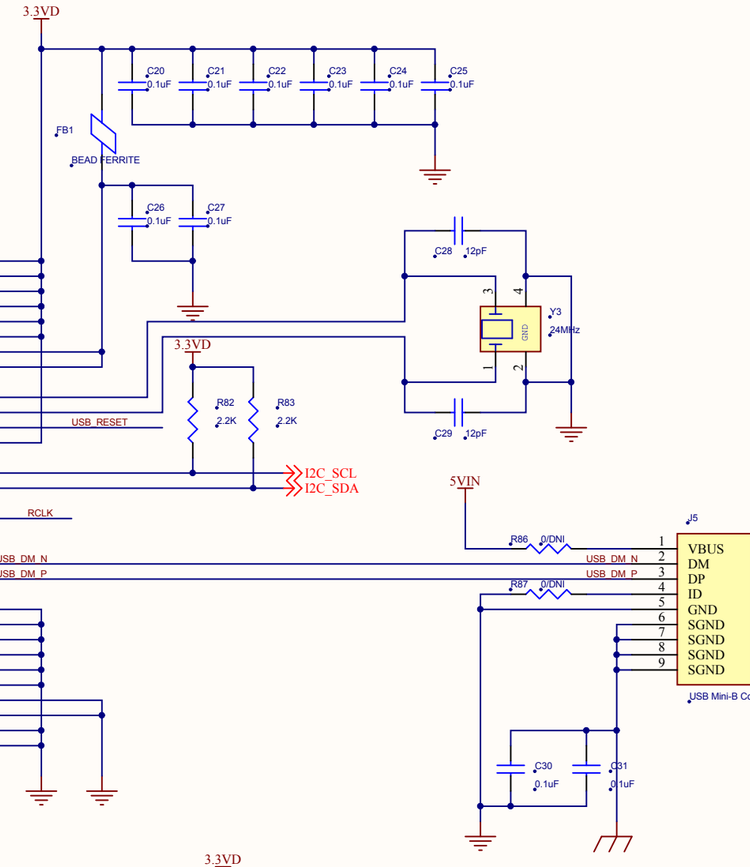

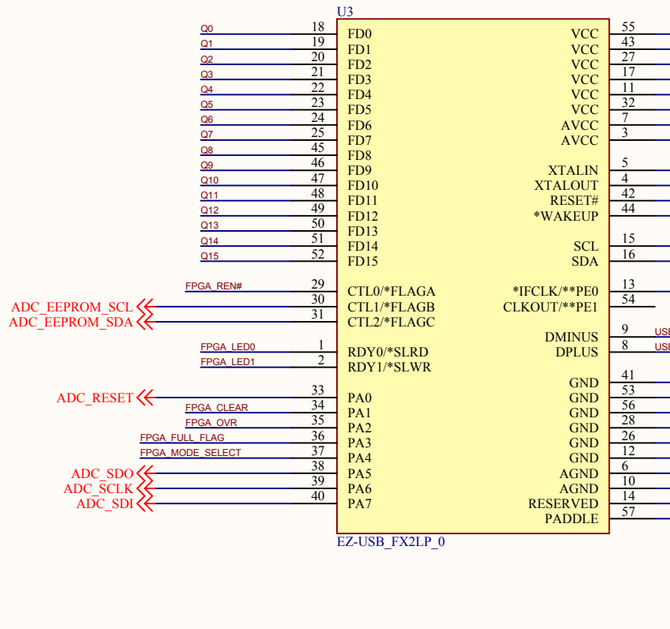

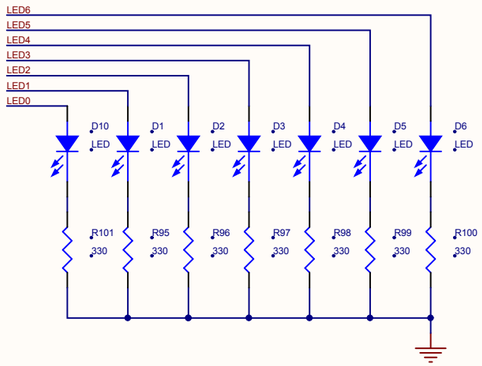

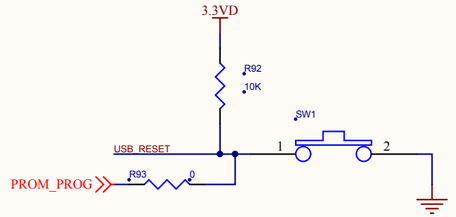

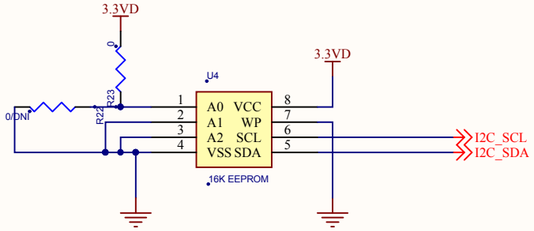

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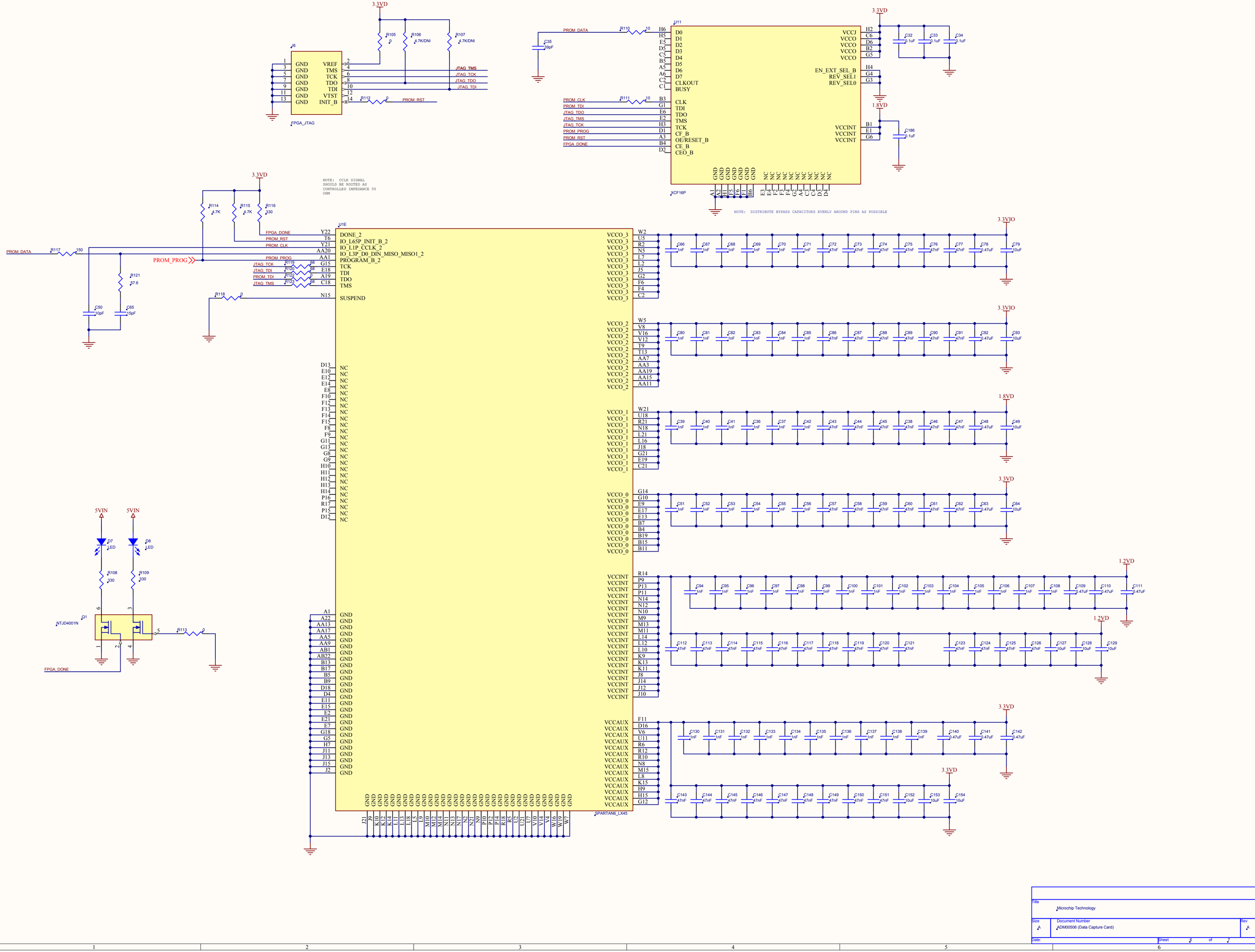

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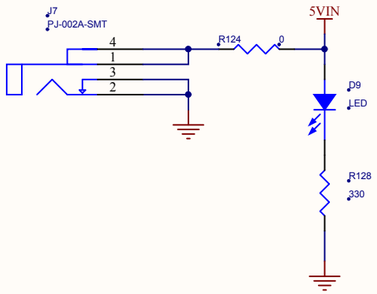
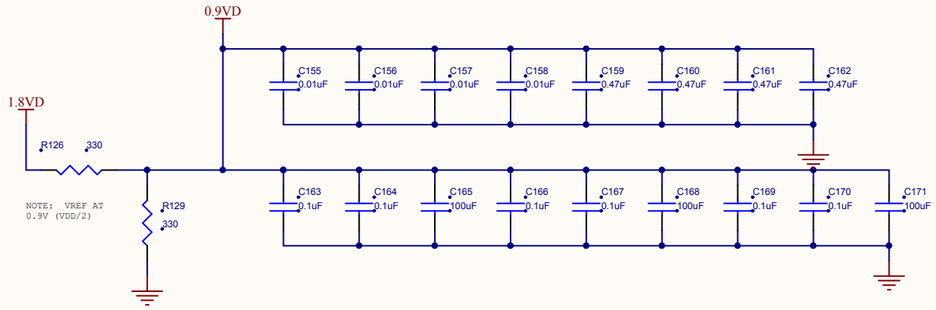
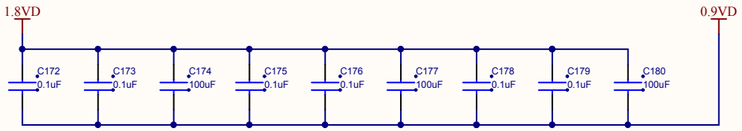
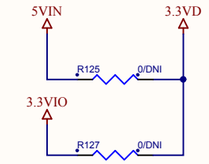
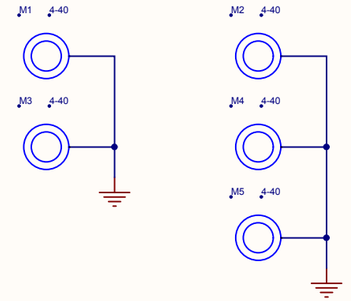


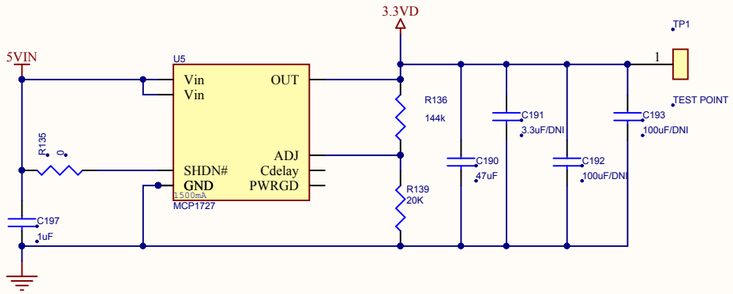


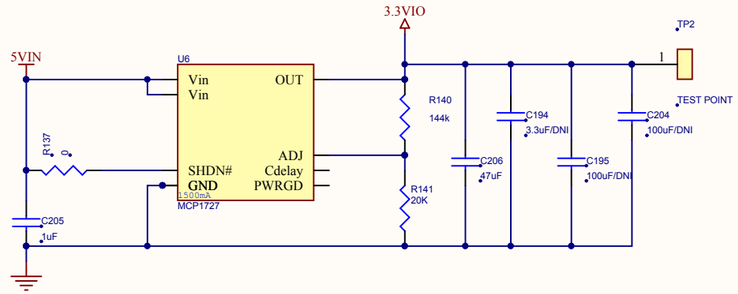


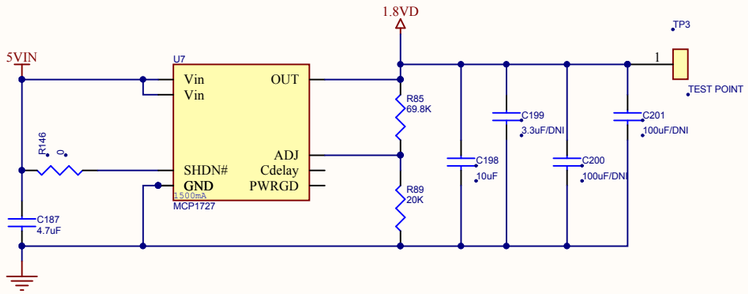


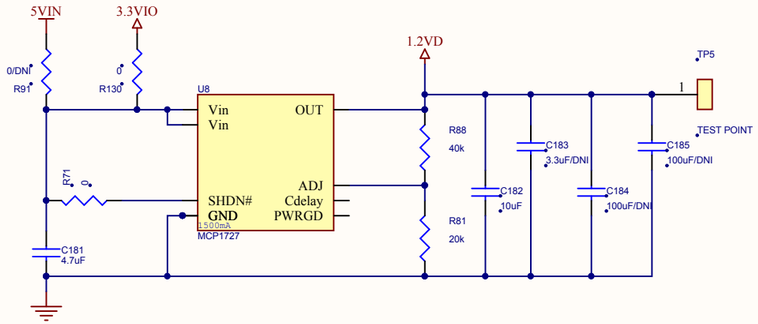
NOTE: USE IF SUPPLYING 3.3V TO EXTERNAL POWER CONNECTOR. MUST ALSO REMOVE OR SHUTDOWN 3.3V REGULATOR.











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