Transmit VGA for Use with RF DACs and Transceivers

Data Sheet **ADL6317**

FEATURES

- Transmit VGA for RF DAC, transceiver, and SoC to power amplifier interface
- RF output frequency range: 1500 MHz to 3000 MHz
- Internal balun with bias-tee to supply RF DAC outputs
- Integrated VVA attenuation range with on-chip DAC: 20.5 dB
- 2-stage high linearity amplifiers
- RF DSA attenuation range: 15.5 dB with 0.5 dB step resolution
- 50 Ω differential inputs and 50 Ω single-ended output
- Fully programmable via a 4-wire SPI
- Single 5 V supply
- 38-terminal, 10.5 mm × 5.5 mm LGA

APPLICATIONS

- 2G/3G/4G/long-term evolution (LTE) in FDD/TDD broadband communication systems

GENERAL DESCRIPTION

The ADL6317 is a transmit variable gain amplifier (VGA) that provides an interface from radio frequency digital-to-analog converters (RF DACs), transceivers, and systems on a chip (SoC) to power amplifiers. Integrated balun and hybrid couplers allow high performance RF capability in the frequency range of 1500 MHz to 3000 MHz.

To optimize performance vs. power level, the ADL6317 includes a voltage variable attenuator (VVA), high linearity amplifiers, and a digital step attenuator (DSA). All of the devices integrated into the ADL6317 are programmable via a 4-wire serial port interface (SPI).

The ADL6317 is manufactured on an advanced silicon germanium (SiGe), bipolar complementary metal oxide semiconductor (BiCMOS) process.

Table 1. Related Devices in Transmit VGA Family

Parameter	Frequency Range (MHz)
ADL6316	500 to 1000
ADL6317	1500 to 3000

FUNCTIONAL BLOCK DIAGRAM

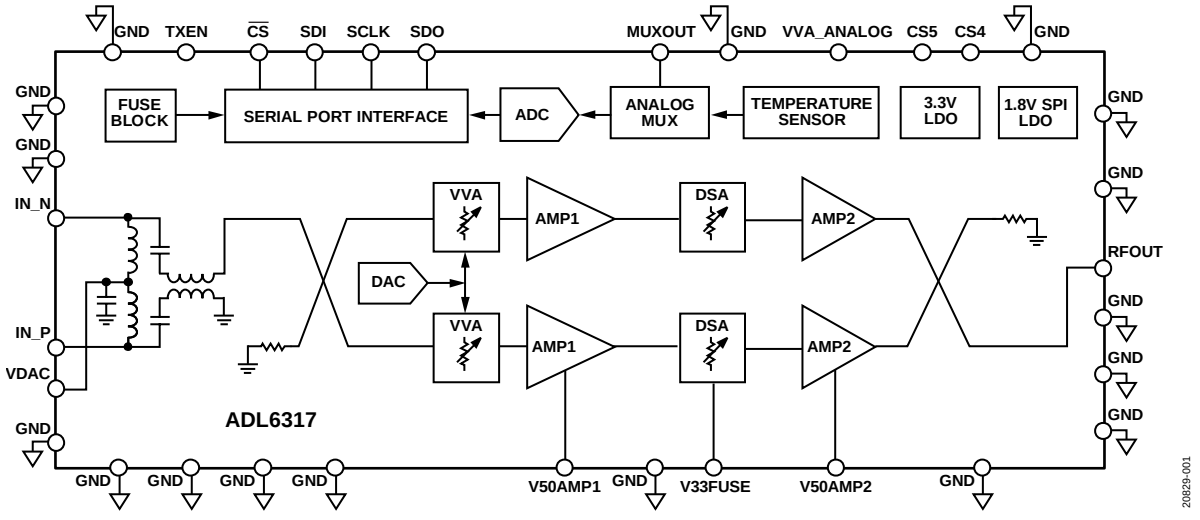

Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support
www.analog.com

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REVISION HISTORY

5/2020—Revision B: Initial Version

SPECIFICATIONS

V_{50AMP1} = V_{50AMP2} = 5 V, T_A = 25°C, input power (P_{IN}) = −25 dBm (−25 dBm per tone for two tones), VVA attenuation = 0 dB, DSA attenuation = 0 dB, source resistance (R_S) = load resistance (R_L) = 50 Ω, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Units
FREQUENCY RANGE		1500		3000	MHz
1850 MHz					
Power Gain			33.7		dB
Output 1 dB Compression Point (OP1dB)			25.7		dBm
Output Second-Order Intercept (OIP2)			49.2		dBm
Output Third-Order Intercept (OIP3)			40.9		dBm
Second Harmonic (HD2)			82.1		dBc
Third Harmonic (HD3)			47.2		dBc
Noise Figure (NF)			6.0		dB
2150 MHz					
Power Gain			33.6		dB
OP1dB			24.8		dBm
OIP2			51.8		dBm
OIP3			38.4		dBm
HD2			76.1		dBc
HD3			48.8		dBc
NF			6.0		dB
2600 MHz					
Power Gain			34.0		dB
OP1dB			22.8		dBm
OIP2			53.8		dBm
OIP3			34.5		dBm
HD2			84.6		dBc
HD3			50.7		dBc
NF			5.5		dB
RF INPUT/OUTPUT CHARACTERISTICS					
Input					
Impedance	Differential		50		Ω
Return Loss	Inband, 2150 MHz		−18		dB
Output					
Impedance	Single-ended		50		Ω
Return Loss	Inband, 2150 MHz		−17.4		dB
Gain Flatness	Deviation from best linear fit at 1850 MHz, 2150 MHz, and 2600 MHz				
	Over ±100 MHz bandwidth		±0.1		dB
	Over ±150 MHz bandwidth		±0.2		dB
VOLTAGE VARIABLE ATTENUATOR	Via 12-bit integrated DAC or external analog voltage on VVA_ANALOG pin				
Range			20.5		dB
Gain Settling Time	Minimum attenuation to maximum attenuation by VVA DAC		386.8		ns
	Maximum attenuation to minimum attenuation by VVA DAC		1.681		µs
DSA Attenuation					
Range			15.5		dB
Resolution			0.5		dB
Gain Settling Time	Minimum attenuation to maximum attenuation		304.4		ns
	Maximum attenuation to minimum attenuation		195.0		ns

Parameter	Test Conditions/Comments	Min	Typ	Max	Units
DIGITAL LOGIC					
Input Voltage	SCLK, SDI, $\overline{CS}$, CS4, CS5, TXEN				
High (V_{IH})		1.07			V
Low (V_{IL})				0.68	V
Input Current					
High (I_{IH})				−100	µA
Low (I_{IL})				100	µA
Output Voltage	SDO				
At 1.8 V	Register 0x121, Bit 4 = 0x0				
High (V_{OH})	Output high current (I_{OH}) = −100 µA or −1 mA static load	1.5			V
Low (V_{OL})	Output low current (I_{OL}) = 100 µA or 1 mA static load			0.2	V
At 3.3 V	Register 0x121, Bit 4 = 0x1				
High (V_{OH})	I_{OH} = −100 µA or −1 mA static load	2.7			V
Low (V_{OL})	I_{OL} = 100 µA or 1 mA static load			0.2	V
POWER SUPPLY					
Voltage		4.75	5.0	5.25	V
Supply Current	High performance mode		435		mA
	Low power mode		310		mA
Power Down Current			6		mA

DIGITAL LOGIC TIMING

Table 3.

Parameter	Description	Min	Typ	Max	Unit
f_{SCLK}	Maximum serial clock rate, $1/t_{SCLK}$		25		MHz
t_{PWH}	Minimum period that SCLK is in logic high state		10		ns
t_{PWL}	Minimum period that SCLK is in logic low state		10		ns
t_{DS}	Setup time between data and rising edge of SCLK		5		ns
t_{DH}	Hold time between data and rising edge of SCLK		5		ns
t_{DCS}	Setup time between falling edge of $\overline{CS}$ and rising edge of SCLK		10		ns
t_{DV}	Maximum time delay between falling edge of SCLK and output data valid for a read operation		5		ns

Timing Diagrams

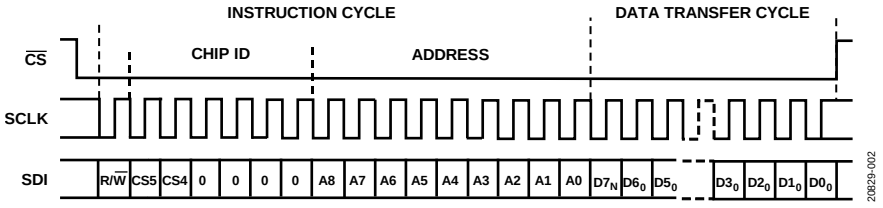


Figure 2. Serial Port Interface Register Timing, MSB First

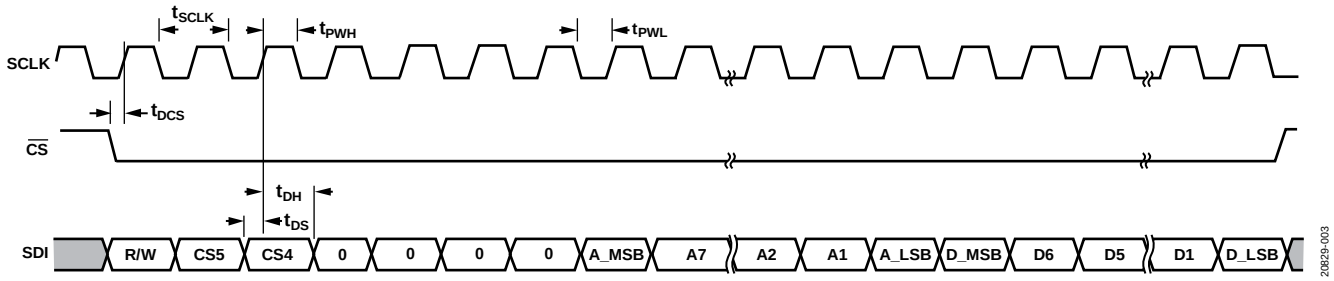


Figure 3. Timing Diagram for the Serial Port Interface Register Write

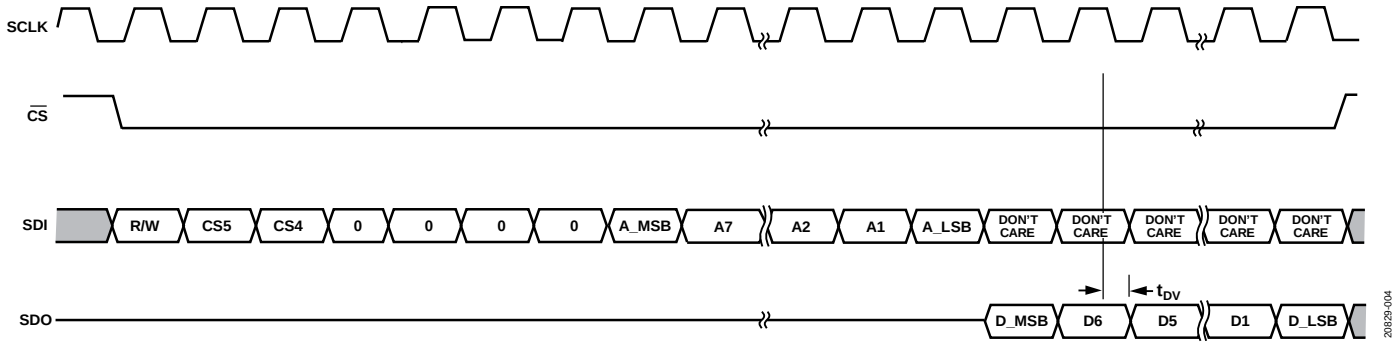


Figure 4. Timing Diagram for Serial Port Interface Register Read

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V50AMP1, V50AMP2	−0.3 V to +5.5V
V33FUSE	−0.3 V to +3.6 V
VDAC	−0.3 V to +3.6 V
VVA_ANALOG	−0.3 V to +3.6 V
$\overline{CS}$, SCLK, SDI, SDO, CS4, CS5, TXEN	−0.3 V to +3.6 V
RF Input Power (IN_N, IN_P) at 50 Ω	10 dBm
Operating Temperature Range (Measured at Exposed Pad)	−40°C to +105°C
Junction Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the conduction thermal resistance from junction to case where the case temperature is measured at the bottom of the package.

The thermal resistance values specified in Table 5 are simulated based on JEDEC specifications (unless specified otherwise) and should be used in compliance with JESD51-12.

Table 5. Thermal Resistance[1, 2]

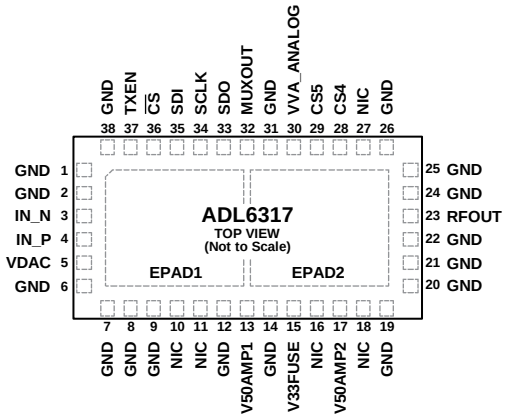
Package Type	θ_{JA}	$\theta_{JC\ BOTTOM}$	Unit
CC-38-1	21.4	7.6	°C/W

[1] For $\theta_{JC\ BOTTOM}$, the case bottom is controlled at105°C and the case top is controlled at 100°C.
[2] Using enhanced heat removal (for example, PCB, heat sink, and airflow) techniques to improve thermal resistance values.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED. THIS PIN HAS NO PHYSICAL CONNECTION WITHIN THE CHIP.
2. EXPOSED PAD 1. EPAD1 IS INTERNALLY CONNECTED TO EPAD2. THE EXPOSED PAD MUST BE CONNECTED TO GROUND FOR ELECTRICAL AND THERMAL PURPOSES.
3. EXPOSED PAD 2. EPAD2 IS INTERNALLY CONNECTED TO EPAD1. THE EXPOSED PAD MUST BE CONNECTED TO GROUND FOR ELECTRICAL AND THERMAL PURPOSES.

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Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 6, 7, 8, 9, 12, 14, 19, 20, 21, 22, 24, 25, 26, 31, 38	GND	Ground.
3	IN_N	RF Input, Negative.
4	IN_P	RF Input, Positive.
5	VDAC	Supply Voltage for External RF DAC. This pin can be left open during operation without the RF DAC.
10, 11, 16, 18, 27	NIC	No Internal Connection. These pins have no physical connection within the chip.
13	V50AMP1	Amplifier 1 Analog Power Supply (5.0 V).
15	V33FUSE	VCO Low Dropout (LDO) Regulator Bypass. This pin is optionally 3.3 V when the 3.3 V LDO regulator is off.
17	V50AMP2	Amplifier 2 Analog Power Supply (5.0 V).
23	RFOUT	RF Output.
28, 29	CS4, CS5	Chip Select. Connect these pins to ground. Refer to the Multiple Chip Operation to Share SPI Bus section for information about the connections in a multiple chip operation.
30	VVA_ANALOG	Analog Voltage Control for VVA.
32	MUXOUT	Test Mux Output.
33	SDO	Serial Port Data Output.
34	SCLK	Serial Port Clock Input.
35	SDI	Serial Port Data Input.
36	$\overline{CS}$	Serial Port Latch Enable Input.
37	TXEN	Amplifier Enable, DSA Attenuation, and Trim Value Selection.
	EPAD1	Exposed Pad 1. EPAD1 is internally connected to EPAD2. The exposed pad must be connected to ground for electrical and thermal purposes.
	EPAD2	Exposed Pad 2. EPAD2 is internally connected to EPAD1. The exposed pad must be connected to ground for electrical and thermal purposes.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{50AMP1} = V_{50AMP2} = 5$ V, $T_A = 25°C$, input power= −25 dBm (−25 dBm per tone for two tones), VVA attenuation = 0 dB, DSA attenuation = 0 dB, $R_S = R_L = 50\ \Omega$, unless otherwise noted.

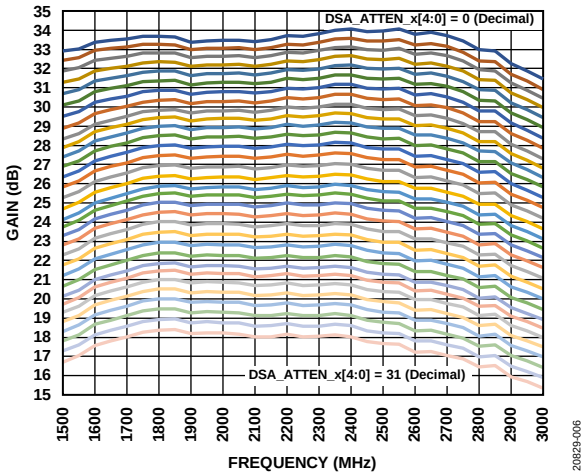

Figure 6. Gain vs. Frequency, 0.5 dB DSA Steps

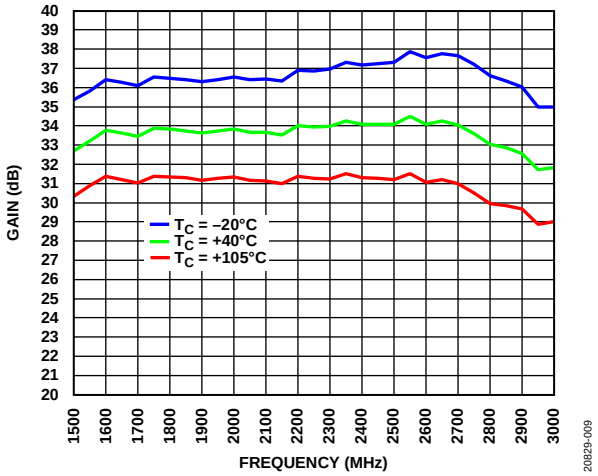

Figure 9. Gain vs. Frequency for Various Temperatures

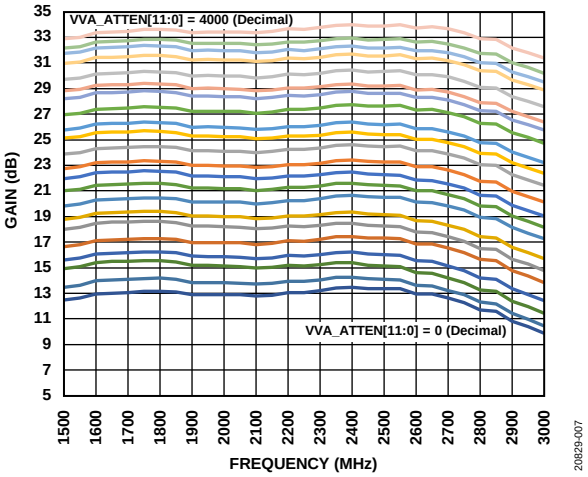

Figure 7. Gain vs. Frequency, 100 VVA_ATTEN[11:0] Steps

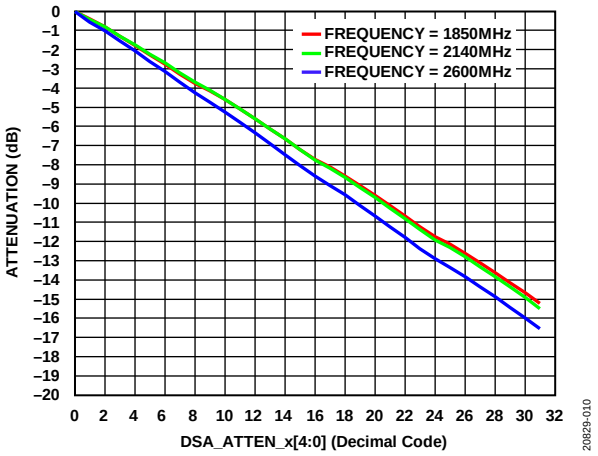

Figure 10. Attenuation vs. DSA_ATTEN_x[4:0] at 1850 MHz, 2150 MHz, and 2600 MHz, VVA Attenuation = 0 dB

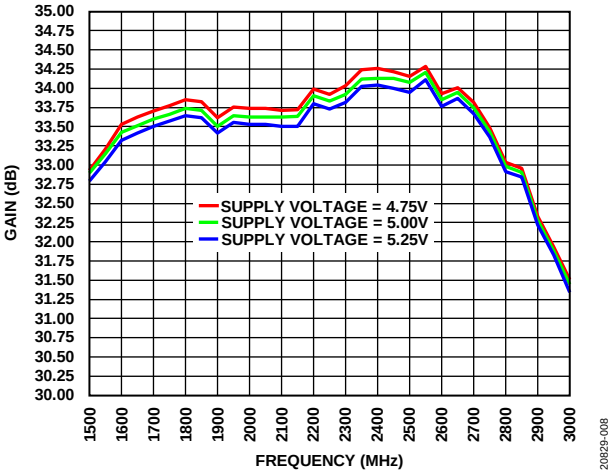

Figure 8. Gain vs. Frequency for Various Supplies

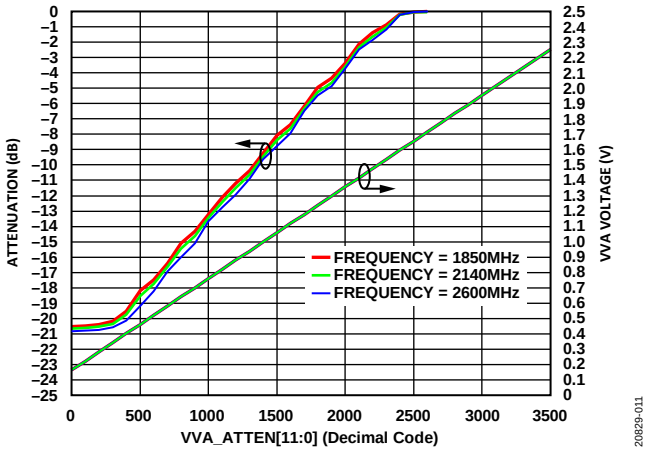

Figure 11. Attenuation and VVA Voltage vs. VVA_ATTEN[11:0] at 1850 MHz, 2150 MHz, and 2600 MHz, DSA Attenuation = 0 dB)

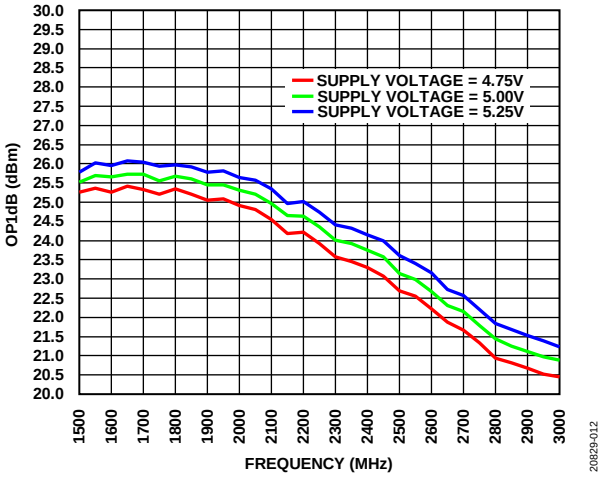

Figure 12. OP1dB vs. Frequency for Various Supplies

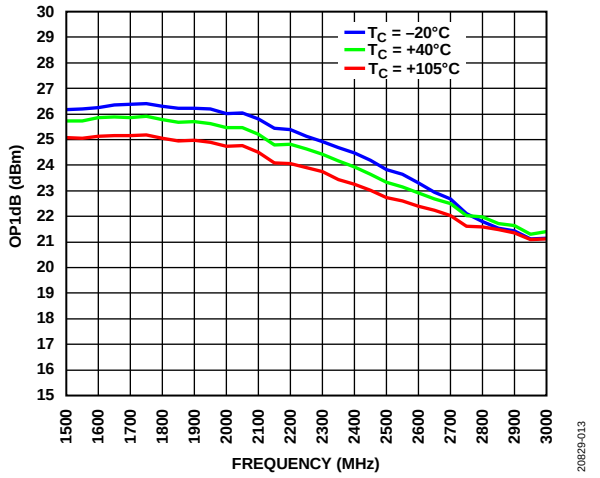

Figure 13. OP1dB vs. Frequency for Various Temperatures

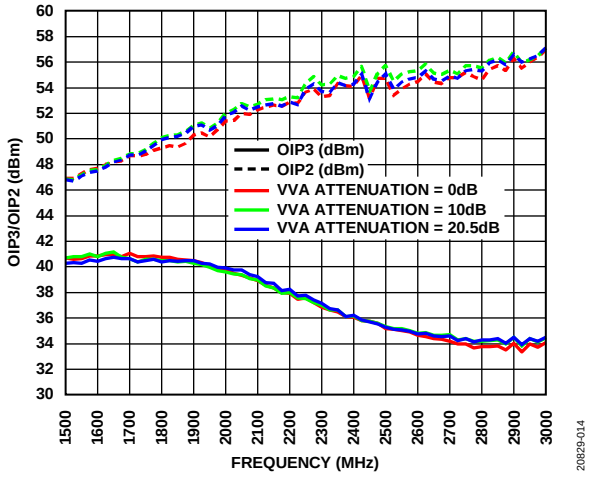

Figure 14. OIP3/OIP2 vs. Frequency at Various VVA Attenuation Values, DSA Attenuation = 0 dB

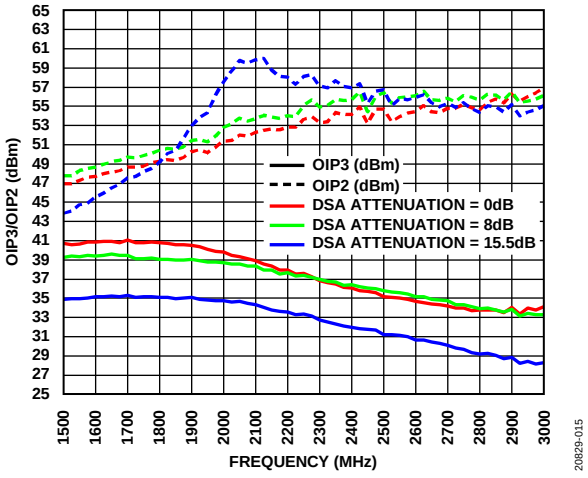

Figure 15. OIP3/OIP2 vs. Frequency at Various DSA Values, VVA Attenuation = 0 dB

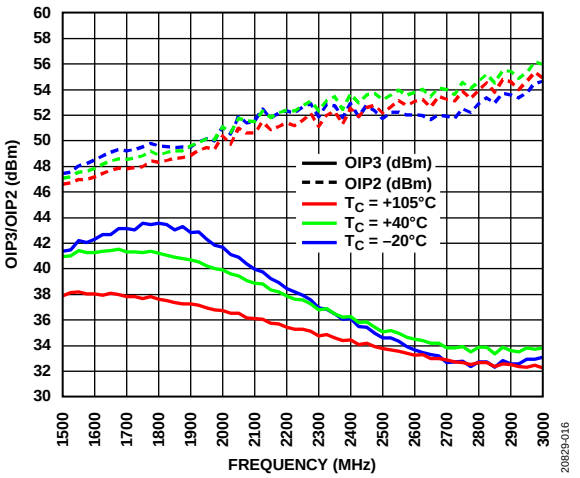

Figure 16. OIP3/OIP2 vs. Frequency for Various Temperatures

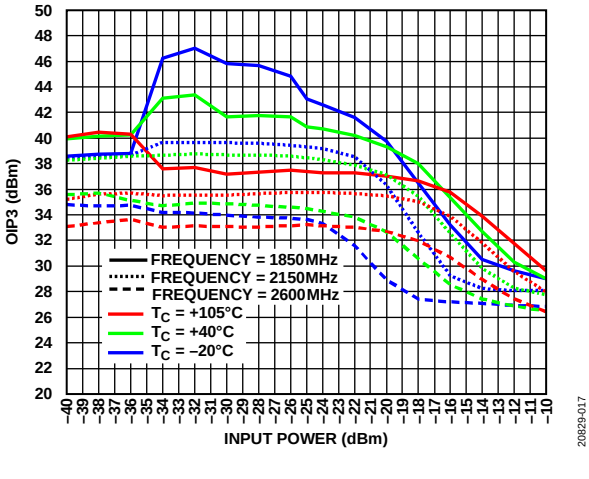

Figure 17. OIP3 vs. Input Power for Various Temperatures at 1850 MHz, 2150 MHz, and 2600 MHz

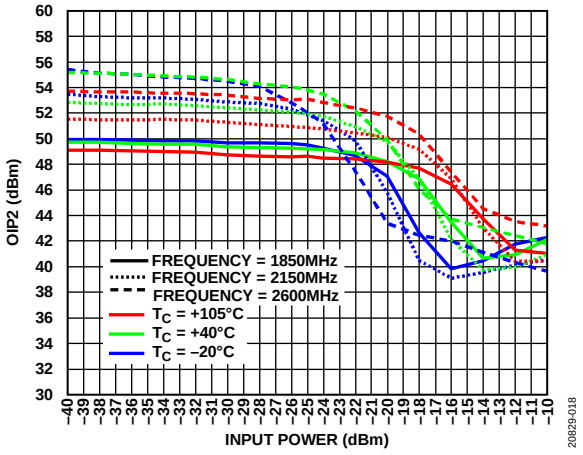

Figure 18. OIP2 vs. Input Power for Various Temperatures at 1850 MHz, 2150 MHz, and 2600 MHz

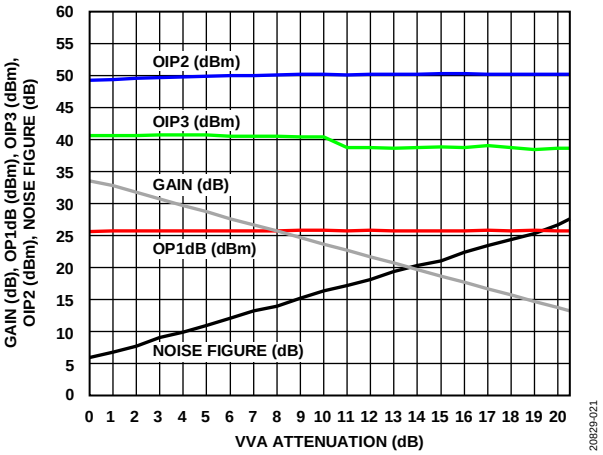

Figure 21. Gain, OP1dB, OIP3, OIP2, Noise Figure vs. VVA Attenuation, DSA Attenuation = 0 dB, Frequency = 1850 MHz

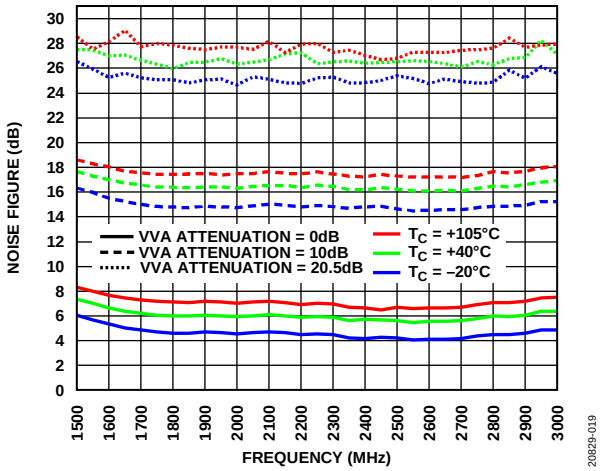

Figure 19. Noise Figure vs. Frequency for Various Temperatures at Various VVA Values, DSA Attenuation = 0 dB

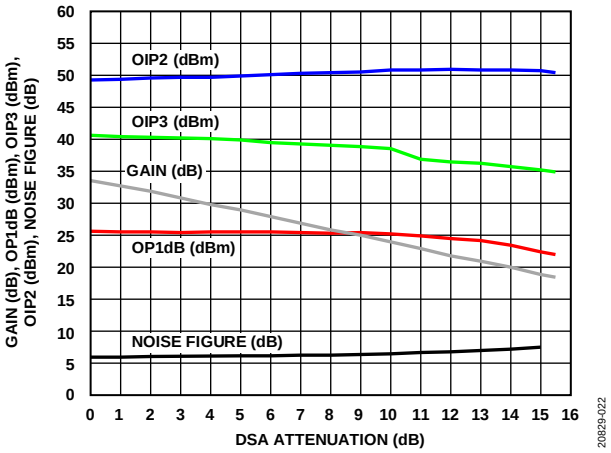

Figure 22. Gain, OP1dB, OIP3, OIP2, Noise Figure vs. DSA Attenuation, VVA Attenuation = 0 dB, Frequency = 1850 MHz

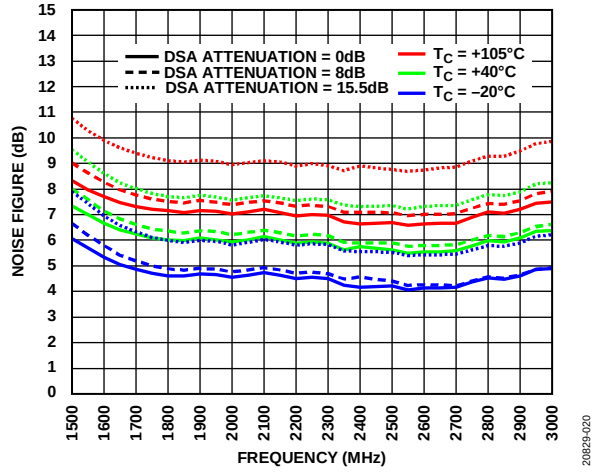

Figure 20. Noise Figure vs. Frequency for Various Temperatures at Various DSA Values, VVA Attenuation = 0 dB

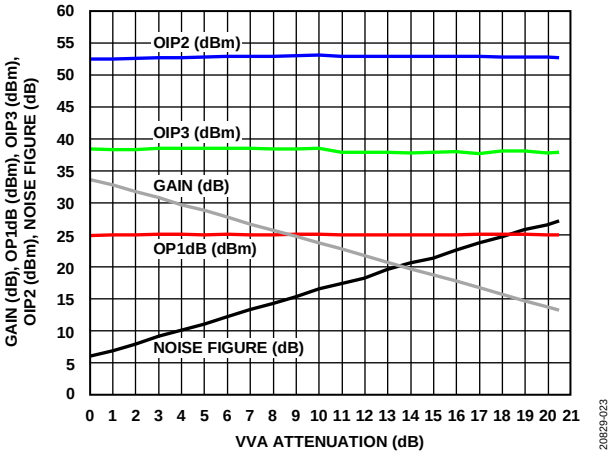

Figure 23. Gain, OP1dB, OIP3, OIP2, Noise Figure vs. VVA Attenuation, DSA Attenuation = 0 dB, Frequency = 2150 MHz

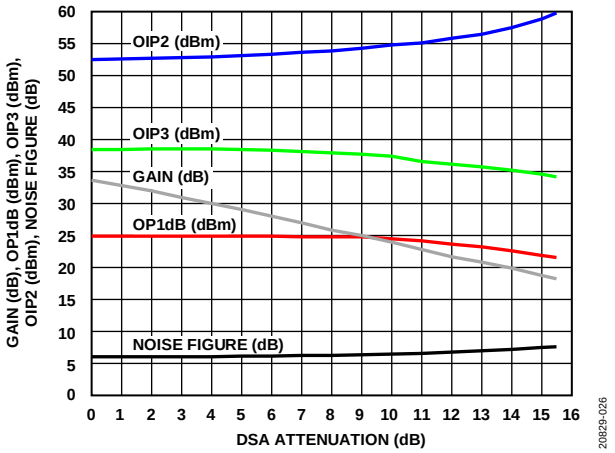

Figure 24. Gain, OP1dB, OIP3, OIP2, Noise Figure vs. DSA Attenuation, VVA Attenuation = 0 dB, Frequency = 2150 MHz

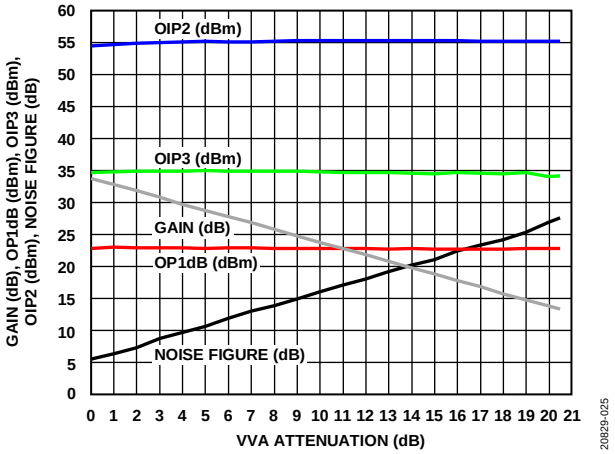

Figure 25. Gain, OP1dB, OIP3, OIP2, Noise Figure vs. VVA Attenuation, DSA Attenuation = 0 dB, Frequency = 2600 MHz

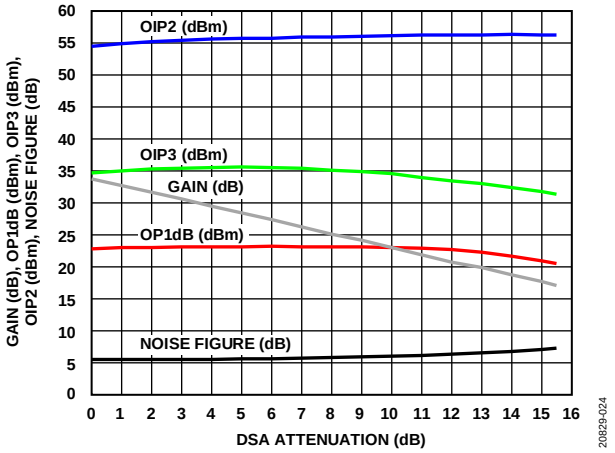

Figure 26. Gain, OP1dB, OIP3, OIP2, Noise Figure vs. DSA Attenuation, VVA Attenuation = 0 dB, Frequency = 2600 MHz

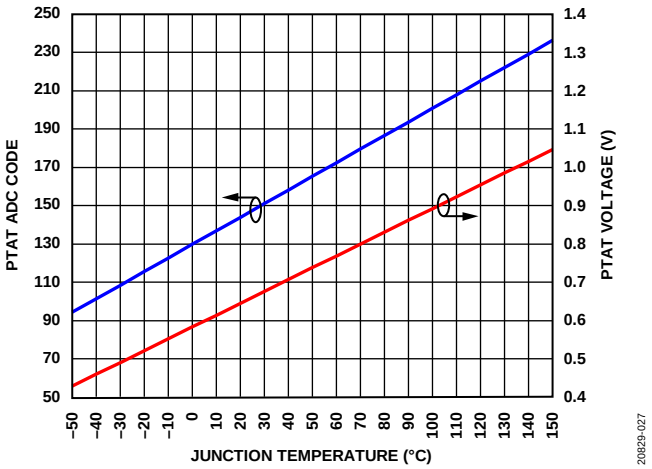

Figure 27. Proportional to Absolute Temperature (PTAT) ADC Code and PTAT Voltage vs. Junction Temperature

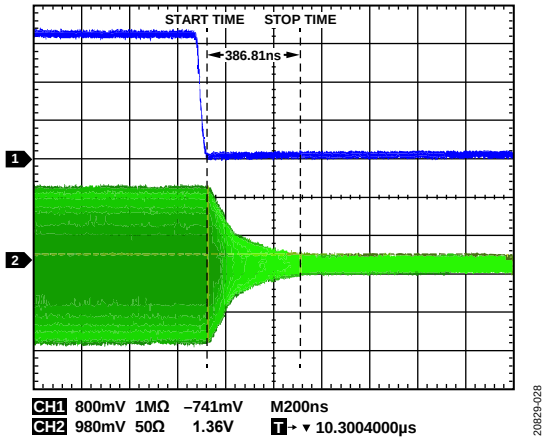

Figure 28. VVA Gain Settling Time, Minimum to Maximum VVA Attenuation

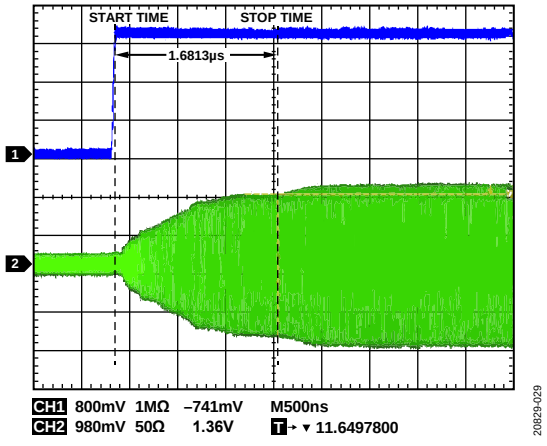

Figure 29. VVA Gain Settling Time, Maximum to Minimum VVA Attenuation

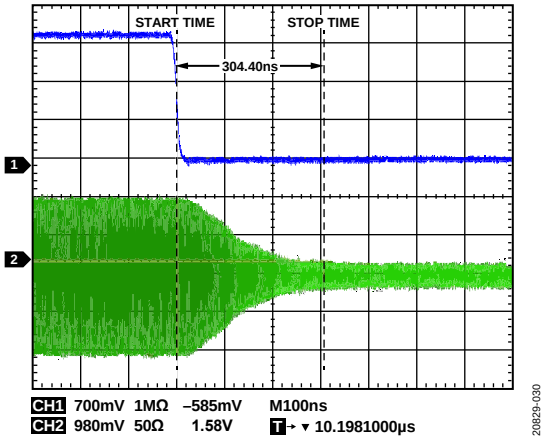

Figure 30. DSA Gain Settling Time, Minimum to Maximum DSA Attenuation

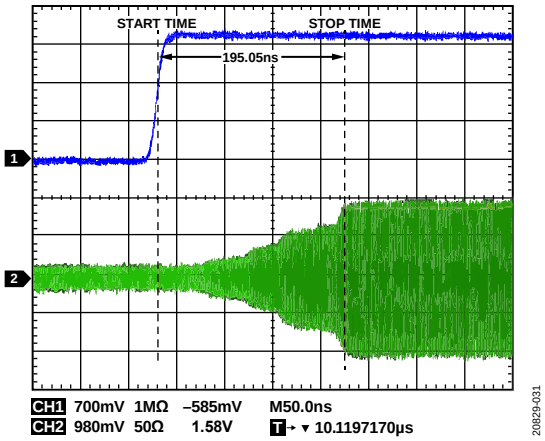

Figure 31. DSA Gain Settling Time, Maximum to Minimum DSA Attenuation

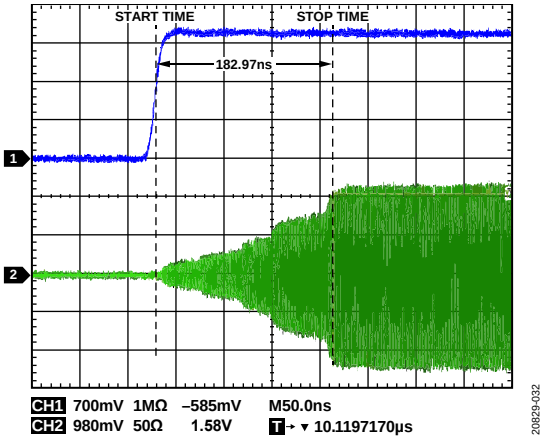

Figure 32. TXEN Response Time, Measured from Amplifier 1 and Amplifier 2 Disabled (DSA Attenuation = 15.5 dB) to Amplifier 1 and Amplifier 2 Enabled, (DSA Attenuation = 0 dB)

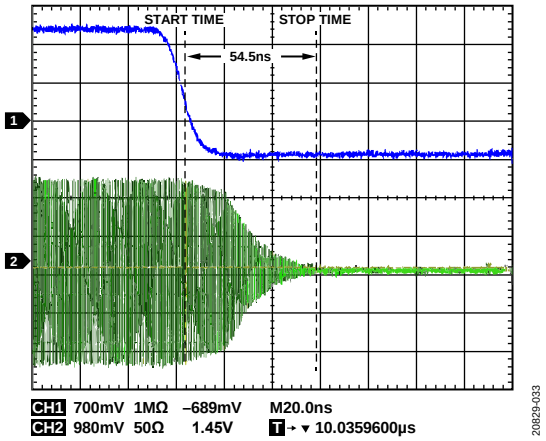

Figure 33. TXEN Response Time Measured from Amplifier 1 and Amplifier 2 Enabled (DSA = 0 dB) to Amplifier 1 and Amplifier 2 Disabled (DSA = 15.5 dB)

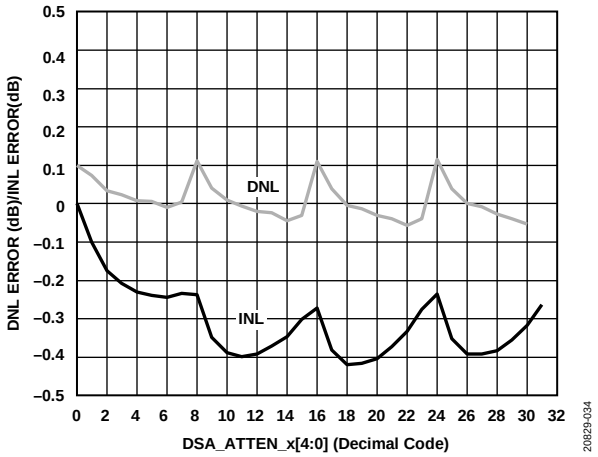

Figure 34. DSA Gain Step Error, Frequency = 1850 MHz

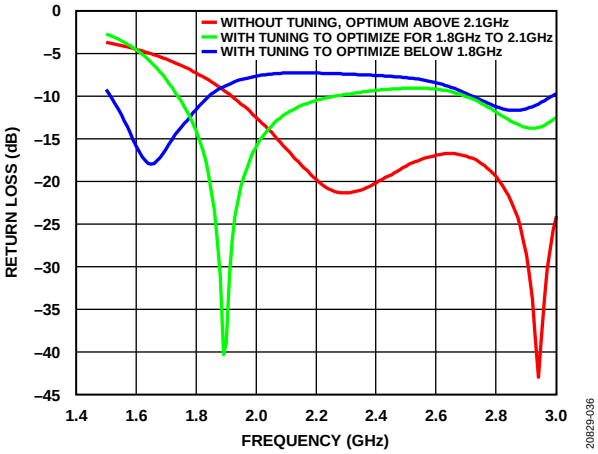

Figure 35. Return Loss of Differential RF Input S11 from 1.5 GHz to 3 GHz

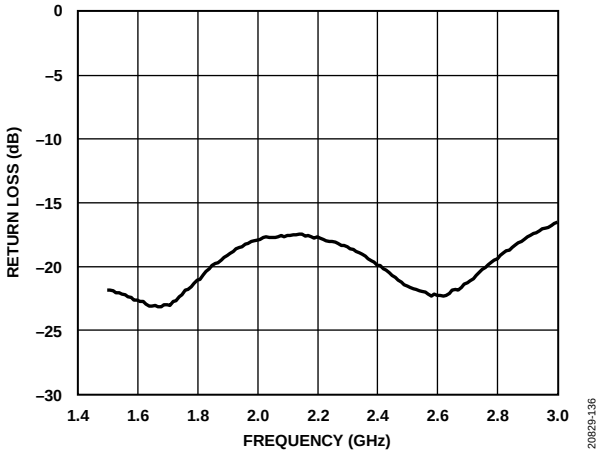

Figure 36. Return Loss of Single-Ended RF Output S22 from 1.5 GHz to 3 GHz

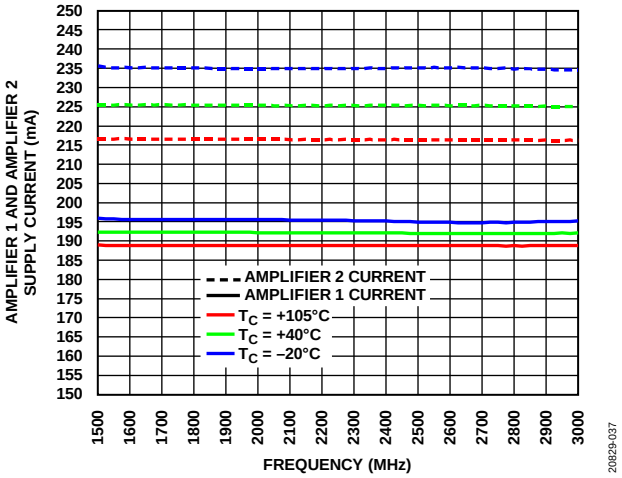

Figure 37. Amplifier 1 and Amplifier 2 Supply Current vs. Frequency for Various Temperatures

THEORY OF OPERATION

The ADL6317 is a highly integrated transmit VGA used to interface an RF DAC to the power amplifier in a transmitter. The ADL6317 targets high dynamic range multicarrier transmitter designs.

The ADL6317 offers multiple gain control options with an integrated 20.5 dB VVA, on-chip DAC control or external voltage control, a high linearity amplifier, an RF DSA with a 15.5 dB attenuation range in 0.5 dB steps, followed by the second stage high linearity amplifier.

Putting all the building blocks of the ADL6317 together, the signal path through the device starts with differential inputs converted to singled-ended by the integrated balun and this single-ended signal is then quadrature coupled by the internal quadrature hybrid.

Next, the integrated VVA, Amplifier 1, DSA, and Amplifier 2 optimize the RF signal amplitude for performance before the RF signal passes through the output quadrature hybrid. All the integrated building blocks of the ADL6317 are programmable via the SPI.

RF INPUT BALUN WITH DAC INTERFACE NETWORK

The ADL6317 converts a single-channel, 50 Ω, input differential signal to a single-ended signal via the integrated balun. Wideband matching allows the DAC to operate over a frequency range from 1500 MHz to 3000 MHz, and a bias tee is included to provide dc bias for the RF DAC.

QUADRATURE HYBRID

Integrated quadrature hybrids at the RF input and RF output allow wideband performance gain and match with a low input and output reflection coefficient to the RF DAC and PA.

RF SIGNAL CHAIN

The RF path includes a 20.5 dB VVA, the first stage of the fixed gain amplifier, a 15.5 dB DSA, and the second stage of the fixed gain amplifier (see Figure 38). The ADL6317 has two modes of control of the VVA attenuation: internal analog control using an integrated 12-bit DAC and external analog control. For internal control, use Register 0x104, Bits[3:0] and Register 0x103, Bits[7:0] to set the attenuation. The digital bits are double buffered to avoid major carrier glitch. For this reason, Register 0x104 must be written before Register 0x103. For external analog control of the VVA, a control voltage is applied to the VVA_ANALOG pin (Pin 30). Sample register writes for VVA control are shown in Figure 38.

Table 7. Register Writes for the Control of VVA

Address	Bits	Settings	Description
0x105	[1:0]	00	DAC to VVA
		10	VVA_ANALOG (Pin 30) to VVA
0x104	[3:0]	User defined	12-bit DAC code to set VVA attenuation; first, write to Register 0x104, Bits[3:0], and then to Register 0x103, Bits[7:0]
0x103	[7:0]	User defined	

Next, the fixed gain amplifier is used in a quadrature balanced configuration. The DSA provides a 15.5 dB range with 0.5 dB step resolution. The digital 5-bit DSA attenuation control is found in Bits[4:0] of Register 0x102 and Register 0x112. Finally, the second stage fixed gain amplifier is used in a quadrature balanced configuration.

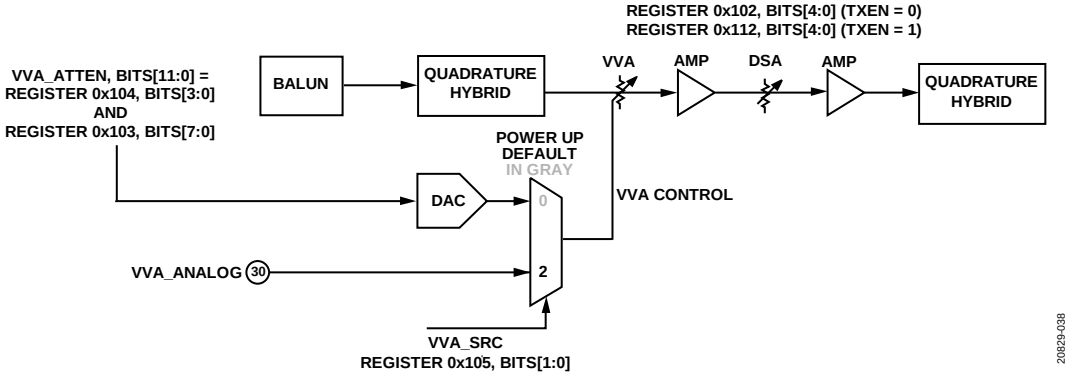

Figure 38. RF Signal Chain

BASIC CONNECTIONS

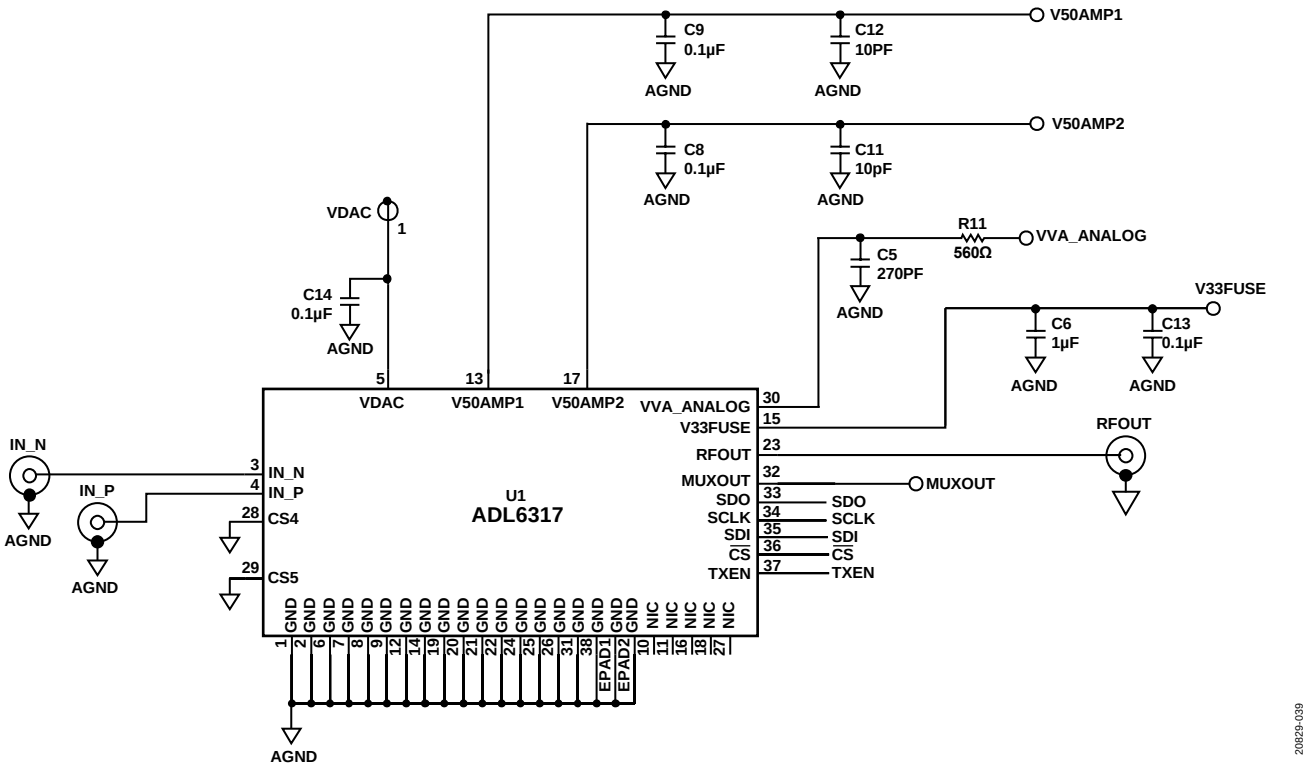

Figure 39. Basic Connections

Table 8. Basic Connections

Functional Blocks	Pin No.	Mnemonic	Description	Basic Connection
5 V	13, 17	V50AMP1, V50AMP2	Amplifier analog supply voltage, 5 V	Decouple these pins via 10 pF and 0.1 µF capacitors to ground. Ensure that the decoupling capacitors are located close to the pins.
Decoupling	15	V33FUSE	3.3 V LDO regulator decoupling	Decouple this pin via 0.1 µF and 1 µF capacitors to ground. Ensure that the decoupling capacitors are located close to the pin.
RF Inputs	5	VDAC	Supply voltage for external RF DAC	VDAC can be left open during operation without the RF DAC.
	3, 4	IN_N, IN_P	Differential RF inputs	Connect the IN_N and IN_P pins to an RF DAC or transceiver output in differential configuration.
VVA	30	VVA_ANALOG	External VVA control voltage input	Voltage input pin to control VVA attenuation.
RF Output	23	RFOUT	Single-ended RF output	Connect RF output to power meter, network analyzer, noise figure meter, or spectrum analyzer.
Serial Port	33	SDO	SPI data output	1.8 V to 3.3 V tolerant logic levels.
	34	SCLK	SPI clock	1.8 V to 3.3 V tolerant logic levels.
	35	SDI	SPI data input	1.8 V to 3.3 V tolerant logic levels.
	36	$\overline{CS}$	Chip select active low	1.8 V to 3.3 V tolerant logic levels.
Auxiliary Mux	32	MUXOUT	Mux output	Connect mux output to multimeter, oscilloscope, or spectrum analyzer.
Chip Selection	28, 29	CS4, CS5	Chip selection	Connect these pins to ground.
Mode Control	37	TXEN	Amplifier enable, DSA attenuation, and trim value selection	1.8 V to 3.3 V tolerant logic levels.
Ground	1, 2, 6 to 9, 12, 14, 19 to 22, 24 to 26, 31, 38	GND	Ground	Connect these pins to the ground of the PCB.
Exposed Pad	Not applicable	EPAD1, EPAD2	Exposed pads	The exposed thermal pads are on the bottom of the package. Solder the exposed pads to the PCB ground. EPAD1 and EPAD2 are internally connected to each other.

PROGRAMMABILITY GUIDE

Viewing the register map at the highest level, the registers are subdivided into the major functional blocks, as shown in Table 9. See the Register Summary section for a complete list of all the registers on the ADL6317.

Table 9. Memory Map Functional Groups

Register Address	Functional Blocks
0x000 to 0x011	Analog Devices, Inc., SPI configuration
0x100 to 0x101, 0x106	Signal path enable
0x103 to 0x105	VVA source, VVA attenuation
0x10B, 0x11B	Amplifier 2 optimization
0x102, 0x107 to 0x10A	DSA attenuation, amplifier enable, amplifier trim, TXEN = 0 mode
0x112, 0x117 to 0x11A	DSA attenuation, amplifier enable, amplifier trim, TXEN = 1 mode
0x120 to 0x121	Auxiliary mux selection, SPI supply control
0x127 to 0x129	ADC clock, temperature readback
0x146 to 0x148	VVA and DSA attenuation readback

SIGNAL PATH MODES

The ADL6317 has two signal path modes. This feature allows two predefined modes of operation to be controlled by TXEN, a real-time external pin with no SPI latency. Table 10 shows the hardware configuration to select the desired mode.

Table 10. Mode Selection and Setup Registers

TXEN (Pin 37)	Mode	Enable, Setup Register
0	TXEN = 0	0x102, 0x107 to 0x10A
1	TXEN = 1	0x112, 0x117 to 0x11A

The controls of each mode of operation reside in a designated subsection of the register map. Each operational mode includes individual control of the enables of the amplifier blocks, DSA attenuation, and power mode. Control of these functions reside in Register 0x102 and Register 0x107 to Register 0x10A for TXEN = 0 mode, or Register 0x112 and Register 0x117 to Register 0x11A for TXEN = 1 mode. The specific mode selected by the logic level on the TXEN pin (Pin 37) determines the state of the registers (see Table 11).

Table 11. Control Registers for the Modes

Register Address	Mode	Function Block
0x102	TXEN = 0	DSA attenuation
0x112	TXEN = 1	DSA attenuation
0x107	TXEN = 0	Amplifier 1 optimization
0x117	TXEN = 1	Amplifier 1 optimization
0x108	TXEN = 0	Amplifier 1 enable
0x118	TXEN = 1	Amplifier 1 enable
0x109	TXEN = 0	Amplifier 2 optimization
0x119	TXEN = 1	Amplifier 2 optimization
0x10A	TXEN = 0	Amplifier 2 enable
0x11A	TXEN = 1	Amplifier 2 enable

Signal Path Enable

The signal path enable bits are located in Register 0x100, Register 0x108, Register 0x118, Register 0x10A, and Register 0x11A. Figure 40 shows a breakdown of the individual blocks that the particular enable bit controls.

AUXILIARY MUX CONTROL

The ADL6317 has multiple auxiliary mux control blocks that allow various modes of operation and monitoring points (see Figure 41 and Table 12).

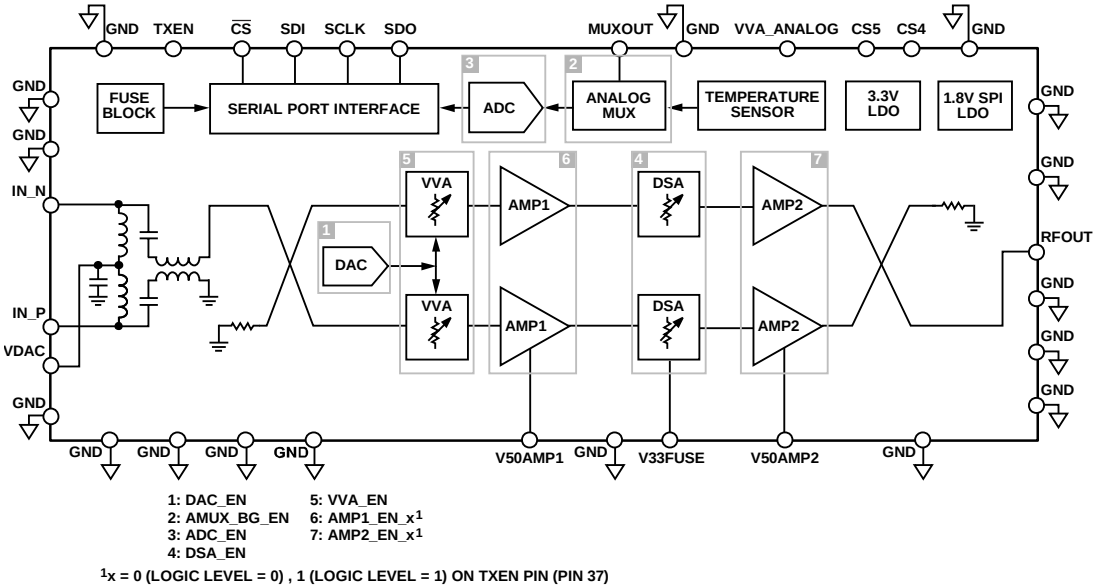

Figure 40. Signal Path Enable Block Diagram

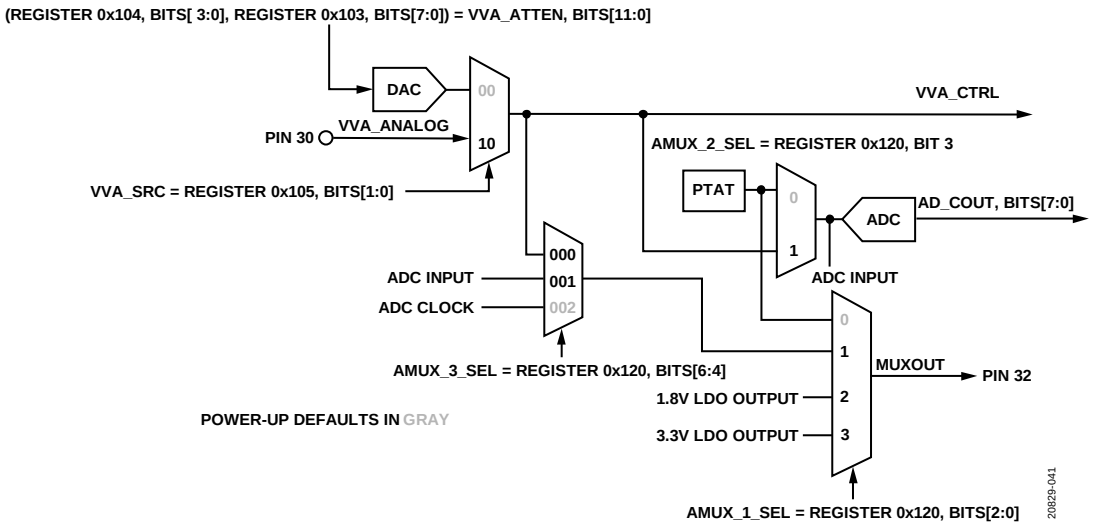

Figure 41. Auxiliary Mux Block Diagram

Table 12. Auxiliary Mux Programming Guide

Bit Name	Register Address	Setting	Description
AMUX_3_SEL	Register 0x120, Bits[6:4]		ADC input, VVA_CTRL, and ADC clock selection on mux. VVA_CTRL is the internal control voltage signal to control VVA attenuation.
		000	VVA_CTRL.
		001	ADC input.
		010	ADC clock.
		011	Not used.
		100	Not used.
		101	Not used.
		110	Not used.
		111	Not used.
AMUX_2_SEL	Register 0x120, Bit 3		ADC input selection.
		0	PTAT to ADC input.
		1	VVA_CTRL to ADC input.
AMUX_1_SEL	Register 0x120, Bits[2:0]		Select mux output.
		000	PTAT.
		001	Output of AMUX_3_SEL.
		010	1.8 V LDO output.
		011	3.3 V LDO output.
		100	GND.
		101	GND.
		110	Not used.
		111	Not used.

SERIAL PORT INTERFACE (SPI)

The SPI of the ADL6317 allows the user to configure the device for specific functions or operations via a 4-wire SPI port. This interface provides users with added flexibility and customization. The serial port interface consists of four control lines: SCLK, SDI, SDO, and $\overline{CS}$. The timing requirements for the SPI port are shown in Table 3.

The ADL6317 protocol consists of a read/write bit, six chip select ID bits, and nine register address bits, followed by eight data bits. Both the address and data fields are organized with the MSB first and end with the LSB by default.

The ADL6317 input logic level for the write cycle is with a 1.8 V logic level (see the digital logic parameter in Table 2).

On a read cycle, the SDO is configurable for 1.8 V (default) or 3.3 V output levels by setting SPI_1P8_3P3_CTRL bit (Register 0x121, Bit 4).

Multiple Chip Operation to Share SPI Bus

Multiple ADL6317 devices, up to four, can be addressed using the same 4-wire SPI, which means no extra $\overline{CS}$ line for each device. For this capability, the chip ID bits of the ADL6317 are reserved as the chip ID (see the SPI interface port as shown in Figure 2).

The ADL6317 ignores any writes to addresses where the six MSBs are not equal to the chip ID, with the exception of Register 0x000 to Register 0x00B. The ADL6317 always accepts writes for these registers regardless of the six MSBs of the address.

The ADL6317 only accepts reads for addresses where the six MSBs are equal to the chip ID, including Register 0x000 to Register 0x00B.

Figure 42 shows how to configure the chip ID and the CS5 and CS4 pins to share a 4-wire SPI. The CS5 and CS4 settings are shown in gray in Figure 42.

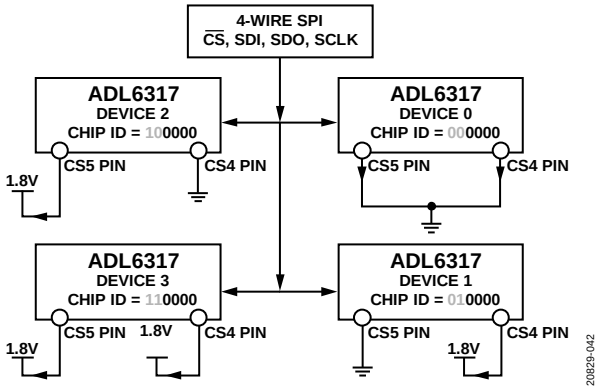

Figure 42. Multiple Chip Configuration to Share SPI Bus

DEVICE SETUP

The recommended sequence of steps to set up the ADL6317 is as follows:

1. Set up the SPI interface. See Table 13.
2. Set up the common parameters, including auxiliary mux control. See Table 14 and Table 15.
3. Set up the operating mode. See Table 16 to Table 19.
   a. Set the attenuation on the DSA.
   b. Enable or disable the amplifiers.
   c. Set the amplifier reference currents.
   d. Set the amplifier for linearity optimization.
   e. Measure the internal temperature.

Table 13. SPI Interface Setup

Address	Setting	Notes
0x000	0x99	Soft reset, MSB first, SDO active (4-wire SPI)
0x001	0x00	Single instruction, master/slave readback, soft reset, and master/slave transfer
0x00A	0x00	Scratch pad

Table 14. Signal Path Trim

Address	Setting	Description
0x100	0xFF	Enable the DAC, auxiliary mux band gap, ADC, bias generator, DSA, and VVA
0x101	0x01	Enable IP3 optimization and 3.3 V LDO regulator
0x106	0x00	Disable the bias current, I_{BIAS}, via the EN_IBIASGEN_RESISTOR bit (default setting)
0x105	0x00	VVA control source from DAC
0x104	0x0F	Attenuation of VVA at minimum attenuation, highest four bits of 12-bit word
0x103	0xFF	Attenuation of VVA at minimum attenuation, lowest eight bits of 12-bit word

Table 15. Auxiliary Mux Control

Address	Setting	Description
0x120	0x00	PTAT to ADC input, PTAT on mux output
0x121	0x00	Set SPI SDO voltage to 1.8 V

Table 16. Power-Down Mode Setup, TXEN = Logic Level 0

Address	Setting	Description
0x102	0x1F	15.5 dB attenuation on DSA
0x107	0x80	Set Amplifier 1 reference current, I_{REF} (TRM_AMP1_IREF_0), for low power mode
0x108	0x80	Disable Amplifier 1
0x109	0x80	Set Amplifier 2 I_{REF} (TRM_AMP2_IREF_0) for low power mode
0x10A	0x80	Disable Amplifier 2

Table 17. Normal Operating Mode Setup, TXEN = Logic Level 1

Address	Setting	Description
0x112	0x00	0 dB attenuation on DSA
0x117	0x82	Set Amplifier 1 I_{REF} (TRM_AMP1_IREF_1)
0x118	0x81	Enable Amplifier 1
0x119	0x82	Set Amplifier 2 I_{REF} (TRM_AMP2_IREF_1)
0x11A	0x81	Enable Amplifier 2

Table 18. Linearity Optimization

Address	Setting	Description
0x10B	0x02	Set the TRM_AMP2_CB bit
0x11B	0x02	Set the TRM_AMP2_IP3 bit

Table 19. Internal Temperature Measurement from ADC Conversion

Address	Setting	Description
0x000	0x18	Make SDO active
0x100	0xFF	Enable ADC
0x127	0x20	Enable ADC clock divider and set ADC clock frequency
0x120	0x00	PTAT to ADC input, PTAT on mux output
0x00A	0xCC	Register dummy write
0x00A	0xCC	Register dummy write
0x00A	0xCC	Register dummy write
0x00A	0xCC	Register dummy write
0x00A	0xCC	Register dummy write
0x129	Not applicable	Read temperature from ADC

APPLICATIONS INFORMATION

LINEARITY OPTIMIZATION

The linearity in the ADL6317 can be optimized through the TRM_AMP2_IP3 (Register 0x11B, Bits[1:0]) and TRM_AMP2_CB (Register 0x10B, Bits[1:0]) settings. Set the IP3_OFF bit (Register 0x101, Bit 1) 0x00 for OIP3 optimization. The TRM_AMP2_IP3 bits control the switches in the second amplifier that enables optimal third-order distortion cancellation and optimal OIP3. The TRM_AMP2_CB bits control the common base bias current on the transistor and allows additional linearity optimization.

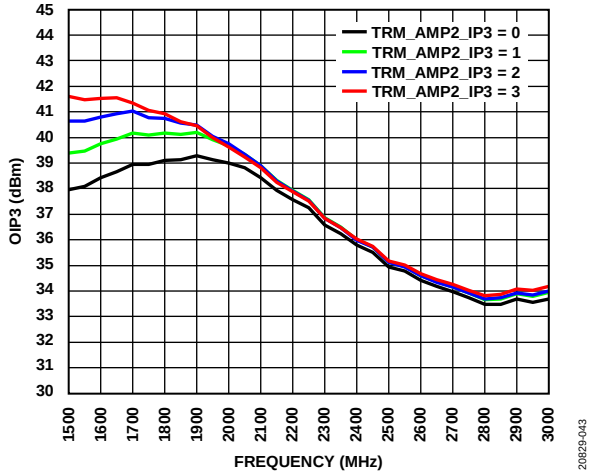

Figure 43. OIP3 vs. RF Frequency for Various TRM_AMP2_IP3 Settings, TRM_AMP2_CB = 0x02, TRM_AMP1_IREF_x and TRM_AMP2_IREF_x = 0x02

Figure 43 shows that the OIP3 is optimizable across the TRM_AMP2_IP3 settings.

Figure 43 shows better than 1.5 dB OIP3 improvement that correlates to 3 dB improvement on IMD3 performance at below 1.9 GHz through linearity optimization.

PERFORMANCE AND POWER OPTIMIZATION

The ADL6317 provides another level of control to optimize power or performance. In applications where performance is critical, the ADL6317 offers performance optimization at the expense of power consumption. However, if low power is the priority, the ADL6317 offers tuning options in the amplifier blocks of the chip to further reduce power consumption.

Table 20 shows that the potential power optimization vs. performance can fine tune the reference current on RF amplifier settings.

ADJACENT AND ALTERNATE CHANNEL POWER RATIOS ON LTE OPERATION

Figure 44 shows the adjacent and alternate channel power ratios (CPR) for the ADL6317 using 5 MHz single-carrier LTE. The adjacent CPR is −70.4 dB and the alternative CPR is −72.9 dB at an RF of 1850 MHz. The adjacent and alternate CPR performance varies over output power. On the ADL6317, the output power can be varied by adjusting the input power, the VVA attenuation, or the DSA attenuation. Figure 45 to Figure 47 show the adjacent and alternate CPR performance vs. output power for the different methods of controlling the ADL6317.

As shown in Figure 45, the optimum adjacent and alternate CPR can be achievable at an output power of +8 dBm, which corresponds to an input power of −24.6 dBm driving the ADL6317 where the internal VVA is set to 0 dB, and the DSA is set to 0 dB attenuation. Figure 46 and Figure 47 show adjacent and alternate CPR performance vs. output power that is adjusted by VVA attenuation and by DSA attenuation, respectively, with −17.2 dBm of input power. Figure 45 to Figure 47 show below −65 dB adjacent and alternate CPR performance at below +10 dBm output power, and there is gradual degradation above +10 dBm from the contribution to the adjacent and alternate CPR performance of the second stage RF amplifier. When fixing the VVA attenuation and sweeping the DSA, the adjacent and alternate CPR performance remains constant below 6 dBm output power (see Figure 47).

Table 20. Power Optimization vs. Performance at 1850 MHz, VVA Attenuation= 0 dB, DSA Attenuation = 0 dB, TRM_AMP2_IP3 = 0x02

TRM_AMPx_IREF_1 Setting (Decimal), Register 0x117 and Register 0x119, Bits[3:0]	DC Power (W)	Gain (dB)	OP1dB (dBm)	OIP3 (dBm)	NF (dB)
3	2.36	33.1	25.8	40.3	6.6
2	2.10	33.1	25.6	40.3	5.9
1	1.84	33.1	25.1	39.2	5.8
0	1.55	32.8	24.3	36.9	5.8

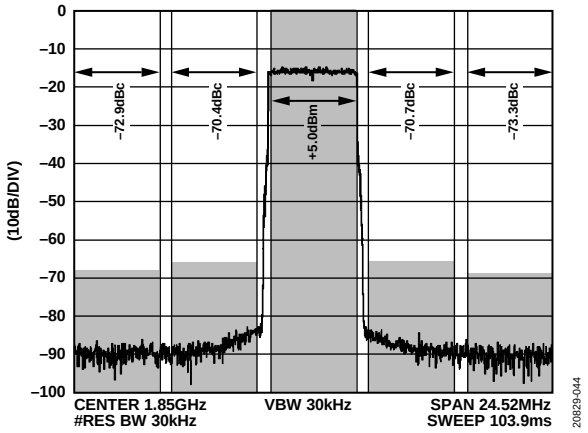

Figure 44. LTE Carrier, Adjacent and Alternate CPR at 1850 MHz, VVA Attenuation = 0 dB, DSA Attenuation = 11 dB, P_{IN} = −17.2 dBm

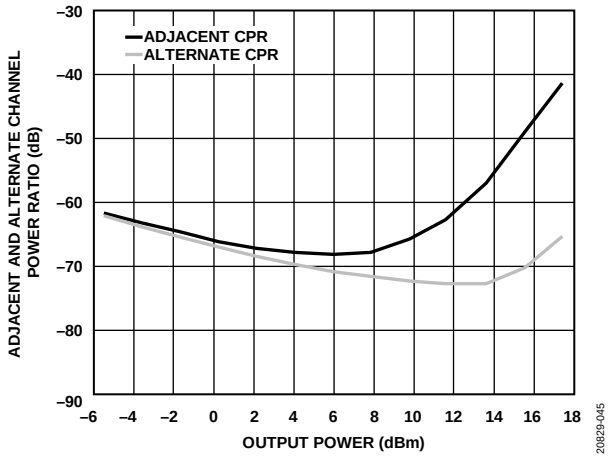

Figure 45. Adjacent and Alternate Channel Power Ratio vs. Output Power (P_{OUT}) by P_{IN} at 1850 MHz, LTE Test Model 1.1 (TM1.1), VVA Attenuation = 0 dB, DSA Attenuation = 0 dB

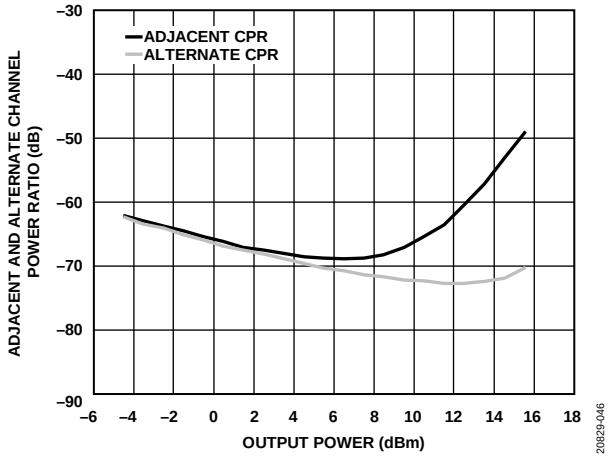

Figure 46. Adjacent and Alternate Channel Power Ratio vs. Output Power (P_{OUT}) by VVA Attenuation at 1850 MHz, LTE TM1.1, P_{IN} = −17.2 dBm, DSA Attenuation = 0 dB

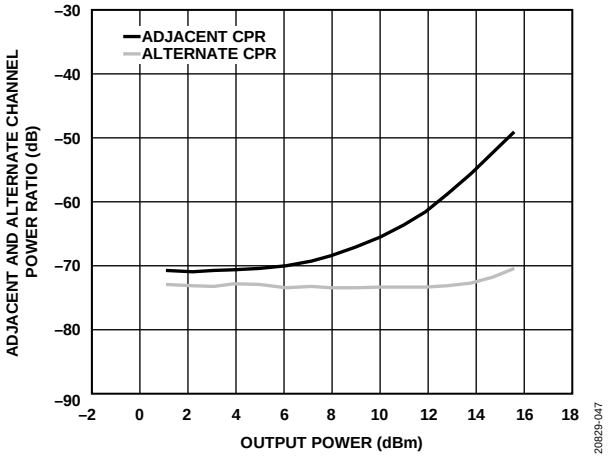

Figure 47. Adjacent and Alternate Channel Power Ratio vs. Output Power (P_{OUT}) by DSA Attenuation at 1850 MHz, LTE TM1.1, P_{IN} = −17.2 dBm, VVA Attenuation = 0 dB

LAYOUT

Solder the exposed pad on the underside of the ADL6317 to a low thermal and electrical impedance ground plane. This pad is typically soldered to an exposed opening in the solder mask on the evaluation board. Notice the use of 19 via holes on the exposed pad of the ADL6317-EVALZ evaluation board. Connect these ground vias to all other ground layers on the evaluation board to maximize heat dissipation from the device package. For more information on the ADL6317-EVALZ evaluation board, contact Analog Devices, Inc.

Ensure that the decoupling capacitors are located close to the supply voltage pins.

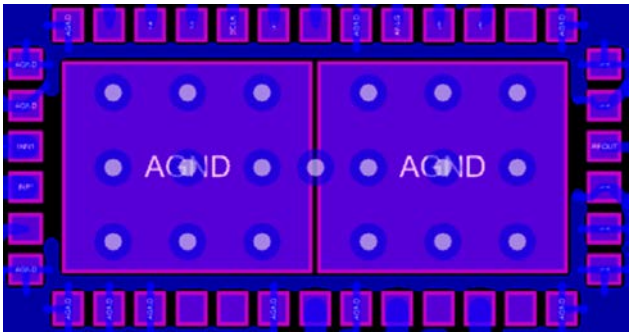

Figure 48. Evaluation Board Layout for the ADL6317-EVALZ

CHARACTERIZATION SETUPS

The primary setup used to characterize the ADL6317 is shown in Figure 49. The setup measures gain, HD2, HD3, OIP2, and OIP3.

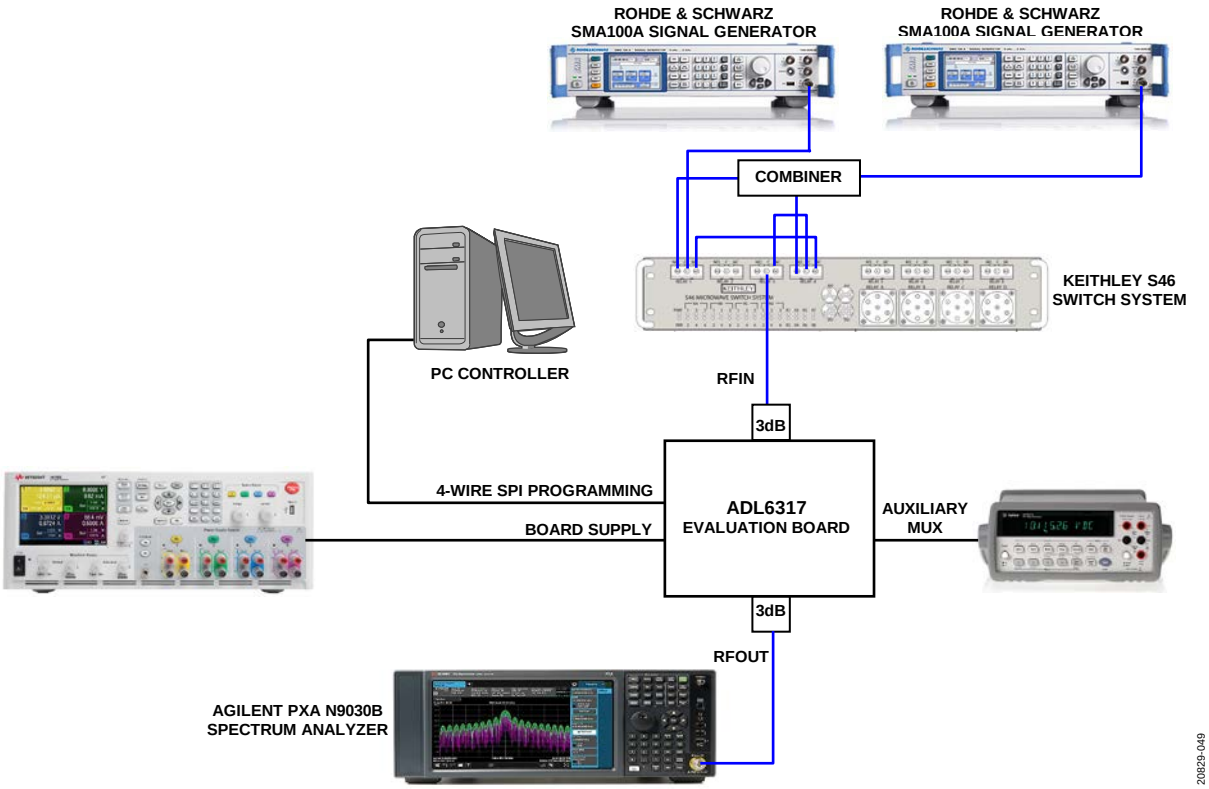

Figure 49. General Characterization Setup

REGISTER SUMMARY

Table 21. Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x000	ADI_SPI_CONFIG	[7:0]	SOFTRESET_	LSB_FIRST_	ENDIAN_	SDOACTIVE_	SDOACTIVE	ENDIAN	LSB_FIRST	SOFTRESET	0x00	R/W
0x001	REG_0X0001	[7:0]	SINGLE_INSTRUCTION	CSB_STALL	MASTER_SLAVE_RB	RESERVED		SOFT_RESET		MASTER_SLAVE_TRANSFER	0x00	R/W
0x003	CHIPTYPE	[7:0]	CHIPTYPE								0x00	R
0x004	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x00	R
0x005	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x00A	SCRATCHPAD	[7:0]	SCRATCHPAD								0x00	R/W
0x00B	SPI_REV	[7:0]	SPI_REV								0x00	R
0x010	VARIANT_FEOL	[7:0]	FEOL				VARIANT				0x00	R
0x011	BEOL_SIF	[7:0]	SIF				BEOL				0x01	R
0x012	SPARE_012	[7:0]	SPARE_012								0x00	R
0x013	SPARE_013	[7:0]	SPARE_013								0x00	R
0x100	SIG_PATH0_0	[7:0]	DAC_EN	AMUX_BG_EN	ADC_EN	EN_IBIASGEN	DSA_EN	VVA_EN	RESERVED		0x40	R/W
0x101	SIG_PATH1_0	[7:0]	RESERVED						IP3_OFF	LDO33_EN	0x01	R/W
0x102	SIG_PATH2_0	[7:0]	RESERVED			DSA_ATTEN_0					0x3F	R/W
0x103	SIG_PATH3_0	[7:0]	VVA_ATTEN[7:0]								0x00	R/W
0x104	SIG_PATH4_0	[7:0]	RESERVED			VVA_ATTEN[11:8]					0x00	R/W
0x105	SIG_PATH5_0	[7:0]	RESERVED						VVA_SRC		0x00	R/W
0x106	SIG_PATH6_0	[7:0]	RESERVED							EN_IBIASGEN_RESISTOR	0x00	R/W
0x107	SIG_PATH7_0	[7:0]	BYPASS_TRM_AMP1_IREF_0	RESERVED		TRM_AMP1_IREF_SEL_0	TRM_AMP1_IREF_0				0x00	R/W
0x108	SIG_PATH8_0	[7:0]	BYPASS_TRM_AMP1_EN_0	RESERVED						AMP1_EN_0	0x00	R/W
0x109	SIG_PATH9_0	[7:0]	BYPASS_TRM_AMP2_IREF_0	RESERVED		TRM_AMP2_IREF_SEL_0	TRM_AMP2_IREF_0				0x00	R/W
0x10A	SIG_PATHA_0	[7:0]	BYPASS_TRM_AMP2_EN_0	RESERVED						AMP2_EN_0	0x00	R/W
0x10B	SIG_PATHB_0	[7:0]	SPARE_10B						TRM_AMP2_CB		0x00	R/W
0x112	SIG_PATH2_1	[7:0]	RESERVED			DSA_ATTEN_1					0x20	R/W
0x117	SIG_PATH7_1	[7:0]	BYPASS_TRM_AMP1_IREF_1	RESERVED		TRM_AMP1_IREF_SEL_1	TRM_AMP1_IREF_1				0x00	R/W
0x118	SIG_PATH8_1	[7:0]	BYPASS_TRM_AMP1_EN_1	RESERVED						AMP1_EN_1	0x00	R/W
0x119	SIG_PATH9_1	[7:0]	BYPASS_TRM_AMP2_IREF_1	RESERVED		TRM_AMP2_IREF_SEL_1	TRM_AMP2_IREF_1				0x00	R/W
0x11A	SIG_PATHA_1	[7:0]	BYPASS_TRM_AMP2_EN_1	RESERVED						AMP2_EN_1	0x00	R/W
0x11B	SIG_PATHB_1	[7:0]	SPARE_11B						TRM_AMP2_IP3		0x00	R/W
0x120	AMUX_SEL	[7:0]	RESERVED	AMUX_3_SEL			AMUX_2_SEL	AMUX_1_SEL			0x20	R/W
0x121	MULTI_FUNC_CTRL_0111	[7:0]	RESERVED			SPI_1P8_3P3_CTRL	AMUX_EX				0x00	R/W
0x127	ADC_CONTROL_	[7:0]	RESERVED		ADC_CLOCK_DIV_EN	ADC_MUX_SEL	RESERVED	ADC_CLK_FREQ			0x00	R/W
0x128	ADC_EOC	[7:0]	RESERVED							ADC_EOC	0x00	R
0x129	ADC_OUT	[7:0]	TEMP_ADC_OUT								0x00	R
0x146	GENERIC_READBACK_2	[7:0]	VVA_ATTEN_RDBK[7:0]								0x00	R
0x147	GENERIC_READBACK_3	[7:0]	RESERVED			VVA_ATTEN_RDBK[11:8]					0x00	R
0x148	GENERIC_READBACK_4	[7:0]	RESERVED		DSA_ATTEN_RDBK						0x00	R

REGISTER DETAILS

Address: 0x000, Reset: 0x00, Name: ADI_SPI_CONFIG

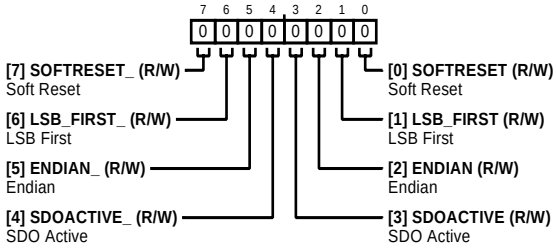

Table 22. Bit Descriptions for ADI_SPI_CONFIG

Bits	Bit Name	Description	Reset	Access
7	SOFTRESET_	Soft Reset. 0: Reset not asserted. 1: Reset asserted.	0x0	R/W
6	LSB_FIRST_	LSB First. 0: MSB first. 1: LSB first.	0x0	R/W
5	ENDIAN_	Endian. 0: Little endian. 1: Big endian.	0x0	R/W
4	SDOACTIVE_	SDO Active. 0: SDO inactive. 1: SDO active.	0x0	R/W
3	SDOACTIVE	SDO Active. 0: SDO inactive. 1: SDO active.	0x0	R/W
2	ENDIAN	Endian. 0: Little endian. 1: Big endian.	0x0	R/W
1	LSB_FIRST	LSB First. 0: MSB first. 1: LSB first.	0x0	R/W
0	SOFTRESET	Soft Reset. 0: Reset not asserted. 1: Reset asserted.	0x0	R/W

Address: 0x001, Reset: 0x00, Name: REG_0X0001

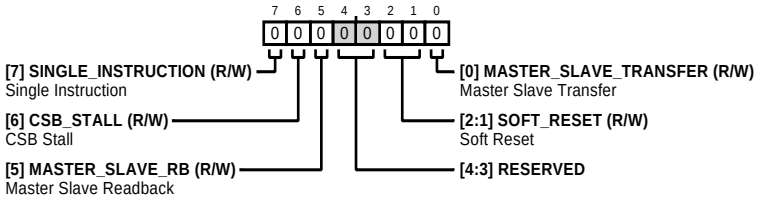

Table 23. Bit Descriptions for REG_0X0001

Bits	Bit Name	Description	Reset	Access
7	SINGLE_INSTRUCTION	Single Instruction	0x0	R/W
6	CSB_STALL	$\overline{CS}$ Stall	0x0	R/W
5	MASTER_SLAVE_RB	Master Slave Readback	0x0	R/W
[4:3]	RESERVED	Reserved	0x0	R
[2:1]	SOFT_RESET	Soft Reset	0x0	R/W
0	MASTER_SLAVE_TRANSFER	Master Slave Transfer	0x0	R/W

Address: 0x003, Reset: 0x00, Name: CHIPTYPE

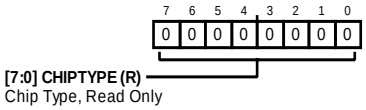

Table 24. Bit Descriptions for CHIPTYPE

Bits	Bit Name	Description	Reset	Access
[7:0]	CHIPTYPE	Chip Type, Read Only	0x0	R

Address: 0x004, Reset: 0x00, Name: PRODUCT_ID_L

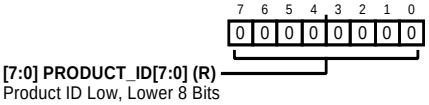

Table 25. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product ID Low, Lower 8 Bits	0x0	R

Address: 0x005, Reset: 0x00, Name: PRODUCT_ID_H

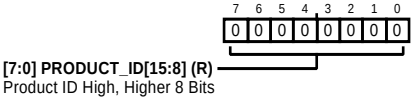

Table 26. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product ID High, Higher 8 Bits	0x0	R

Address: 0x00A, Reset: 0x00, Name: SCRATCHPAD

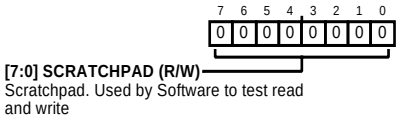

Table 27. Bit Descriptions for SCRATCHPAD

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCHPAD	Scratchpad. Used by Software to test read and write.	0x0	R/W

Address: 0x00B, Reset: 0x00, Name: SPI_REV

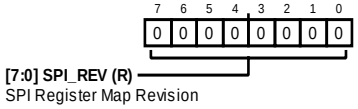

Table 28. Bit Descriptions for SPI_REV

Bits	Bit Name	Description	Reset	Access
[7:0]	SPI_REV	SPI Register Map Revision	0x0	R

Address: 0x010, Reset: 0x00, Name: VARIANT_FEOL

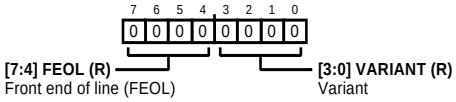

Table 29. Bit Descriptions for VARIANT_FEOL

Bits	Bit Name	Description	Reset	Access
[7:4]	FEOL	Front end of line (FEOL)	0x0	R
[3:0]	VARIANT	Variant	0x0	R

Address: 0x011, Reset: 0x01, Name: BEOL_SIF

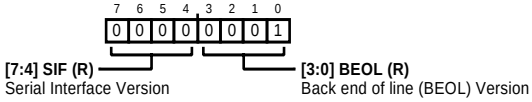

Table 30. Bit Descriptions for BEOL_SIF

Bits	Bit Name	Description	Reset	Access
[7:4]	SIF	Serial Interface Version	0x0	R
[3:0]	BEOL	Back end of line (BEOL) Version	0x1	R

Address: 0x012, Reset: 0x00, Name: SPARE_0012

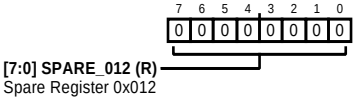

Table 31. Bit Descriptions for SPARE_0012

Bits	Bit Name	Description	Reset	Access
[7:0]	SPARE_012	Spare Register 0x012	0x0	R

Address: 0x013, Reset: 0x00, Name: SPARE_013

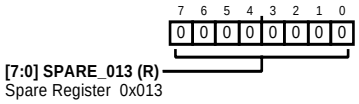

Table 32. Bit Descriptions for SPARE_013

Bits	Bit Name	Description	Reset	Access
[7:0]	SPARE_013	Spare Register 0x013	0x0	R

Address: 0x100, Reset: 0x40, Name: SIG_PATH0_0

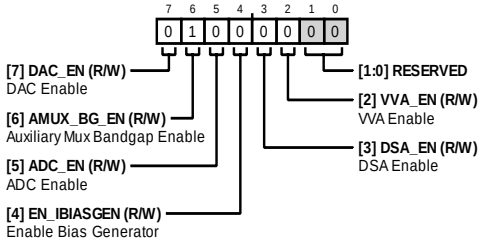

Table 33. Bit Descriptions for SIG_PATH0_0

Bits	Bit Name	Description	Reset	Access
7	DAC_EN	DAC Enable. 0: Disable DAC. 1: Enable DAC.	0x0	R/W
6	AMUX_BG_EN	Auxiliary Mux Band Gap Enable. 0: Disable auxiliary mux band gap. 1: Enable auxiliary mux band gap.	0x1	R/W
5	ADC_EN	ADC Enable. 0: Disable ADC. 1: Enable ADC.	0x0	R/W
4	EN_IBIASGEN	Enable Bias Generator. 0: Disable bias generator. 1: Enable bias generator.	0x0	R/W
3	DSA_EN	DSA Enable. 0: Disable DSA. 1: Enable DSA.	0x0	R/W
2	VVA_EN	VVA Enable. 0: Disable VVA. 1: Enable VVA.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Address: 0x101, Reset: 0x01, Name: SIG_PATH1_0

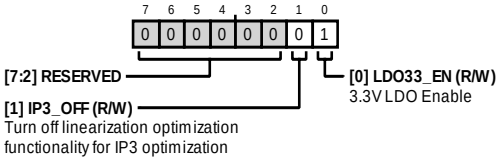

Table 34. Bit Descriptions for SIG_PATH1_0

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved.	0x0	R
1	IP3_OFF	Turn off linearization optimization functionality for IP3 optimization. 0: Turn on linearization optimization functionality. 1: Turn off linearization optimization functionality.	0x0	R/W
0	LDO33_EN	3.3 V LDO Enable. 0: Disable 3.3 V LDO. 1: Enable 3.3 V LDO.	0x1	R/W

Address: 0x102, Reset: 0x3F, Name: SIG_PATH2_0

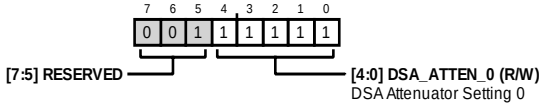

Table 35. Bit Descriptions for SIG_PATH2_0

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x1	R
[4:0]	DSA_ATTEN_0	DSA Attenuator Setting 0. 0: 0 dB. 1: 0.5 dB. 10: 1 dB. 11: 1.5 dB. 100: 2 dB. 101: 2.5 dB. 110: 3 dB. 111: 3.5 dB. 1000: 4 dB. 1001: 4.5 dB. 1010: 5 dB. 1011: 5.5 dB. 1100: 6 dB. 1101: 6.5 dB. 1110: 7 dB. 1111: 7.5 dB. 10000: 8 dB. 10001: 8.5 dB. 10010: 9 dB. 10011: 9.5 dB. 10100: 10 dB. 10101: 10.5 dB. 10110: 11 dB. 10111: 11.5 dB.	0x1F	R/W

Bits	Bit Name	Description	Reset	Access
		11000: 12 dB. 11001: 12.5 dB. 11010: 13 dB. 11011: 13.5 dB. 11100: 14 dB. 11101: 14.5 dB. 11110: 15 dB. 11111: 15.5 dB.		

Address: 0x103, Reset: 0x00, Name: SIG_PATH3_0

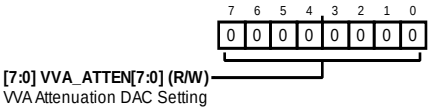

Table 36. Bit Descriptions for SIG_PATH3_0

Bits	Bit Name	Description	Reset	Access
[7:0]	VVA_ATTEN[7:0]	VVA Attenuation DAC Setting	0x0	R/W

Address: 0x104, Reset: 0x00, Name: SIG_PATH4_0

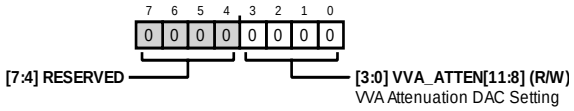

Table 37. Bit Descriptions for SIG_PATH4_0

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved	0x0	R
[3:0]	VVA_ATTEN[11:8]	VVA Attenuation DAC Setting	0x0	R/W

Address: 0x105, Reset: 0x00, Name: SIG_PATH5_0

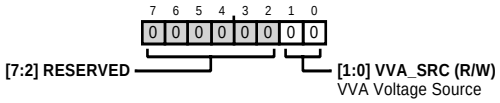

Table 38. Bit Descriptions for SIG_PATH5_0

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved	0x0	R
[1:0]	VVA_SRC	VVA Voltage Source 00: DAC to VVA 10: Pin 30 to VVA	0x0	R/W

Address: 0x106, Reset: 0x00, Name: SIG_PATH6_0

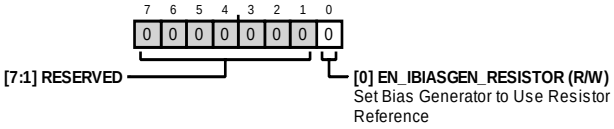

Table 39. Bit Descriptions for SIG_PATH6_0

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved	0x0	R
0	EN_IBIASGEN_RESISTOR	Set Bias Generator to Use Resistor Reference 0: Disable I_{BIAS} 1: Enable I_{BIAS}	0x0	R/W

Address: 0x107, Reset: 0x00, Name: SIG_PATH7_0

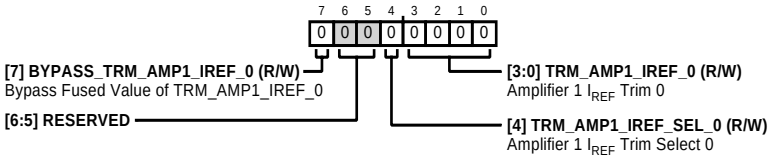

Table 40. Bit Descriptions for SIG_PATH7_0

Bits	Bit Name	Description	Reset	Access
7	BYPASS_TRM_AMP1_IREF_0	Bypass Fused Value of TRM_AMP1_IREF_0	0x0	R/W
[6:5]	RESERVED	Reserved	0x0	R
4	TRM_AMP1_IREF_SEL_0	Amplifier 1 I_{REF} Trim Select 0	0x0	R/W
[3:0]	TRM_AMP1_IREF_0	Amplifier 1 I_{REF} Trim 0	0x0	R/W

Address: 0x108, Reset: 0x00, Name: SIG_PATH8_0

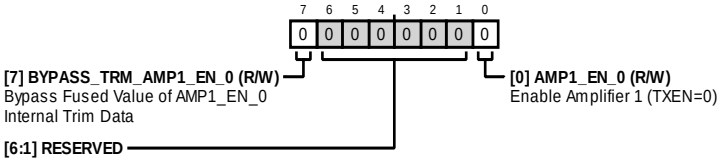

Table 41. Bit Descriptions for SIG_PATH8_0

Bits	Bit Name	Description	Reset	Access
7	BYPASS_TRM_AMP1_EN_0	Bypass Fused Value of AMP1_EN_0 Internal Trim Data	0x0	R/W
[6:1]	RESERVED	Reserved	0x0	R
0	AMP1_EN_0	Enable Amplifier 1 (TXEN = 0)	0x0	R/W

Address: 0x109, Reset: 0x00, Name: SIG_PATH9_0

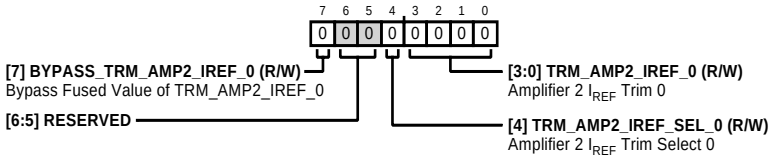

Table 42. Bit Descriptions for SIG_PATH9_0

Bits	Bit Name	Description	Reset	Access
7	BYPASS_TRM_AMP2_IREF_0	Bypass Fused Value of TRM_AMP2_IREF_0	0x0	R/W
[6:5]	RESERVED	Reserved	0x0	R
4	TRM_AMP2_IREF_SEL_0	Amplifier 2 I_{REF} Trim Select 0	0x0	R/W
[3:0]	TRM_AMP2_IREF_0	Amplifier 2 I_{REF} Trim 0	0x0	R/W

Address: 0x10A, Reset: 0x00, Name: SIG_PATHA_0

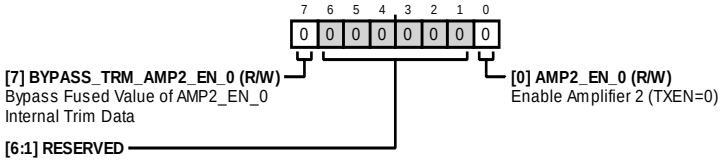

Table 43. Bit Descriptions for SIG_PATHA_0

Bits	Bit Name	Description	Reset	Access
7	BYPASS_TRM_AMP2_EN_0	Bypass Fused Value of AMP2_EN_0 Internal Trim Data	0x0	R/W
[6:1]	RESERVED	Reserved	0x0	R
0	AMP2_EN_0	Enable Amplifier 2 (TXEN = 0)	0x0	R/W

Address: 0x10B, Reset: 0x00, Name: SIG_PATHB_0

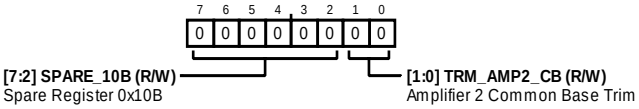

Table 44. Bit Descriptions for SIG_PATHB_0

Bits	Bit Name	Description	Reset	Access
[7:2]	SPARE_10B	Spare Register 0x10B	0x0	R/W
[1:0]	TRM_AMP2_CB	Amplifier 2 Common Base Trim	0x0	R/W

Address: 0x112, Reset: 0x20, Name: SIG_PATH2_1

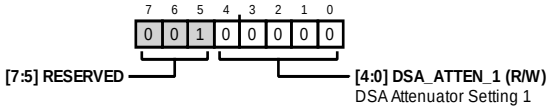

Table 45. Bit Descriptions for SIG_PATH2_1

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x1	R
[4:0]	DSA_ATTEN_1	DSA Attenuator Setting 1. 0: 0 dB. 1: 0.5 dB. 10: 1 dB. 11: 1.5 dB. 100: 2 dB. 101: 2.5 dB. 110: 3 dB. 111: 3.5 dB. 1000: 4 dB. 1001: 4.5 dB. 1010: 5 dB. 1011: 5.5 dB. 1100: 6 dB. 1101: 6.5 dB. 1110: 7 dB. 1111: 7.5 dB. 10000: 8 dB. 10001: 8.5 dB. 10010: 9 dB. 10011: 9.5 dB. 10100: 10 dB. 10101: 10.5 dB. 10110: 11 dB. 10111: 11.5 dB. 11000: 12 dB. 11001: 12.5 dB. 11010: 13 dB. 11011: 13.5 dB. 11100: 14 dB. 11101: 14.5 dB. 11110: 15 dB. 11111: 15.5 dB.	0x0	R/W

Address: 0x117, Reset: 0x00, Name: SIG_PATH7_1

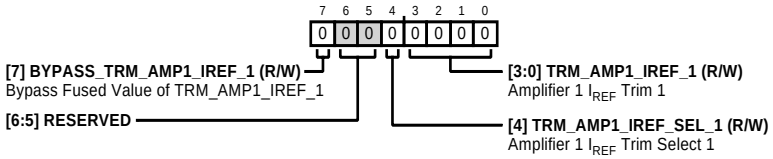

Table 46. Bit Descriptions for SIG_PATH7_1

Bits	Bit Name	Description	Reset	Access
7	BYPASS_TRM_AMP1_IREF_1	Bypass Fused Value of TRM_AMP1_IREF_1	0x0	R/W
[6:5]	RESERVED	Reserved	0x0	R
4	TRM_AMP1_IREF_SEL_1	Amplifier 1 I_{REF} Trim Select 1	0x0	R/W
[3:0]	TRM_AMP1_IREF_1	Amplifier 1 I_{REF} Trim 1	0x0	R/W

Address: 0x118, Reset: 0x00, Name: SIG_PATH8_1

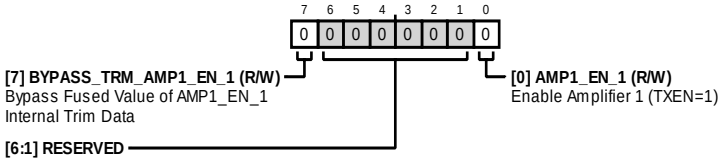

Table 47. Bit Descriptions for SIG_PATH8_1

Bits	Bit Name	Description	Reset	Access
7	BYPASS_TRM_AMP1_EN_1	Bypass Fused Value of AMP1_EN_1 Internal Trim Data	0x0	R/W
[6:1]	RESERVED	Reserved	0x0	R
0	AMP1_EN_1	Enable Amplifier 1 (TXEN = 1)	0x0	R/W

Address: 0x119, Reset: 0x00, Name: SIG_PATH9_1

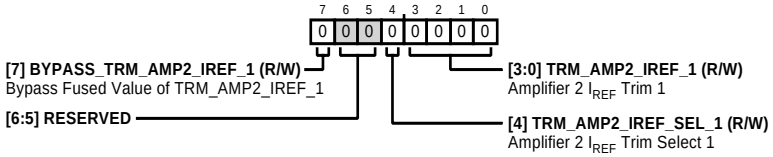

Table 48. Bit Descriptions for SIG_PATH9_1

Bits	Bit Name	Description	Reset	Access
7	BYPASS_TRM_AMP2_IREF_1	Bypass Fused Value of TRM_AMP2_IREF_1	0x0	R/W
[6:5]	RESERVED	Reserved	0x0	R
4	TRM_AMP2_IREF_SEL_1	Amplifier 2 I_{REF} Trim Select 1	0x0	R/W
[3:0]	TRM_AMP2_IREF_1	Amplifier 2 I_{REF} Trim 1	0x0	R/W

Address: 0x11A, Reset: 0x00, Name: SIG_PATHA_1

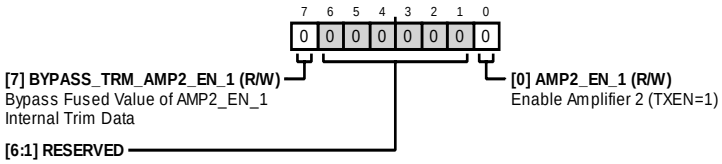

Table 49. Bit Descriptions for SIG_PATHA_1

Bits	Bit Name	Description	Reset	Access
7	BYPASS_TRM_AMP2_EN_1	Bypass Fused Value of AMP2_EN_1 Internal Trim Data	0x0	R/W
[6:1]	RESERVED	Reserved	0x0	R
0	AMP2_EN_1	Enable Amplifier 2 (TXEN = 1)	0x0	R/W

Address: 0x11B, Reset: 0x00, Name: SIG_PATHB_1

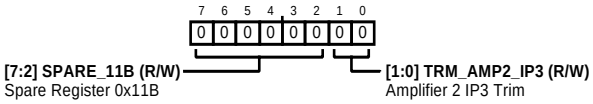

Table 50. Bit Descriptions for SIG_PATHB_1

Bits	Bit Name	Description	Reset	Access
[7:2]	SPARE_11B	Spare Register 0x11B	0x0	R/W
[1:0]	TRM_AMP2_IP3	Amplifier 2 IP3 Trim 00: Trim Mode 0 01: Trim Mode 1 10: Trim Mode 2 11: Trim Mode 3	0x0	R/W

Address: 0x120, Reset: 0x20, Name: AMUX_SEL

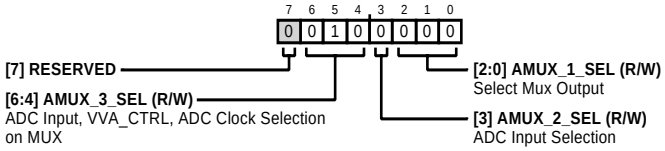

Table 51. Bit Descriptions for AMUX_SEL

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R/W
[6:4]	AMUX_3_SEL	ADC Input, VVA_CTRL, ADC Clock Selection on Mux. 000: VVA_CTRL. 001: ADC input. 010: ADC clock. 011 to 111: Not used.	0x2	R/W
3	AMUX_2_SEL	ADC Input Selection. 0: PTAT to ADC input. 1: VVA_CTRL to ADC input.	0x0	R/W
[2:0]	AMUX_1_SEL	Select Mux Output. 000: PTAT. 001: Output of AMUX_3_SEL. 010: 1.8 V LDO output. 011: 3.3 V LDO output. 100: GND. 101: GND. 110: Not used. 111: Not used.	0x0	R/W

Address: 0x121, Reset: 0x00, Name: MULTI_FUNC_CTRL_0111

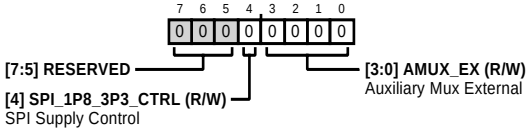

Table 52. Bit Descriptions for MULTI_FUNC_CTRL_0111

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved	0x0	R
4	SPI_1P8_3P3_CTRL	SPI Supply Control 0: 1.8 V readback 1: 3.3 V readback	0x0	R/W
[3:0]	AMUX_EX	Auxiliary Mux External	0x0	R/W

Address: 0x127, Reset: 0x00, Name: ADC_CONTROL

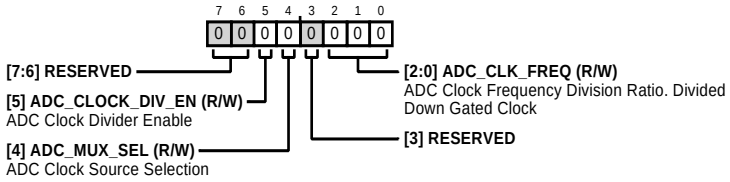

Table 53. Bit Descriptions for ADC_CONTROL

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	ADC_CLOCK_DIV_EN	ADC Clock Divider Enable. 0: Disable ADC clock divider. 1: Enable ADC clock divider.	0x0	R/W
4	ADC_MUX_SEL	ADC Clock Source Selection. 0: ADC clock from SCLK. 1: Not used.	0x0	R/W
3	RESERVED	Reserved.	0x0	R
[2:0]	ADC_CLK_FREQ	ADC Clock Frequency Division Ratio. Divided Down Gated Clock. 000: ADC clock at SCLK/2. 001: ADC clock at SCLK/1. 010: ADC clock at SCLK/2. 011: ADC clock at SCLK/4.	0x0	R/W

Address: 0x128, Reset: 0x00, Name: ADC_EOC

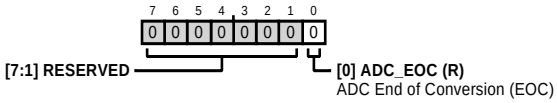

Table 54. Bit Descriptions for ADC_EOC

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved	0x0	R
0	ADC_EOC	ADC End of Conversion (EOC)	0x0	R

Address: 0x129, Reset: 0x00, Name: ADC_OUT

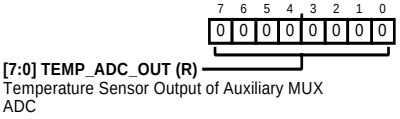

Table 55. Bit Descriptions for ADC_OUT

Bits	Bit Name	Description	Reset	Access
[7:0]	TEMP_ADC_OUT	Temperature Sensor Output of Auxiliary Mux ADC	0x0	R

Address: 0x146, Reset: 0x00, Name: GENERIC_READBACK_2

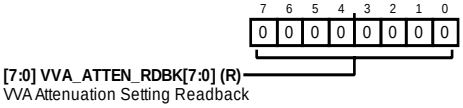

Table 56. Bit Descriptions for GENERIC_READBACK_2

Bits	Bit Name	Description	Reset	Access
[7:0]	VVA_ATTEN_RDBK[7:0]	VVA Attenuation Setting Readback	0x0	R

Address: 0x147, Reset: 0x00, Name: GENERIC_READBACK_3

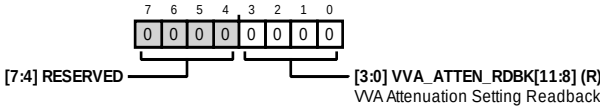

Table 57. Bit Descriptions for GENERIC_READBACK_3

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved	0x0	R
[3:0]	VVA_ATTEN_RDBK[11:8]	VVA Attenuation Setting Readback	0x0	R

Address: 0x148, Reset: 0x00, Name: GENERIC_READBACK_4

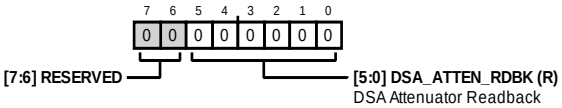

Table 58. Bit Descriptions for GENERIC_READBACK_4

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved	0x0	R
[5:0]	DSA_ATTEN_RDBK	DSA Attenuator Readback	0x0	R

OUTLINE DIMENSIONS

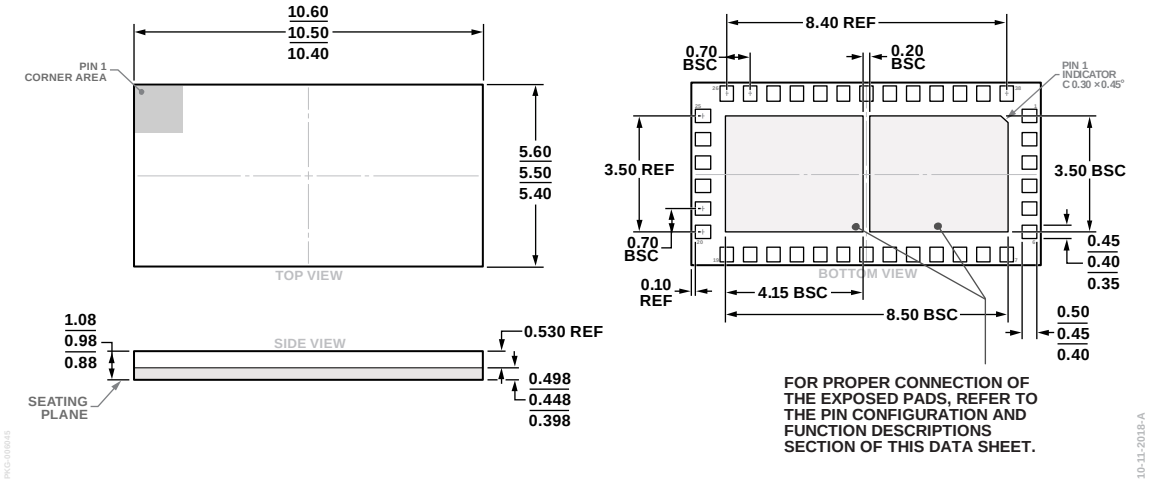

Figure 50. 38-Terminal Land Grid Array [LGA]
(CC-38-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range[2]	Package Description	Package Option
ADL6317ACCZ	–40°C to +105°C	38-Terminal Land Grid Array [LGA]	CC-38-1
ADL6317ACCZ-R7	–40°C to +105°C	38-Terminal Land Grid Array [LGA]	CC-38-1
ADL6317-EVALZ		Evaluation Board	

[1] Z = RoHS Compliant Part
[2] Measured at the exposed pad.

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