

High-Performance WVGA Display Module with maXTouch[®] Information Sheet

The High-Performance WVGA Display Module with maXTouch (AC320005-5) is designed for evaluating the Microchip graphics display solution and graphics library for 32-bit microcontrollers. This board is compatible with both versions of the Multimedia Expansion Board II (DM320005-2 or DM320005-5), as well as with Xplained Pro and Xplained Ultra evaluation kits. This board has a TFT 800 x 480 display with a 24-bit parallel RGB interface with a maXTouch capacitive touch interface.

Features

- 800 x 480 TFT display
- maXTouch MXT460
- QTouch[®] QT1070 (with four navigation keys)
- 4 K-bit 1-wire EEPROM
- Integrated Projective Capacitive Touch (PCAP) panel

Running the High-Performance WVGA Display Module with maXTouch Demonstration Code

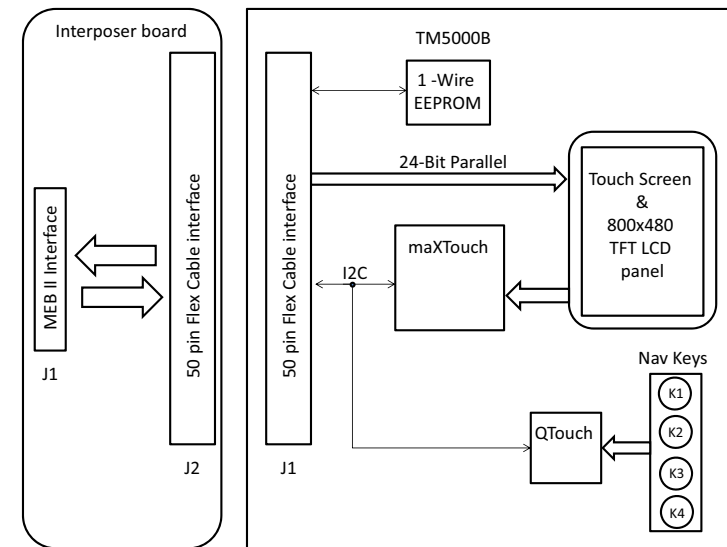
For free Microchip demonstration code and additional information, visit the MPLAB[®] Harmony web page at: www.microchip.com/Harmony.

After MPLAB Harmony is installed, refer to the following MPLAB Harmony installation folder for demonstration purposes:

C:\microchip\harmony\

To work with older Xplained Pro and Xplained Ultra evaluation kits, disconnect the ribbon connector from the adapter board and connect it to the GFX port (50 flex) of the Xplained Pro or Xplained Ultra.

FIGURE 1: WVGA DISPLAY MODULE BLOCK DIAGRAM



Americas

Atlanta - 678-957-9614
 Austin - 512-257-3370
 Boston - 774-760-0087
 Chicago - 630-285-0071
 Cleveland - 216-447-0464
 Dallas - 972-818-7423
 Detroit - 248-848-4000
 Houston - 281-894-5983
 Indianapolis - 317-773-8323
 Los Angeles - 949-462-9523
 New York - 631-435-6000
 Phoenix - 480-792-7200
 Santa Clara - 408-961-6444
 Toronto - 905-673-0699

Europe

Austria - Wels - 43-7242-2244-39
 Denmark - Copenhagen - 45-4450-2828
 France - Paris - 33-1-69-53-63-20
 Germany - Munich - 49-89-627-144-0
 Italy - Milan - 39-0331-742611
 Netherlands - Drunen - 31-416-690399
 Spain - Madrid - 34-91-708-08-90
 UK - Wokingham - 44-118-921-5869

Asia/Pacific

Australia - Sydney - 61-2-9868-6733
 China - Beijing - 86-10-8569-2100

Asia/Pacific (Continued)

China - Chengdu - 86-28-8665-5511
 China - Chongqing - 86-23-8980-9588
 China - Hangzhou - 86-571-8792-8115
 China - Hong Kong SAR - 852-2943-5100
 China - Nanjing - 86-25-8473-2460
 China - Qingdao - 86-532-8502-7355
 China - Shanghai - 86-21-5407-5533
 China - Shenyang - 86-24-2334-2829
 China - Shenzhen - 86-755-8864-2200
 China - Wuhan - 86-27-5980-5300
 China - Xiamen - 86-592-2388138
 China - Xian - 86-29-8833-7252
 China - Zhuhai - 86-756-3210040
 India - Bangalore - 91-80-3090-4444
 India - New Delhi - 91-11-4160-8631
 India - Pune - 91-20-3019-1500
 Japan - Osaka - 81-6-6152-7160
 Japan - Tokyo - 81-3-6880-3770
 Korea - Daegu - 82-53-744-4301
 Korea - Seoul - 82-2-554-7200
 Malaysia - Kuala Lumpur - 60-3-6201-9857
 Malaysia - Penang - 60-4-227-8870
 Philippines - Manila - 63-2-634-9065
 Singapore - 65-6334-8870
 Taiwan - Hsin Chu - 886-3-5778-366
 Taiwan - Kaohsiung - 886-7-213-7840
 Taiwan - Taipei - 886-2-2508-8600
 Thailand - Bangkok - 66-2-694-1351

01/11/17



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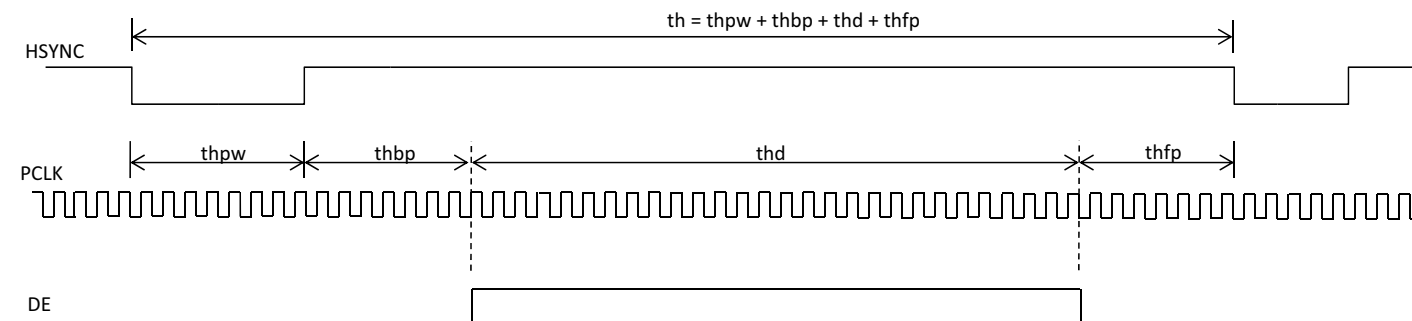
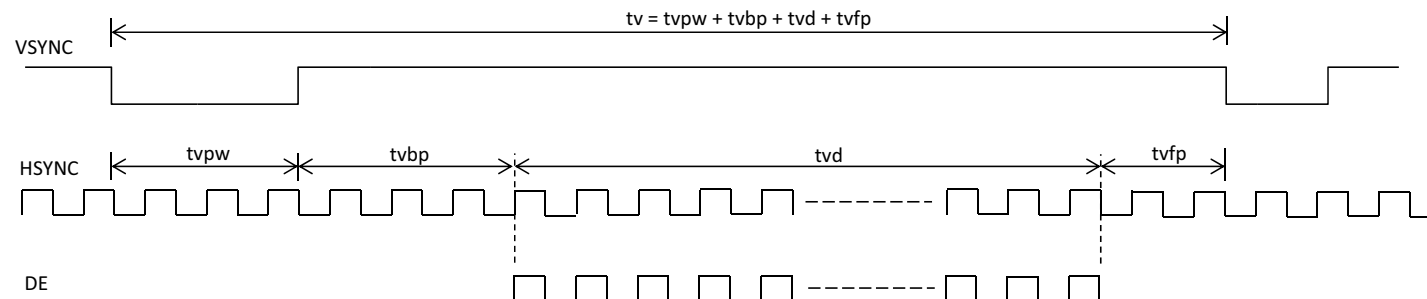
DS50002681A



High-Performance WVGA Display Module with maXTouch® Board Timing Specifications

TABLE 1: TIMING SPECIFICATION VALUES

| Parameter | Symbol | Spec. | | | Unit |
|---------------------------|--------|-------|------|------|-------|
| | | Min. | Typ. | Max. | |
| Clock Cycle | 1/PCLK | - | 30 | 40 | MHz |
| Hsync Cycle | 1/th | - | 10.7 | - | kHz |
| Vsync Cycle | 1/tv | - | 19 | - | Hz |
| Horizontal Signal | | | | | |
| Horizontal Cycle | th | - | 928 | - | CLK |
| Horizontal Display Period | thd | 800 | 800 | 800 | CLK |
| Horizontal Front Porch | thfp | - | 40 | - | CLK |
| Horizontal Pulse width | thpw | 1 | 48 | - | CLK |
| Horizontal Back Porch | thbp | - | 40 | - | CLK |
| Vertical Signals | | | | | |
| Vertical Cycle | tv | - | 525 | - | Hsync |
| Vertical Display Period | tvd | 480 | 480 | 480 | Hsync |
| Vertical Front Porch | tvfp | - | 13 | - | Hsync |
| Vertical Pulse Width | tvpw | 1 | 3 | - | Hsync |
| Vertical Back Porch | tvbp | - | 29 | - | Hsync |

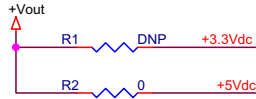


Bottom Contacts Use Type 1 FFC

Xplained Interface

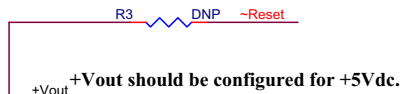
| | | |
|----|----|-----------|
| J2 | 1 | ONE WIRE |
| | 2 | GND |
| | 3 | LCDDAT0 |
| | 4 | LCDDAT1 |
| | 5 | LCDDAT2 |
| | 6 | LCDDAT3 |
| | 7 | GND |
| | 8 | LCDDAT4 |
| | 9 | LCDDAT5 |
| | 10 | LCDDAT6 |
| | 11 | LCDDAT7 |
| | 12 | GND |
| | 13 | LCDDAT8 |
| | 14 | LCDDAT9 |
| | 15 | LCDDAT10 |
| | 16 | LCDDAT11 |
| | 17 | GND |
| | 18 | LCDDAT12 |
| | 19 | LCDDAT13 |
| | 20 | LCDDAT14 |
| | 21 | LCDDAT15 |
| | 22 | GND |
| | 23 | LCDDAT16 |
| | 24 | LCDDAT17 |
| | 25 | LCDDAT18 |
| | 26 | LCDDAT19 |
| | 27 | GND |
| | 28 | LCDDAT20 |
| | 29 | LCDDAT21 |
| | 30 | LCDDAT22 |
| | 31 | LCDDAT23 |
| | 32 | GND |
| | 33 | PCLK |
| | 34 | VSYNC |
| | 35 | HSYNC |
| | 36 | DE |
| | 37 | SCK |
| | 38 | MOSI |
| | 39 | MISO |
| | 40 | ~SS |
| | 41 | DISP |
| | 42 | SDA |
| | 43 | SCL |
| | 44 | ~CHG mxt |
| | 45 | ~CHG QT |
| | 46 | LCD_PWM |
| | 47 | ~Reset IN |
| | 48 | +Vout |
| | 49 | +Vout |
| | 50 | GND |

CON50



~CHG_QT is connected to Pin 53 for future use if desired.

SCK, MOSI, MISO and ~SS are connected to Pins 54, 56, 58 and 57 (respectively) for future use if desired.

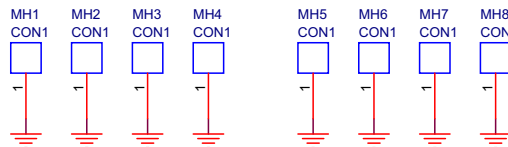


Debug Header

| | | |
|----|----|----------|
| J3 | 1 | GND |
| | 2 | ~CHG QT |
| | 3 | ~CHG mxt |
| | 4 | SCL |
| | 5 | SDA |
| | 6 | DE |
| | 7 | HSYNC |
| | 8 | VSYNC |
| | 9 | PCLK |
| | 10 | GND |

CON10

Mounting Holes



MEB II Interface

| | | | | |
|----------|----|----|----------|-----|
| GND | J1 | 1 | 2 | GND |
| GND | 3 | 4 | GND | |
| +3.3Vdc | 5 | 6 | +3.3Vdc | |
| LCDDAT12 | 7 | 8 | LCDDAT8 | |
| LCDDAT13 | 9 | 10 | LCDDAT9 | |
| LCDDAT14 | 11 | 12 | LCDDAT10 | |
| LCDDAT15 | 13 | 14 | LCDDAT11 | |
| LCDDAT16 | 15 | 16 | LCDDAT0 | |
| LCDDAT17 | 17 | 18 | LCDDAT1 | |
| LCDDAT18 | 19 | 20 | LCDDAT2 | |
| LCDDAT19 | 21 | 22 | LCDDAT3 | |
| LCDDAT20 | 23 | 24 | LCDDAT4 | |
| GND | 25 | 26 | GND | |
| +3.3Vdc | 27 | 28 | +3.3Vdc | |
| LCDDAT21 | 29 | 30 | LCDDAT5 | |
| LCDDAT22 | 31 | 32 | LCDDAT6 | |
| LCDDAT23 | 33 | 34 | LCDDAT7 | |
| PCLK | 35 | 36 | ONE WIRE | |
| VSYNC | 37 | 38 | HSYNC | |
| DE | 39 | 40 | | |
| ~CHG mxt | 41 | 42 | SCL | |
| | 43 | 44 | SDA | |
| LCD_PWM | 45 | 46 | DISP | |
| GND | 47 | 48 | GND | |
| +5Vdc | 49 | 50 | +5Vdc | |
| ~CHG QT | 51 | 52 | SCK | |
| ~Reset | 53 | 54 | MOSI | |
| ~SS | 55 | 56 | MISO | |
| GND | 57 | 58 | GND | |
| | 59 | 60 | | |

DF12 (3.0)-60DS-05V (86)

ONE_WIRE is connected to Pin 38 for future use if desired.

Microchip "LCD_CS" is not used by PDA LCD interface

Microchip "LCD_Reset" is connected to PDA "DISP". When DISP is low the LCD is in standby mode. When DISP is high the LCD is in normal display mode.

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[AC320005-5](#)