



# RF Power LDMOS Transistor

## N-Channel Enhancement-Mode Lateral MOSFET

This 51 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2300 to 2400 MHz.

### 2300 MHz

- Typical Doherty Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Vdc,  $I_{DQA} = 500$  mA,  $V_{GSB} = 0.5$  Vdc,  $P_{out} = 51$  W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)
2300 MHz	15.5	50.7	7.7	-33.4
2350 MHz	15.6	50.6	7.6	-35.2
2400 MHz	15.5	50.4	7.4	-35.6

### Features

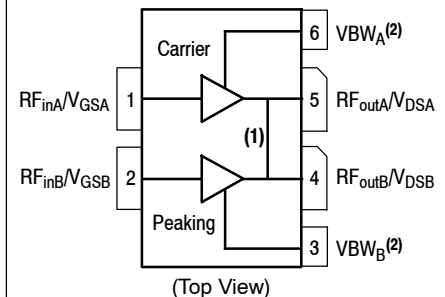
- Advanced high performance in-package Doherty
- Designed for wide instantaneous bandwidth applications
- Greater negative gate-source voltage range for improved Class C operation
- Able to withstand extremely high output VSWR and broadband operating conditions
- Designed for digital predistortion error correction systems

**A2T23H200W23SR6**

**2300–2400 MHz, 51 W AVG., 28 V  
 AIRFAST RF POWER LDMOS  
 TRANSISTOR**



**ACP-1230S-4L2S**



**Figure 1. Pin Connections**

1. Pin connections 4 and 5 are DC coupled and RF independent.
2. Device cannot operate with  $V_{DD}$  current supplied through pin 3 and pin 6.

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-6.0, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature Range	$T_C$	-40 to +150	°C
Operating Junction Temperature Range (1,2)	$T_J$	-40 to +225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 78°C, 51 W Avg., W-CDMA, 28 Vdc, $I_{DQA} = 500$ mA, $V_{GSB} = 0.5$ Vdc, 2350 MHz	$R_{\theta JC}$	0.29	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Charge Device Model (per JESD22-C101)	C3

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics (4)**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 32$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	5	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 5$ Vdc, $V_{DS} = 0$ Vdc)	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics - Side A, Carrier**

Gate Threshold Voltage ( $V_{DS} = 10$ Vdc, $I_D = 101$ $\mu\text{Adc}$ )	$V_{GS(th)}$	2.1	2.5	2.9	Vdc
Gate Quiescent Voltage ( $V_{DD} = 28$ Vdc, $I_D = 500$ mAdc, Measured in Functional Test)	$V_{GSA(Q)}$	2.2	2.6	3.0	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10$ Vdc, $I_D = 1.0$ Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

**On Characteristics - Side B, Peaking**

Gate Threshold Voltage ( $V_{DS} = 10$ Vdc, $I_D = 180$ $\mu\text{Adc}$ )	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10$ Vdc, $I_D = 1.8$ Adc)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.nxp.com/RF/calculators>.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.nxp.com/RF> and search for AN1955.
4. Side A and Side B are tied together for these measurements.

(continued)

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Functional Tests</b> <sup>(1,2,3)</sup> (In NXP Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$ , $I_{DQA} = 500\text{ mA}$ , $V_{GSB} = 0.5\text{ Vdc}$ , $P_{out} = 51\text{ W Avg.}$ , $f = 2300\text{ MHz}$ , Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	$G_{ps}$	14.0	15.5	16.6	dB
Drain Efficiency	$\eta_D$	48.3	50.7	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.0	7.7	—	dB
Adjacent Channel Power Ratio	ACPR	—	-33.4	-30.5	dBc

**Load Mismatch** <sup>(3)</sup> (In NXP Doherty Test Fixture, 50 ohm system)  $I_{DQA} = 500\text{ mA}$ ,  $V_{GSB} = 0.5\text{ Vdc}$ ,  $f = 2350\text{ MHz}$ , 12  $\mu\text{sec(on)}$ , 10% Duty Cycle

VSWR 10:1 at 32 Vdc, 316 W Pulsed CW Output Power (3 dB Input Overdrive from 158 W Pulsed CW Rated Power)	No Device Degradation
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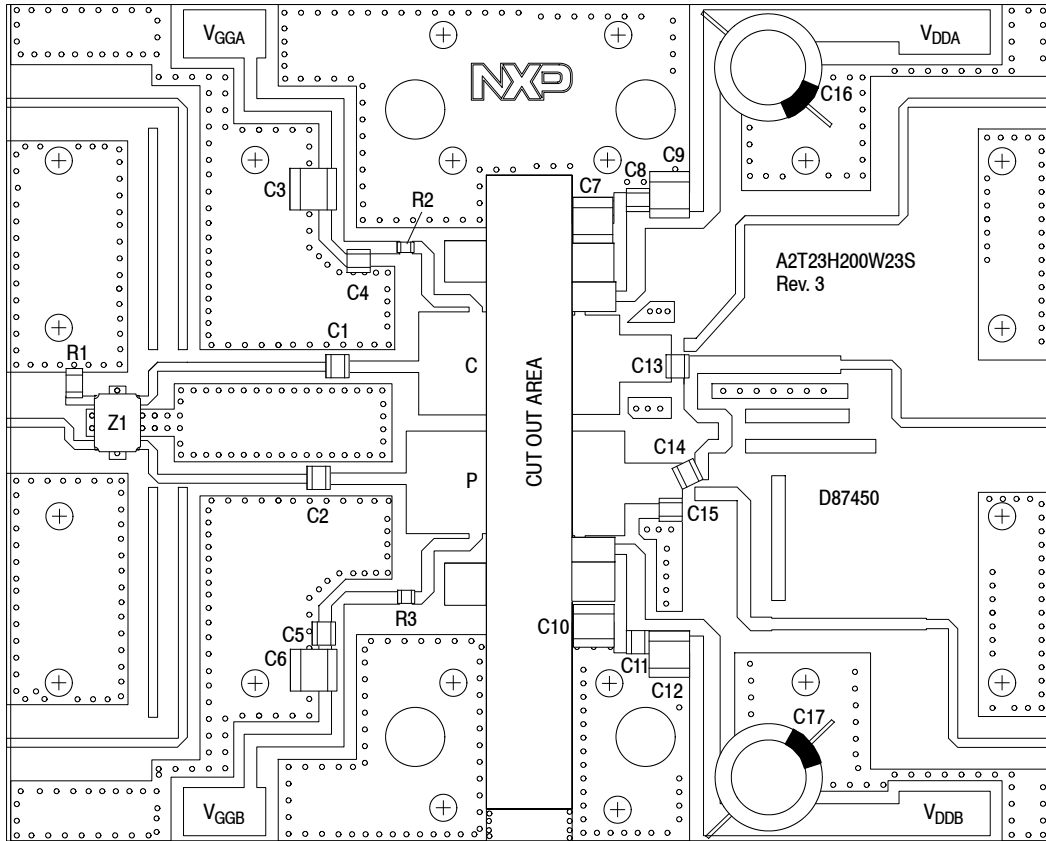
**Typical Performance** <sup>(3)</sup> (In NXP Doherty Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQA} = 500\text{ mA}$ ,  $V_{GSB} = 0.5\text{ Vdc}$ , 2300–2400 MHz Bandwidth

$P_{out}$ @ 3 dB Compression Point <sup>(4)</sup>	$P_{3dB}$	—	288	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2300–2400 MHz bandwidth)	$\Phi$	—	-12	—	$^\circ$
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	$VBW_{res}$	—	180	—	MHz
Gain Flatness in 100 MHz Bandwidth @ $P_{out} = 51\text{ W Avg.}$	$G_F$	—	0.3	—	dB
Gain Variation over Temperature ( $-30^\circ\text{C}$ to $+85^\circ\text{C}$ )	$\Delta G$	—	0.005	—	dB/ $^\circ\text{C}$
Output Power Variation over Temperature ( $-30^\circ\text{C}$ to $+85^\circ\text{C}$ )	$\Delta P_{1dB}$	—	0.008	—	dB/ $^\circ\text{C}$

**Table 5. Ordering Information**

Device	Tape and Reel Information	Package
A2T23H200W23SR6	R6 Suffix = 150 Units, 56 mm Tape Width, 13-inch Reel	ACP-1230S-4L2S

- $V_{DDA}$  and  $V_{ddb}$  must be tied together and powered by a single DC power supply.
- Part internally matched both on input and output.
- Measurements made with device in an asymmetrical Doherty configuration.
- $P_{3dB} = P_{avg} + 7.0\text{ dB}$  where  $P_{avg}$  is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.



Note:  $V_{DDA}$  and  $V_{DDB}$  must be tied together and powered by a single DC power supply.

**Figure 2. A2T23H200W23SR6 Test Circuit Component Layout**

**Table 6. A2T23H200W23SR6 Test Circuit Component Designations and Values**

Part	Description	Part Number	Manufacturer
C1, C2, C4, C5, C8, C11, C13, C14	6.2 pF Chip Capacitor	ATC100B6R2CT500X	ATC
C3, C6, C7, C9, C10, C12	10 $\mu$ F Chip Capacitor	C5750X7S2A106M	TDK
C15	0.6 pF Chip Capacitor	ATC100B0R6CT500X	ATC
C16, C17	470 $\mu$ F, 63 V Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
R1	50 $\Omega$ , 4 W Chip Resistor	ATCCW12010T0050GBK	ATC
R2, R3	2.7 $\Omega$ , 1/4 W Chip Resistor	CRCW12062R7FKEA	Vishay
Z1	2700 MHz Band, 90°, 3 dB Hybrid Coupler	X3C25P1-02S	Anaren
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D87450	MTL

TYPICAL CHARACTERISTICS — 2300–2400 MHz

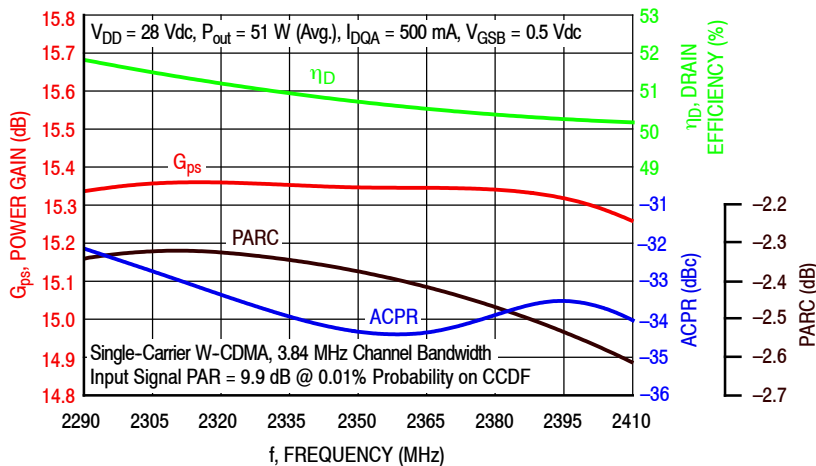


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 51$  Watts Avg.

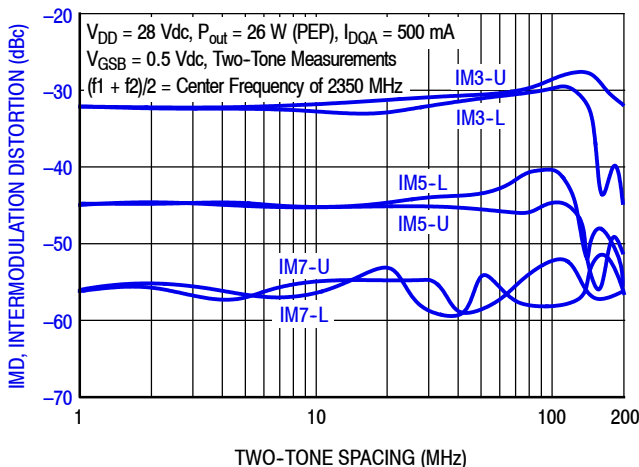


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

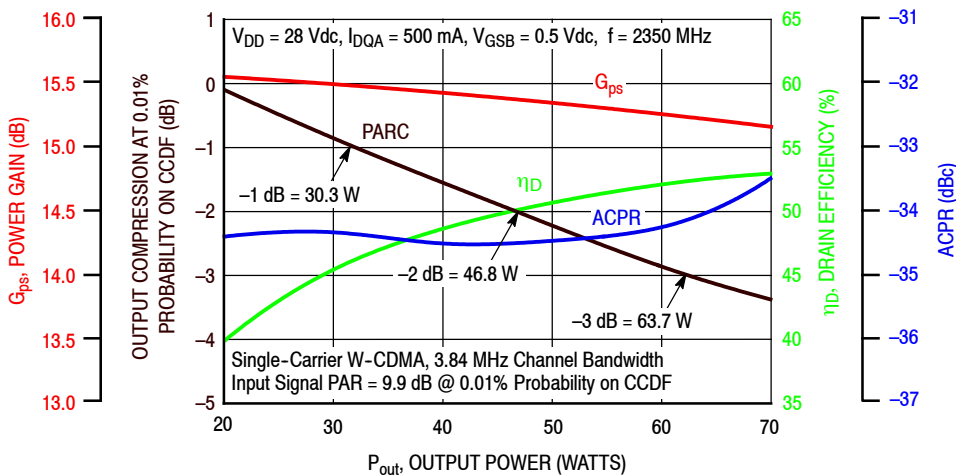


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 2300–2400 MHz

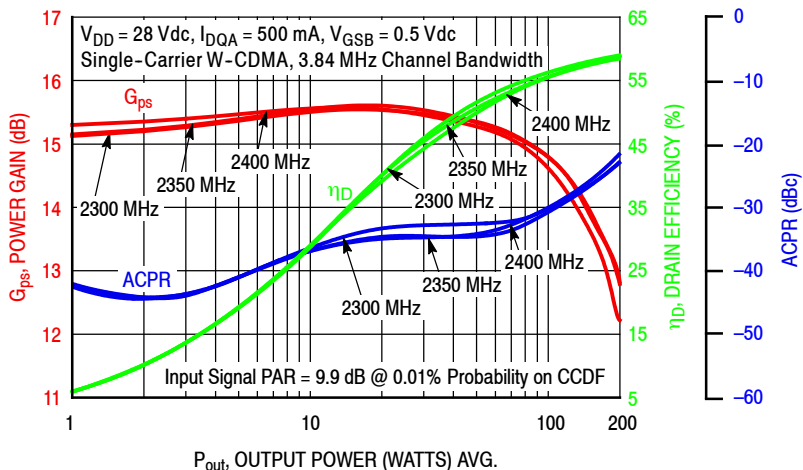


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

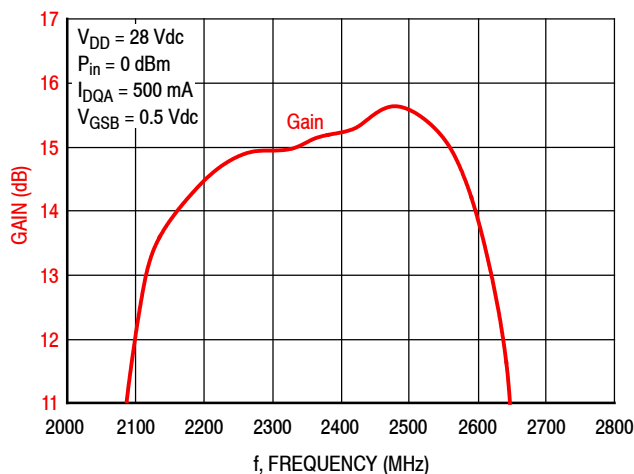


Figure 7. Broadband Frequency Response

**Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning**

$V_{DD} = 28$  Vdc,  $I_{DQA} = 491$  mA, Pulsed CW, 10  $\mu$ sec(on), 10% Duty Cycle

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Output Power					
			P1dB					
			$Z_{load}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2300	2.14 – j9.08	2.96 + j9.22	3.18 – j5.98	17.2	50.6	115	56.5	–12
2350	3.01 – j9.85	3.99 + j10.1	3.27 – j6.00	17.5	50.6	114	56.2	–12
2400	4.23 – j10.7	5.55 + j10.5	3.19 – j6.07	17.4	50.5	112	55.5	–12

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Output Power					
			P3dB					
			$Z_{load}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2300	2.14 – j9.08	2.77 + j9.58	3.10 – j6.23	15.1	51.4	139	58.3	–17
2350	3.01 – j9.85	3.85 + j10.7	3.20 – j6.23	15.3	51.4	138	58.2	–17
2400	4.23 – j10.7	5.72 + j11.2	3.18 – j6.70	15.1	51.3	135	57.0	–17

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

$Z_{source}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{in}$  = Impedance as measured from gate contact to ground.

$Z_{load}$  = Measured impedance presented to the output of the device at the package reference plane.

**Table 8. Carrier Side Load Pull Performance — Maximum Efficiency Tuning**

$V_{DD} = 28$  Vdc,  $I_{DQA} = 491$  mA, Pulsed CW, 10  $\mu$ sec(on), 10% Duty Cycle

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Drain Efficiency					
			P1dB					
			$Z_{load}^{(1)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2300	2.14 – j9.08	2.97 + j9.65	8.46 – j2.55	20.6	47.9	62	67.4	–21
2350	3.01 – j9.85	4.14 + j10.4	6.90 – j3.39	20.2	48.6	73	67.0	–18
2400	4.23 – j10.7	5.95 + j10.6	7.09 – j2.62	20.4	48.1	64	67.0	–19

f (MHz)	$Z_{source}$ ( $\Omega$ )	$Z_{in}$ ( $\Omega$ )	Max Drain Efficiency					
			P3dB					
			$Z_{load}^{(2)}$ ( $\Omega$ )	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM ( $^\circ$ )
2300	2.14 – j9.08	2.68 + j9.76	6.93 – j3.44	18.1	49.4	87	68.9	–26
2350	3.01 – j9.85	3.90 + j10.8	6.65 – j3.64	18.0	49.5	88	68.6	–25
2400	4.23 – j10.7	5.79 + j11.6	5.76 – j2.37	18.3	49.0	79	67.6	–29

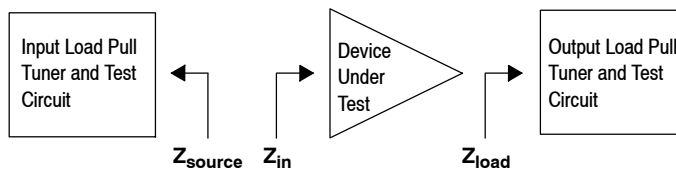
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

$Z_{source}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{in}$  = Impedance as measured from gate contact to ground.

$Z_{load}$  = Measured impedance presented to the output of the device at the package reference plane.



**Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning**

V<sub>DD</sub> = 28 Vdc, V<sub>G<sub>SB</sub></sub> = 0.5 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z <sub>source</sub> (Ω)	Z <sub>in</sub> (Ω)	Max Output Power					
			P1dB					
			Z <sub>load</sub> <sup>(1)</sup> (Ω)	Gain (dB)	(dBm)	(W)	η <sub>D</sub> (%)	AM/PM (°)
2300	2.88 – j7.97	1.95 + j7.63	2.55 – j4.07	14.4	53.2	209	58.5	–28
2350	4.25 – j8.11	2.88 + j8.55	2.55 – j4.14	14.7	53.2	209	59.4	–28
2400	6.32 – j8.44	4.68 + j9.25	2.56 – j4.40	14.7	53.1	202	57.1	–30

f (MHz)	Z <sub>source</sub> (Ω)	Z <sub>in</sub> (Ω)	Max Output Power					
			P3dB					
			Z <sub>load</sub> <sup>(2)</sup> (Ω)	Gain (dB)	(dBm)	(W)	η <sub>D</sub> (%)	AM/PM (°)
2300	2.88 – j7.97	2.12 + j7.93	2.75 – j4.55	12.3	53.9	244	60.3	–35
2350	4.25 – j8.11	3.26 + j8.94	2.69 – j4.51	12.5	53.8	242	60.2	–34
2400	6.32 – j8.44	5.52 + j9.59	2.72 – j4.72	12.6	53.7	233	57.6	–36

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

Z<sub>source</sub> = Measured impedance presented to the input of the device at the package reference plane.

Z<sub>in</sub> = Impedance as measured from gate contact to ground.

Z<sub>load</sub> = Measured impedance presented to the output of the device at the package reference plane.

**Table 10. Peaking Side Load Pull Performance — Maximum Efficiency Tuning**

V<sub>DD</sub> = 28 Vdc, V<sub>G<sub>SB</sub></sub> = 0.5 Vdc, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z <sub>source</sub> (Ω)	Z <sub>in</sub> (Ω)	Max Drain Efficiency					
			P1dB					
			Z <sub>load</sub> <sup>(1)</sup> (Ω)	Gain (dB)	(dBm)	(W)	η <sub>D</sub> (%)	AM/PM (°)
2300	2.88 – j7.97	1.73 + j7.55	5.17 – j1.68	15.4	51.6	143	69.2	–35
2350	4.25 – j8.11	2.53 + j8.48	3.89 – j1.70	15.7	51.8	151	68.9	–34
2400	6.32 – j8.44	4.08 + j9.26	3.66 – j1.84	15.7	51.6	143	67.4	–35

f (MHz)	Z <sub>source</sub> (Ω)	Z <sub>in</sub> (Ω)	Max Drain Efficiency					
			P3dB					
			Z <sub>load</sub> <sup>(2)</sup> (Ω)	Gain (dB)	(dBm)	(W)	η <sub>D</sub> (%)	AM/PM (°)
2300	2.88 – j7.97	1.98 + j7.90	4.25 – j3.01	13.3	53.0	200	68.9	–40
2350	4.25 – j8.11	2.95 + j8.91	3.96 – j2.10	13.6	52.5	178	69.2	–42
2400	6.32 – j8.44	4.98 + j9.70	3.60 – j2.09	13.7	52.3	169	67.3	–45

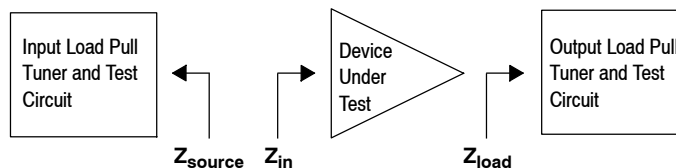
(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

Z<sub>source</sub> = Measured impedance presented to the input of the device at the package reference plane.

Z<sub>in</sub> = Impedance as measured from gate contact to ground.

Z<sub>load</sub> = Measured impedance presented to the output of the device at the package reference plane.





## P1dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2350 MHz

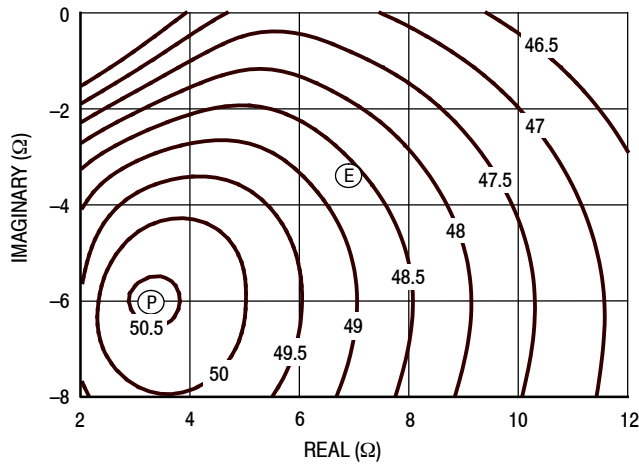


Figure 8. P1dB Load Pull Output Power Contours (dBm)

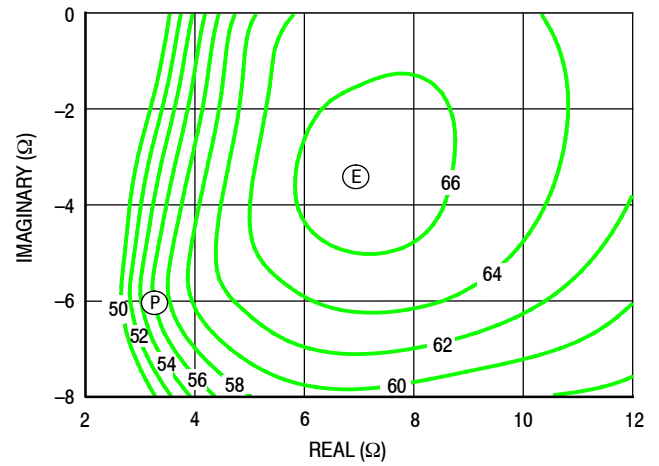


Figure 9. P1dB Load Pull Efficiency Contours (%)

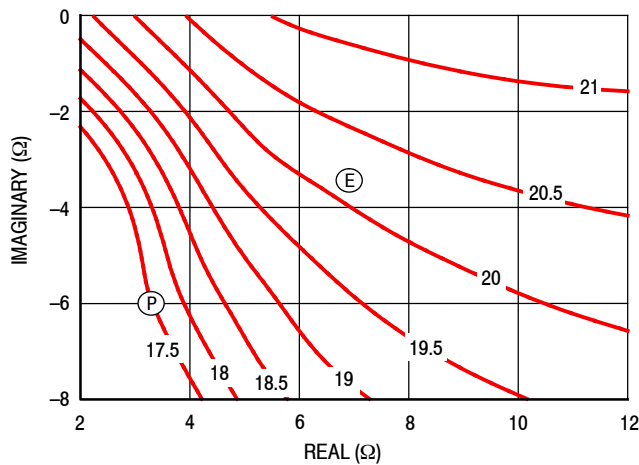


Figure 10. P1dB Load Pull Gain Contours (dB)

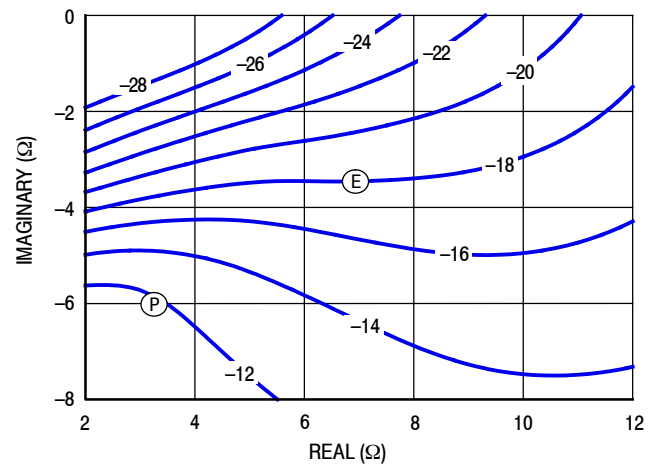


Figure 11. P1dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

### P3dB – TYPICAL CARRIER SIDE LOAD PULL CONTOURS — 2350 MHz

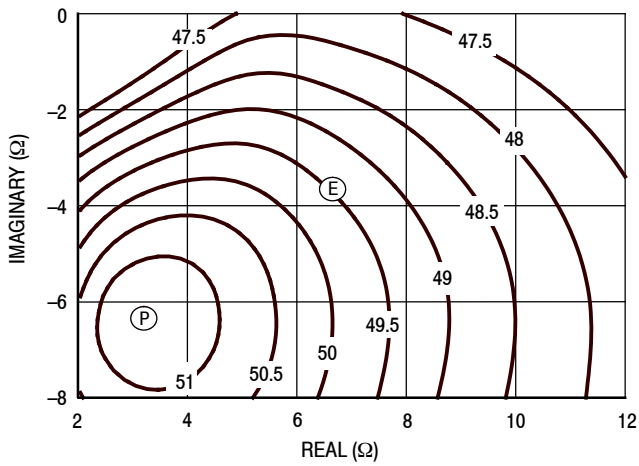


Figure 12. P3dB Load Pull Output Power Contours (dBm)

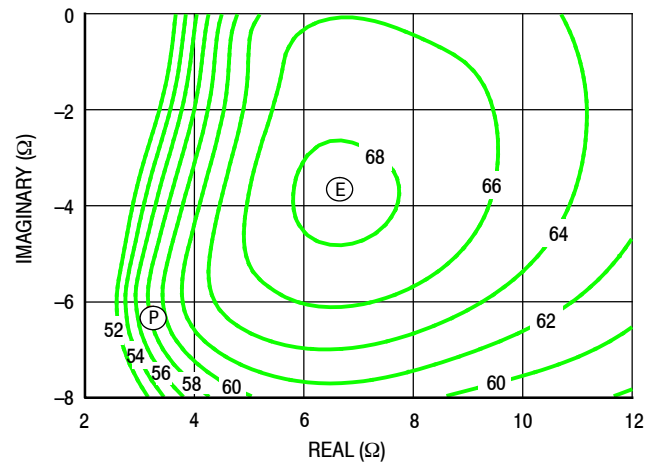


Figure 13. P3dB Load Pull Efficiency Contours (%)

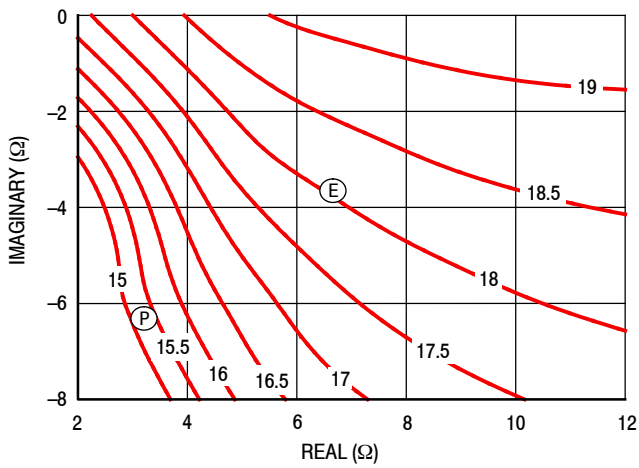


Figure 14. P3dB Load Pull Gain Contours (dB)

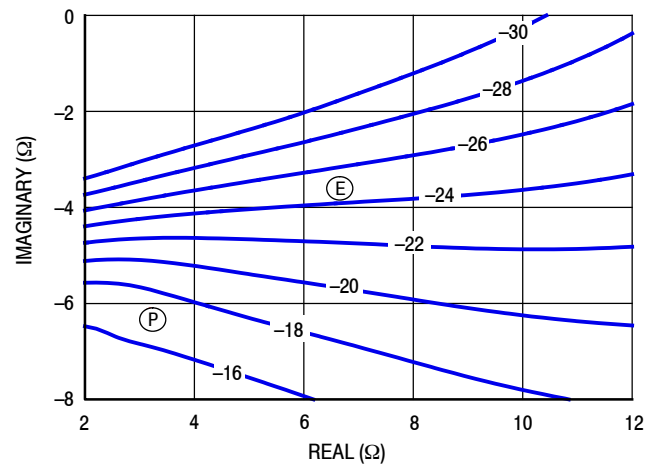


Figure 15. P3dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P1dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2350 MHz

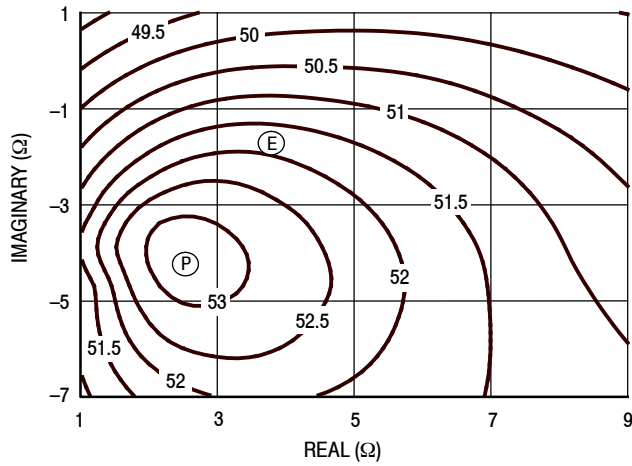


Figure 16. P1dB Load Pull Output Power Contours (dBm)

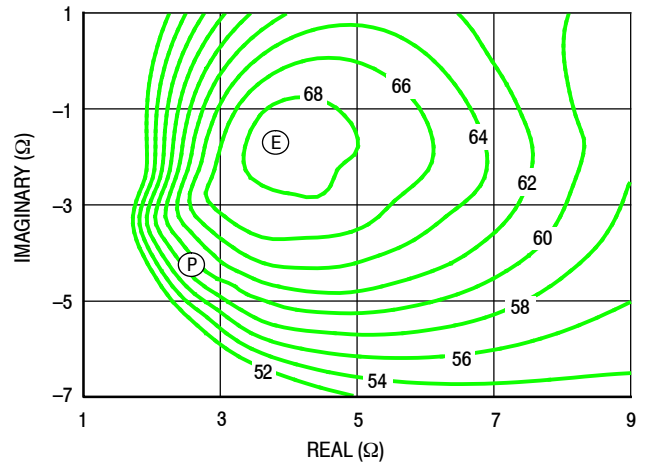


Figure 17. P1dB Load Pull Efficiency Contours (%)

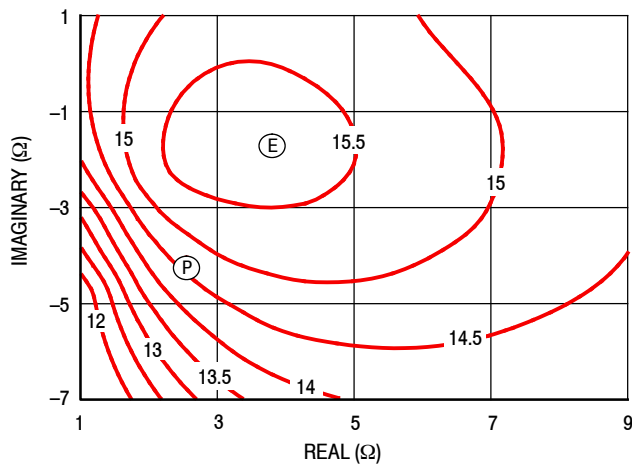


Figure 18. P1dB Load Pull Gain Contours (dB)

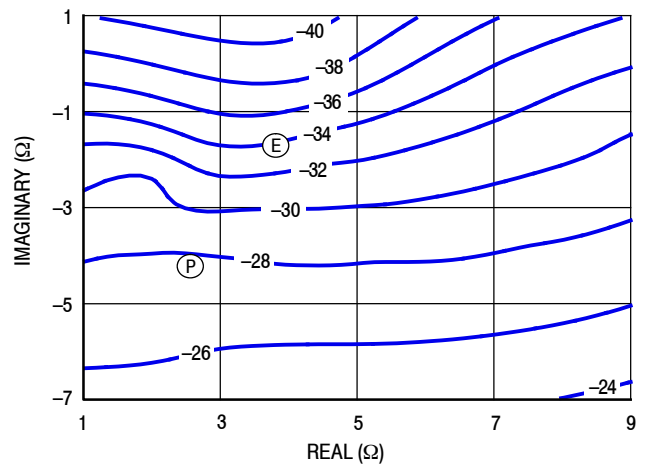


Figure 19. P1dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

### P3dB – TYPICAL PEAKING SIDE LOAD PULL CONTOURS — 2350 MHz

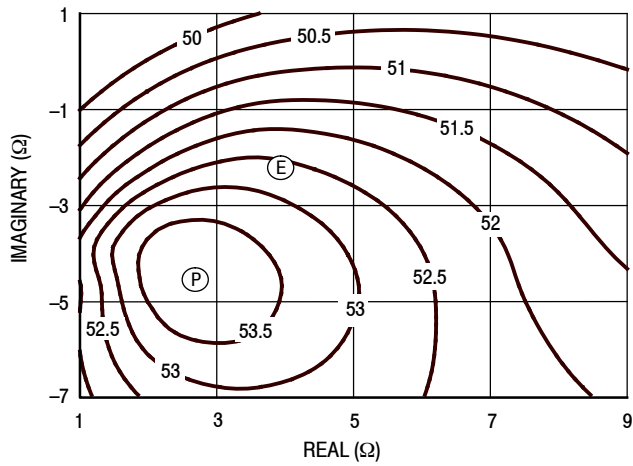


Figure 20. P3dB Load Pull Output Power Contours (dBm)

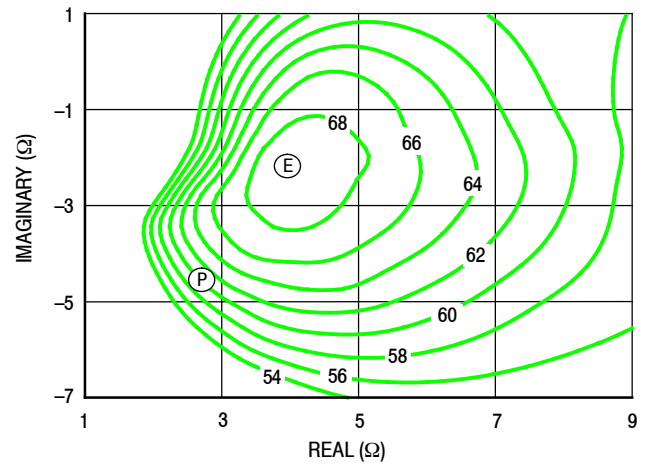


Figure 21. P3dB Load Pull Efficiency Contours (%)

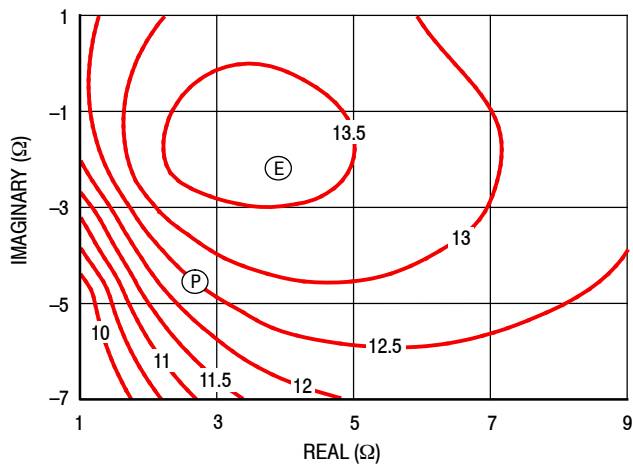


Figure 22. P3dB Load Pull Gain Contours (dB)

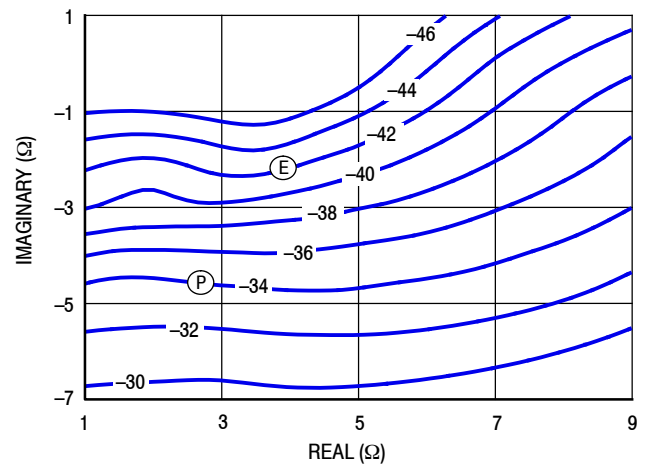
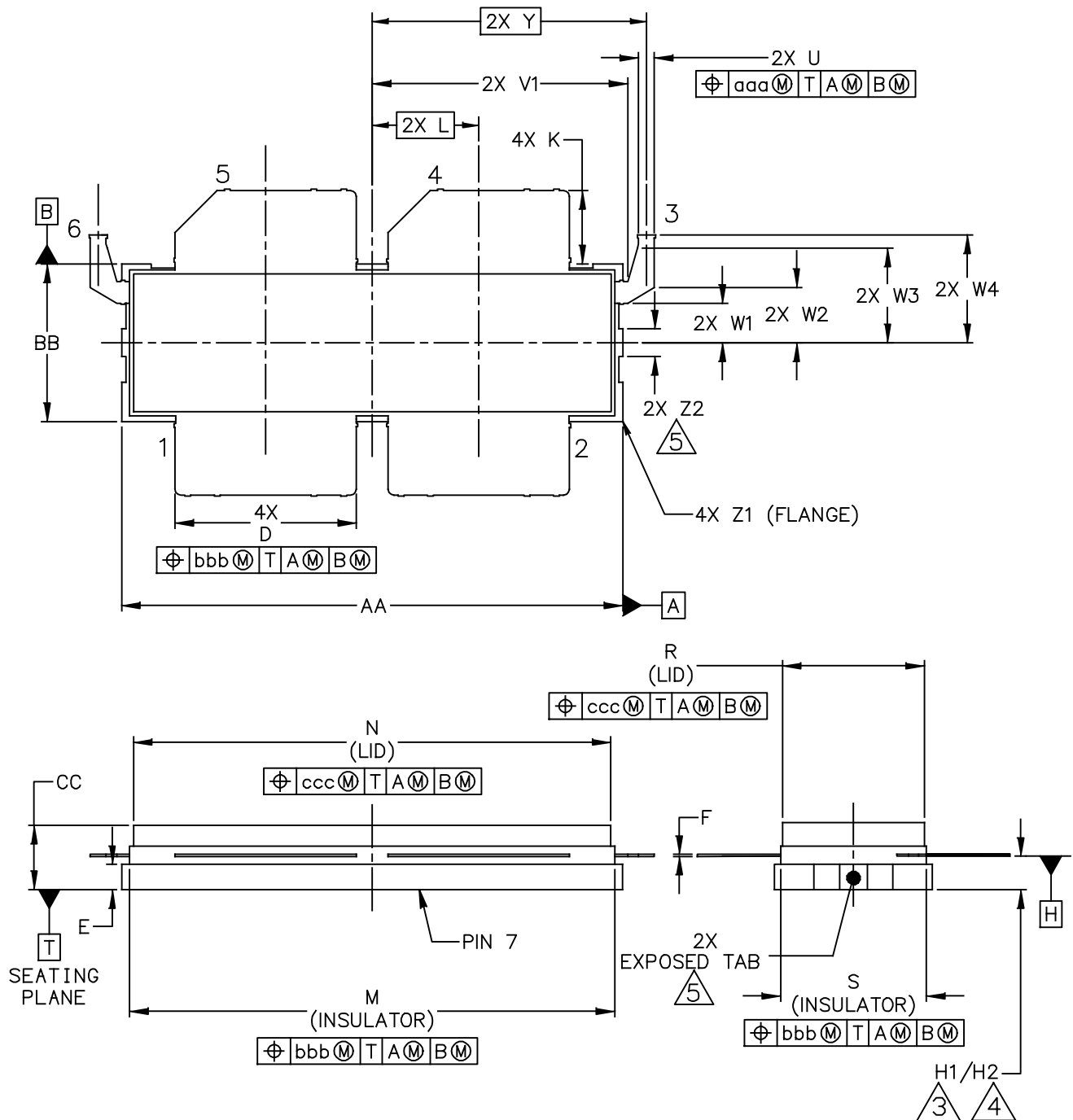


Figure 23. P3dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

### PACKAGE DIMENSIONS



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	STANDARD: NON-JEDEC	
	SOT1800-4	21 JUN 2017

A2T23H200W23SR6

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE.

5. THESE SURFACES OF THE HEAT SLUG ARE NOT PART OF THE SOLDERABLE SURFACES AND MAY REMAIN UNPLATED.

6. DATUM H IS LOCATED AT THE BOTTOM OF THE LEAD FRAME AND IS COINCIDENT WITH THE LEAD WHERE THE LEADS EXIT THE PLASTIC BODY.

7. DIMENSIONS M AND S DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .012 INCH (0.30 MM) PER SIDE. DIMENSIONS M AND S DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

8. DIMENSIONS D, U AND K DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .010 INCH (0.25 MM) TOTAL IN EXCESS OF THE D, U AND K DIMENSION AT MAXIMUM MATERIAL CONDITION.

9. DATUM A AND B TO BE DETERMINED AT DATUM T.

DIM	INCHES		MILLIMETERS		DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	1.265	1.275	32.13	32.39	S	.365	.375	9.27	9.53
BB	.395	.405	10.03	10.29	U	.035	.045	0.89	1.14
CC	.160	.190	4.06	4.83	V1	.640	.655	16.26	16.64
D	.455	.465	11.56	11.81	W1	.105	.115	2.67	2.92
E	.062	.069	1.57	1.75	W2	.135	.145	3.43	3.68
F	.004	.007	0.10	0.18	W3	.245	.255	6.22	6.48
H1	.082	.090	2.08	2.29	W4	.265	.281	6.73	7.14
H2	.078	.094	1.98	2.39	Y	0.695 BSC		17.65 BSC	
K	.175	.195	4.45	4.95	Z1	R.000	R.040	R0.00	R1.02
L	0.270 BSC		6.86 BSC		Z2	.060	.100	1.52	2.54
M	1.219	1.241	30.96	31.52	aaa	.015		0.38	
N	1.218	1.242	30.94	31.55	bbb	.010		0.25	
R	.365	.375	9.27	9.53	ccc	.020		0.51	

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21 JUN 2017

## PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

### Application Notes

- AN1908: Solder Reflow Attach Method for High Power RF Devices in Air Cavity Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### Software

- Electromigration MTTF Calculator
- .s2p File

### Development Tools

- Printed Circuit Boards

### To Download Resources Specific to a Given Part Number:

1. Go to <http://www.nxp.com/RF>
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	July 2017	• Initial release of data sheet

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