Document Number: A2T18S166W12S
Rev. 0, 04/2018

RF Power LDMOS Transistor

N–Channel Enhancement–Mode Lateral MOSFET

This 38 W RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 1805 to 1995 MHz.

1800 MHz

- Typical Single–Carrier W–CDMA Performance: V_{DD} = 28 Vdc, I_{DQ} = 800 mA, P_{out} = 38 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1805 MHz	18.0	35.3	6.9	–34.5	–18
1840 MHz	18.1	34.4	6.8	–34.7	–19
1880 MHz	17.6	34.2	6.7	–34.3	–12

1900 MHz

- Typical Single–Carrier W–CDMA Performance: V_{DD} = 28 Vdc, I_{DQ} = 800 mA, P_{out} = 38 W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

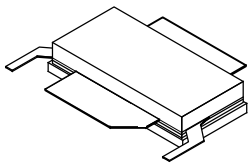
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1930 MHz	17.8	31.2	6.8	–34.6	–16
1960 MHz	18.3	31.7	6.8	–34.4	–22
1995 MHz	18.6	32.8	6.8	–34.0	–14

Features

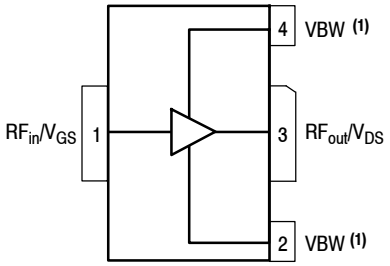
- Designed for wide instantaneous bandwidth applications
- Greater negative gate–source voltage range for improved Class C operation
- Able to withstand extremely high output VSWR and broadband operating conditions
- Optimized for Doherty applications

A2T18S166W12SR3

1805–1995 MHz, 38 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



NI–780S–2L2L



(Top View)

Figure 1. Pin Connections

1. Device can operate with V_{DD} current supplied through pin 2 and pin 4.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	–0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	–6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Case Operating Temperature Range	T_C	–40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	–40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 74°C, 38 W CW, 28 Vdc, I_{DQ} = 800 mA, 1840 MHz	$R_{\theta JC}$	0.38	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JS-001-2017)	2
Charge Device Model (per JS-002-2014)	C3

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	5	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 160 μAdc)	$V_{GS(th)}$	1.4	1.9	2.5	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 800 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.2	2.7	3.0	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 1.6 Adc)	$V_{DS(on)}$	0.05	0.15	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

(continued)

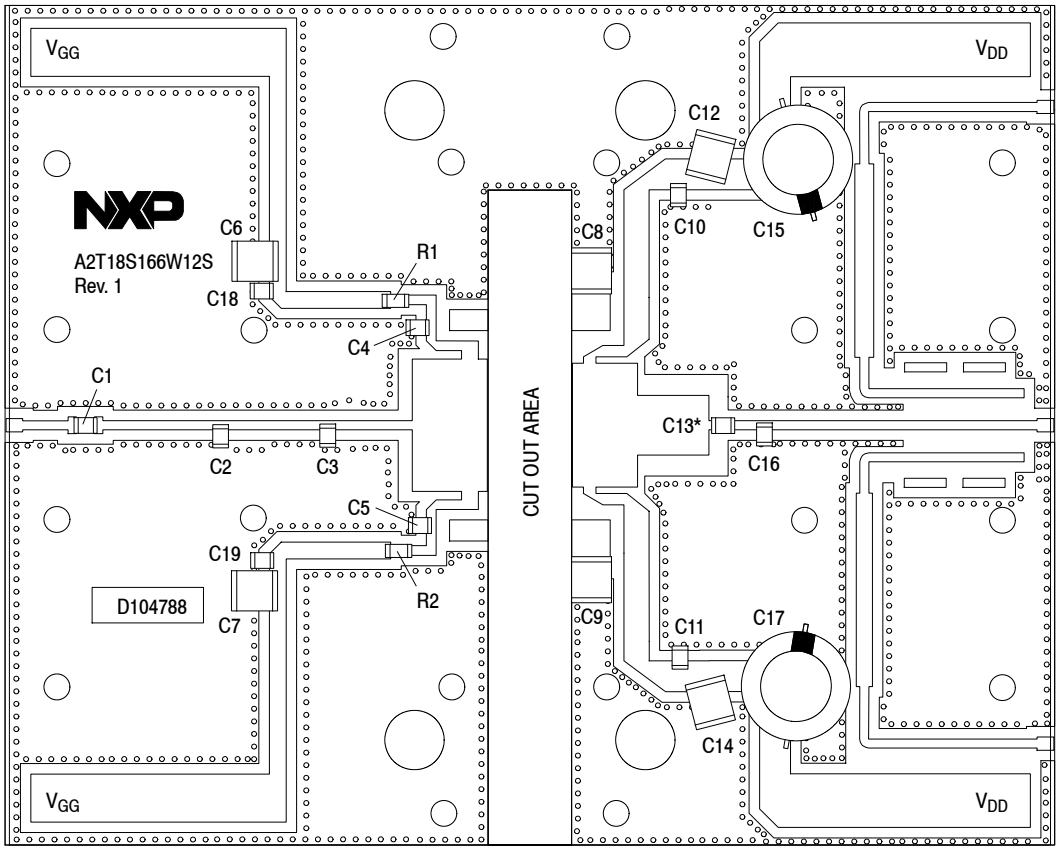
Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1) (In NXP Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 800 mA, P_{out} = 38 W Avg., f = 1840 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	17.2	18.1	20.2	dB
Drain Efficiency	η_D	32.0	34.4	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	6.2	6.8	—	dB
Adjacent Channel Power Ratio	ACPR	—	–34.7	–31.5	dBc
Input Return Loss	IRL	—	–19	–8	dB
Load Mismatch (In NXP Test Fixture, 50 ohm system) I_{DQ} = 800 mA, f = 1840 MHz, 12 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 32 Vdc, 214 W Pulsed CW Output Power (3 dB Input Overdrive from 151 W Pulsed CW Rated Power)	No Device Degradation				
Typical Performance (In NXP Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 800 mA, 1805–1880 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	158	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1805–1880 MHz frequency range.)	Φ	—	–16	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	100	—	MHz
Gain Flatness in 75 MHz Bandwidth @ P_{out} = 38 W Avg.	G_F	—	0.2	—	dB
Gain Variation over Temperature (–30°C to +85°C)	ΔG	—	0.012	—	dB/°C
Output Power Variation over Temperature (–30°C to +85°C)	ΔP1dB	—	0.007	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
A2T18S166W12SR3	R3 Suffix = 250 Units, 44 mm Tape Width, 13-inch Reel	NI-780S-2L2L

1. Part internally matched both on input and output.



*C13 is mounted vertically.

Figure 2. A2T18S166W12SR3 Test Circuit Component Layout

Table 6. A2T18S166W12SR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	8.2 pF Chip Capacitor	ATC100B8R2CT500XT	ATC
C2	3.6 pF Chip Capacitor	ATC100B3R6CT500XT	ATC
C3	3.3 pF Chip Capacitor	ATC100B3R3CT500XT	ATC
C4, C5	1.6 pF Chip Capacitor	ATC100B1R6CT500XT	ATC
C6, C7, C8, C9, C12, C14	10 μF Chip Capacitor	C5750X7S2A106M230KB	TDK
C10, C11, C18, C19	12 pF Chip Capacitor	ATC100B120JT500XT	ATC
C13	6.8 pF Chip Capacitor	ATC100B6R8CT500XT	ATC
C15, C17	470 μF, 63 V Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
C16	0.6 pF Chip Capacitor	ATC100B0R6BT500XT	ATC
R1, R2	2.7 Ω, 1/4 W Chip Resistor	CRCW12062R70FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D104788	MTL

TYPICAL CHARACTERISTICS — 1805–1880 MHz

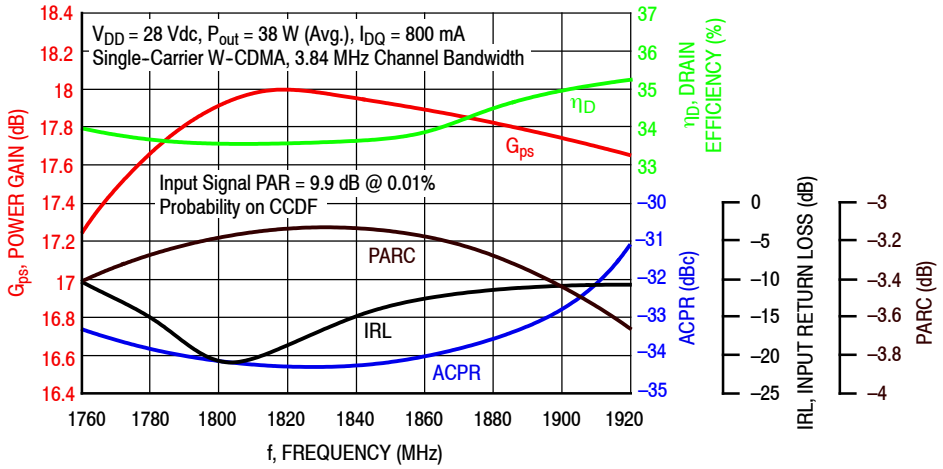


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 38 Watts Avg.

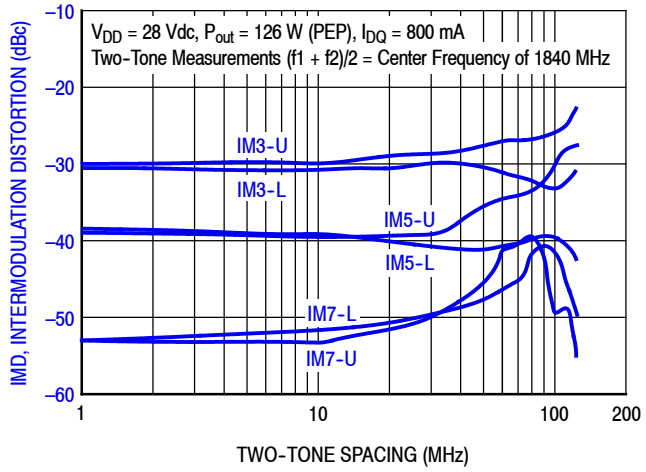


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

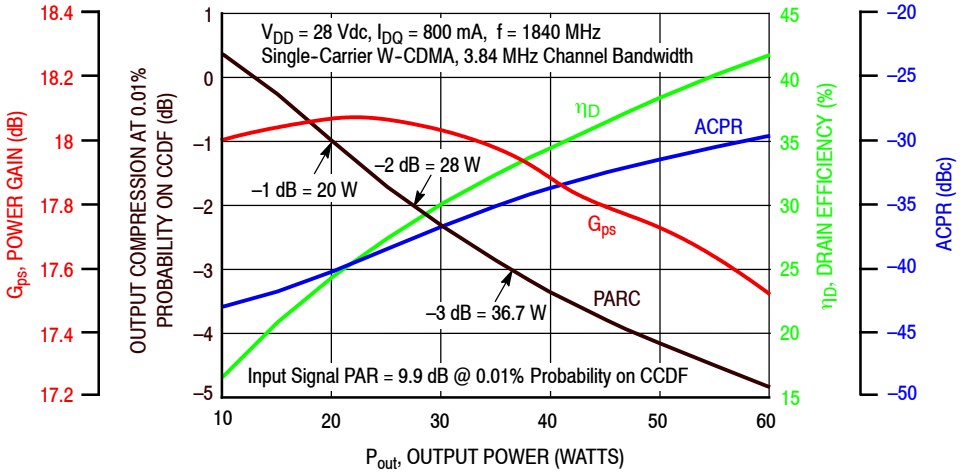


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 1805–1880 MHz

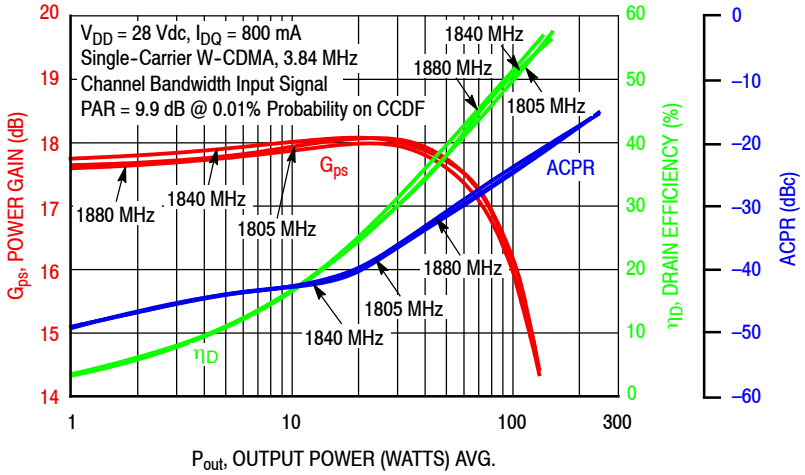


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

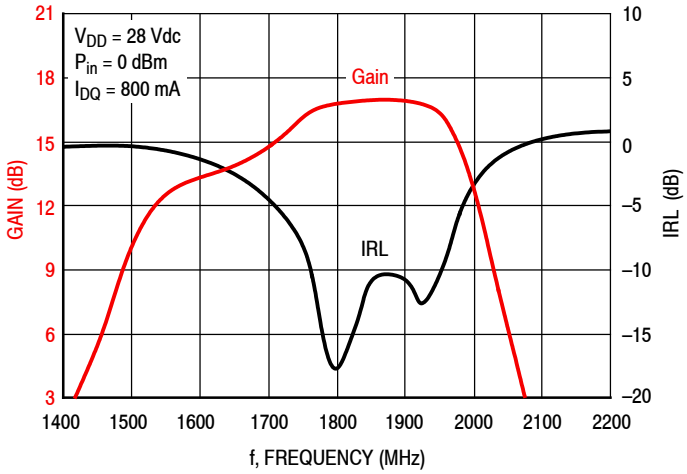


Figure 7. Broadband Frequency Response

Table 7. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ} = 788 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	0.58 – j1.44	0.66 + j1.42	0.93 – j2.07	19.2	52.6	183	59.7	–12
1840	0.67 – j1.69	0.80 + j1.60	0.91 – j2.26	19.0	52.7	186	59.0	–12
1880	0.90 – j1.77	1.01 + j1.88	0.94 – j2.39	19.1	52.6	182	59.9	–12

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	0.58 – j1.44	0.59 + j1.49	0.91 – j2.28	16.9	53.4	218	60.7	–17
1840	0.67 – j1.69	0.71 + j1.69	0.92 – j2.42	16.9	53.5	222	61.6	–17
1880	0.90 – j1.77	0.92 + j2.00	0.92 – j2.56	16.8	53.4	216	60.6	–16

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

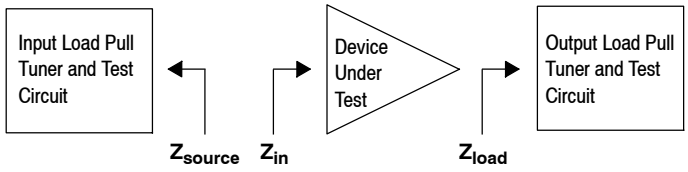
Table 8. Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ} = 788 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	0.58 – j1.44	0.64 + j1.51	2.09 – j1.52	22.0	50.8	119	72.6	–18
1840	0.67 – j1.69	0.78 + j1.71	2.25 – j1.32	22.4	50.2	104	72.0	–20
1880	0.90 – j1.77	0.96 + j2.01	1.81 – j1.31	22.1	50.3	108	72.2	–20

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	0.58 – j1.44	0.55 + j1.54	2.09 – j1.32	20.2	51.2	131	73.9	–27
1840	0.67 – j1.69	0.68 + j1.73	1.96 – j1.54	19.9	51.4	138	73.4	–27
1880	0.90 – j1.77	0.87 + j2.04	1.71 – j1.64	19.7	51.6	143	73.4	–26

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL LOAD PULL CONTOURS — 1840 MHz

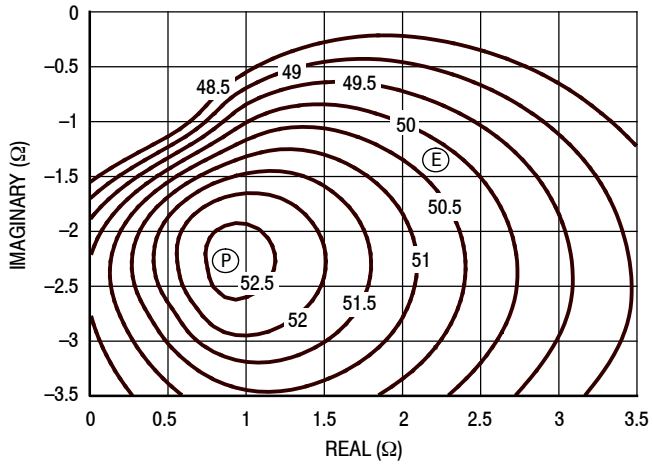


Figure 8. P1dB Load Pull Output Power Contours (dBm)

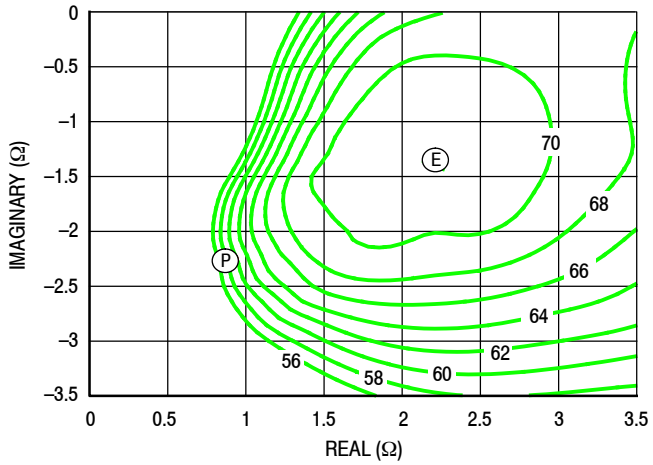


Figure 9. P1dB Load Pull Efficiency Contours (%)

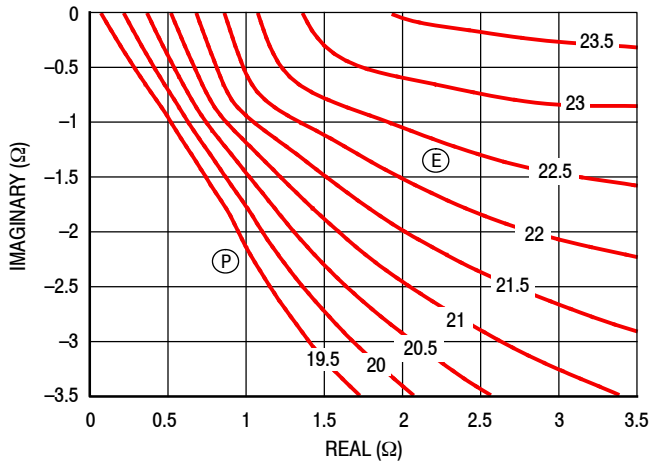


Figure 10. P1dB Load Pull Gain Contours (dB)

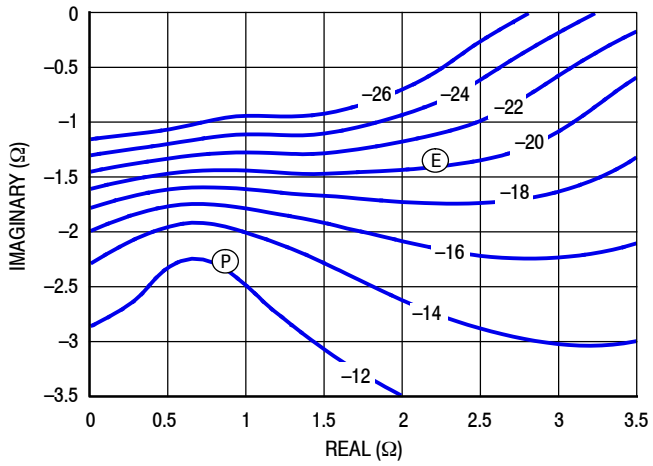


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power
Ⓔ = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 1840 MHz

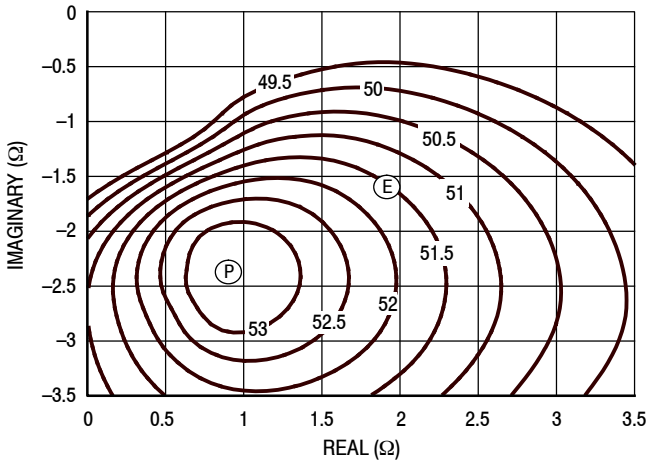


Figure 12. P3dB Load Pull Output Power Contours (dBm)

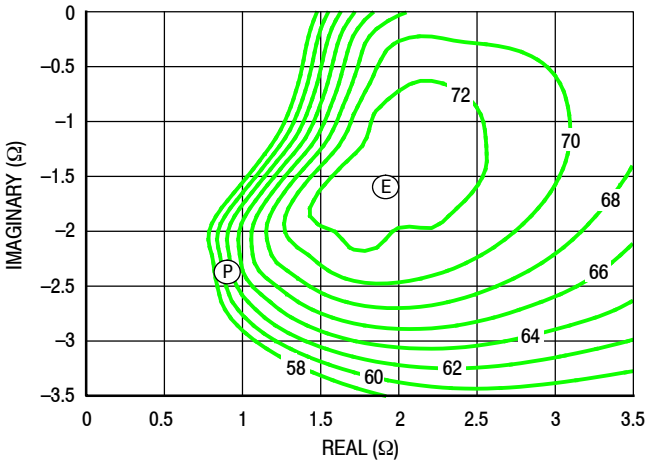


Figure 13. P3dB Load Pull Efficiency Contours (%)

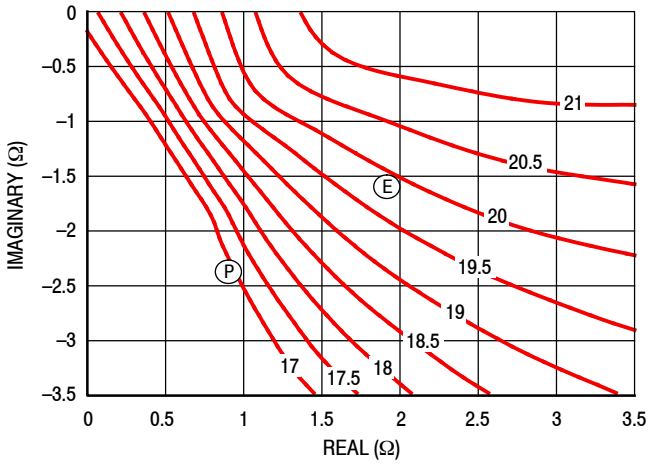


Figure 14. P3dB Load Pull Gain Contours (dB)

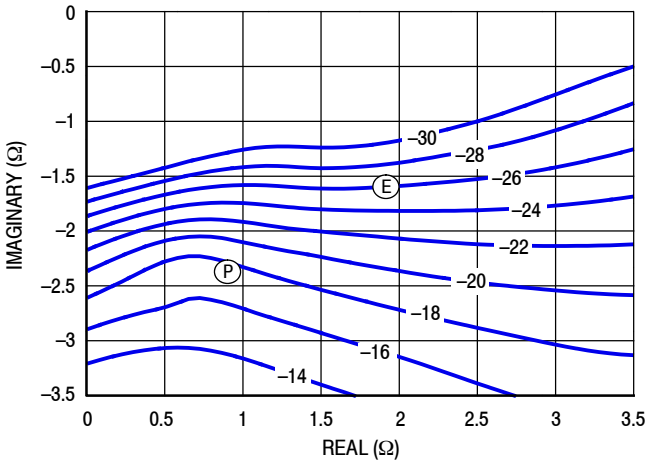


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

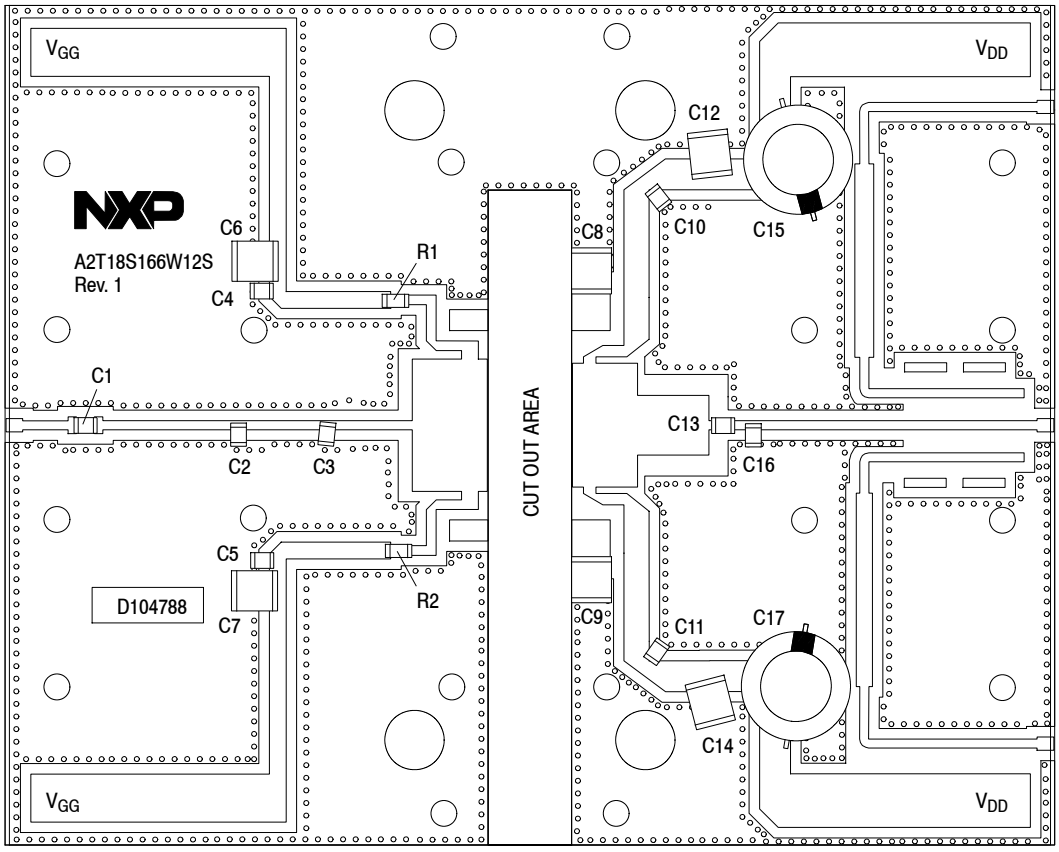


Figure 16. A2T18S166W12SR3 Test Circuit Component Layout — 1930–1995 MHz

Table 9. A2T18S166W12SR3 Test Circuit Component Designations and Values — 1930–1995 MHz

Part	Description	Part Number	Manufacturer
C1	8.2 pF Chip Capacitor	ATC100B8R2CT500XT	ATC
C2	3.6 pF Chip Capacitor	ATC100B3R6CT500XT	ATC
C3	3 pF Chip Capacitor	ATC100B3R0CT500XT	ATC
C4, C5, C10, C11	12 pF Chip Capacitor	ATC100B120JT500XT	ATC
C6, C7, C8, C9, C12, C14	10 μF Chip Capacitor	C5750X7S2A106M230KB	TDK
C13	6.8 pF Chip Capacitor	ATC100B6R8CT500XT	ATC
C15, C17	470 μF, 63 V Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
C16	0.1 pF Chip Capacitor	ATC100B0R1BT500XT	ATC
R1, R2	2.7 Ω, 1/4 W Chip Resistor	CRCW12062R70FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D104788	MTL

TYPICAL CHARACTERISTICS — 1930–1995 MHz

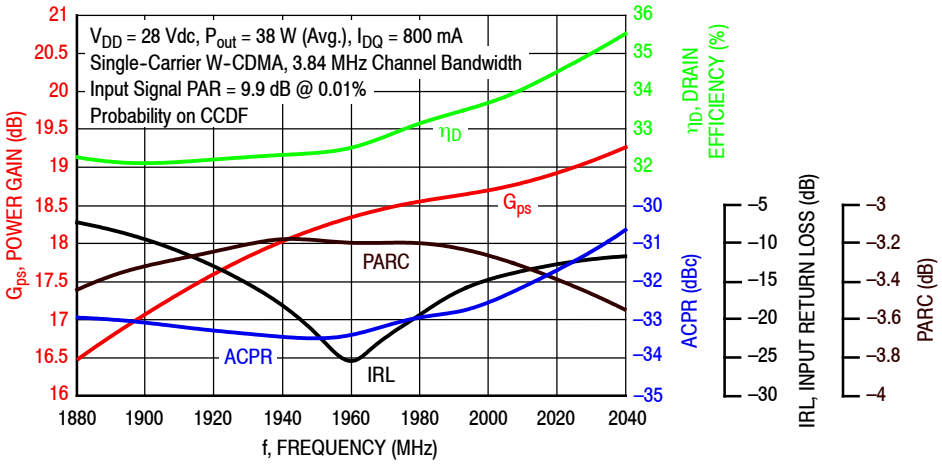


Figure 17. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 38 Watts Avg.

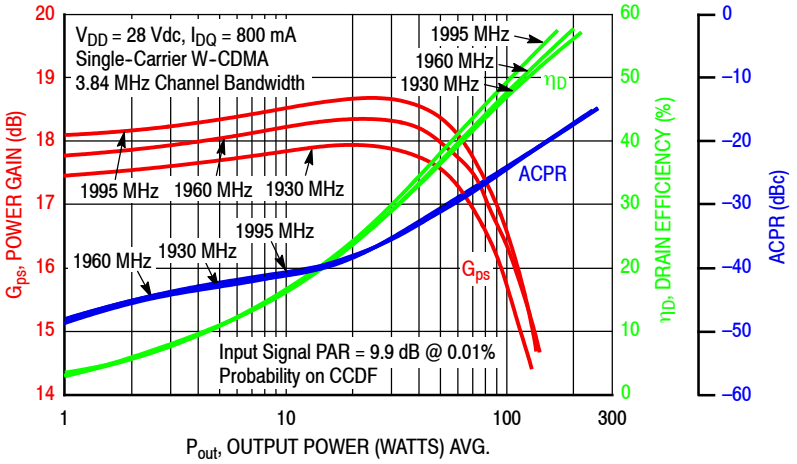


Figure 18. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

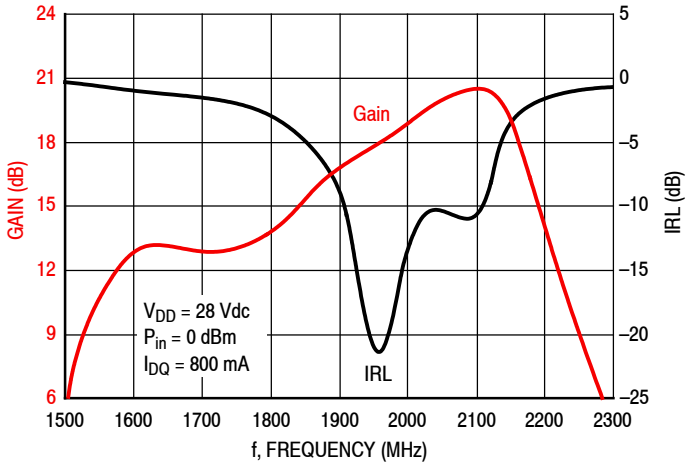


Figure 19. Broadband Frequency Response

Table 10. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ} = 785 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	1.27 – j2.25	1.32 + j2.33	0.98 – j2.55	19.2	52.6	183	60.0	–12
1960	1.53 – j2.83	1.64 + j2.64	0.94 – j2.65	19.1	52.6	183	58.8	–13
1995	1.86 – j3.04	2.16 + j3.06	0.96 – j2.69	19.4	52.6	181	59.7	–12

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	1.27 – j2.25	1.22 + j2.50	0.98 – j2.71	17.0	53.4	217	61.1	–16
1960	1.53 – j2.83	1.55 + j2.87	0.94 – j2.79	16.8	53.4	217	60.0	–17
1995	1.86 – j3.04	2.09 + j3.37	0.96 – j2.83	17.1	53.3	216	60.1	–17

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

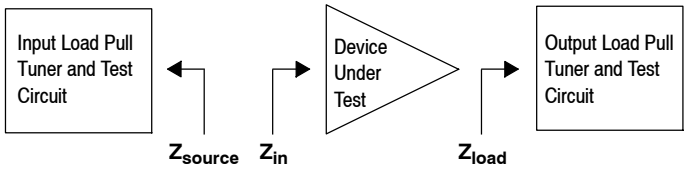
Table 11. Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ} = 785 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	1.27 – j2.25	1.30 + j2.44	1.74 – j1.68	21.9	50.8	120	71.3	–18
1960	1.53 – j2.83	1.61 + j2.81	1.58 – j1.57	22.2	50.5	113	71.2	–22
1995	1.86 – j3.04	2.20 + j3.17	1.57 – j1.93	21.9	51.0	127	70.4	–18

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	1.27 – j2.25	1.18 + j2.54	1.65 – j1.93	19.5	51.9	156	72.5	–24
1960	1.53 – j2.83	1.53 + j2.97	1.70 – j1.57	20.2	51.0	127	72.6	–29
1995	1.86 – j3.04	2.05 + j3.46	1.48 – j1.90	19.8	51.7	149	72.2	–26

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB – TYPICAL LOAD PULL CONTOURS — 1960 MHz

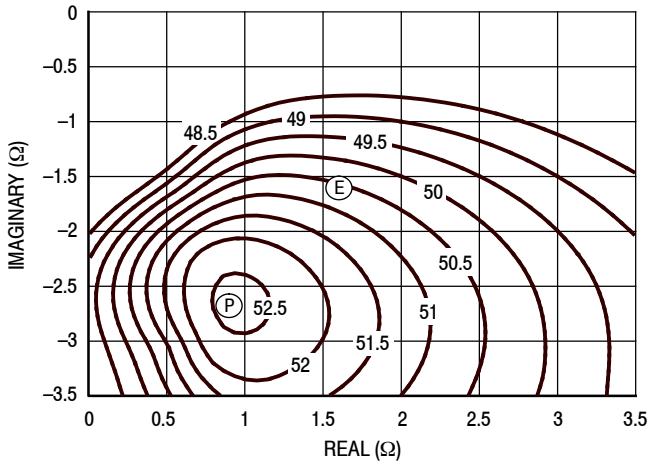


Figure 20. P1dB Load Pull Output Power Contours (dBm)

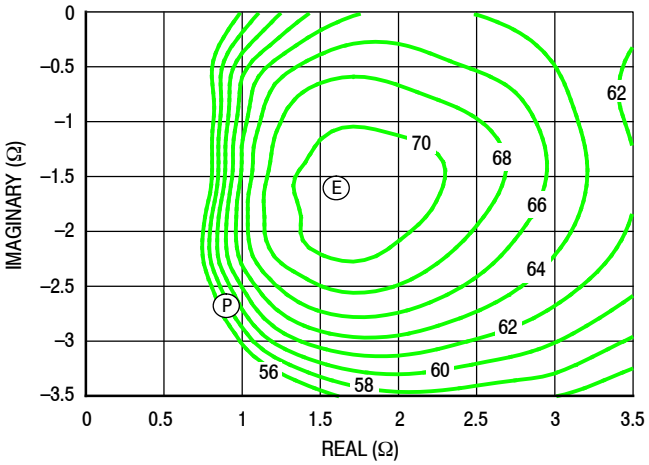


Figure 21. P1dB Load Pull Efficiency Contours (%)

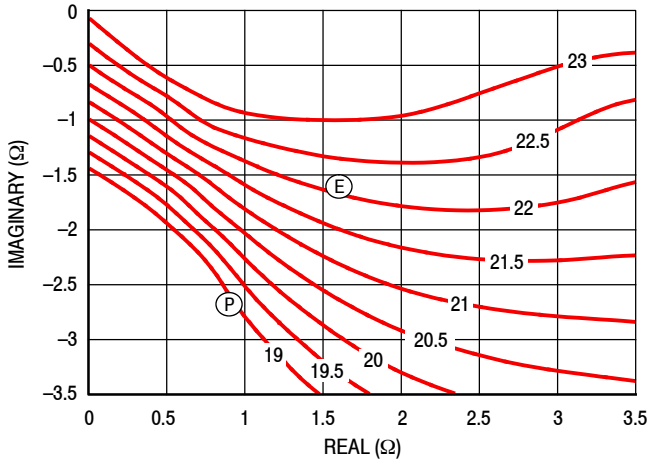


Figure 22. P1dB Load Pull Gain Contours (dB)

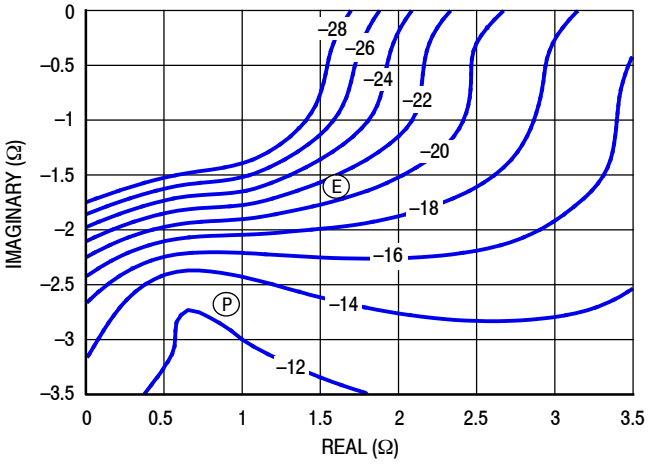


Figure 23. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 1960 MHz

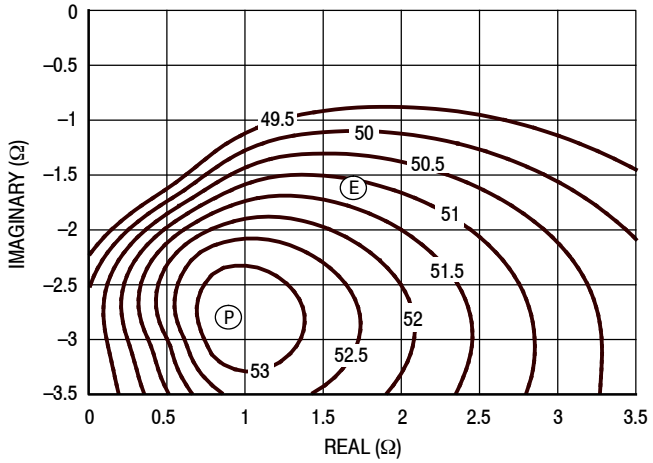


Figure 24. P3dB Load Pull Output Power Contours (dBm)

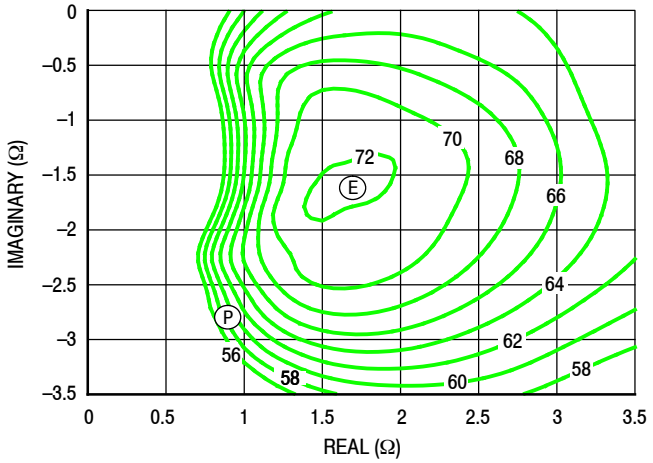


Figure 25. P3dB Load Pull Efficiency Contours (%)

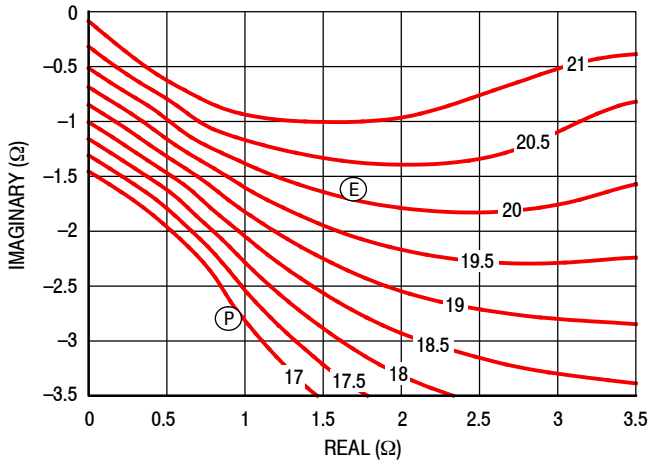


Figure 26. P3dB Load Pull Gain Contours (dB)

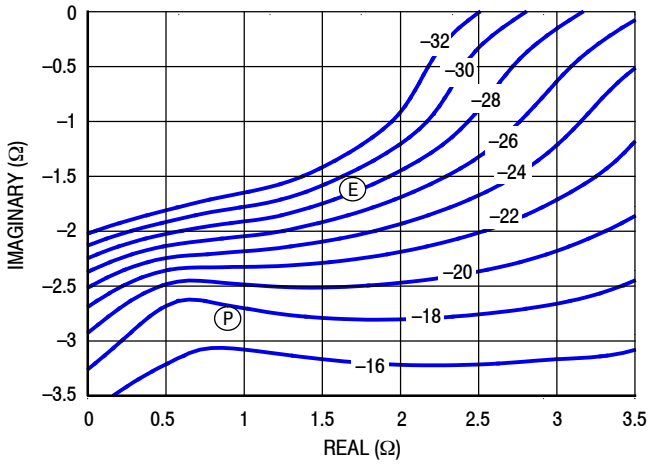


Figure 27. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

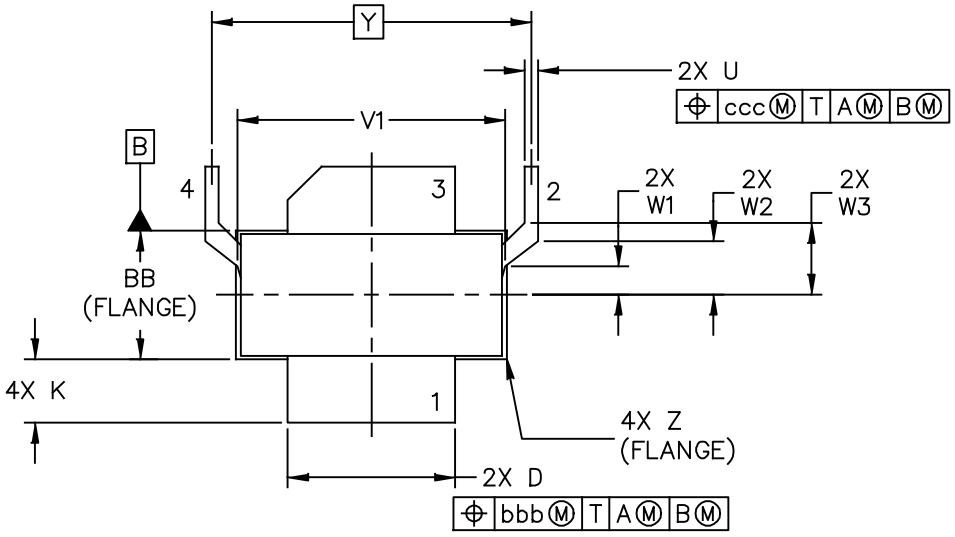
Gain

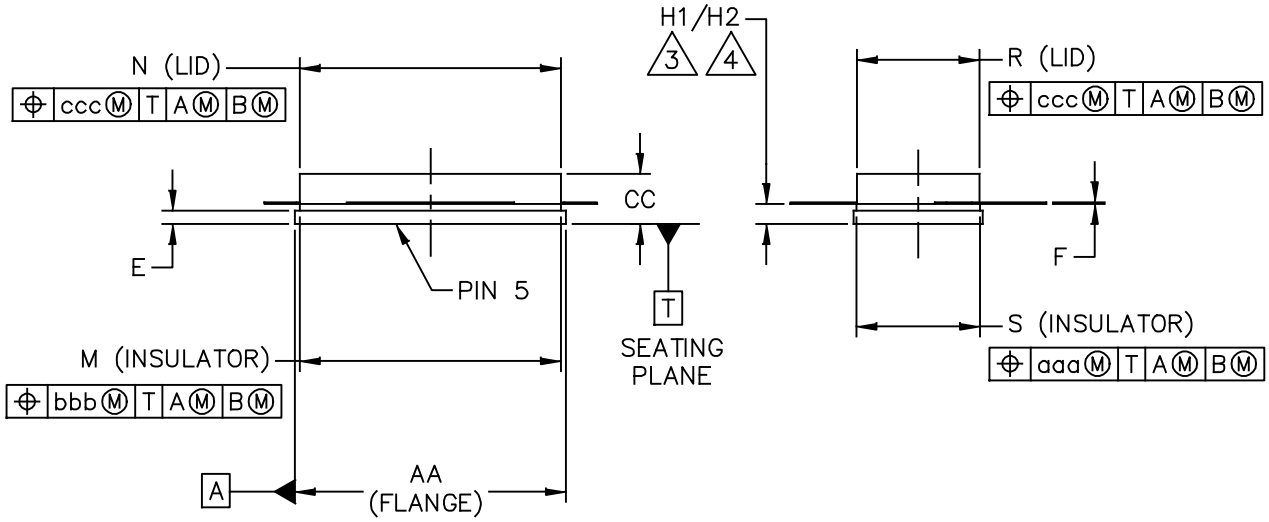
Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS





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	SOT1785−1	16 MAR 2016

NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE TO CLEAR THE EPOXY FLOW OUT PARALLEL TO DATUM B. H1 APPLIES TO PINS 1 & 3. H2 APPLIES TO PINS 2 & 4.
4. TOLERANCE OF DIMENSION H2 IS TENTATIVE AND COULD CHANGE ONCE SUFFICIENT MANUFACTURING DATA IS AVAILABLE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
BB	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
CC	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
D	.495	.505	12.57	12.83	V1	.795	.805	20.19	20.45
E	.035	.045	0.89	1.14	W1	.080	.090	2.03	2.29
F	.004	.007	0.10	0.18	W2	.155	.165	3.94	4.19
H1	.057	.067	1.45	1.70	W3	.210	.220	5.33	5.59
H2	.054	.070	1.37	1.78	Y	.956 BSC		24.28 BSC	
K	.170	.210	4.32	5.33	Z	R.000	R.040	R0.00	R1.02
M	.774	.786	19.66	19.96	aaa	.005		0.13	
N	.772	.788	19.61	20.02	bbb	.010		0.25	
					ccc	.015		0.38	

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SOT1785–1 16 MAR 2016

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1908: Solder Reflow Attach Method for High Power RF Devices in Air Cavity Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Apr. 2018	• Initial release of data sheet

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