BittWare a **molex** company

520N-MX
PCIe FPGA Board

Stratix 10 FPGA Board with 16GB HBM2
Powerful solution for accelerating memory-bound applications

Designed for compute acceleration, the 520N-MX is a PCIe board featuring Intel's Stratix 10 MX2100 FPGA with integrated HBM2 memory. The size and speed of HBM2 (16GB at up to 512GB/s) enables acceleration of memory-bound applications. The board's 100G QSFP28s are ideal for clustering, and OCuLink connectors allow expansion.

Both traditional HDL and higher abstraction C, C++ and OpenCL-based tool flows are supported. Deliverables include an optimized board support package (BSP) for the Intel OpenCL SDK.

The 520N-MX features a Board Management Controller (BMC) for advanced system monitoring and control, which greatly simplifies platform integration and management.

Tool Flow Flexibility for Software- or Hardware-Based Development

BittWare OpenCL FPGA Tools
- · OpenCL support for software-orientated customers
- · Abstration for faster development
- · Push-button flow for FPGA executable, driver, and API
- · Add optimized HDL IP cores to OpenCL designs as libraries
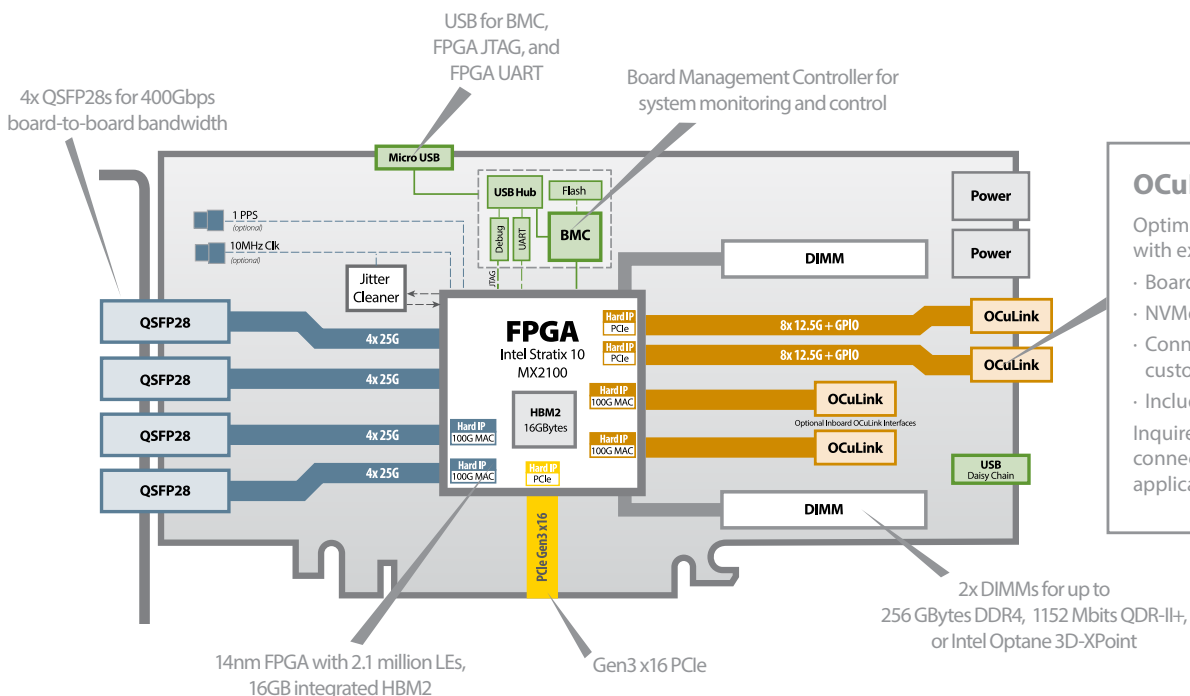
BittWare HDL FPGA Tools
- · Traditional VHDL/Verilog support for hardware-orientated customers
- · Hand-code for ultimate performance
- · High-Level Synthesis (HLS) available for rapid development
- · FPGA card designed to support standard Intel IP cores for Stratix 10

key features

| Intel Stratix 10 **MX2100** | 16GB HBM2 up to **512GB/s** | OpenCL BSP |

USB for BMC, FPGA JTAG, and FPGA UART

Board Management Controller for system monitoring and control

4x QSFP28s for 400Gbps board-to-board bandwidth

Micro USB

USB Hub · Flash · Debug · UART · BMC · JTAG

1 PPS *(optional)*
10MHz Clk *(optional)*

Jitter Cleaner

QSFP28 — 4x 25G
QSFP28 — 4x 25G
QSFP28 — 4x 25G
QSFP28 — 4x 25G

FPGA Intel Stratix 10 MX2100

Hard IP 100G MAC · HBM2 16GBytes · Hard IP 100G MAC · Hard IP PCIe

Hard IP PCIe — 8x 12.5G + GPIO — OCuLink
Hard IP PCIe — 8x 12.5G + GPIO — OCuLink
Hard IP 100G MAC — OCuLink
Hard IP 100G MAC — OCuLink

Optional Inboard OCuLink Interfaces

DIMM

Power
Power

USB Daisy Chain

DIMM

PCIe Gen3 x16

OCuLink Expansion Ports

Optimize the 520N-MX for your application with expansion:
- · Board-to-board interconnect
- · NVMe access for storage acceleration
- · Connect to accessory boards for customization options
- · Includes GPIO

Inquire about customized Molex connectors/cables as required for your application.

14nm FPGA with 2.1 million LEs, 16GB integrated HBM2

Gen3 x16 PCIe

2x DIMMs for up to 256 GBytes DDR4, 1152 Mbits QDR-II+, or Intel Optane 3D-XPoint

Additional Services

Take advantage of BittWare's range of design, integration, and support options

Customization
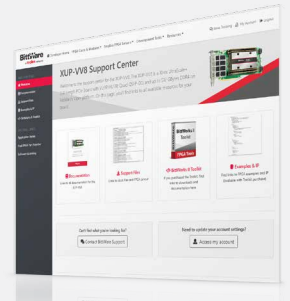Additional specification options or accessory boards to meet your exact needs.

Server Integration
Available pre-integrated in our TeraBox servers in a range of configurations.

Application Optimization
Ask about our services to help you port, optimize, and benchmark your application.

Service and Support
BittWare Developer Site provides online documentation and issue tracking.

Board Specifications

FPGA	• Intel Stratix 10 MX
	  • MX2100 in an F2597 package
	  • 16GBytes on-chip High Bandwidth Memory (HBM2) DRAM, 410 GB/s (speed grade 2)
	  • Core speed grade -2: I/O speed grade -2
	• Contact BittWare for other Stratix 10 MX options

On-board Flash	• 2Gbit Flash memory for booting FPGA
External memory	• 2x 288-pin DIMM slots each fitted with 16GB modules by default, i.e., 32GB total on board (options up to 256GB total) • Contact BittWare for QDR-II+ & Intel Optane (3D-Xpoint) DIMM options
Host interface	• x16 Gen3 interface direct to FPGA, connected to PCIe hard IP
QSFP cages	• 4 QSFP28 cages on front panel connected directly to FPGA via 16 transceivers • User programmable low jitter clocking supporting 10/25/40/100GbE • Each QSFP28 can be independently clocked • Jitter cleaner for network recovered clocking • 2 QSFP28s have available 100GbE MAC hard IP
OCuLink	• 2x edge connectors (A, B) @ 12.5G per lane (default); each supports PCIe Gen 3 x8 hard IP, GPIO, and PCIe master and optional input clocking • 2x inner connectors (C, D) @ 25G per lane (optional); 1x 100GbE MAC hard IP per OCuLink
Board Management Controller	• Voltage, current, temperature monitoring • Power sequencing and reset • Field upgrades • FPGA configuration and control • Clock configuration • Low bandwidth BMC-FPGA comms with SPI link • USB 2.0 • PLDM support • Voltage overrides

Cooling	• Standard: double-width active heatsink (with fan) • Optional: double-width passive heatsink • Optional: double-width liquid cooling
Electrical	• On-board power derived from 12V PCIe slot & two AUX connectors (one 8-pin, one 6-pin) • Power dissipation is application dependent • Typical max power consumption 225W
Environmental	• Operating temperature: 5°C to 35°C
Quality	• Manufactured to ISO9001:2015 IPC-A-610-Class III • RoHS compliant • CE, FCC & ICES approvals
Form factor	• Standard-height PCIe dual-slot board • 4.376 x 10.5 inches (111 x 266.7 mm)

Development Tools

|	
FPGA development	BIST - Built-In Self-Test for CentOS 7 provided with source code (pinout, gateware, PCIe driver & host test application)
Application development	Supported design flows - Intel FPGA OpenCL SDK, Intel High-Level Synthesis (C/C++) & Quartus Prime Pro (HDL, Verilog, VHDL, etc.)

Deliverables

• 520N-MX FPGA board
• USB cable (front panel access)
• Built-In Self-Test (BIST)
• OpenCL HPC Board Support Package (BSP)
• 1-year access to online Developer Site
• 1-year hardware warranty

To learn more, visit **www.BittWare.com**

intel. STRATiX 10

intel partner Titanium
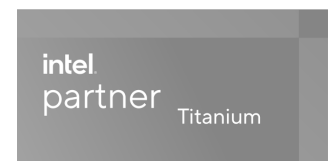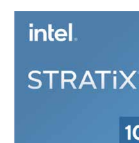
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