HFC0500

Fixed Frequency Flyback Controller with Ultra-low No Load Power Consumption

The Future of Analog IC Technology®

DESCRIPTION

HFC0500 is a fixed-frequency current-mode controller with internal slope compensation. It is specifically designed for the medium-power, off-line, flyback, switch-mode power supplies. HFC0500 is a green-mode highly efficient controller. At light loads, the controller freezes the peak current and reduces its switching frequency down to 25kHz to offer excellent light-load efficiency. At very light loads, the controller enters burst mode to achieve very low standby power consumption.

HFC0500 offers frequency jittering to help dissipate energy generated by conducted noise.

HFC0500 employs overpower compensation function to narrow the difference of over power protection point between low line and high line.

HFC0500 also has X-cap discharge function to discharge the X-cap when the input is unplugged. This aids in lowering no load power.

HFC0500 features multiple protections that include thermal shutdown (TSD), VCC under-voltage lockout (UVLO), overload protection (OLP), over-voltage protection (OVP), and brown-out protection.

HFC0500 is available in an SOIC8-7A package.

FEATURES

- Fixed-frequency current-mode control with internal slope compensation
- Frequency foldback down to 25kHz at light loads
- Burst mode for low standby power consumption, meeting EuP Lot 6
- Frequency jitter to reduce EMI signature
- X-cap discharge function
- Adjustable overpower compensation
- Internal high-voltage current source
- VCC under-voltage lockout with hysteresis (UVLO)
- Brown-out protection on HV
- Overload protection with programmable delay
- Thermal shutdown (auto-restart with hysteresis)
- Latch-off for external over-voltage protection (OVP) and over-temperature protection (OTP) on TIMER
- Latch-off for Vcc over voltage protection
- Short-circuit protection
- Programmable soft start

APPLICATIONS

- AC/DC power for small and large appliances
- AC/DC adapters for notebook computers, tablets, and smart phones
- Offline battery chargers
- LCD TVs and monitors

All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance.

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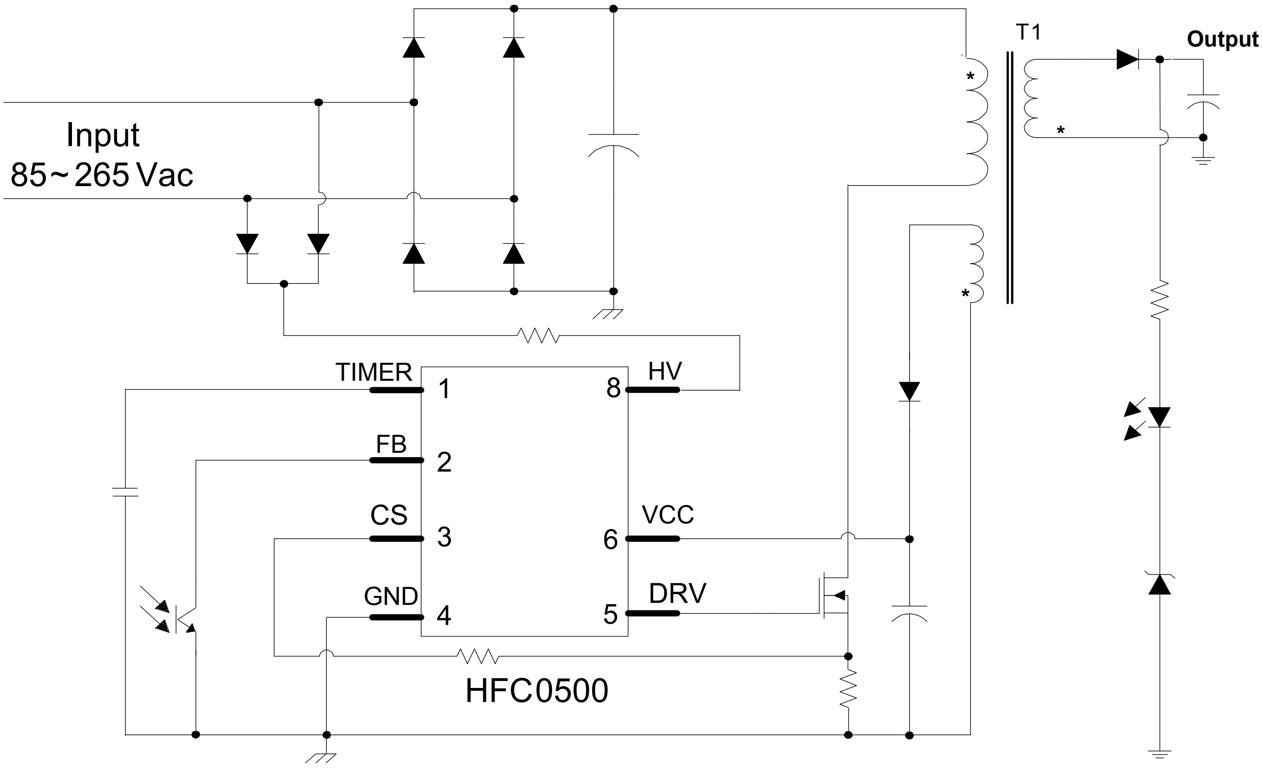
TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number*	Package	Top Marking
HFC0500GS	SOIC8-7A	*See Below*

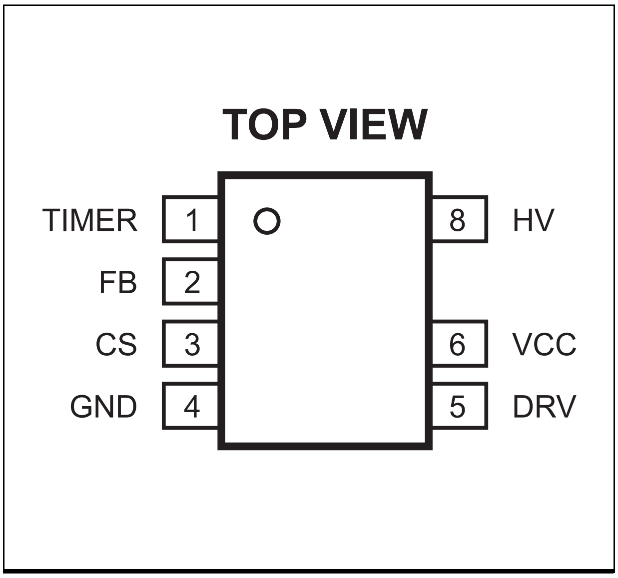
* For Tape & Reel, add suffix –Z (e.g. HFC0500GS–Z);

TOP MARKING

HFC0500
LLLLLLLL
MPSYWW

HFC0500: first seven digits of the part number;
LLLLLLLL: lot number;
MPS: MPS prefix:
Y: year code;
WW: week code:

PACKAGE REFERENCE



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ABSOLUTE MAXIMUM RATINGS [(1)]

HV .... -0.7V to 700V
V_{CC}, DRV to GND............................ -0.3V to 30V
FB, TIMER, CS to GND .... -0.3V to 7V
Continuous Power Dissipation (T_A = +25°C) [(2)]
.... 1.3W
Junction Temperature................................ 150°C
Lead Temperature .... 260°C
Storage Temperature ....-60°C to +150°C
ESD Capability Human Body Model (except HV and DRV) 4.0kV
ESD Capability Human Body Model (DRV) 3.5kV
ESD Capability Human Body Model (HV) 1.8kV
ESD capability for Machine Mode 400V

Recommended Operation Conditions [(3)]

Operating Junction Temp (T_J) ..-40°C to +125°C
Operating V_{CC} range .... 9V to 24V

Thermal Resistance [(4)]

	θ_{JA}	θ_{JC}	
SOIC8-7A	96	45	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERICS

V_{CC}=18V, T_J=-40°C ~ 125°C, Min & Max are guaranteed by characterization, typical is tested under 25℃, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Start-up Current Source (HV)						
Supply Current from HV	I_{HV_400}	V_{CC}= 12V, V_{HV}=400V	1.5	2.8	5	mA
	I_{HV_120}	V_{CC}= 12V, V_{HV}=120V	1.5	2.7	5	
Leakage Current from HV	I_{LK_400}	V_{CC} increases to 18V then decreases to 14V, V_{HV}=400V	1	16	25	μA
	I_{LK_200}	V_{CC} increases to 18V then decreases to 14V, V_{HV}=200V	1	13	22	μA
Break Down Voltage	V_{BR}	T_J = 25°C	700	790		V
Supply Voltage Management (V_{CC})						
VCC Increasing Level at which the Current Source Turns-Off	VCC_{OFF}		12.5	15.5	18	V
VCC Decreasing Level above which Soft Start Takes Place if HV>HV_{ON}	VCC_{SS}		10.5	12	13	V
VCC Hysteresis for Brown-in Detection	VCC_{OFF} - VCC_{SS}		1.35	3.5		V
VCC Decreasing Level at which the Current Source Turns-On	VCC_{ON}		7.3	8.5	9.6	V
VCC UVLO Hysteresis	VCC_{OFF} - VCC_{ON}		5	7		V
VCC Re-charge Level when Protection Takes Place	VCC_{PRO}		4.9	5.5	6.2	V
VCC Decreasing Level at which the Latch off Phase Ends	VCC_{LATCH}			2.5		V
Internal IC Consumption	I_{CC}	V_{FB}=2V,C_L=1nF, V_{CC}=12V	1.1	1.8	2.7	mA
Internal IC Consumption, Latch off Phase	$I_{CCLATCH}$	V_{CC}=VCC_{OFF}-1V, T_J=25℃	520	700	880	μA
Voltage on the VCC above which the Controller Latches off (OVP)	V_{OVP}		24	26.5	28.5	V
Blanking Duration on the OVP Comparator	T_{OVP}			60		μs

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ELECTRICAL CHARACTERICS *(continued)*

V_{CC}=18V, T_J=-40°C ~125°C, Min & Max are guaranteed by characterization, typical is tested under 25℃, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Brown-out						
HV Turn on Threshold Voltage	HV_{ON}	V_{HV} going up,T_J=25℃	95	107	119	V
HV Turn off Threshold Voltage	HV_{OFF}	V_{HV} going down, T_J=25℃	86	97	110	V
Brown-out Hysteresis	ΔHV	T_J=25℃	7.5	10	12.5	V
Timer Duration for Line Cycle Drop-out	T_{HV}	C_{TIMER}=47nF	40			ms
Oscillator						
Oscillator Frequency	f_{OSC}	V_{FB}>1.85V,T_J=25℃	62	65	68	kHz
Frequency Jittering Amplitude, in Percentage of f_{OSC}	A_{jitter}	V_{FB}>1.85V,T_J=25℃	±5	±6.5	±8.3	%
Frequency jittering entry level	V_{FB_JITTER}				1.95	V
Frequency Jittering Modulation Period	T_{jitter}	C_{TIMER}=47nF		3.7		ms
Current Sense						
Current Limit Point	V_{ILIM}		0.93	1	1.07	V
Short Circuit Protection Point	V_{SCP}		1.3	1.47	1.63	V
Current limitation when frequency foldback	V_{FOLD}	V_{FB}=1.85V	0.63	0.68	0.73	V
Current limitation when entry Burst	V_{IBURL}	V_{FB}=0.7V		0.11		V
Current limitation when leave Burst	V_{IBURH}	V_{FB}=0.8V		0.15		V
Leading Edge Blanking for V_{ILIM}	T_{LEB1}			350		ns
Leading Edge Blanking for V_{SCP}	T_{LEB2}			270		ns
Slope of the Compensation Ramp	S_{RAMP}		18	25	32	mV/µs
Feedback (FB)						
Internal Pull-up Resistor	R_{FB}		11.5	14	16.5	kΩ
Internal Pull-up Voltage	V_{DD}			4.3		V
V_{FB} to Internal Current Setpoint Division Ratio	K_{FB1}	V_{FB}=2V	2.55	2.8	3.05	--
V_{FB} to Internal Current Setpoint Division Ratio	K_{FB2}	V_{FB}=3V	2.8	3.1	3.4	--
FB Decreasing Level at which the Controller Enters the Burst Mode	V_{BURL}		0.63	0.7	0.77	V
FB Increasing Level at which the Controller Leaves the Burst Mode	V_{BURH}		0.72	0.8	0.88	V

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ELECTRICAL CHARACTERICS *(continued)*

V_{CC}=18V, T_J=-40°C ~125°C, Min & Max are guaranteed by characterization, typical is tested under 25℃, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Over Load Protection						
FB Level at which the Controller Enters the OLP after a Dedicated time	V_{OLP}			3.7		V
Time Duration before OLP when FB Reaches Protection Point	T_{OLP}	C_{TIMER}=47nF	40			ms
Over Power Compensation						
V_{HV} to I_{OPC} Ratio	K_{OPC}			0.45		μA/V
Current out of CS	I_{OPC}	V_{HV}=120V,V_{FB}=2.5V		0		μA
		V_{HV}=155V,V_{FB}=2.5V		13		
		V_{HV}=310V,V_{FB}=2.5V		85		
		V_{HV}=380V,V_{FB}=2.5V, T_J=25℃	90	119	148	
FB Voltage below which Compensation is Removed	$V_{OPC(OFF)}$		0.55			V
FB Voltage above which Compensation is Applied Fully	$V_{OPC(ON)}$				2.2	V
Frequency Foldback						
FB Voltage Threshold below which Frequency Foldback Starts	$V_{FB(FOLD)}$			1.8		V
Minimum Switching Frequency	$F_{OSC(min)}$	T_J=25℃	21	25	30	kHz
FB Voltage Threshold below which Frequency Foldback Ends	$V_{FB(FOLDE)}$			1.0		V
Latch-off Input(Integration in TIMER)						
The Threshold below which Controller is Latched	$V_{TIMER(LATCH)}$		0.7	1	1.3	V
Blanking Duration on Latch Detection	T_{LATCH}			12		μs

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ELECTRICAL CHARACTERICS *(continued)*

V_{CC}=18V, T_J=-40°C~125°C, Min & Max are guaranteed by characterization, typical is tested under 25℃, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DRV Voltage						
Driver Voltage High Level	V_{High}	C_L=1nF,V_{CC}=12V		10.3		V
Driver Voltage Clamp Level	V_{Clamp}	C_L=1nF,V_{CC}=24V		13.4		V
Driver Voltage Low Level	V_{Low}	C_L=1nF,V_{CC}=24V		16		mV
Driver Voltage Rise Time	T_R	C_L=1nF,V_{CC}=16V		13		ns
Driver Voltage Fall Time	T_F	C_L=1nF,V_{CC}=16V		23		ns
Driver Pull-up Resistance	$R_{Pull-up}$	C_L=1nF,V_{CC}=16V		8		Ω
Driver Pull-down Resistance	$R_{Pull-down}$	C_L=1nF,V_{CC}=16V		10		Ω
Thermal Shutdown						
Thermal Shutdown Threshold (5)				150		℃
Thermal Shutdown Hysteresis (5)				25		℃

Notes:

5) This parameter is guaranteed by design.

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PIN FUNCTIONS

Pin #	Name	Description
1	TIMER	Timer. This pin combines the soft start, frequency jittering, along with the timer functions for OLP, brown-out protection, and X-cap discharge. The IC can be latched off by pulling this pin low.
2	FB	Feedback. Use a pull-down opto-coupler to control output regulation.
3	CS	Current Sense. Senses the primary side current for current-mode operation, and provides a means for over power compensation adjustment.
4	GND	IC Ground.
5	DRV	Drive Signal Output.
6	VCC	Power Supply.
8	HV	High-Voltage Current Source. Includes brown-out and X-cap discharge functions.

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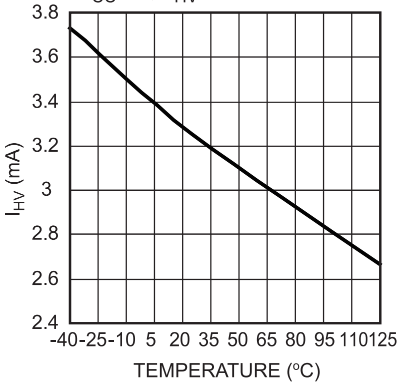
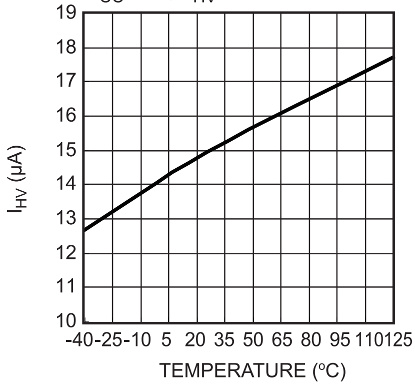
TYPICAL CHARACTERISTICS

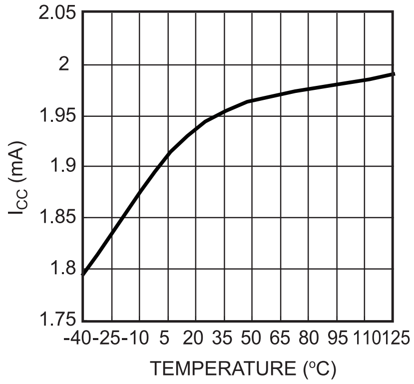
Supply Current from HV vs. Temperature
V_{CC}=6V, V_{HV}=400V



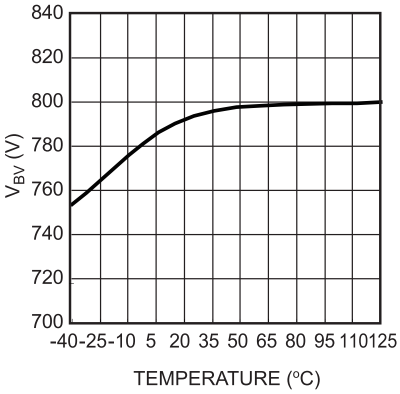
Leakage Current from HV vs. Temperature
V_{CC}=14V, V_{HV}=400V



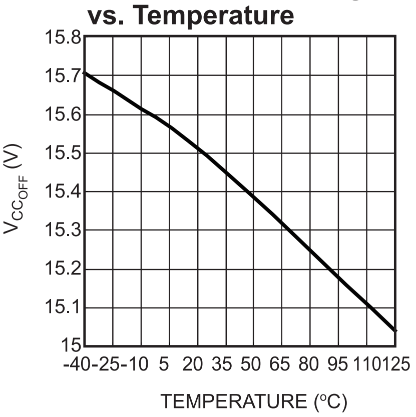
Internal IC Consumption vs. Temperature



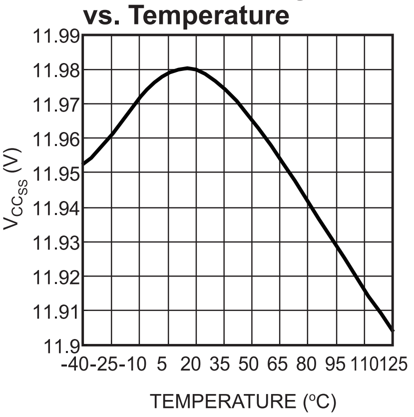
Break-Down Voltage vs. Temperature



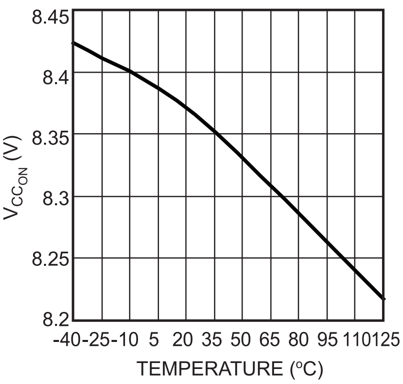
V_{CC} Curent-Source Turn-off Level, Rising vs. Temperature



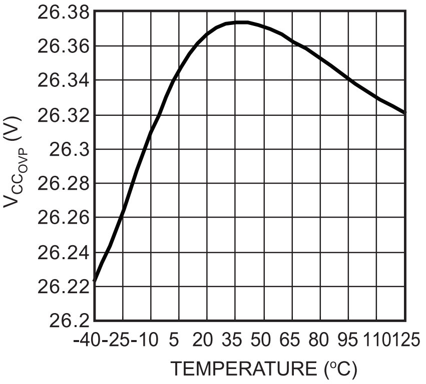
V_{CC} Threshold for HV Turn-On Detection, Falling vs. Temperature



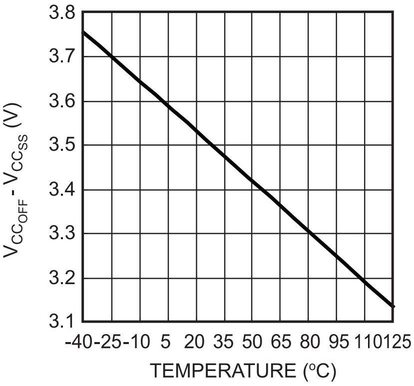
V_{CC} Current Source Turn-On Level, Falling vs. Temperature



Voltage above V_{CC} where the Controller Latchs off (OVP) vs. Temperature



V_{CC} Hysteresis for HV Turn-On Detection vs. Temperature



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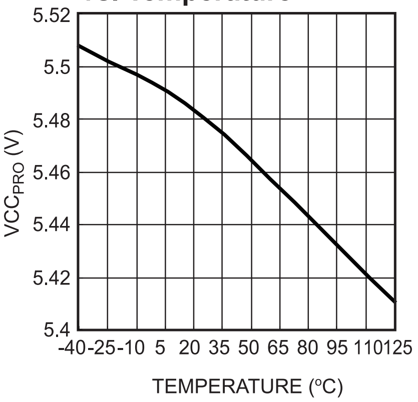
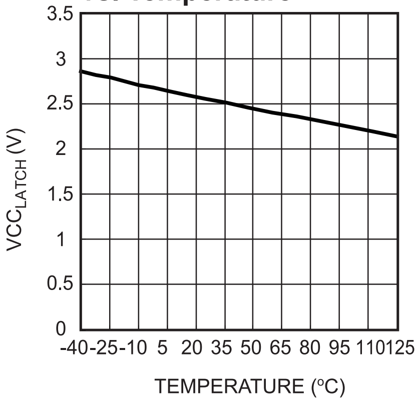
TYPICAL CHARACTERISTICS *(continued)*

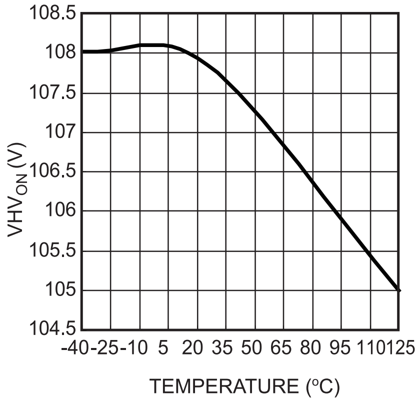
V_{CC} Recharge Level where Protection Occurs vs. Temperature



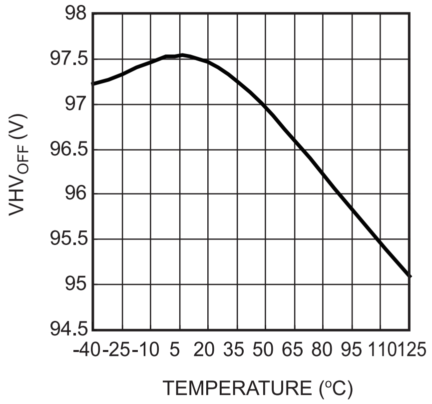
V_{CC} Decreasing Level when Latch-off Phase Ends vs. Temperature



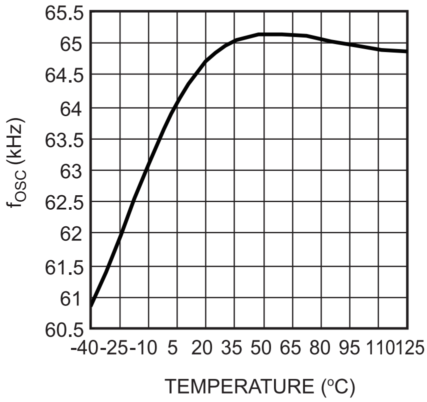
HV Turn-on Threshold vs. Temperature



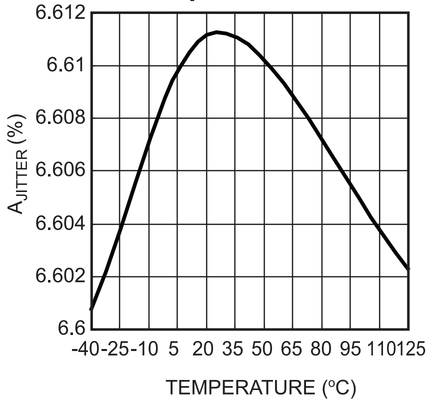
HV Turn-off Threshold vs. Temperature



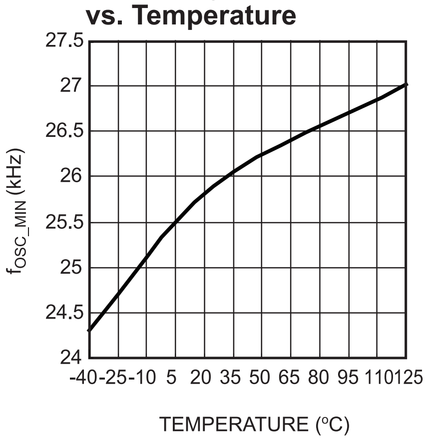
Oscillator Frequency vs. Temperature



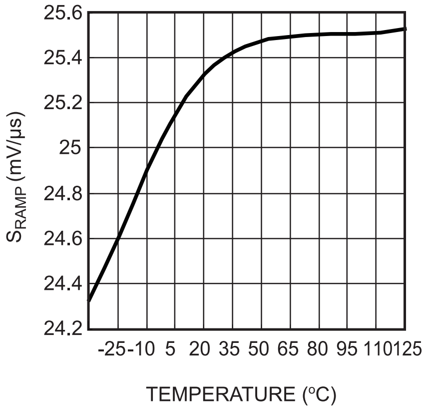
Frequency Jitter Amplitude in Percentage of f_{OSC} vs. Temperature



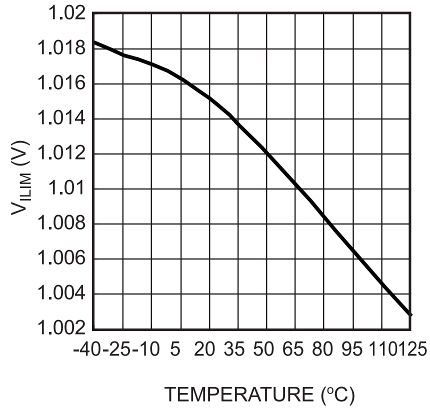
Minimum Switching Frequency vs. Temperature



Slope of the Compensation Ramp vs. Temperature



Current Limit vs. Temperature



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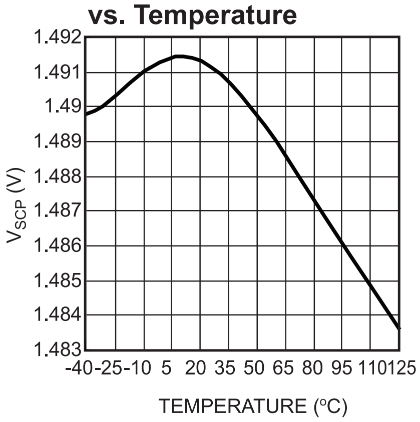
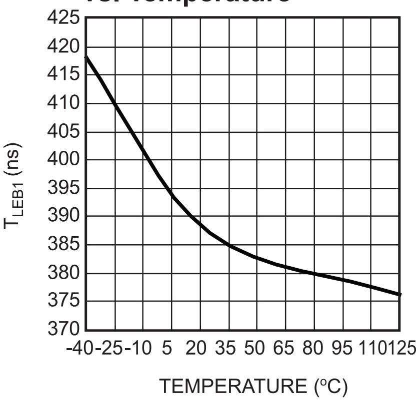
TYPICAL CHARACTERISTICS *(continued)*

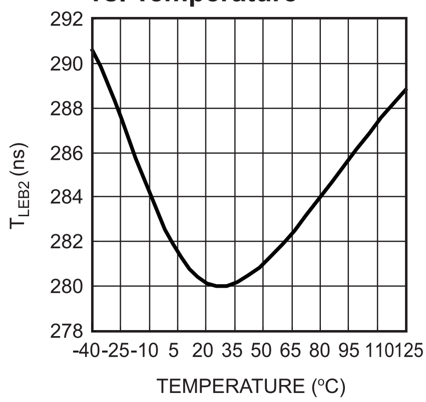
Short Circuit Protection Level vs. Temperature



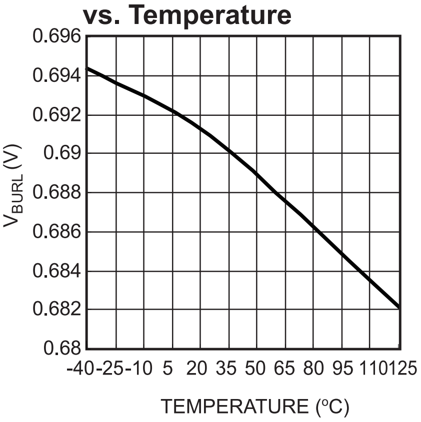
Leading Edge Blanking for V_{ILIM} vs. Temperature



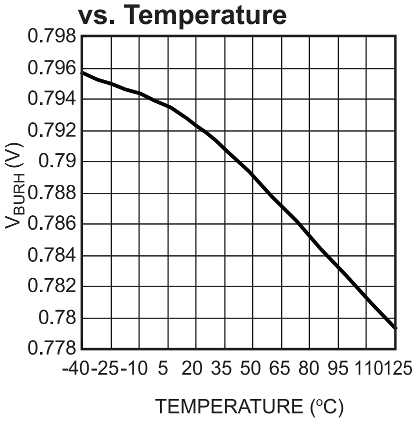
Leading Edge Blanking for V_{SCP} vs. Temperature



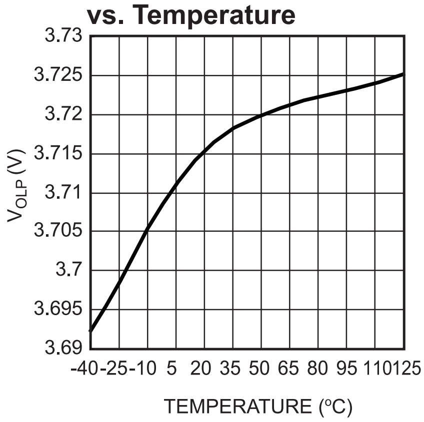
FB Level (Falling) at Which Controller Enters Burst Mode vs. Temperature



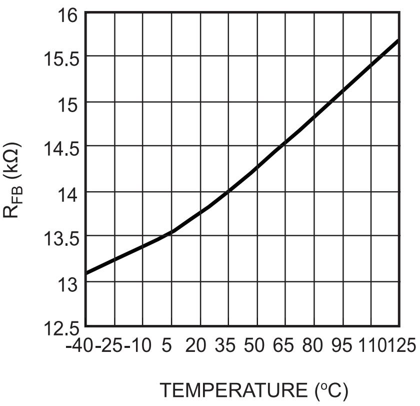
FB Level (Rising) at Which Controller Exits Burst Mode vs. Temperature



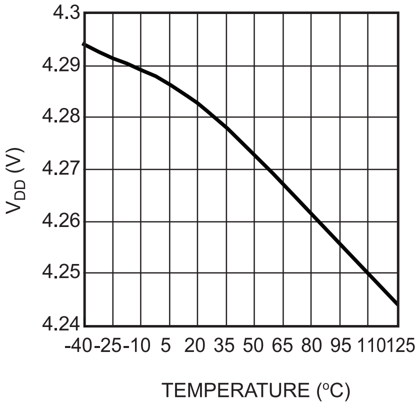
FB Level at Which Controller Enters OLP after Blanking Time vs. Temperature



FB Internal Pull-up Resistor vs. Temperature



FB Internal Pull-up Voltage vs. Temperature



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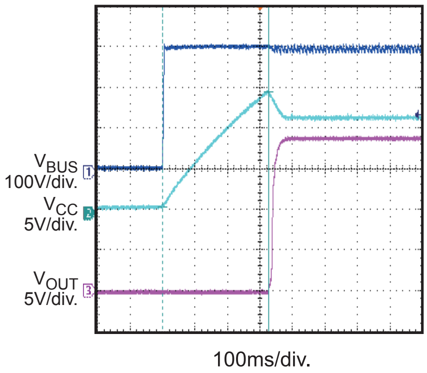
TYPICAL PERFORMANCE CHARACTERISIC

V_{IN}=230VAC, V_{OUT}=19V, I_{OUT}=2.35A, unless otherwise noted.

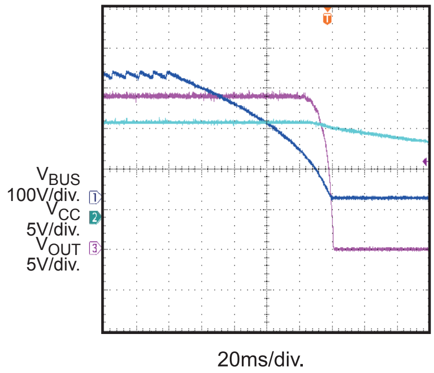
Input Power Start Up

$230V_{AC}$ Full Load

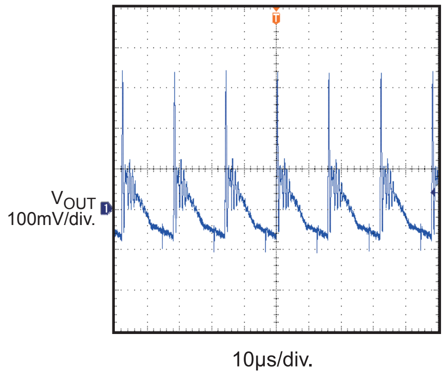


Input Power Shut Down

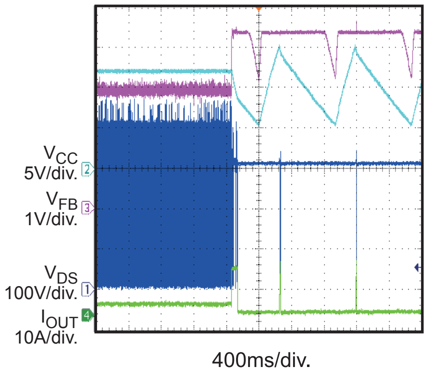
$230V_{AC}$ Full Load



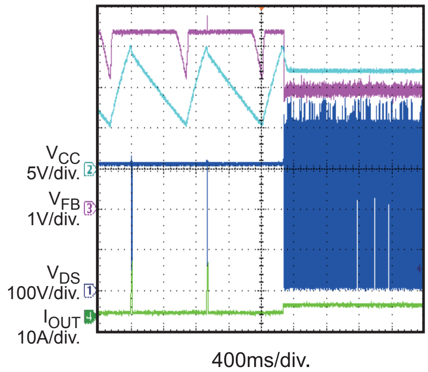
Output Ripple



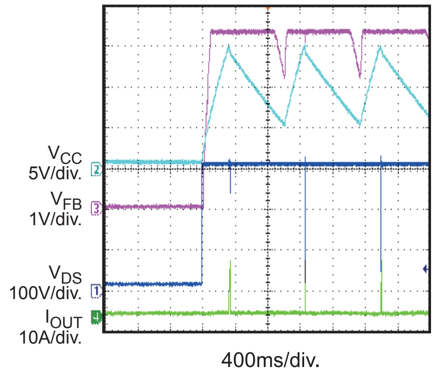
SCP Entery



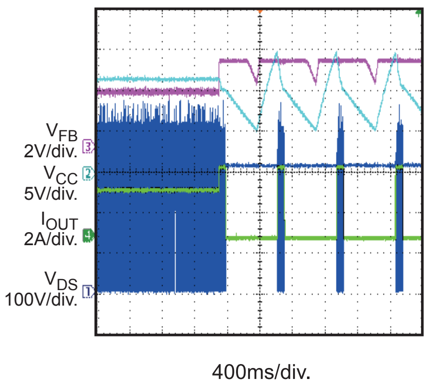
SCP Rescovery



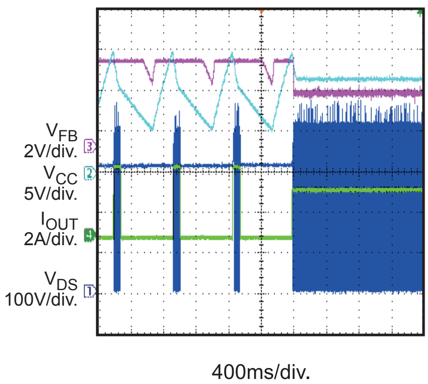
SCP Power On



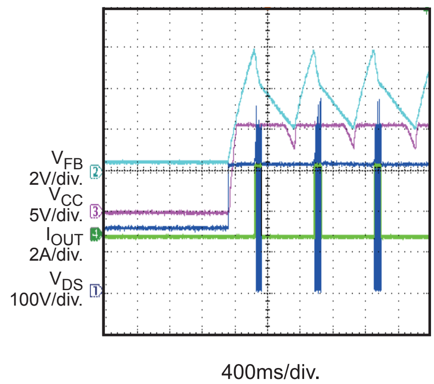
OLP Entry



OLP Rescovery



OLP Power On



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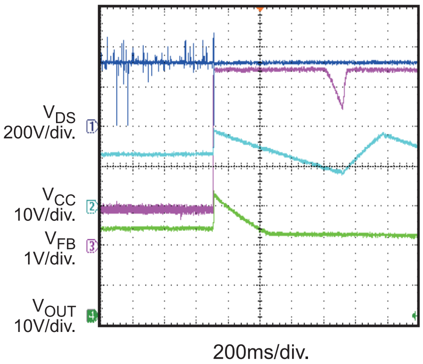
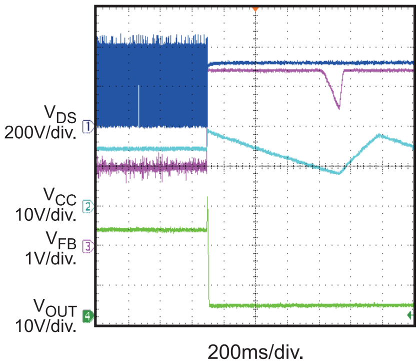
TYPICAL PERFORMANCE CHARACTERISIC *(continued)*

V_{IN}=230VAC, V_{OUT}=19V, I_{OUT}=2.35A, T_A=25°C, unless otherwise noted.

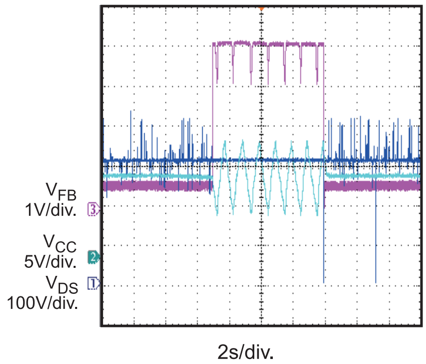
OVP
No Load



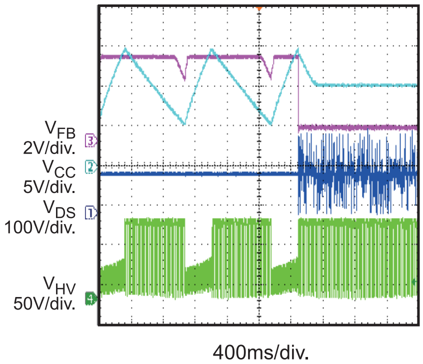
OVP
Full Load



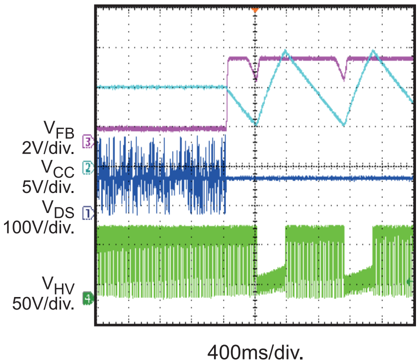
OTP
No Load



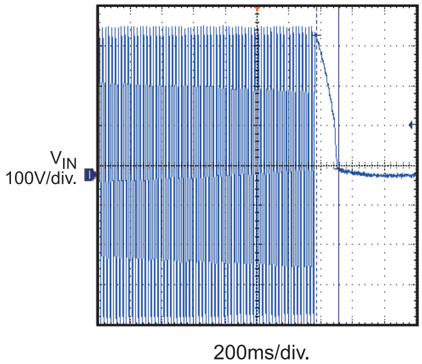
Brown-In



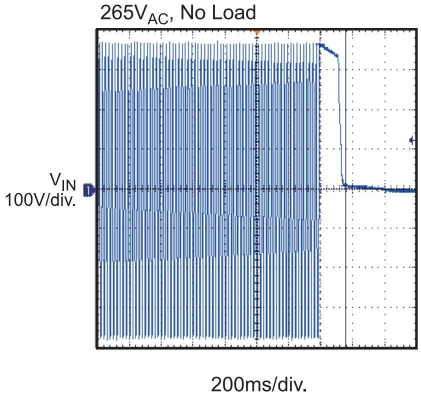
Brown-Out



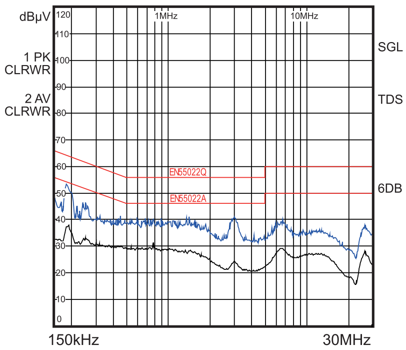
X-Cap Discharge
265V_{AC}, Full Load



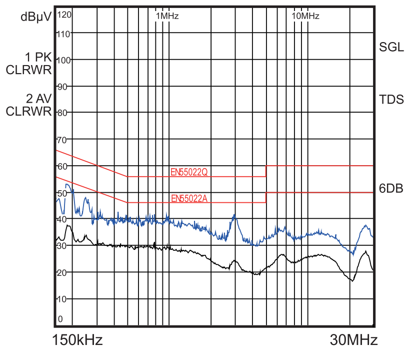
X-Cap Discharge
265V_{AC}, No Load



Conducted EMI
230V_{AC}, L Wire



Conducted EMI
230V_{AC}, N Wire



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TYPICAL PERFORMANCE CHARACTERISIC *(continued)*

V_{IN}=230VAC, V_{OUT}=19V, I_{OUT}=2.35A, T_A=25°C, unless otherwise noted.

No Load Power Consumption

V_{IN} (VAC/Hz)	85/60	115/60	230/50	265/50
P_{IN} (mW)	73.63	67.31	72.37	78.86

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OPERATION

HFC0500 incorporates all the necessary features to build a reliable switch-mode power supply. It is a fixed-frequency current-mode controller with internal slope compensation. At light loads, the controller freezes the peak current and reduces its switching frequency down to 25kHz to minimize switching losses. When the output power falls below a given level, the controller enters burst mode. It also has excellent EMI performance due to frequency jittering.

Its high level of integration requires very few external components.

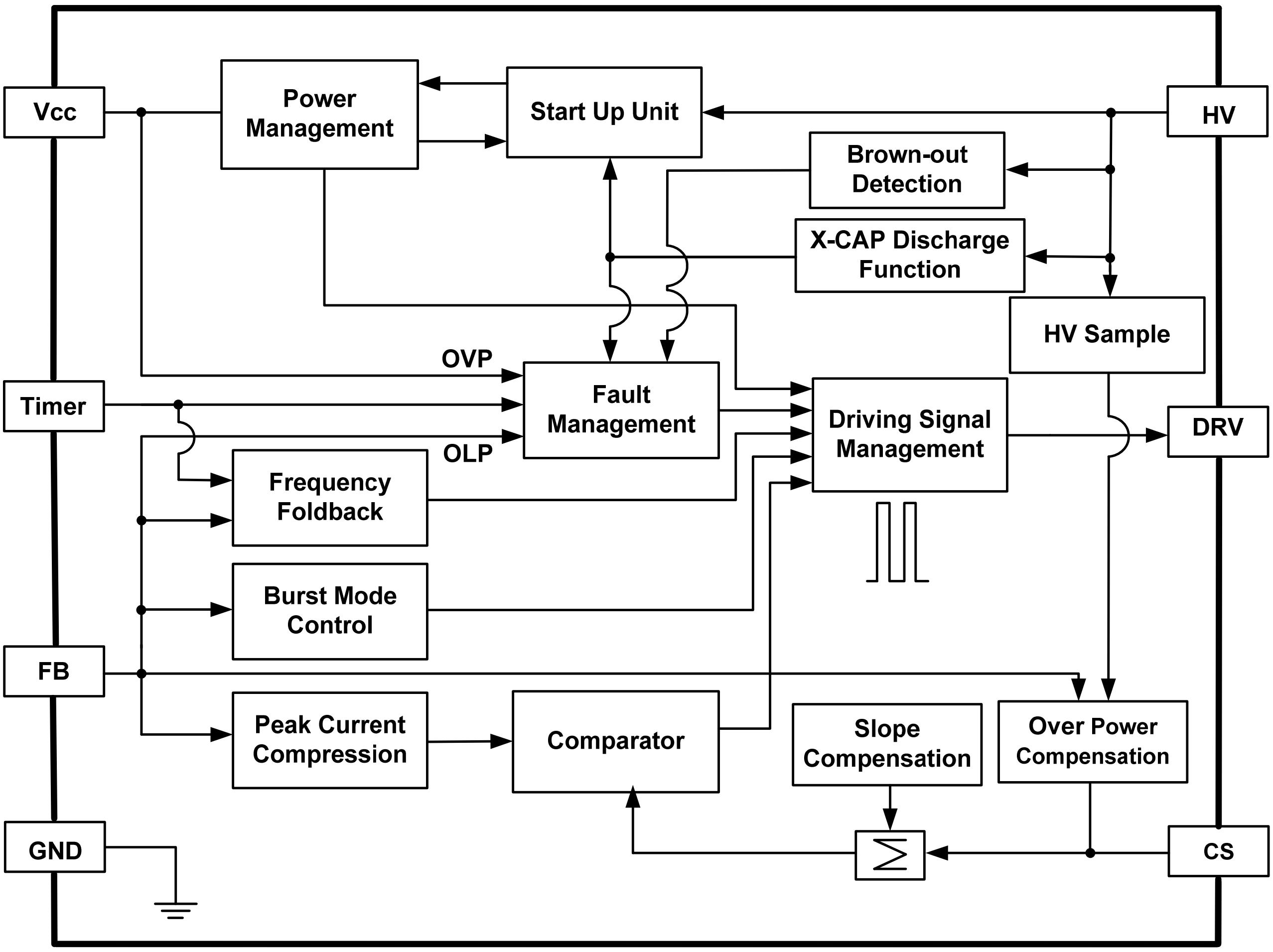

Figure 1: Functional Block Diagram

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Fixed-Frequency with Jitter

Frequency jitter reduces EMI by spreading the energy over the jitter frequency range. Figure 2 shows the circuit of frequency jittering.

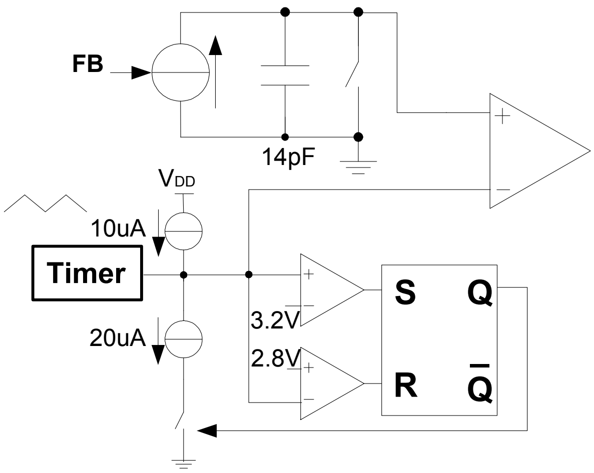

Figure 2: Frequency Jitter Circuit

A controlled current sourced (fixed at 2.72μA when V_{FB}=2V) charges the internal 14pF capacitor. Comparing the capacitor voltage to the TIMER voltage determines the switching frequency as per equation (1). Frequency jitter is accomplished by varing V_{TIMER} between 3.2V and 2.8V per equation (2).

$$f_s = \frac{1}{14pF \cdot V_{TIMER} / 2.72\mu A + 0.2\mu s} \quad (1)$$

$$T_{jitter} = 2 \cdot \frac{C_{TIMER} \cdot (3.2V - 2.8V)}{10\mu A} \quad (2)$$

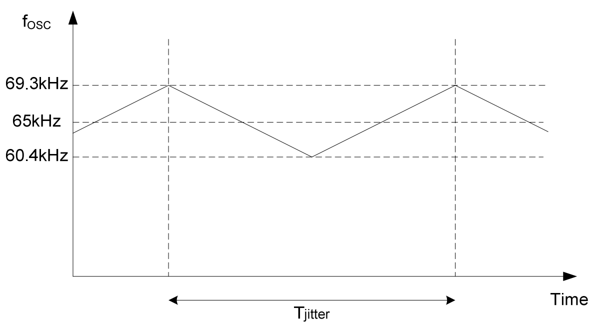

Figure 3: Frequency Jitter

Frequency Foldback

The HFC0500 implements frequency foldback at light load condition to improve overall efficiency.

When the load decreases to a given level (1.0V<V_{FB}<1.8V), the controller freezes the peak current (as measured on CS, typically 0.7V) while reducing its switching frequency to 25kHz. This reduces the switching loss. If the load continues to decrease, the peak current decreases with 25kHz fixed frequency to avoid audible noise. Figure 4 shows the frequency vs. V_{FB} and peak current (V_{CS}) vs. V_{FB}.

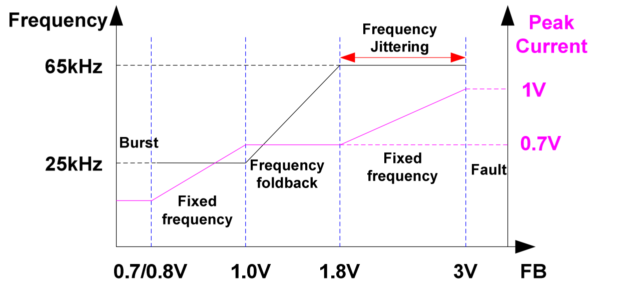

Figure 4: Frequency and Peak Current (V_{CS}) vs. V_{FB}

Current-Mode Operation with Slope Compensation

V_{FB} controls the primary-peak current. When the peak current reaches the level determined by V_{FB}, DRV turns off. The controller can also be used in continuous conduction mode (CCM) with a wide input voltage range because of its internal slope compensation (25mV/μs, typical), avoiding sub-harmonic oscillations above 50% duty cycle.

High Voltage Startup Current Source with Brown-Out Detection

At start up, the internal high-voltage current source from HV supplies the IC. The IC turns off the current source as soon as V_{CC} reaches VCC_{OFF} (15V, typical), and detects the voltage on HV. Once the HV voltage exceeds HV_{ON} before V_{CC} drops down to VCC_{SS} (12V, typical), the controller starts switching. Otherwise the system treats the condition as a brown-out and

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latches DRV low. When V_{CC} drops to VCC_{PRO} (5.3V, typical), the high-voltage current source turns on to recharge V_{CC}. The auxiliary transformer winding supplies the IC after the controller starts switching. If V_{CC} falls below VCC_{ON} (8.0V, typical), the switching pulse stops and the current source turns on again. Figure 5 shows the typical V_{CC} under-voltage lockout waveform.

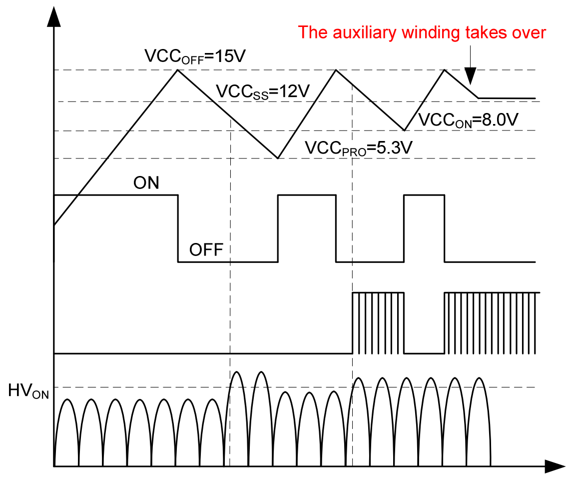

Figure 5: V_{CC} Under-Voltage Lockout

The V_{CC} lower threshold UVLO drops from 8V to 5.3V under fault conditions, such as OLP, SCP, brown-out, and OTP.

Soft Start

Soft start is externally programmable with a capacitor on TIMER. As this capacitor charges from 1V to 1.75V with 1/4 the normal charge current, the peak current limit threshold gradually increases from 0.25V to 1V while gradually increasing the switching frequency. Figure 6 shows the typical soft-start waveform. The TIMER capacitor determines the start-up duration as follow equation (3).

$$T_{Soft-start} = \frac{C_{TIMER} \cdot (1.75V - 1V)}{10/4\mu A} \quad (3)$$

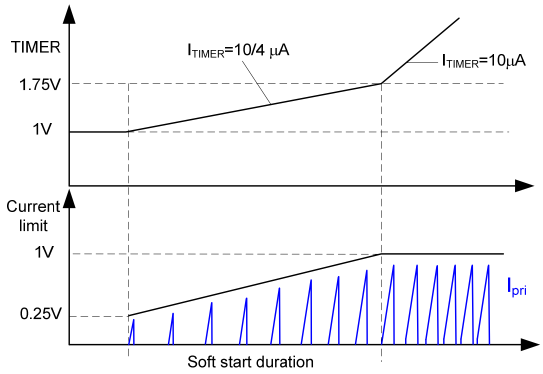

Figure 6: Soft-Start

Burst Mode

To minimize power dissipation in no load or light load, HFC0500 employs burst-mode operation. As the load decreases, V_{FB} decreases. The IC will enter burst-mode when V_{FB} drops below the lower threshold V_{BURL}(0.7V, typical), stopping output switching. At this point, the output voltage starts to drop, which causes V_{FB} to increase again. Once V_{FB} exceeds V_{BURH}(0.8V, typical), switching resumes. Burst mode alternately enables and disables MOSFET switching, thereby reducing no load or light load switching losses.

Adjustable Over Power Compensation

An offset current which is proportional to the input voltage is added to current sense voltage. By choosing the value of the resistor in series with the CS, the amount of compensation can be adjusted to the application for more accurate output power limit at total input range. Figure 7 and Figure 8 show the compensation current relation to FB and peak voltage on HV respectively.

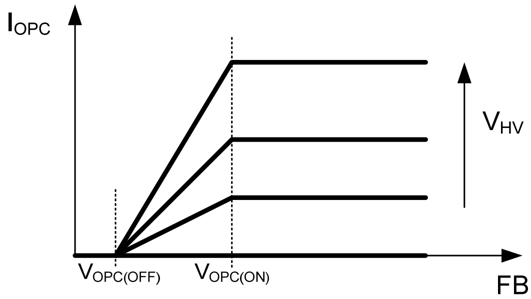

Figure 7: Compensation Current vs. FB and HV Voltage

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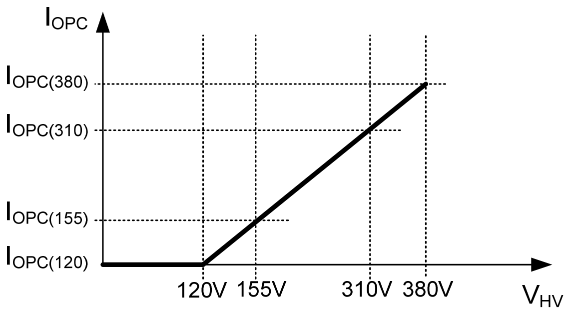

Figure 8: Compensation Current vs. Peak of Rectified Input Line AC Voltage

Timer-Based Over-Load Protection

In a flyback converter, if the switching frequency is fixed, maximum output power is limited by the peak current. The output voltage drops below the set value when the output power exceeds the power limit. This reduces the current through the opto-coupler, pulling V_{FB} high.

When FB is higher than V_{OLP} (3.7V, typical) which is considered as an error flag, the timer begins to count. If the error flag is removed during the count, the timer resets. If the timer count reaches 17, OLP triggers. This timer duration avoids triggering OLP during the power supply start-up or short load transients. Figure 9 shows OLP function.

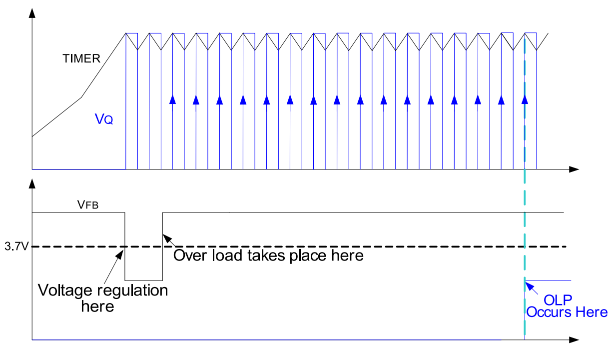

Figure 9: Over Load Takes Place Here

Timer-Based Brown-Out Protection

The brown-out protection block is similar to the OLP block. When the HV voltage drops below HV_{OFF} (98V, typical) which is considered as an error flag, the timer starts to count. Once the HV voltage is higher than HV_{OFF}, the timer resets. When the timer counts to 17, brown-out protection triggers and the switching stops.

Short-Circuit Protection (SCP)

The HFC0500 has short-circuit protection if V_{CS} reaches V_{SCP} (1.45V, typical) after a reduced leading-edge blanking time (T_{LEB2}). As soon as the fault disappears, the power supply resumes operation.

Thermal Shutdown (TSD)

To prevent any thermal damage, HFC0500 stops switching when the temperature exceeds 150°C. As soon as the temperature drops below 125°C, the power supply resumes operation. During TSD, the V_{CC} UVLO lower threshold drops from 8.0V to 5.3V.

V_{CC} Over-Voltage Protection (OVP)

The HFC0500 enters latched fault condition if V_{CC} goes above V_{OVP} (26.5V, typical) for 60µs. The controller stays fully latched until V_{CC} drops below VCC_{LATCH} (2.5V, typical), i.e. when the user unplugs the power supply from the main input and re-plugs it. The situation usually happens when the opto-coupler fails, which results in the loss of output voltage regulation.

TIMER Latch-Off for OVP and OTP

Pulling TIMER down lower than $V_{TIMER(LATCH)}$ (1V, typical) for 12µs can also latch off the IC. This function can be used for external OVP and OTP etc.

X-Cap Discharge Function

X capacitors are typically positioned across a power supply's input terminals to filter differential mode EMI noise. These components pose a potential hazard because they can store unsafe levels of voltage energy after the AC line is disconnected. Generally, resistors in parallel to the X-cap provide a discharge path to meet safety standards, but these discharge resistors produce a constant loss while the AC is connected, and contribute to no-load and standby input power consumption.

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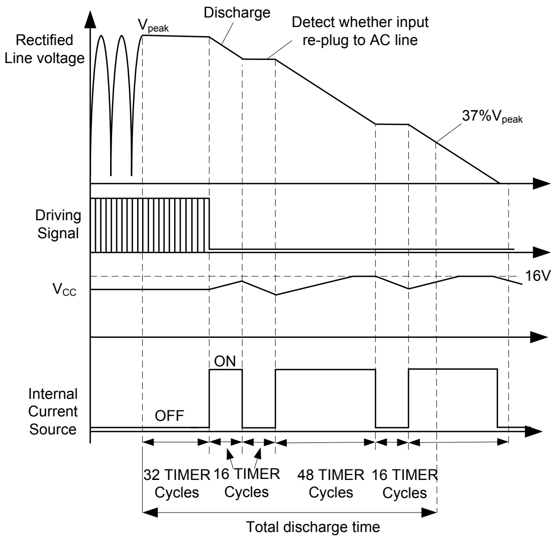

Figure 10: X-Cap Discharger

The HFC0500's HV acts as a smart X-cap discharger. When the AC voltage is applied, the internal high-voltage current source turns off to block HV current and the IC monitors the HV voltage. When removing the AC voltage, the IC turns on the high-voltage current source after about 32 TIMER cycles to discharge the X-cap energy. The first discharge duration is 16 cycles. After the first discharge, the IC turns off the current source for 16 cycles to detect whether the input is re-plugged to the AC line. If the AC input remains disconnected, the IC turns on the current source for 48 cycles to discharge again, and then off for 16 cycles to re-detect repeatedly until the voltage on X-cap drops to V_{CC}. Once the reconnected AC input is detected, the high-voltage current source remains off until V_{CC} drops to VCC_{PRO} (5.3V), and then restarts the system by recharging Vcc. Figure 10 shows the discharge function waveforms.

This approach provides an intelligent discharge path for the X-cap, eliminating the power loss form external discharge resistors.

Clamped Driver

DRV is clamped at V_{Clamp} (13.4V, typical) when V_{CC} exceeds 16V, allowing the use of any standard MOSFET.

Leading-Edge Blanking

An internal leading-edge blanking (LEB) unit containing two LEB times is employed between the CS and the current comparator input to avoid premature switching pulse termination due to parasitic capacitances. During the blanking time, the current comparator is disabled and can not turn off the external MOSFET. Figure 11 shows the LEB waveform.

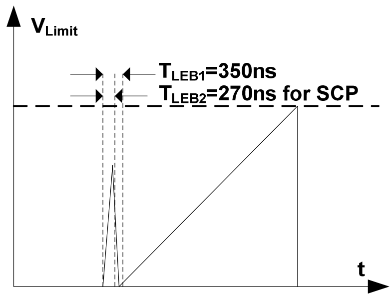

Figure 11: Leading-Edge Blanking

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APPLICATION INFORMATION

VCC Capacitor Selection

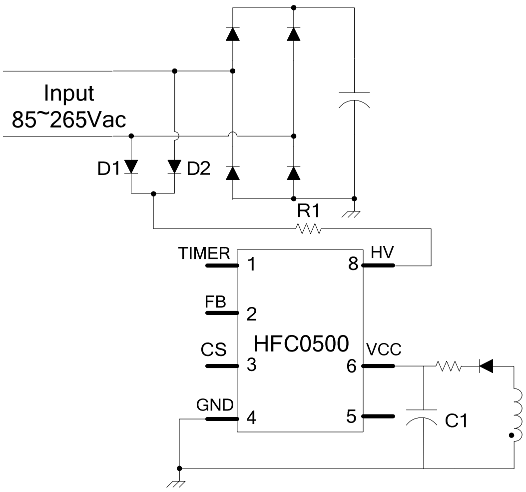

Figure 12: Start-Up Circuit

Figure 12 shows the start-up circuit. The values of R1 and C1 determine the system start-up delay time: a larger R1 or C1 increases the start-up delay. The V_{CC} duration (from $V_{CC,OFF}$ to $V_{CC,SS}$) for brown-out detection should exceed half of the input period, equation (4) provides an estimated value for the V_{CC} capacitor, where $I_{CC(noswitch)}$ is the internal consumption (close to $I_{CClatch}$), and T_{input} is period of the AC input. For most applications, choose a V_{CC} capacitor value that exceeds 10µF.

$$C_{VCC} > \frac{I_{CC(noswitch)} \cdot 0.5 \cdot T_{input}}{VCC_{OFF} - VCC_{SS}} \qquad (4)$$

A higher value R1 decreases the current of internal high-voltage current source especially at low input condition. It is necessary to make sure the practical supply current from HV is not smaller than the corresponding internal IC consumption current which is the same as $I_{CCLATCH}$. Thus for universal input range R1 should be smaller than 80k and 20k is generally recommended.

Primary-Side Inductor Design (L_m)

With internal slope compensation, HFC0500 supports CCM when the duty cycle exceeds 50%. Set a ratio (K_P) of the primary inductor's ripple current amplitude vs. the peak current value to $0<K_P\leq1$, where K_P=1 for DCM. Figure 13 shows the relevant waveforms. A larger inductor leads to a smaller K_P, which can reduce RMS current but increase transformer size. An optimal K_P value is between 0.6 and 0.8 for the universal input range and 0.8 to 1 for 230VAC input range.

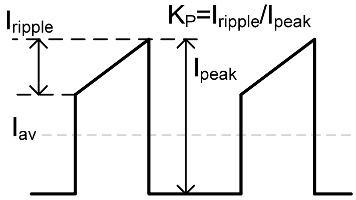

Figure 13: Typical Primary-Current Waveform

The input power (P_{in}) at the minimum input can be estimated as:

$$P_{in} = \frac{V_O \cdot I_O}{\eta} \qquad (5)$$

Where V_O is the output voltage, I_O is the rated output current, η is the estimated efficiency, generally it is between 0.75 and 0.85 depending on the input range and output application.

For CCM at minimum input, the converter duty cycle is:

$$D = \frac{(V_O + V_F) \cdot N}{(V_O + V_F) \cdot N + V_{in(min)}} \qquad (6)$$

Where:

V_F is the secondary diode's forward voltage,

N is the transformer turn ratio, and

$V_{in(min)}$ is the minimum voltage on bulk capacitor.

The MOSFET turn-on time is:

$$T_{on} = D \cdot T_s \qquad (7)$$

Where T_s is the frequency jitter's dominant switching period, $\frac{1}{T_s} = f_s = 65kHz$.

The average, peak, ripple and valley values of the primary current are described as follows:

$$I_{av} = \frac{P_{in}}{V_{in(min)}} \qquad (8)$$

$$I_{peak} = \frac{I_{av}}{(1 - \frac{K_P}{2}) \cdot D} \qquad (9)$$

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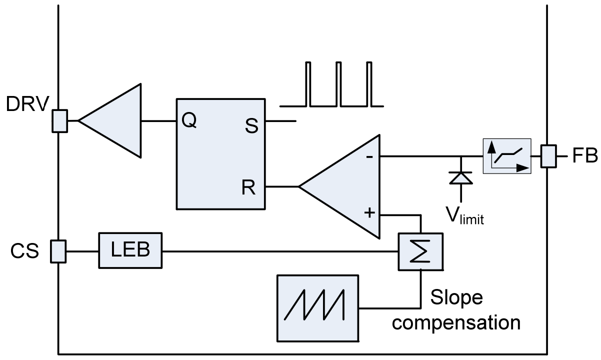
$$I_{ripple} = K_P \cdot I_{peak} \quad (10)$$

$$I_{valley} = (1 - K_P) \cdot I_{peak} \quad (11)$$

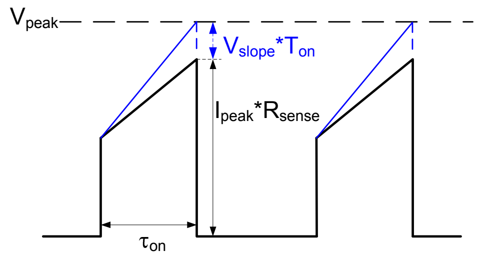
The following equation estimates L_m as:

$$L_m = \frac{V_{in(min)} \cdot T_{on}}{I_{ripples}} \quad (12)$$

Current-Sense Resistor



a) Peak-Current-Comparator Circuit



b) Typical Waveform

Figure 14: Peak-Current Comparator

Figure 14 shows the peak-current-comparator logic and the subsequent waveform. When the sum of the sensing resistor voltage and the slope compensator reaches V_{peak}, the comparator goes HIGH to reset the RS flip-flop, and the DRV is pulled down to turn off the MOSFET. The maximum current limit (V_{limit}, as measured by V_{CS}) is 0.95V. The slope compensator (V_{slope}) is ~25mV/µs. Given a certain margin, use 0.95×V_{limit} as V_{peak} at full load. Then the voltage on sensing resistor can be obtained:

$$V_{sense} = 95\% \cdot V_{limit} - V_{slope} \cdot T_{on} \quad (13)$$

So the value of the sense resistor is:

$$R_{sense} = \frac{V_{sense}}{I_{peak}} \quad (14)$$

Select the current sense resistor with an appropriate power rating. The following equation gives the sense resistor power loss:

$$P_{sense} = \left[\left(\frac{I_{peak} + I_{valley}}{2}\right)^2 + \frac{1}{12}\left(I_{peak} - I_{valley}\right)^2\right] \cdot D \cdot R_{sense}$$

(15)

Low-Pass Filter on CS

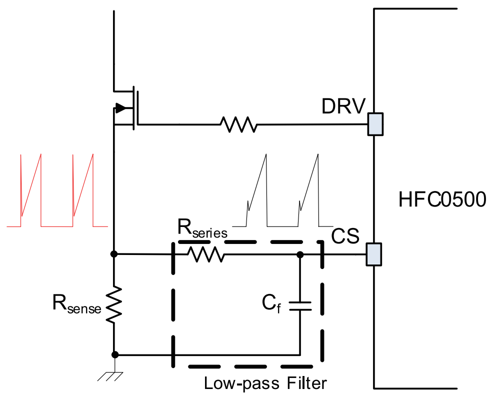


Figure 15: Low-Pass Filter on CS

A small capacitor connected to the CS with R_{series} forms a low-pass filter for noise filtering when the MOSFET turns on and off, as showed in Figure 15. The low-pass filter's R×C constant should not exceed 1/3 of the leading-edge blanking period for SCP (T_{LEB2}, 270ns, typical), otherwise the filtered sensed voltage cannot reach the SCP point (1.45V) to trigger SCP if an output short circuit occurs.

Over Power Compensation

HFC0500 has the over power compensation function (OPC) by drawing current from CS. The purpose of OPC is to minimize OLP difference caused by different input voltage. The offset current is proportional to the input peak voltage sensed by HV.

Suppose the resistor in current sensing loop is R_{series}, and the input voltage 220Vac, then the compensation voltage on the CS can be calculated as:

$$V_{comp} = R_{series} \cdot I_{opc\_310V} \quad (16)$$

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The compensation criteria is making the FB voltage under full load condition is similar whether in high line or low line.

Jitter Period

Frequency jitter is an effective method to reduce EMI by dissipating energy. The n_{th}-order harmonic noise bandwidth is $B_{Tn} = n \cdot (2 \cdot \Delta f + f_{jitter})$, where Δf is the frequency jitter amplitude. If B_{Tn} exceeds the resolution bandwidth (RBW) of the spectrum analyzer (200Hz for noise frequency less than 150 kHz, 9 kHz for noise frequency between 150 kHz to 30MHz), the spectrum analyzer receives less noise energy.

The capacitor on the TIMER determines the period of the frequency jitter. A 10μA current source charges the capacitor; when the TIMER voltage reaches 3.2V, another 10μA current source discharges the capacitor to 2.8V. This charging and discharging cycle repeats.

Equation (2) describes the jitter period in theory; a smaller f_{jitter} is more effective at EMI reduction. However, the measurement bandwidth requires that f_{jitter} should be large compared to spectrum analyzer RBW for effective EMI reduction. Also, f_{jitter} should be less than the control-loop-gain crossover frequency to avoid disturbing the output voltage regulation. At the same time, we must consider the practical application when selected the Timer capacitor. Too large capacitor may cause failing startup at full load because of the long soft startup duration showed as equation (3). At the same time too small timer capacitor will cause timer period get smaller, so the timer count capability is overload, and some logic problem may be occurs. So for most applications, f_{jitter} between 200Hz and 400Hz is recommended.

X-Cap Discharge Time

Figure 10 shows the X-cap discharger waveforms. The maximum discharge time occurs at a high-line input with no-load condition.

The maximum discharge delay time is

$$T_{delay} = 32 \cdot T_{jitter} \quad (17)$$

The Xcap is discharged from a high-voltage constant current source (I_{HV_120V}, 2.5mA typically) into HV. The current-source discharge time for the X-cap to drop to 37% of peak voltage can be estimated by:

$$T_{discharge} = \frac{C_X \cdot 63\% \cdot \sqrt{2} \cdot V_{ac(max)}}{I_{HV\_120V}} \quad (18)$$

Where C_X is the X-cap capacitance, $V_{ac(max)}$ is the maximum AC-input RMS value.

The first discharging period is 16×T_{jitter}, with subsequent period equal to 48×T_{jitter}. Then the discharge sections times can approximately as:

$$n = \frac{T_{discharge} - 16 \cdot T_{jitter}}{48 \cdot T_{jitter}} + 1 \quad (19)$$

For every discharge section, there is a certain period (16×Tjitter) for detection as follow:

$$T_{detect} = 16 \cdot T_{jitter} \cdot (n - 1) \quad (20)$$

As a result, the total discharge time is then:

$$T_{total} = T_{delay} + T_{discharge} + T_{detect} \quad (21)$$

The total discharge time is relative to T_{jitter} which is dependent on C_{TIMER}. For example, if C_{TIMER} is 47nF and T_{jitter}=3.7ms, the X-cap discharge margin is 1s due to X-cap value tolerance (±10% typically). It is recommended to select an X-cap less than 3.3μF.

Though the X-cap has been discharged, it may still retain a high-voltage on the bulk capacitor. For safety, make sure it is released before debugging the board.

Ramp Compensation

When adopting peak current control, sub harmonic oscillation will occur when D>0.5 in CCM. HFC0500 is equipped with internal ramp compensation to solve this problem. α is calculated by the following equation (22). For stable operation, α must be less than 1.

$$\alpha = \frac{\frac{D_{max} \cdot V_{in(min)}}{(1-D_{max}) \cdot L_m} \cdot R_{sense} - m_a}{\frac{V_{in(min)}}{L_m} \cdot R_{sense} + m_a} \quad (22)$$

Where m_a=18mV/us, is the minimum internal slope value of the compensation ramp, $\frac{V_{in(min)}}{L_m} \cdot R_{sense}$ and $\frac{D_{max} \cdot V_{in(min)}}{(1-D_{max}) \cdot L_m} \cdot R_{sense}$ is slew rate

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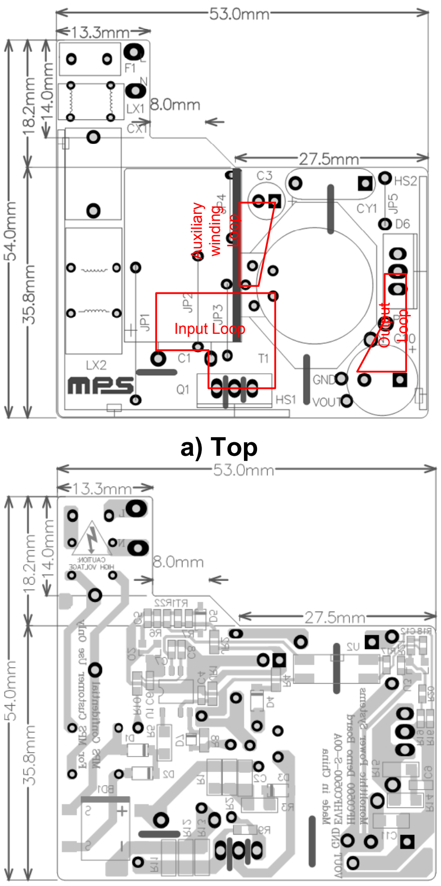
of the primary-side and equivalent secondary-side voltage sensed by CS resistor respectively.

PCB Layout Guide

PCB layout is very important to achieve reliable operation, good EMI performance and good thermal performance. Follow these guidelines to optimize performance:

1) Minimize the power stage loop area. This includes the input loop (C1 - T1 - Q1 – R11/R12/R13 – C1), the auxiliary winding loop (T1 – D4 – R4 – C3 – T1), and the output loop (T1 – D6 – C10 – T1).
2) The input loop GND and control circuit should be separate and only connect at C1.
3) Connecting the Q1 heat-sink to the primary GND plane to improve EMI.
4) Place the control circuit capacitors (such as those for FB, CS and VCC) close to IC to decouple noise.



a) Top

b) Bottom

Figure 16: PCB Layout

Design Example

Below is a design example of HFC0500 for power adapter applications.

Table 1: Design Spec.

V_{IN}	85 to 265VAC
V_{OUT}	19V
I_{OUT}	2.35A

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TYPICAL APPLICATION CIRCUIT

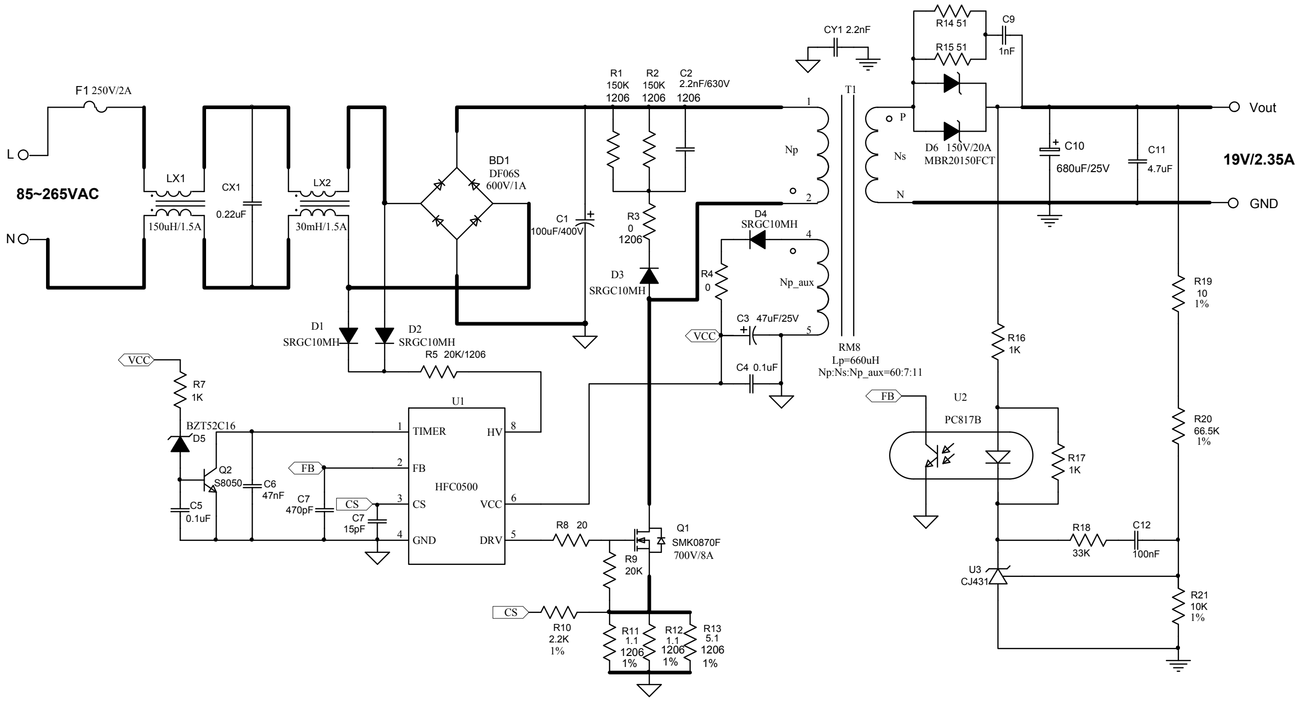
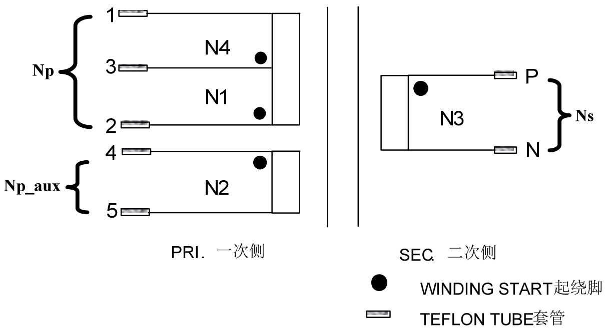
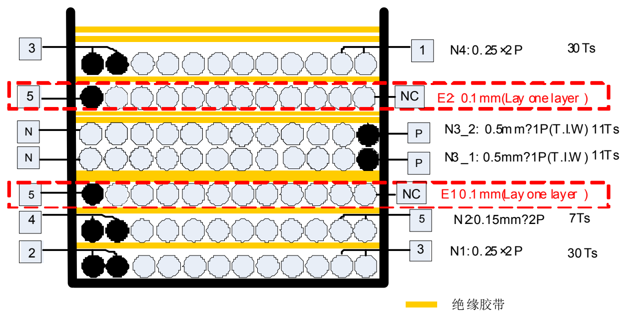


Figure 17: Example of a Typical Application



a) Connection Diagram



b) Winding Diagram

Figure18: Transformer Structure

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Table 2: Winding Order

Tape (T)	Winding	Terminal Start—>End	Wire Size (φ)	Turns (T)	Tube
	N1	2—>3	0.25mm*2	30	matching with wire
1					
	N2	4—>5	0.15mm*2	7	matching with wire
1					
2	E1	5—>Nc	0.1mm*12	Wind with tight tension across entire bobbin evenly	
	N3	P—>N	0.5mm*2(T.I,W)	11	
2	E2	5—>NC	0.1mm*2	Wind with tight tension across entire bobbin evenly	
1	N4	3—>1	0.25mm*2	30	matching with wire

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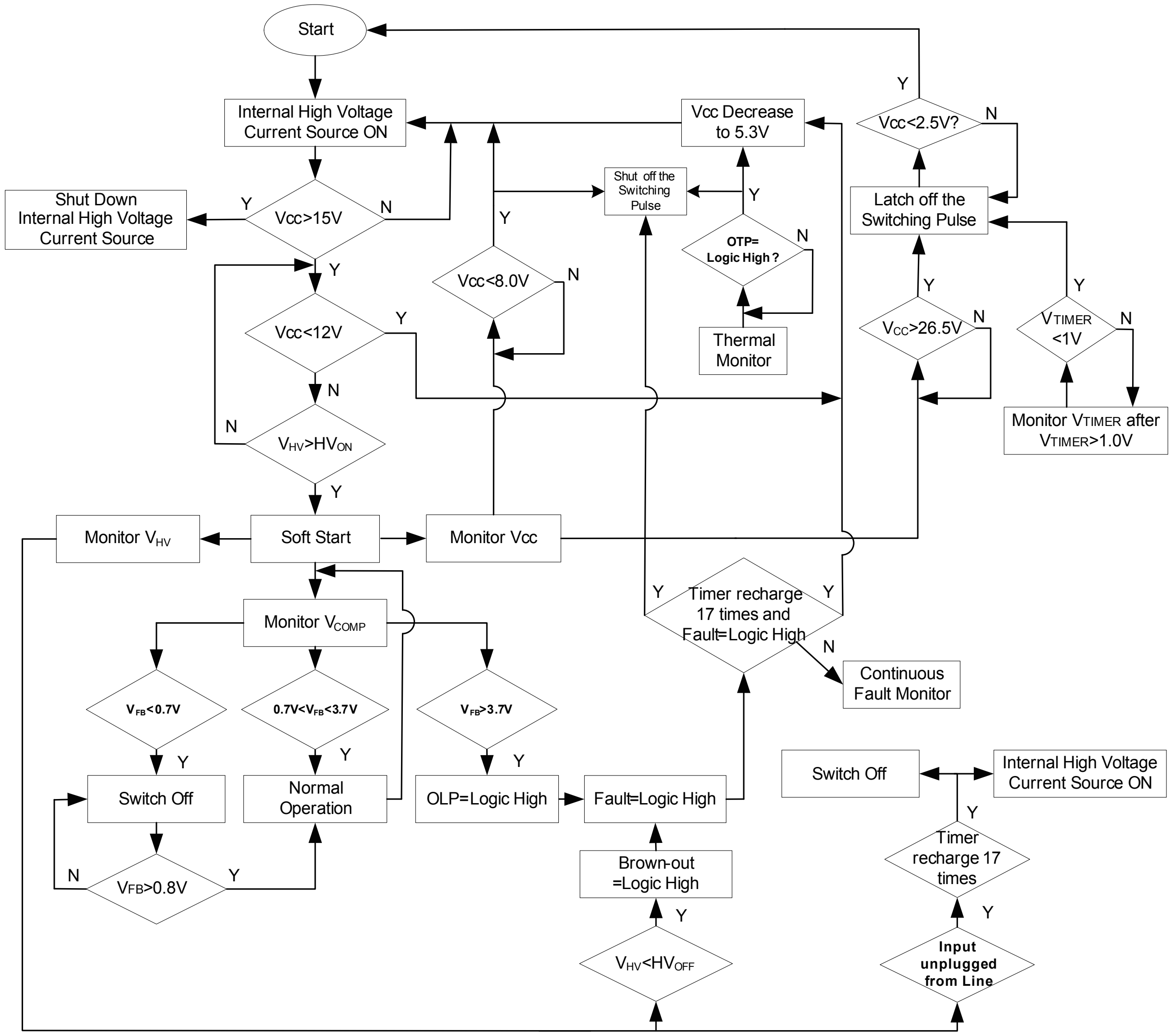
FLOW CHART



UVLO, brown-out, OTP & OLP is auto restart, OVP on VCC and Latch-off on TIMER are latch mode

Release from the latch condition, need to unplug from the main input.

Figure19: Control Flow Chart

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EVOLUTION OF THE SIGNALS IN PRESENCE OF FAULTS

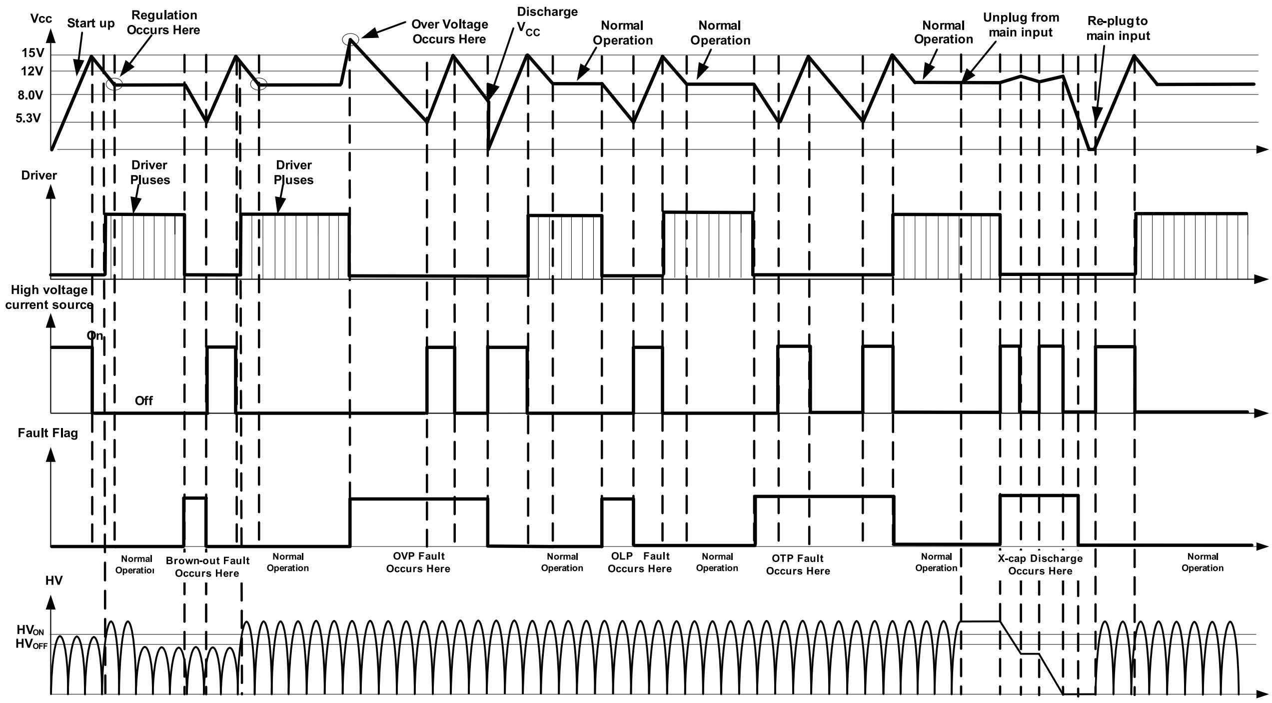

Figure 20: Signal Evolution in the Presence of Faults

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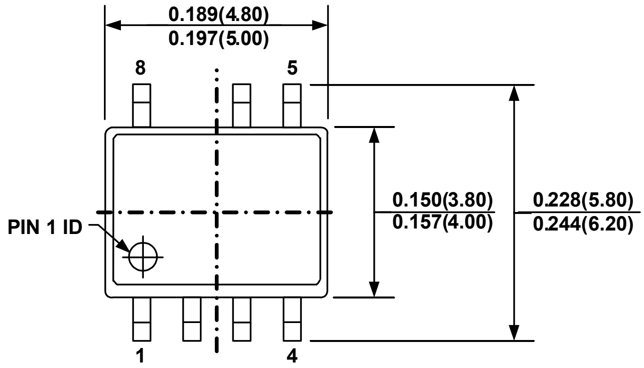
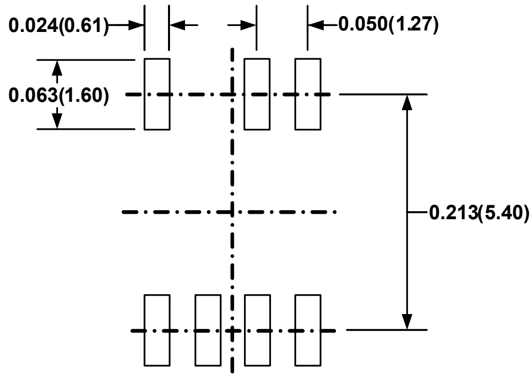
PACKAGE INFORMATION

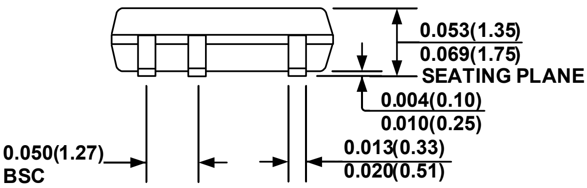
SOIC8-7A



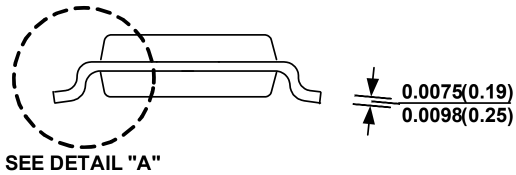
TOP VIEW



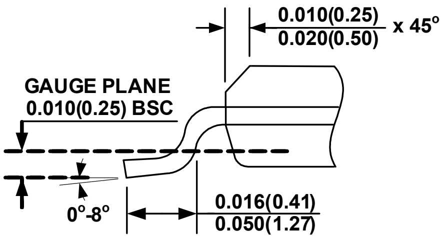
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) JEDEC REFERENCE IS MS-012.
6) DRAWING IS NOT TO SCALE.

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