DS90LV804 4-Channel 800 Mbps LVDS Buffer/Repeater

Check for Samples: DS90LV804

FEATURES

- **800 Mbps Data Rate per Channel**
- **Low Output Skew and Jitter**
- **LVDS/CML/LVPECL Compatible Input, LVDS Output**
- **On-Chip 100Ω Input and Output Termination**
- **12 kV ESD Protection on LVDS Outputs**
- **Single 3.3V Supply**
- **Very Low Power Consumption**
- **Industrial -40 to +85°C Temperature Range**
- **Small WQFN Package Footprint**

DESCRIPTION

The DS90LV804 is a four channel 800 Mbps LVDS buffer/repeater. In many large systems, signals are distributed across cables and signal integrity is highly dependent on the data rate, cable type, length, and the termination scheme.

In order to maximize signal integrity, the DS90LV804 features both an internal input and output (source) termination to eliminate these extra components from the board, and to also place the terminations as close as possible to receiver inputs and driver output. This is especially significant when driving longer cables.

The DS90LV804, available in the WQFN (Leadless Leadframe Package) package, minimizes the footprint, and improves system performance.

An output enable pin is provided, which allows the user to place the LVDS outputs and internal biasing generators in a TRI-STATE®, low power mode.

The differential inputs interface to LVDS, and Bus LVDS signals such as those on TI's 10-, 16-, and 18-bit Bus LVDS SerDes, as well as CML and LVPECL. The differential inputs are internally terminated with a 100Ω resistor to improve performance and minimize board space. This function is especially useful for boosting signals over lossy cables or point-to-point backplane configurations.

Block and Connection Diagrams

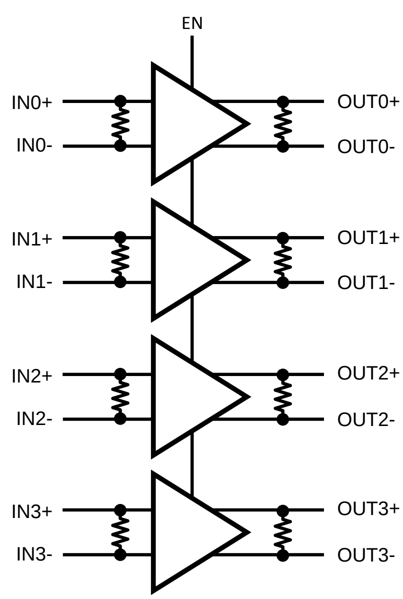
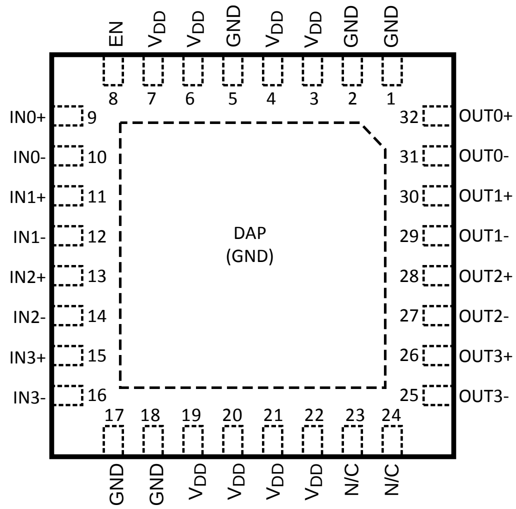


Figure 1. DS90LV804 Block Diagram



DS90LV804 WQFN Pinout
(Top View)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)

Supply Voltage (V_{DD})		−0.3V to +4.0V
CMOS Input Voltage (EN)		−0.3V to (V_{DD}+0.3V)
LVDS Input Voltage (2)		−0.3V to (V_{DD}+0.3V)
LVDS Output Voltage		−0.3V to (V_{DD}+0.3V)
LVDS Output Short Circuit Current		+90 mA
Junction Temperature		+150°C
Storage Temperature		−65°C to +150°C
Lead Temperature (Solder, 4sec)		260°C
Max Pkg Power Capacity @ 25°C		4.16W
Thermal Resistance	θ_{JA}	29.5°C/W
	θ_{JC}	3.5°C/W
Package Derating above +25°C		33.3mW/°C
ESD Last Passing Voltage (LVDS output pins)	HBM, 1.5kΩ, 100pF	12 kV
	EIAJ, 0Ω, 200pF	250V
	Charged Device Model	1000V
ESD Last Passing Voltage (All other pins)	HBM, 1.5kΩ, 100pF	8 kV
	EIAJ, 0Ω, 200pF	250V
	Charged Device Model	1000V

(1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. TI does not recommend operation of products outside of recommended operation conditions.
(2) V_{ID} max < 2.4V

Recommended Operating Conditions

Supply Voltage (V_{CC})		3.15V to 3.45V
Input Voltage (V_I)(1)		0V to V_{DD}
Output Voltage (V_O)		0V to V_{DD}
Operating Temperature (T_A)	Industrial	−40°C to +85°C

(1) V_{ID} max < 2.4V

Electrical Characteristics

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
LVTTL DC SPECIFICATIONS (EN)						
V_{IH}	High Level Input Voltage		2.0		V_{DD}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{DD} = V_{DDMAX}$	−10		+10	μA
I_{IL}	Low Level Input Current	$V_{IN} = V_{SS}$, $V_{DD} = V_{DDMAX}$	−10		+10	μA
C_{IN1}	Input Capacitance	Any Digital Input Pin to V_{SS}		3.5		pF
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA	−1.5	−0.8		V
LVDS INPUT DC SPECIFICATIONS (INn±)						
V_{TH}	Differential Input High Threshold(2)	V_{CM} = 0.8V to 3.4V, V_{DD} = 3.45V		0	100	mV
V_{TL}	Differential Input Low Threshold(2)	V_{CM} = 0.8V to 3.4V, V_{DD} = 3.45V	−100	0		mV
V_{ID}	Differential Input Voltage	V_{CM} = 0.8V to 3.4V, V_{DD} = 3.45V	100		2400	mV
V_{CMR}	Common Mode Voltage Range	V_{ID} = 150 mV, V_{DD} = 3.45V	0.05		3.40	V
C_{IN2}	Input Capacitance	IN+ or IN− to V_{SS}		3.5		pF
I_{IN}	Input Current	V_{IN} = 3.45V, $V_{DD} = V_{DDMAX}$	−10		+10	μA
		V_{IN} = 0V, $V_{DD} = V_{DDMAX}$	−10		+10	μA
LVDS OUTPUT DC SPECIFICATIONS (OUTn±)						
V_{OD}	Differential Output Voltage(2)	R_L = 100Ω external resistor between OUT+ and OUT−	250	500	600	mV
ΔV_{OD}	Change in V_{OD} between Complementary States		−35		35	mV
V_{OS}	Offset Voltage(3)		1.05	1.18	1.475	V
ΔV_{OS}	Change in V_{OS} between Complementary States		−35		35	mV
I_{OS}	Output Short Circuit Current	OUT+ or OUT− Short to GND		−60	−90	mA
C_{OUT2}	Output Capacitance	OUT+ or OUT− to GND when TRI-STATE		5.5		pF
SUPPLY CURRENT (Static)						
I_{CC}	Total Supply Current	All inputs and outputs enabled and active, terminated with external differential load of 100Ω between OUT+ and OUT-.		117	140	mA
I_{CCZ}	TRI-STATE Supply Current	EN = 0V		2.7	6	mA

(1) Typical parameters are measured at V_{DD} = 3.3V, T_A = 25°C. They are for reference purposes, and are not production-tested.
(2) Differential output voltage V_{OD} is defined as ABS(OUT+–OUT−). Differential input voltage V_{ID} is defined as ABS(IN+–IN−).
(3) Output offset voltage V_{OS} is defined as the average of the LVDS single-ended output voltages at logic high and logic low states.

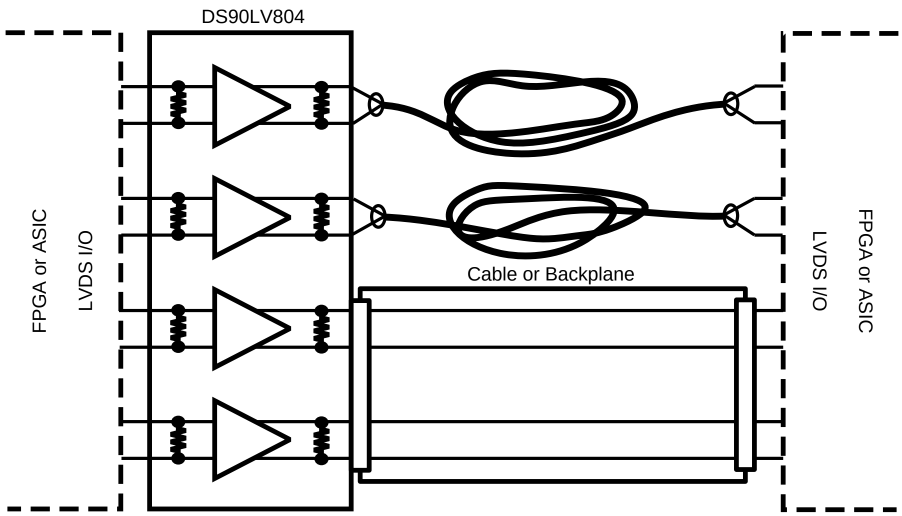
Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless other specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Units
SWITCHING CHARACTERISTICS—LVDS OUTPUTS						
t_{LHT}	Differential Low to High Transition Time	Use an alternating 1 and 0 pattern at 200 Mbps, measure between 20% and 80% of V_{OD}[4]		210	300	ps
t_{HLT}	Differential High to Low Transition Time			210	300	ps
t_{PLHD}	Differential Low to High Propagation Delay	Use an alternating 1 and 0 pattern at 200 Mbps, measure at 50% V_{OD} between input to output.		2.0	3.2	ns
t_{PHLD}	Differential High to Low Propagation Delay			2.0	3.2	ns
t_{SKD1}	Pulse Skew	$\|t_{PLHD}–t_{PHLD}\|$[4]		25	80	ps
t_{SKCC}	Output Channel to Channel Skew	Difference in propagation delay (t_{PLHD} or t_{PHLD}) among all output channels[4]		50	125	ps
t_{SKP}	Part to Part Skew	Common edge, parts at same temp and V_{CC}[4]			1.1	ns
t_{JIT}	Jitter[5]	RJ - Alternating 1 and 0 at 400 MHz[6]		1.1	1.5	psrms
		DJ - K28.5 Pattern, 800 Mbps[7]		15	35	psp-p
		TJ - PRBS 2^{23}-1 Pattern, 800 Mbps[8]		30	55	psp-p
t_{ON}	LVDS Output Enable Time	Time from EN to OUT± change from TRI-STATE to active.			300	ns
t_{OFF}	LVDS Output Disable Time	Time from EN to OUT± change from active to TRI-STATE.			12	ns

(4) Not production tested. Ensured by statistical analysis on a sample basis at the time of characterization.
(5) Jitter is not production tested, but ensured through characterization on a sample basis.
(6) Random Jitter, or RJ, is measured RMS with a histogram including 1500 histogram window hits. The input voltage = V_{ID} = 500mV, 50% duty cycle at 400 MHz, $t_r = t_f$ = 50ps (20% to 80%).
(7) Deterministic Jitter, or DJ, is measured to a histogram mean with a sample size of 350 hits. The input voltage = V_{ID} = 500mV, K28.5 pattern at 800 Mbps, $t_r = t_f$ = 50ps (20% to 80%). The K28.5 pattern is repeating bit streams of (0011111010 1100000101).
(8) Total Jitter, or TJ, is measured peak to peak with a histogram including 3500 window hits. Stimulus and fixture Jitter has been subtracted. The input voltage = V_{ID} = 500mV, 2^{23}-1 PRBS pattern at 800 Mbps, $t_r = t_f$ = 50ps (20% to 80%).

Typical Application



APPLICATION INFORMATION

INTERNAL TERMINATIONS

The DS90LV804 has integrated termination resistors on both the input and outputs. The inputs have a 100Ω resistor across the differential pair, placing the receiver termination as close as possible to the input stage of the device. The LVDS outputs also contain an integrated 100Ω ohm termination resistor, this resistor is used to reduce the effects of Near End Crosstalk (NEXT) and does not take the place of the 100 ohm termination at the inputs to the receiving device. The integrated terminations improve signal integrity and decrease the external component count resulting in space savings.

OUTPUT CHARACTERISTICS

The output characteristics of the DS90LV804 have been optimized for point-to-point backplane and cable applications, and are not intended for multipoint or multidrop signaling.

TRI-STATE MODE

The EN input activates a hardware TRI-STATE mode. When the TRI-STATE mode is active (EN=L), all input and output buffers and internal bias circuitry are powered off and disabled. Outputs are tri-stated in TRI-STATE mode. When exiting TRI-STATE mode, there is a delay associated with turning on bandgap references and input/output buffer circuits as indicated in the LVDS Output Switching Characteristics

INPUT FAILSAFE BIASING

External pull up and pull down resistors may be used to provide enough of an offset to enable an input failsafe under open-circuit conditions. This configuration ties the positive LVDS input pin to V_{DD} thru a pull up resistor and the negative LVDS input pin is tied to GND by a pull down resistor. The pull up and pull down resistors should be in the 5kΩ to 15kΩ range to minimize loading and waveform distortion to the driver. The common-mode bias point ideally should be set to approximately 1.2V (less than 1.75V) to be compatible with the internal circuitry. Please refer to application note AN-1194 "Failsafe Biasing of LVDS Interfaces" for more information.

INPUT INTERFACING

The DS90LV804 accepts differential signals and allow simple AC or DC coupling. With a wide common mode range, the DS90LV804 can be DC-coupled with all common differential drivers (that is, LVPECL, LVDS, CML). Figure 2, Figure 3, and Figure 4 illustrate typical DC-coupled interface to common differential drivers. Note that the DS90LV804 inputs are internally terminated with a 100Ω resistor.

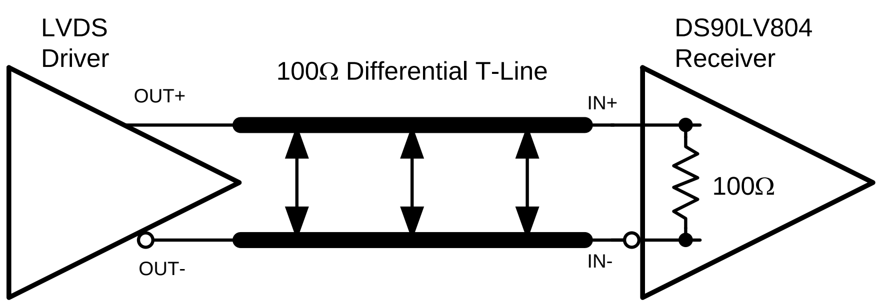


Figure 2. Typical LVDS Driver DC-Coupled Interface to DS90LV804 Input

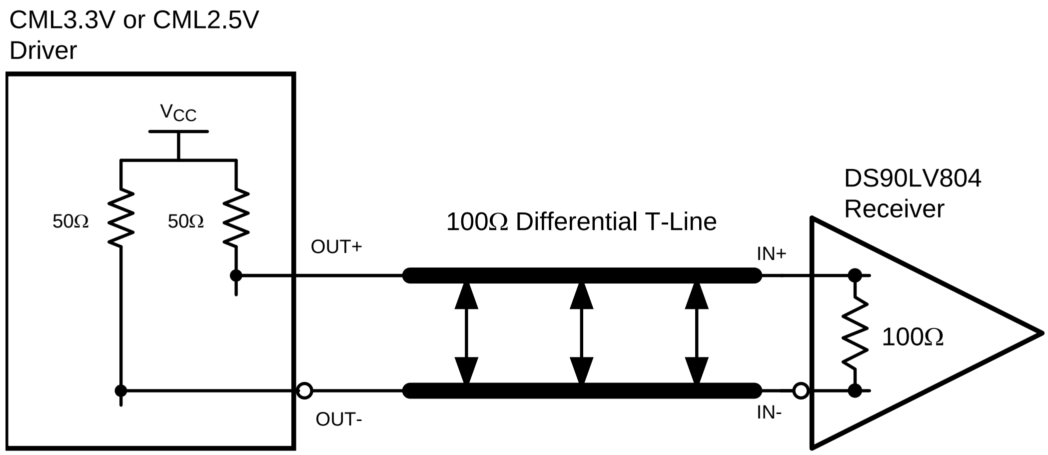


Figure 3. Typical CML Driver DC-Coupled Interface to DS90LV804 Input

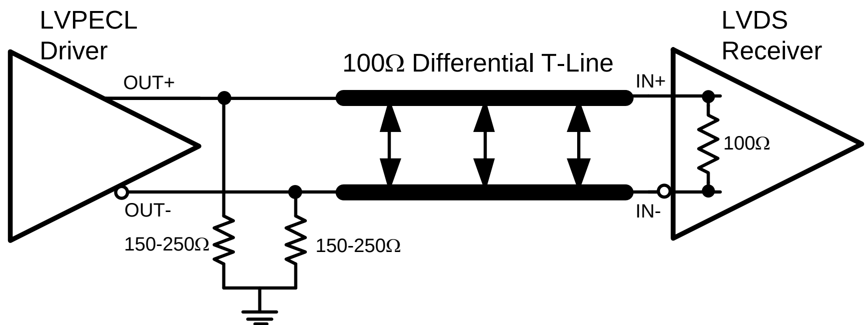


Figure 4. Typical LVPECL Driver DC-Coupled Interface to DS90LV804 Input

OUTPUT INTERFACING

The DS90LV804 outputs signals that are compliant to the LVDS standard. Their outputs can be DC-coupled to most common differential receivers. Figure 5 illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check respective receiver's data sheet prior to implementing the suggested interface implementation.

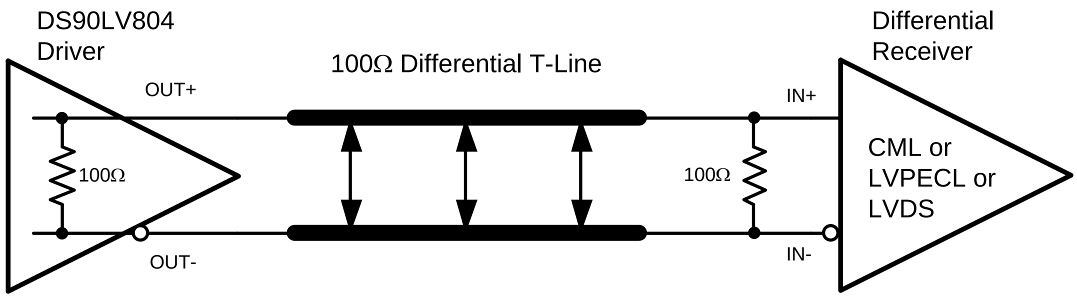


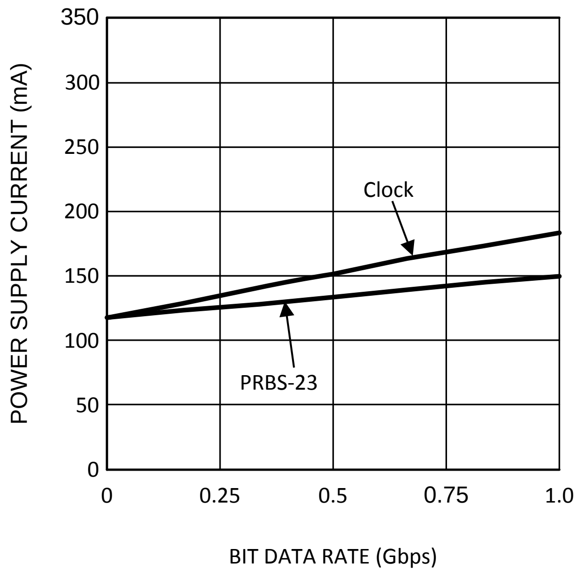
Figure 5. Typical DS90LV804 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

PIN DESCRIPTIONS

Pin Name	WQFN Pin Number	I/O, Type	Description
DIFFERENTIAL INPUTS			
IN0+ IN0−	9 10	I, LVDS	Channel 0 inverting and non-inverting differential inputs.
IN1+ IN1−	11 12	I, LVDS	Channel 1 inverting and non-inverting differential inputs.
IN2+ IN2−	13 14	I, LVDS	Channel 2 inverting and non-inverting differential inputs.
IN3+ IN3−	15 16	I, LVDS	Channel 3 inverting and non-inverting differential inputs.
DIFFERENTIAL OUTPUTS			
OUT0+ OUT0−	32 31	O, LVDS	Channel 0 inverting and non-inverting differential outputs[(1)]
OUT1+ OUT1−	30 29	O, LVDS	Channel 1 inverting and non-inverting differential outputs[(1)]
OUT2+ OUT2−	28 27	O, LVDS	Channel 2 inverting and non-inverting differential outputs[(1)]
OUT3+ OUT3-	26 25	O, LVDS	Channel 3 inverting and non-inverting differential outputs[(1)]
DIGITAL CONTROL INTERFACE			
EN	8	I, LVTTL	Enable pin. When EN is LOW, the driver is disabled and the LVDS outputs are in TRI-STATE. When EN is HIGH, the driver is enabled. LVCMOS/LVTTL level input.
POWER			
V_{DD}	3, 4, 6, 7, 19, 20, 21, 22	I, Power	V_{DD} = 3.3V, ±5%
GND	1, 2, 5, 17, 18[(2)]	I, Power	Ground reference for LVDS and CMOS circuitry. For the WQFN package, the DAP is used as the primary GND connection to the device. The DAP is the exposed metal contact at the bottom of the WQFN-32 package. It should be connected to the ground plane with at least 4 vias for optimal AC and thermal performance. The pin numbers listed should also be tied to ground for proper biasing.
N/C	23, 24		No Connect

(1) The LVDS outputs do not support a multidrop (BLVDS) environment. The LVDS output characteristics of the DS90LV804 device have been optimized for point-to-point backplane and cable applications.
(2) Note that for the WQFN package the GND is connected thru the DAP on the back side of the WQFN package in addition to grounding actual pins on the package as listed.

Typical Performance Characteristics



A. Dynamic power supply current was measured while running a clock or PRBS 2^{23}-1 pattern with all 4 channels active. V_{CC} = 3.3V, T_A = +25°C, V_{ID} = 0.5V, V_{CM} = 1.2V

Figure 6. Power Supply Current vs Bit Data Rate

PACKAGING INFORMATION

The Leadless Leadframe Package (WQFN) is a leadframe based chip scale package (CSP) that may enhance chip speed, reduce thermal impedance, and reduce the printed circuit board area required for mounting. The small size and very low profile make this package ideal for high density PCBs used in small-scale electronic applications such as cellular phones, pagers, and handheld PDAs. The WQFN package is offered in the no Pullback configuration. In the no Pullback configuration the standard solder pads extend and terminate at the edge of the package. This feature offers a visible solder fillet after board mounting.

The WQFN has the following advantages:

- Low thermal resistance
- Reduced electrical parasitics
- Improved board space efficiency
- Reduced package height
- Reduced package mass

For more details about WQFN packaging technology, refer to applications note AN-1187, "Leadless Leadframe Package".

REVISION HISTORY

Changes from Revision K (April 2013) to Revision L	Page
• Changed layout of National Data Sheet to TI format	8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90LV804TSQ	NRND	WQFN	RTV	32	1000	TBD	Call TI	Call TI	-40 to 85	804TSQ	
DS90LV804TSQ/NOPB	ACTIVE	WQFN	RTV	32	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	804TSQ	Samples
DS90LV804TSQX/NOPB	ACTIVE	WQFN	RTV	32	4500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	804TSQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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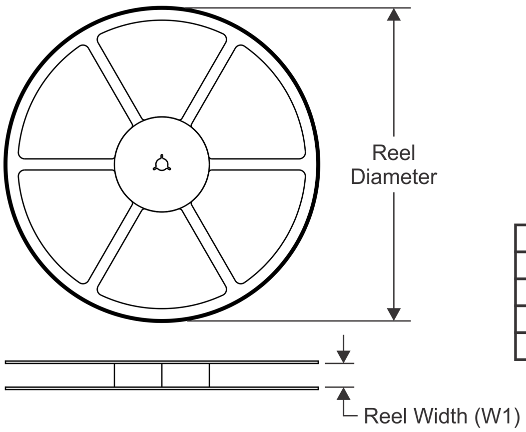
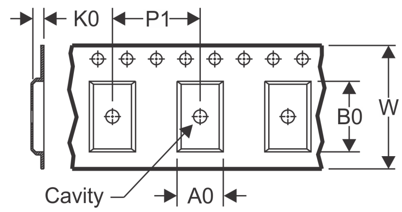
TAPE AND REEL INFORMATION

REEL DIMENSIONS

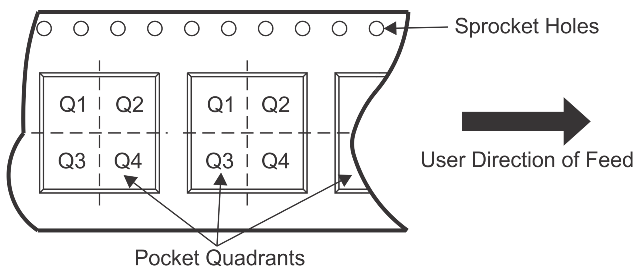


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

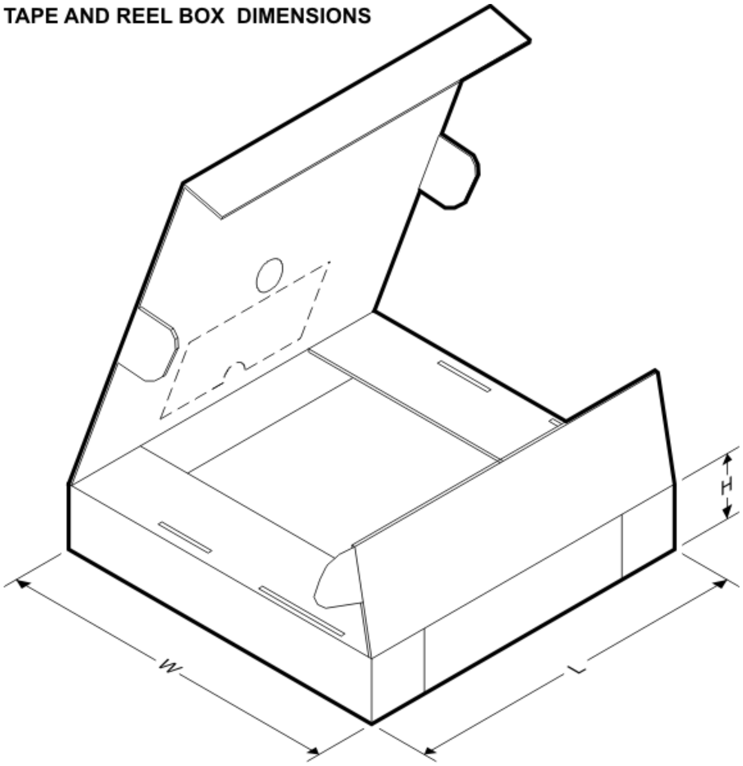
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

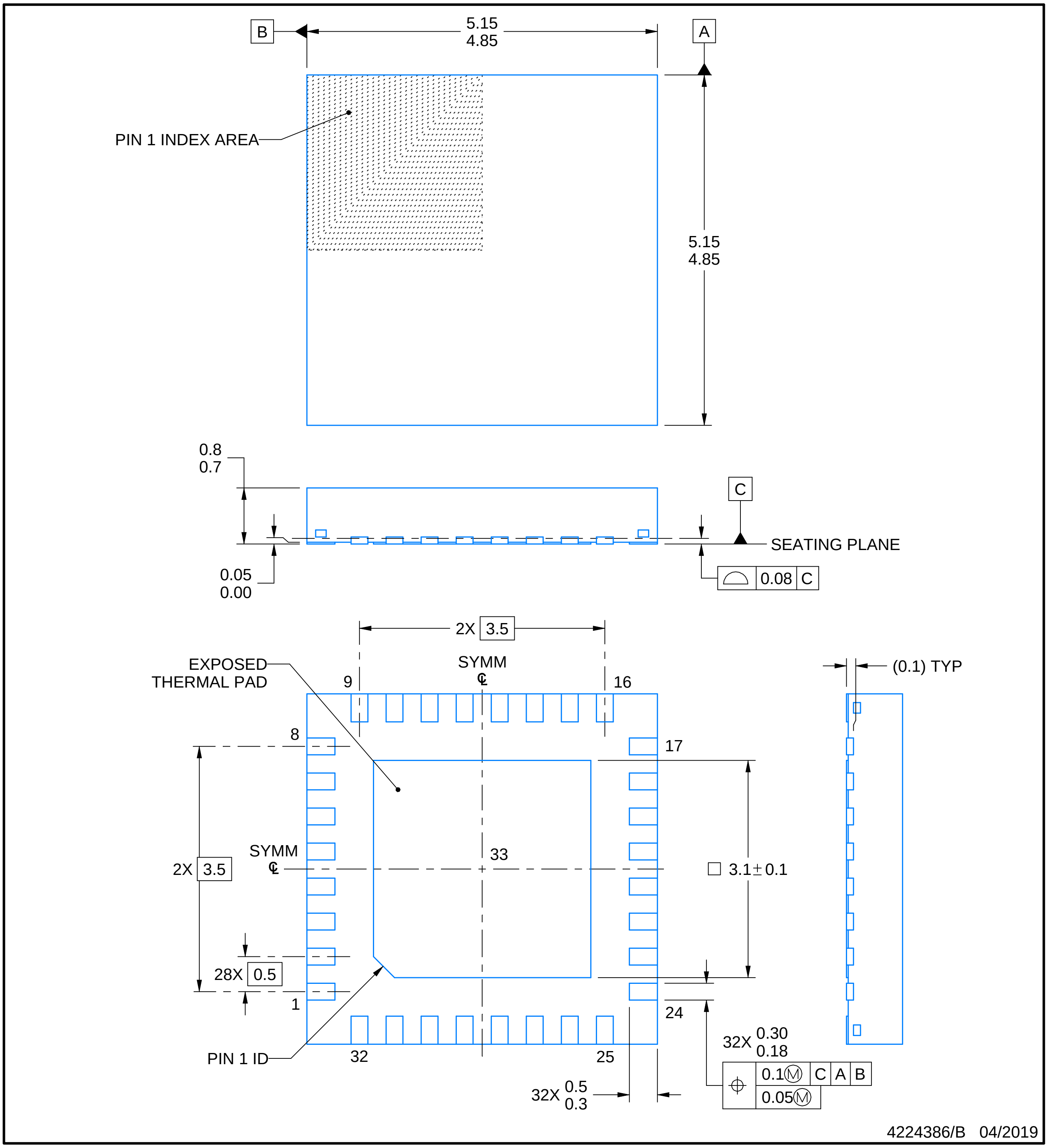
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90LV804TSQ	WQFN	RTV	32	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
DS90LV804TSQ/NOPB	WQFN	RTV	32	1000	178.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1
DS90LV804TSQX/NOPB	WQFN	RTV	32	4500	330.0	12.4	5.3	5.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



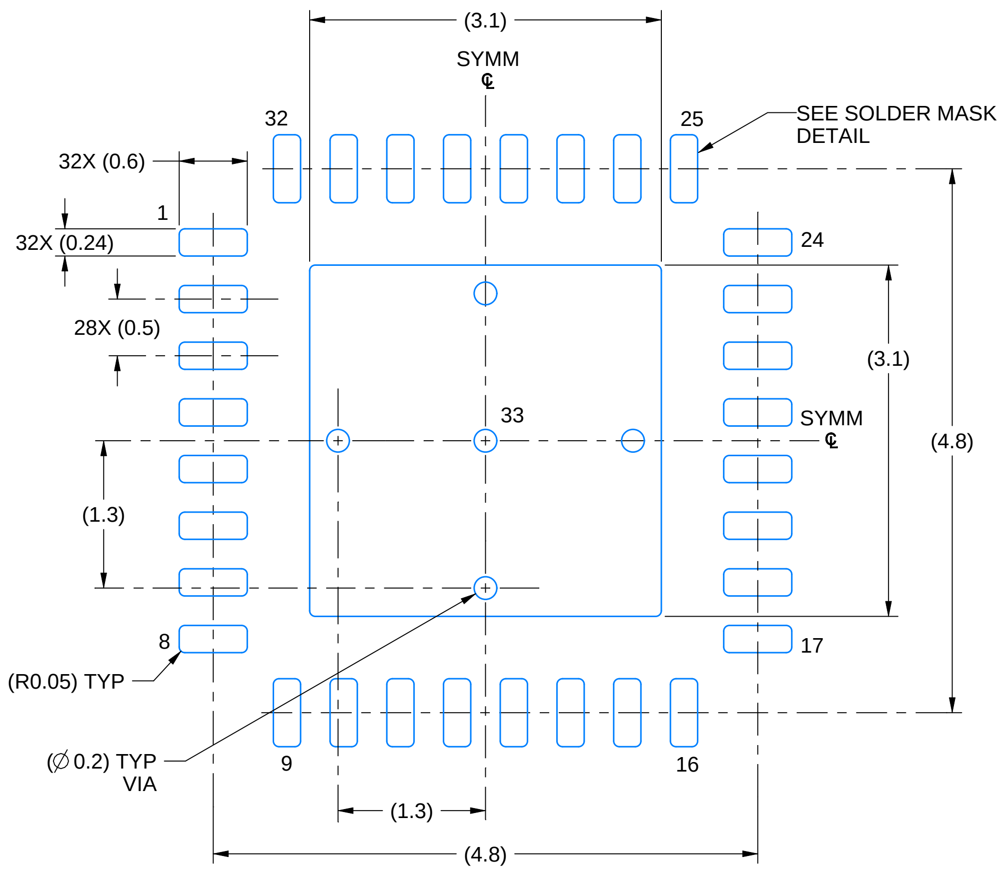
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90LV804TSQ	WQFN	RTV	32	1000	210.0	185.0	35.0
DS90LV804TSQ/NOPB	WQFN	RTV	32	1000	210.0	185.0	35.0
DS90LV804TSQX/NOPB	WQFN	RTV	32	4500	367.0	367.0	35.0

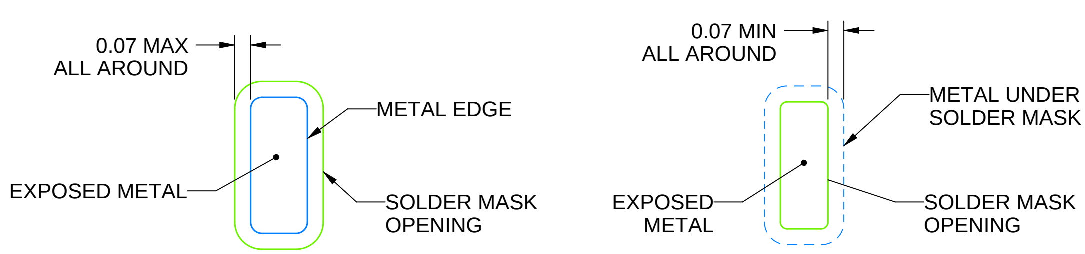


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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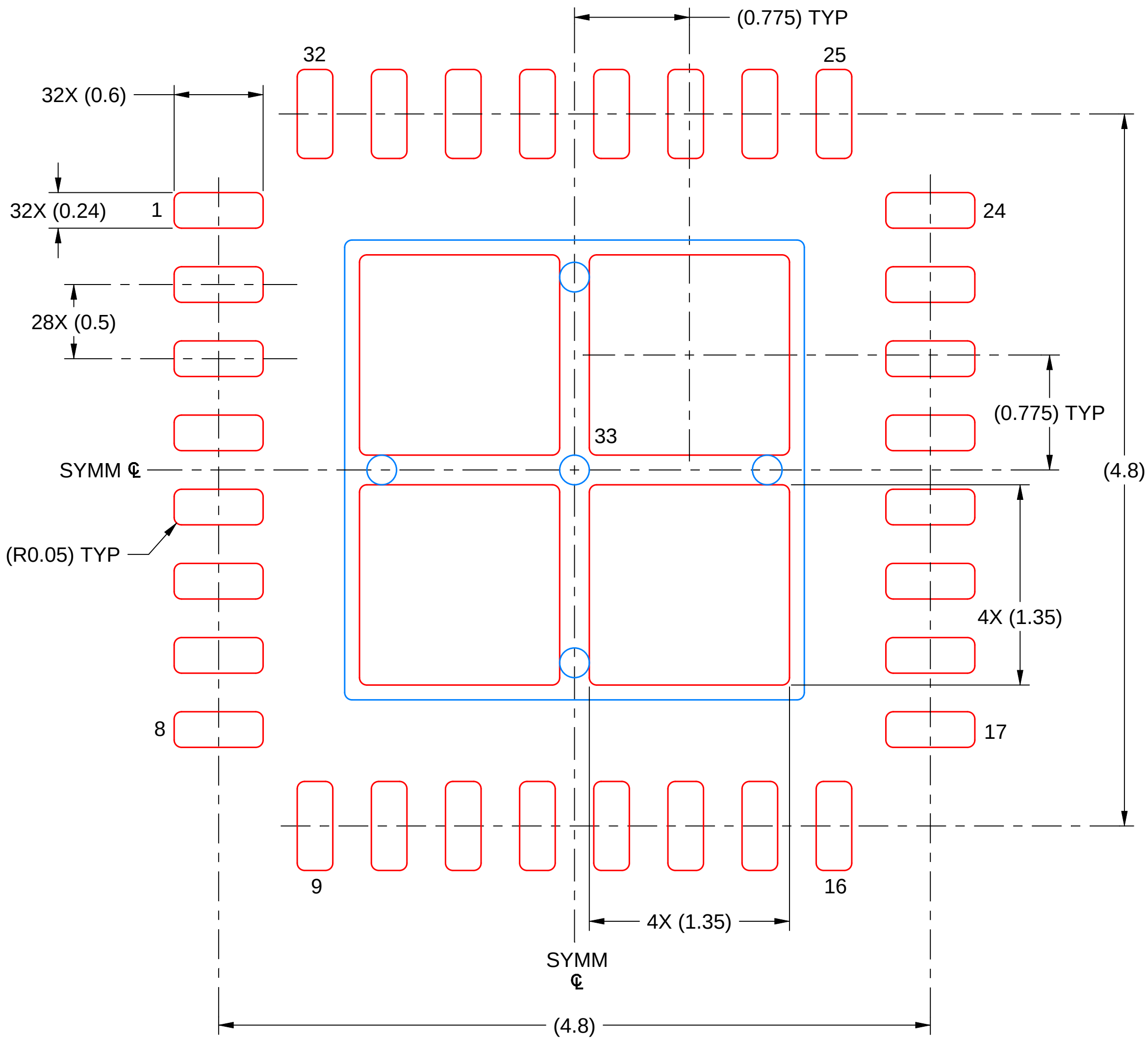
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 33
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.