NAND Flash Memory

(AX20NV4G8)

Features

- Interface
  - Open NAND Flash Interface (ONFI 1.0) compliant
  - x8
- Technology
  - Single-level cell (SLC)
  - 1xnm NAND Process
- Operating Voltage Range
  - VCC: 2.70V – 3.60V
- Operating Temperature Range
  - Industrial: -40°C to 85°C
- Packages
  - 48-pin TSOP (12mm x 20mm)
  - 63-ball FBGA (9mm x 11mm)
- Device Signature
  - Manufacturer's ID
  - Device ID
  - Device Parameters
  - Unique ID
- Quality and Reliability
  - Error Correction Code: 1-bit / 544 bytes of data
  - Data retention: 10 years
  - Endurance (P/E cycles): 60K (Typ.)
  - Block zero (block address 00h) is a valid block when shipped from factory and will remain valid for at least 1K P/E cycles with ECC
- Memory Array Organization
  - x8
    - Page size: 2176 bytes (2048 + 128 bytes)
  - Block size: 64 pages (128K + 8K bytes)
  - Device size: 4096 blocks (2 Planes)
- Firmware SLC Region
- Data Protection
  - Volatile / Non-Volatile
  - OTP Array: 64 pages of One-Time-Programmable memory area (1 block)
- Device Status
  - Ready/busy# (R/B#) signal: hardware method for detecting internal operation completion status
- Advanced Command Set
  - Page data move (copy back): Internal data move
  - Multi-plane Commands

Performance

Device Operation	Values	Units
Single Plane Read	45.0 (Typical)	µs
Multiple Plane Read	55.0 (Typical)	µs
Read Cycle Time	20.0 (Minimum)	ns
Program Page Time	350.0 (Typical)	µs
Block Erase Time	4.0 (Typical)	ms
Standby	100.0 (Maximum)	µA
Read page	25.0 (Typical)	mA

Table of Contents

General Description

Axia Memory Technology's AX20NV4Gx is a 3.0V 4Gbit NAND Flash organized as 2176 bytes × 64 pages × 4096 blocks. All read and program operations are performed using a 2176-byte register; allows data to be transferred to and from the memory array in 2176-bytes increments. The erase operation is implemented in a single block unit (2176 bytes × 64 pages). ECC is included for higher data reliability.

Axia's NAND Flash devices communicate through an asynchronous ONFI 1.0 compatible interface for high-performance I/O operations. It is a multiplexed 8-bit (I/O8) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection (WP#) and monitor device status (R/B#). This hardware interface creates a low pin-count device with a standard pinout that remains the same in Axia's NAND device family, enabling future upgrades to higher densities with no board redesign.

Axia's AX20NV4Gx NAND Flash supports multi-plane program and erase operations. Program operation with multi-plane structure allows 2 pages to be programmed at a time (one in each plane). Similarly, erase operation with multi-page structure allows 2 blocks to be erased at a time (one in each plane). This reduces overall program and erase times compared to similar operations in single-plane structure.

Additionally, Axia's NAND Flash devices support a copy back function which optimizes management of defective blocks. When a page program operation fails, the data already loaded in the page buffer can be directly programmed to another page inside the same array section without the time-consuming serial data insertion phase.

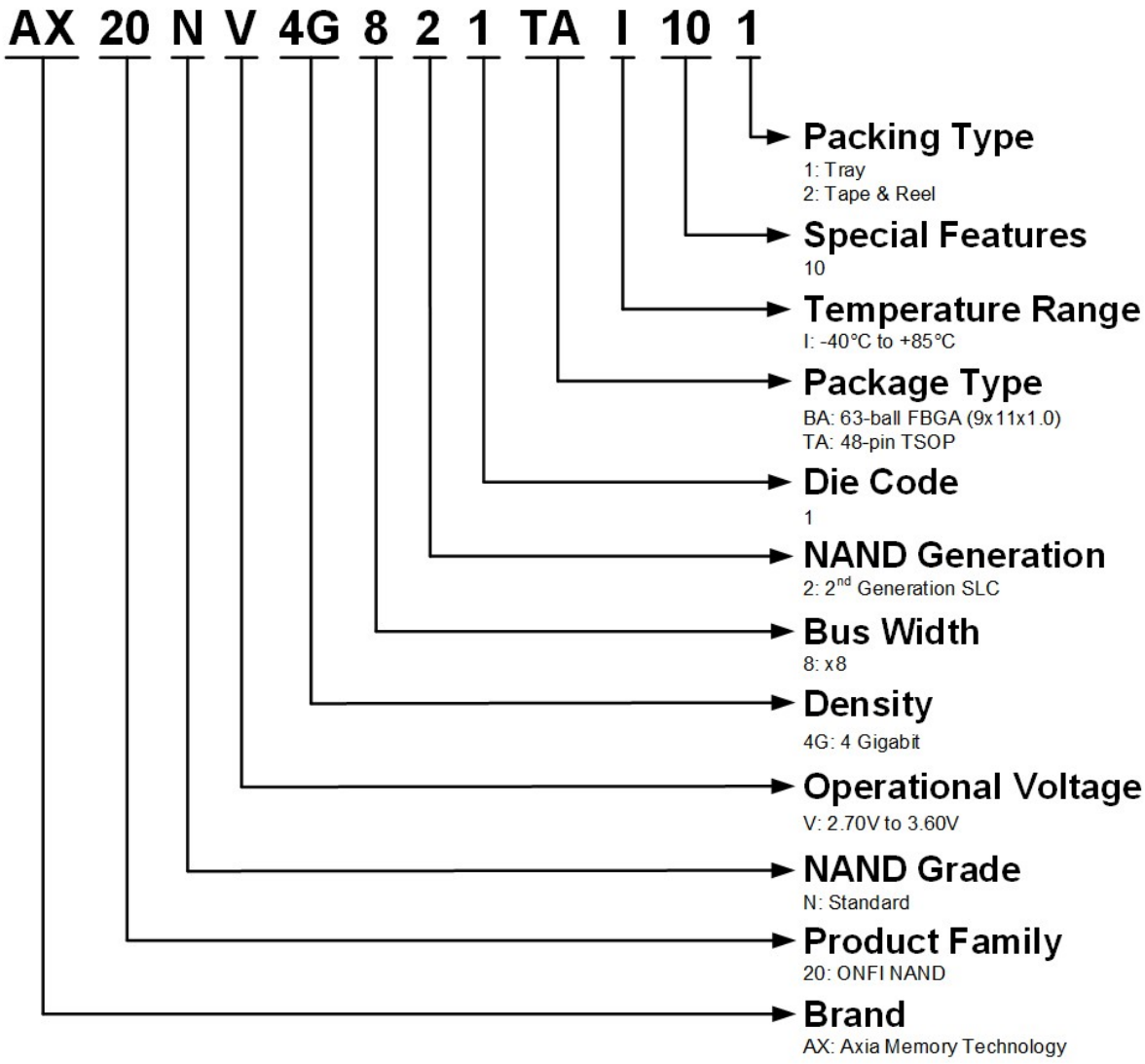
And finally, Axia's NAND Flash devices provide special features listed below in Table 1:

Table 1: Special Features

#	Feature Description	Details
1	One-Time Programmable Area	Size: 1 block (128K + 8K bytes)
2	Unique Identifier	Size: 16 bytes
3	Firmware SLC Region	

Ordering Options

The ordering part numbers are firmed by a valid combination of the following options:



Valid Combinations — Standard

Valid Combinations list includes device configurations currently available. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 2: Valid Combinations List

Valid Combinations								
Base Part Number	**Bus Width**	**Generation**	**Die Code**	**Package type**	**Temperature Range**	**Special Features**	**Packing Type**	**Part Number**
AX20NV4G	x8	2	1	BA, TA	I	10	1, 2	AX20NV4G821BAI101
								AX20NV4G821TAI101
								AX20NV4G821BAI102

Signal Description and Assignment

Figure 1: Device Pinout

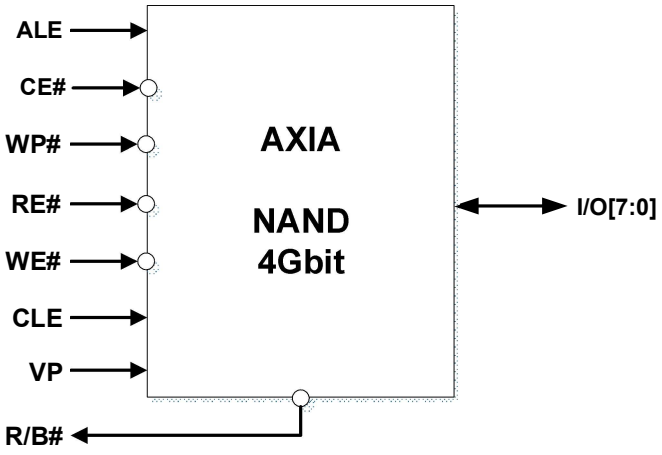


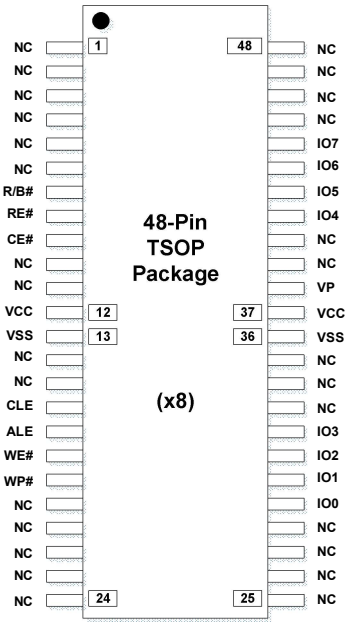
Table 3: Signal Description

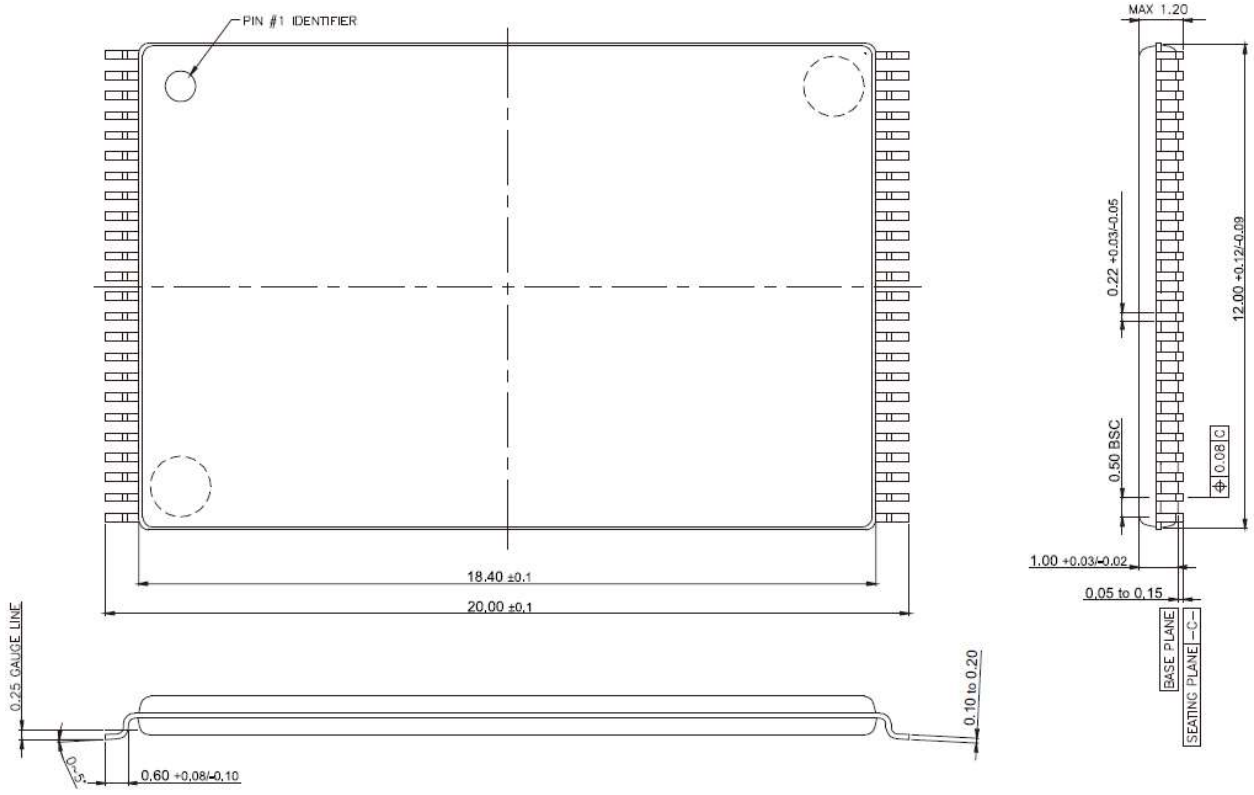
Signal	Type	Description
CE#	Input	**Chip enable:** Enables or disables the NAND Flash.
CLE	Input	**Command latch enable:** Loads a command from x8 - I/O[7:0] into the command register.
ALE	Input	**Address latch enable:** Loads an address from x8 - I/O[7:0] into the address register.
WE#	Input	**Write enable:** Transfers commands, addresses, and serial data from the host system to the NAND Flash.
RE#	Input	**Read enable:** Transfers serial data from the NAND Flash to the host system.
WP#	Input	**Write protect:** Enables or disables array PROGRAM and ERASE operations.
VP	Input	**Volatile protect:** Enables or disables block granular array PROGRAM and ERASE operations. Has a weak internal pull-down to disable protection if the input is left floating.
R/B#	Output	**Ready/busy:** An open-drain, active-low output that requires an external pull-up resistor. This signal indicates NAND Flash activity.
I/O [7:0] - x8	Input/Output	**Data inputs/outputs:** The bidirectional I/Os transfer address, data, and command information.
V_{CC}	Supply	**V_{CC}:** Core and I/O power supply.
V_{SS}	Supply	**V_{SS}:** Core and I/O ground supply.
NC		**Not Connected:** NCs are not internally connected. They can be driven or left unconnected.

Package Options

48-Pin TSOP (Top View)

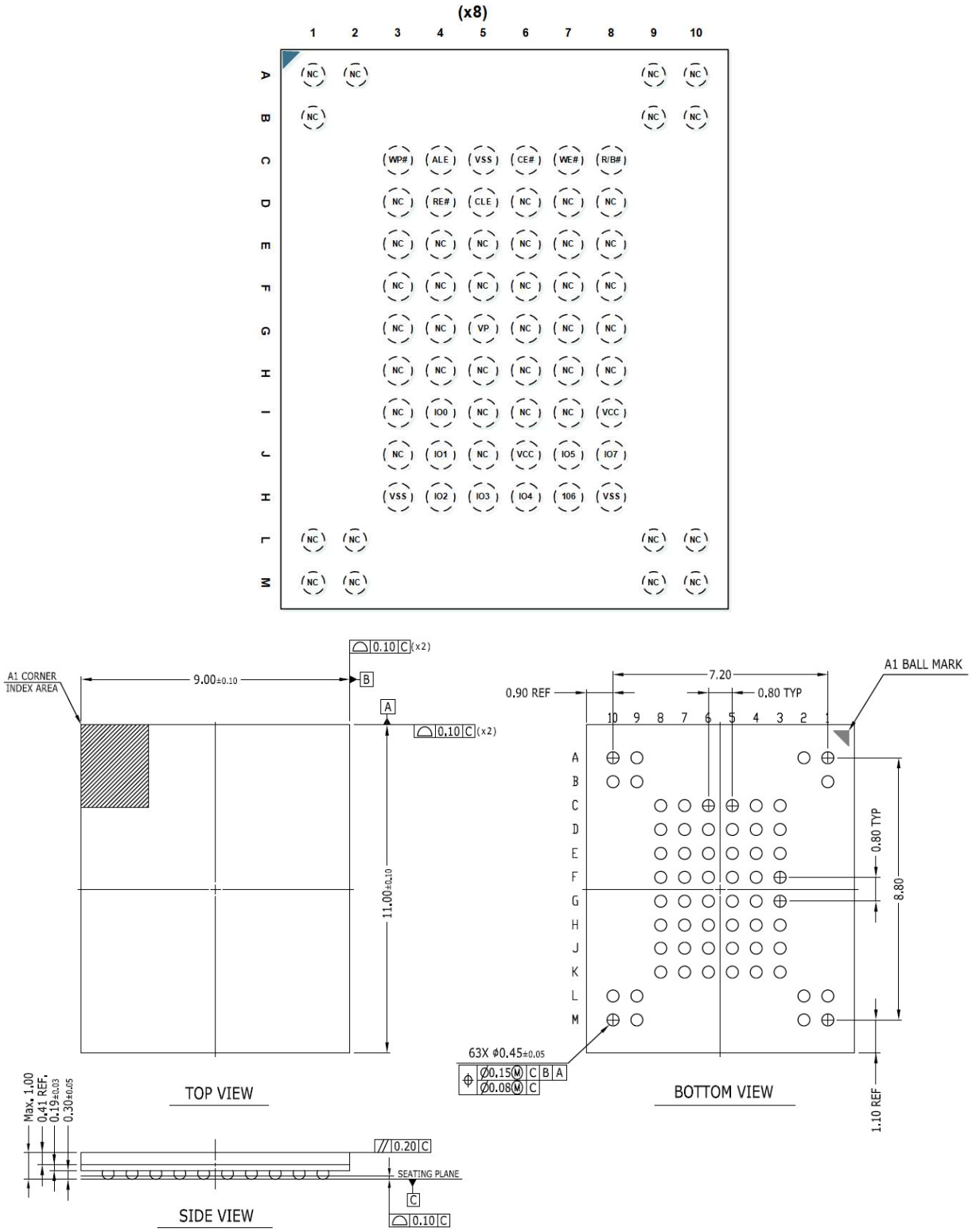
Figure 2: 48-Pin TSOP Pinout and Dimensions





63-Ball FBGA (Balls Down, Top View)

Figure 3: 63-Ball FBGA Pinout and Dimensions

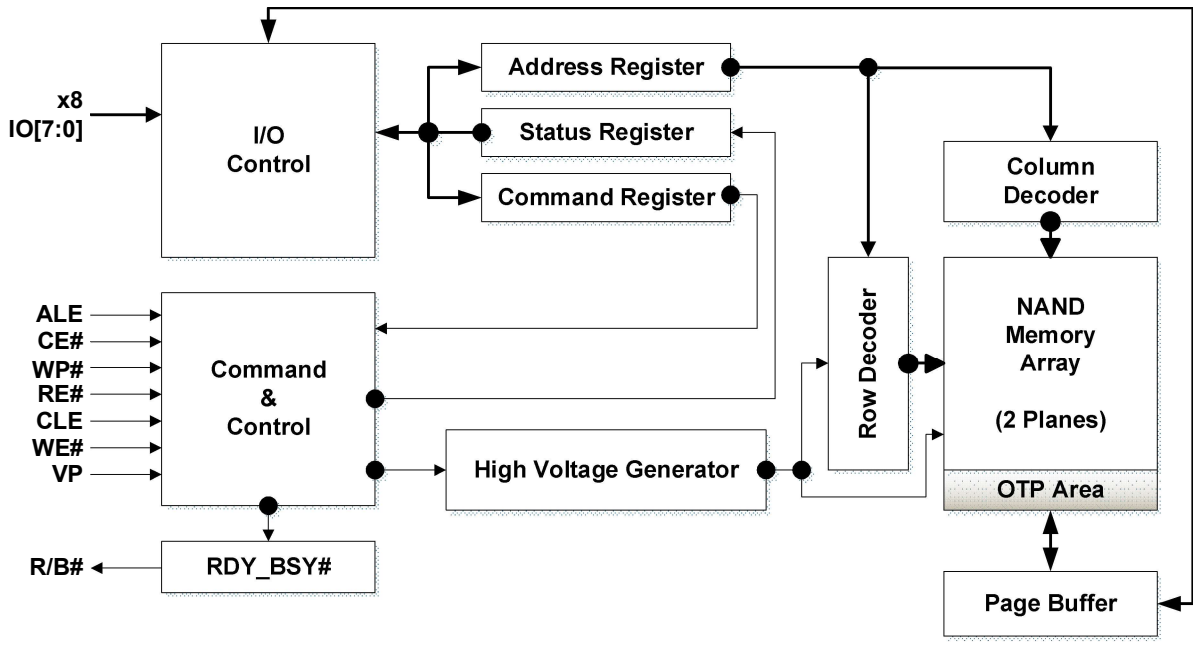


Architecture

Axia's NAND Flash devices use ONFI 1.0 compatible interface for all operations. Data, commands, and addresses are multiplexed onto the I/O pins. The commands received at the I/Os are latched into a command register and are used to determine the operations the device must perform. The addresses are latched into an address register and sent either to a row decoder to select a row address, or to a column decoder to select a column address. Data is transferred to or from the NAND Flash memory array either in a byte format (x8) through a page buffer (data buffer). The NAND Flash memory array is programmed and read using page-based operations and is erased using block-based operations. The status register reports the status of all operations.

Axia's NAND Flash devices offer a protected, one-time programmable (OTP) NAND Flash memory area. 64 full pages (2176 bytes per page) of OTP data are available on the device and the entire range is guaranteed to be good. The OTP area is accessible only through the OTP commands. Customers can use the OTP area any way they choose for permanent data storage. The OTP area leaves the factory in an unwritten state (all bits are 1s). Programming or partial-page programming enables the user to program 0 bits in the OTP area. The OTP area cannot be erased. Protecting the OTP area prevents further programming of the area.

Figure 4: Functional Block Diagram



Memory Array Architecture & Addressing

Figure 5: Memory Array Architecture

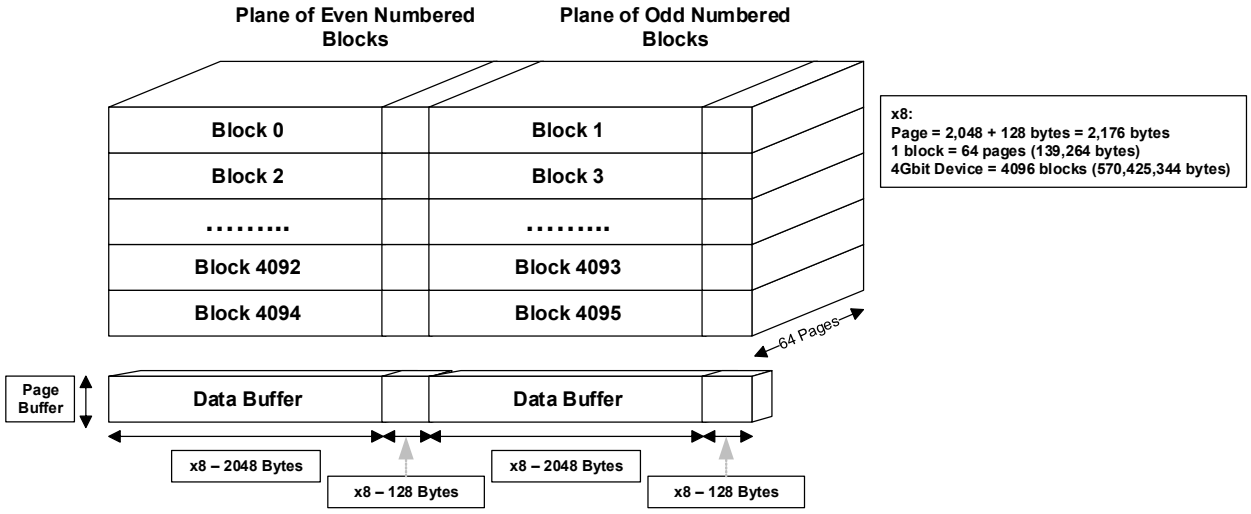


Table 4: Array Addressing Sequence – x8

x8:								
Cycle	**IO[7]**	**IO[6]**	**IO[5]**	**IO[4]**	**IO[3]**	**IO[2]**	**IO[1]**	**IO[0]**
First	BYTA7	BYTA6	BYTA5	BYTA4	BYTA3	BYTA2	BYTA1	BYTA0
Second	Logic '0'	Logic '0'	Logic '0'	Logic '0'	BYTA11	BYTA10	BYTA9	BYTA8
Third	BA7	BA6 / PLA	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	Logic '0'	Logic '0'	Logic '0'	Logic '0'	BA19	BA18	BA17	BA16

Notes:

1. BYTAx: Byte based Column address, WRDAx: Word based Column address, PAx: Page address, BAx: Block address, PLA: Plane address
2. Block address concatenated with page address = actual page address
3. 1st and 2nd address cycles form the column Address, whereas 3rd, 4th and 5th address cycles form the row address

Table 5: Block Address

Row Address	Block Number
000000h ~ 00003Fh	Block 0 (Plane 0)
000040h ~ 00007Fh	Block 1 (Plane 1)
000080h ~ 0000BFh	Block 2 (Plane 0)
0000C0h ~ 0000FFh	Block 3 (Plane 1)
•••	•••
03FF40h ~ 03FF7Fh	Block 4093 (Plane 1)
03FF80h ~ 03FFBFh	Block 4094 (Plane 0)
03FFC0h ~ 03FFFFh	Block 4095 (Plane 1)

Configuration Register (Address 90h)

Table 6: Configuration Register 1 (90h) Definition

Status Register Bits	Name	Function	Default State	Description
CR[7]	RSVD	Reserved for Future Use	0	Reserved for Future Use
CR[6]	RSVD	Reserved for Future Use	0	Reserved for Future Use
CR[5]	RSVD	Reserved for Future Use	0	Reserved for Future Use
CR[4]	ECCM	On-Die ECC Mode Configuration	0	0 = Mode 1 1 = Mode 2
CR[3]	RSVD	Reserved for Future Use	1	Reserved for Future Use Note: This bit must always be set to Logic 1 (High)
CR[2]	RSVD	Reserved for Future Use	0	Reserved for Future Use
CR[1]	OTPEP	OTP Area Entry and Protection	00	00: OTP Area Not Selected 01: OTP Area Selected (Entry) 10: Reserved 11: OTP Area Protected from Programming (Locked)
CR[0]				

Notes:

1. CR[4] – ECCM: This bit configures the internal ECC Mode of operation.
   a. Mode 1: This mode indicates if a page has a high ECC error count and is recommended to rewrite the page. If set to '1', it is recommended to rewrite the entire page. If cleared to '0', it is in normal state (internal ECC enabled, error counts are in safe level).
   b. Mode 2: This mode indicates if the page has more ECC errors than the internal engine can correct (UECC). If set to '1', it indicates that the ECC has failed and the page is uncorrectable. If cleared to '0', then it is in normal state (internal ECC enabled, safely working).

Configuration Register (Address 80h)

Table 7: Configuration Register 2 (80h) Definition

Status Register Bits	Name	Function	Default State	Description
CR[7]	RSVD	Reserved for Future Use	0	Reserved for Future Use
CR[6]	RSVD	Reserved for Future Use	0	Reserved for Future Use
CR[5]	RSVD	Reserved for Future Use	0	Reserved for Future Use
CR[4]	RSVD	Reserved for Future Use	0	Reserved for Future Use
CR[3]	IODRV	I/O Drive Strength Configuration	0000	0000: 18Ω – Full Strength 0001: 25Ω – 75% of Full Strength 0010: 35Ω – 50% of Full Strength 0011: 50Ω – 25% of Full Strength 0100 – 1111: Reserved for Future Use
CR[2]				
CR[1]				
CR[0]				

Status Register

Table 8: Status Register Definition

Status Register Bits	Name	Function	Default State	Description
SR[7]	WRPT	WP# based Device Protection	1	0 = Device is protected - WP# is Low 1 = Device Is not protected - WP# is High
SR[6]	RDY	Device Ready Status Bit	1	0 = Device is busy - not ready 1 = Device is not busy - ready
SR[5]	ARDY	Memory Array Ready Status Bit	1	0 = Memory Array is busy - not ready 1 = Memory Array is not busy - ready
SR[4]	ECCS	Error Correction Code (ECC) Status	0	0 = Error Count Normal 1 = Page Uncorrectable / Recommend Re-program
SR[3]	OTPS	One-Time Programmable (OTP) Area Protection Status	0	0 = OTP Area not protected 1 = OTP Area protected
SR[2]	RSVD	Reserved for Future Use	0	Reserved for Future Use
SR[1]	RSVD	Reserved for Future Use	0	Reserved for Future Use
SR[0]	PES	Program and Erase Status of the Current Command	0	0 = Program or Erase was successful 1 = Program or Erase was not successful

Notes:

1. SR[7] – WRPT: If set to '1', the device is not write protected and can be programmed or erased. If cleared to '0', then the device is write protected and cannot be programmed or erased. This is always valid regardless of state of the R/B#.
2. SR[6] - RDY: If set to '1', the device is ready for another command and all other status bits are valid. If cleared to '0', then the last command issued is not yet complete and all other status bits are not valid.
3. SR[5] – ARDY: If set to '1', all array operations are complete. If cleared to zero, then there is a command being processed or an array operation in progress.
4. SR[4] – ECCS: If the internal ECC is On, this bit indicates if the last read contained ECC errors. It is supported in two modes; selected using configuration register address 90h bit [4].
   a. Mode 1: This mode indicates if a page has a high ECC error count and is recommended to rewrite the page. If set to '1', it is recommended to rewrite the entire page. If cleared to '0', it is in normal state (internal ECC enabled, error counts are in safe level).
   b. Mode 2: This mode indicates if the page has more ECC errors than the internal engine can correct (UECC). If set to '1', it indicates that the ECC has failed and the page is uncorrectable. If cleared to '0', then it is in normal state (internal ECC enabled, safely working).
5. SR[3] – OTPS: This bit indicates whether the OTP is in protected mode (locked down). This bit is set to '1' if the OTP is locked down and a program command is issued. It is cleared to '0' when either not in OTP mode, or power-up or when Reset command is issued.
6. SR[0] – PES: This bit is valid for program and erase operations and shows whether the operation was a success or a failure. For two plane operation, it indicates that one or both planes failed.

Block Protection Status Register

Table 9: Block Protection Status Register Definition

Status Register Bits	Name	Function	Default State	Description
BSR[7]	RSVD	Reserved for Future Use	0	Reserved for Future Use
BSR[6]	RSVD	Reserved for Future Use	0	Reserved for Future Use
BSR[5]	RSVD	Reserved for Future Use	0	Reserved for Future Use
BSR[4]	PBLS	Permanent Block Lock Status	0	0 = Permanent Block Lock Disabled (Not Locked Down) 1 = Permanent Block Lock Enabled (Locked Down)
BSR[3]	BPLS	Block Permanent Lock Status	1	0 = Addressed Block is Protected (Locked) 1 = Addressed Block is not Protected (Not Locked)
BSR[2] **BSR[1]** **BSR[0]**	BVLS	Block Volatile Lock Status	110	000: Reserved 001: Addressed Block is Protected (Locked down) 010: Addressed Block is Protected (Locked) 011: Reserved 100: Reserved 101: Addressed Block is not Protected (Not Locked), Volatile Protection Enabled (Locked Down) 110: Addressed Block is not Protected (Not Locked), Volatile Protection Disabled (Not Locked Down) 111: Reserved

Identification Definition (Address 00h)

Table 10: Device Identification Definition (Address 00h)

Byte #		Options	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value
0	Manufacturer's ID	MID	1	0	1	0	1	1	0	1	ADh
1	Device ID	4Gbit, x8, 3.3V	1	1	0	1	1	1	0	0	DCh
2	Device Characteristics	Internal Device # 1							0	0	x8 ↓ 00h
		Internal Device # 2							0	1	
		Internal Device # 4							1	0	
		Internal Device # 8							1	1	
		Cell Type - 2 LEVEL					0	0			
		Cell Type - 4 LEVEL					0	1			
		Cell Type - 8 LEVEL					1	0			
		Cell Type - 16 LEVEL					1	1			
		Simultaneous Programmed Pages - 1			0	0					
		Simultaneous Programmed Pages - 2			0	1					
		Simultaneous Programmed Pages - 4			1	0					
		Simultaneous Programmed Pages - 8			1	1					
		Interleaved Programming - Not Supported		0							
		Interleaved Programming - Supported		1							
		Cache Program - Not Supported	0								
		Cache Program - Supported	1								
3	Array Architecture	Page Size - 1KB							0	0	x8 ↓ 05h
		Page Size - 2KB							0	1	
		Page Size - 4KB							1	0	
		Page Size - 8KB							1	1	
		Spare Area Size - 64 bytes per 2048 bytes					0	0			
		Spare Area Size - 128 bytes per 2048 bytes					0	1			
		Spare Area Size - 256 bytes per 2048 bytes					1	0			
		Spare Area Size - 512 bytes per 2048 bytes					1	1			
		Block Size - 128KB	0		0	0					
		Block Size - 256KB	0		0	1					
		Block Size - 512KB	0		1	0					
		Block Size - 1024KB	0		1	1					
	Interface Type	x8		0							
		x16		1							
4	Number of Planes	1 Plane					0	0			x8 ↓
		2 Planes					0	1			

Byte #		Options	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value
		4 Planes					1	0			04h
		8 Planes					1	1			
	Reserved	Reserved for Future Use	0	0	0	0			0	0	

Identification Definition (Address 20h)

Table 11: Device Identification Definition (Address 20h)

Byte #	Option	Value
0	"O"	4Fh
1	"N"	4Eh
2	"F"	46h
3	"I"	49h

Parameter Page Structure & Values

Table 12: Parameter Page Structure & Values

Byte #	O/M	Description	Values
Revision Information & Features Block			
0 - 3	M	Signature "O" "N" "F" "I"	4Fh, 4Eh, 46h, 49h
4 - 5	M	Revision Number	02h, 00h
6 - 7	M	Features Supported Bit # Value 0 1 = Supports 16-bit Data bus 1 1 = Supports multiple LUN operations 2 1 = Supports non-sequential page programming 3 1 = Supports interleaved operations 4 1 = Supports odd to even page Copy Back 5 - 15 0 = Reserved	1Eh, 00h
8 - 9	M	Optional Commands Supported Bit # Value 0 1 = Supports Page Cache Program 1 1 = Supports Read Cache 2 1 = Supports Get/Set features 3 1 = Supports Read Status Enhanced 4 1 = Supports Copy back 5 1 = Supports Read Unique ID 6 - 15 0 = Reserved	3Ch, 00h
10- 31		Reserved (0)	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
Manufacturer's Information Block			
32 - 43	M	Manufacturer's ID (12 ASCII Characters)	53h, 4Bh, 48h, 59h, 4Eh, 49h, 58h, 20h, 20h, 20h, 20h, 20h
44 - 63	M	Device Model (20 ASCII Characters)	48h, 32h, 37h, 55h, 34h, 47h, 38h, 46h, 32h, 47h, 44h, 41h, 2Dh, 42h, 49h, 20h, 20h, 20h, 20h, 20h
64	M	JEDEC Manufacturer's ID	ADh
65 - 66	O	Date Code	00h, 00h
67 - 79		Reserved (0)	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
Memory Organization Block			
80 - 83	M	Number of Data Bytes per Page (2048 Bytes)	00h, 08h, 00h, 00h
84 - 85	M	Number of Spare Bytes per Page (128 Bytes)	80h, 00h
86 - 89	M	Number of Data Bytes per Partial Page (512 Bytes)	00h, 02h, 00h, 00h
90 - 91	M	Number of Spare Bytes per Partial Page (32 Bytes)	20h, 00h
92 - 95	M	Number of Pages per Block (64 Pages)	40h, 00h, 00h, 00h
96 - 99	M	Number of Blocks per Logical Unit (LUN) (4096)	00h, 10h, 00h, 00h
100	M	Number of Logical Units (LUNs)	01h

Byte #	O/M	Description	Values
101	M	Number of address cycles Bit # Value 0 - 3 Row Address Cycles 4 - 7 Column Address Cycles	23h
102	M	Number of Bits per Cell	01h
103 - 104	M	Bad Blocks Number per LUN (80)	50h, 00h
105 - 106	M	Block Endurance	60h, EAh
107	M	Guaranteed Valid Blocks at Beginning of Target	00h
108 - 109	M	Block Endurance for Guaranteed Valid Blocks	60h, EAh
110	M	Number of Programs per Page	04h
111	M	Partial Programming Attributes Bit # Value 0 1 = Partial Page programming has Constraints 1 - 3 1 = Reserved (0) 4 1 = Partial Page Layout 5 - 7 0 = Reserved	10h
112	M	Number of Bits ECC Correctability	01h
113	M	Number of Interleaved Address Bits Bit # Value 0 - 3 Number of Interleaved Address Bits 4 - 7 Reserved (0)	01h
114	M	Interleaved Operation Attributes Bit # Value 0 Overlapped / concurrent Interleaving Support 1 1 = No Block Address Restrictions 2 1 = Program Cache Supported 3 Address Restrictions for Program Cache 4 - 7 0 = Reserved	00h
115 - 127		Reserved (0)	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
Electrical Parameter Block			
128	M	I/O Pin Capacitance (10pF)	00h
129 - 130	M	Timing Mode Support Bit # Value 0 1 = Supports Timing mode 0 1 1 = Supports Timing mode 1 2 1 = Supports Timing mode 2 3 1 = Supports Timing mode 3 4 1 = Supports Timing mode 4 5 1 = Supports Timing mode 5 6 - 15 0 = Reserved	00h, 00h
131 - 132	M	Program Cache Timing Mode Support Bit # Value 0 1 = Supports Timing mode 0 1 1 = Supports Timing mode 1 2 1 = Supports Timing mode 2 3 1 = Supports Timing mode 3 4 1 = Supports Timing mode 4 5 1 = Supports Timing mode 5 6 - 15 0 = Reserved	00h, 00h

Byte #	O/M	Description	Values
133 - 134	M	t_{PROG} Maximum Page Program Time (µs)	58h, 02h
135 - 136	M	t_{BERS} Maximum Block Erase Time (µs)	10h, 27h
137 - 138	M	t_R Maximum Page Read Time (µs)	C2h, 01h
139 - 140		t_{CCS} Minimum Change Column Setup Time (ns)	C8h, 00h
141 - 163		Reserved (0)	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
		Vendor Block	
164 - 165	M	Vendor Specific Revision Number	00h, 00h
166 - 253		Vendor Specific	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
254 - 255	M	Integrity CRC	F9h, 0Ah
		Redundant Parameter Pages	
256 - 511	M	Value of Bytes 0 - 255	Not Available
512 - 767	M	Value of Bytes 0 - 255	Not Available
768 +	O	Additional Redundant Parameter Pages	Not Available

Device Protection

Write Protect WP#

The write protect# (WP#) signal enables or disables PROGRAM and ERASE operations within the Flash device. When WP# is Low, PROGRAM and ERASE operations are disabled. When WP# is High, PROGRAM and ERASE operations are enabled.

It is recommended that the host drive WP# Low during power-on until VCC is stable to prevent inadvertent PROGRAM and ERASE operations.

WP# must be transitioned only when the device is in Standby and prior to beginning a command sequence. After a command sequence is complete and the device is ready, WP# can be transitioned. After WP# is transitioned, the host must wait t_{WW} before issuing a new command.

The WP# signal is always an active input, even when CE# is High. This signal should not be multiplexed with other signals.

Volatile Protection (Temporary)

The volatile protection also enables or disables PROGRAM and ERASE operations, however, the protection is temporary. Power cycling resets the protection settings to the default status (all blocks are protected if VP pin is High).

The Volatile Protection method can protect all blocks or a selected range of continuous blocks from PROGRAM and ERASE operations. The block range is selected by issuing a set of commands which consist of specifying a Lower Boundary Address and an Upper Boundary Address to unprotect – remember when VP pin is High after a power cycle, all blocks are protected. The VP pin's input level is latched during power-up and determines whether the Volatile Protection is enabled or disabled.

The block range to protect from PROGRAM and ERASE operations is selected using Unlock Block commands (23h and 24h). The Unlock Block Lower command (23h) sets the lower block address and must be followed by the Unlock Block Upper command (24h) to sets the upper block address. This address range is now unprotected – PROGRAM and ERASE operations are enabled. Any blocks that lie outside this range are protected. These unprotected blocks can be protected again by issuing the Lock All Blocks Volatile (2Ah) command. Selecting the range of blocks to unlock (unprotect) can be followed by a Lock Down Volatile command (2Ch) to set the Volatile Protection until the next power-down cycle. Following the Lock Down Volatile command, the device ignores the status of the VP pin and all further Volatile Protection command till the next power cycle.

The device does offer the option to unprotect the complementary range of blocks. This is achieved by setting an invert-bit in the Unlock command address field. If the invert-bit is set to Logic '0', the unprotected area is within and inclusive of the upper and lower block addresses; if the bit is set to Logic '1', the un-protected area is outside and exclusive of the upper and lower block addresses.

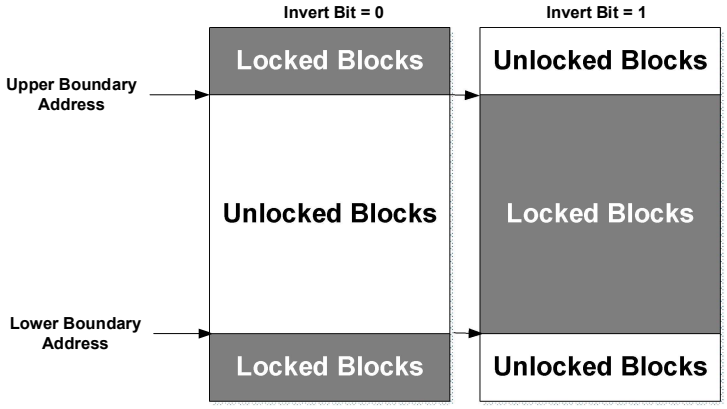
Table 13: Volatile protection Unlock Addressing Sequence – x8

x8:								
Cycle	**IO[7]**	**IO[6]**	**IO[5]**	**IO[4]**	**IO[3]**	**IO[2]**	**IO[1]**	**IO[0]**
First	BA[1]	BA[0]/PLA	Logic '0'	Logic '0'	Logic '0'	Logic '0'	Logic '0'	Invert Bit
Second	BA[9]	BA[8]	BA[7]	BA[6]	BA[5]	BA[4]	BA[3]	BA[2]
Third	Logic '0'	Logic '0'	Logic '0'	Logic '0'	BA[13]	BA[12]	BA[11]	BA[10]

Notes:

1. BAx: Block address, PLA: Plane address
2. The invert bit is set by 24h command to select whether the unprotected range is inside or outside of the range boundary. The bit is DON'T CARE for 23h command.

Figure 6: Volatile Protection range Options



Non-Volatile Protection (Permanent)

The non-volatile protection enables or disables PROGRAM and ERASE operations, however, the protection is permanent. Multiple groups of blocks can be protected at the same time. Once a group of blocks is protected, it can no longer be unprotected.

The non-volatile protection method can protect up to 64 blocks (0 to 63) organized in groups of 4 contiguous blocks. The Program Non-Volatile command sequence (4Ch-03h-1Dh-41h-80h) is used for enabling the protection. Selecting the group of blocks to protect can be followed by a Lock Down Non-volatile command sequence (4Ch-03h-1Dh-41h-80h). When this Lock Down Non-volatile command sequence is issued, all groups of blocks protected by non-volatile protection are permanently protected from program and erase operations and a non-volatile block protection command sequence can no longer be used to protect additional groups. The non-volatile protection settings are maintained after a power cycle.

The group of blocks being protected is determined by the hex value (y) in the fourth address cycle. Moreover, non-volatile block protection command sequence can only be issued for a maximum of 16 times - thus if the y value or a protected group is selected twice, then there is a group that would not be protected.

Table 14: Block Group Protection Scheme – Fourth Address Cycle Value

Y Value	Protected Group	Blocks Protected
0000	0	0,1,2,3
0001	1	4,5,6,7
0010	2	8,9,10,11
0011	3	12,13,14,15
0100	4	16,17,18,19
0101	5	20,21,22,23
0110	6	24,25,26,27
0111	7	28,29,30,31
1000	8	32,33,34,35
1001	9	36,37,38,39
1010	10	40,41,42,43
1011	11	44,45,46,47
1100	12	48,49,50,51
1101	13	52,53,54,55
1110	14	56,57,58,59
1111	15	60,61,62,63

One-Time Programmable (OTP) Region

The One-Time Programmable (OTP) Region is a single block (64 pages) which can be programmed only once. The OTP region does not support ERASE operations. There are two ways to access the OTP region; OTP AREA ENTRY command sequence (29h-17h-04h-19h) or by issuing PROGRAM CONFIGURATION REGISTERS (EFh) command with address 90h and setting the OTPEP bits to '0b01'. To exit the OTP region, a RESET command (FFh) must be entered. If OTP sequence is detected, on-die ECC engine is automatically disabled. Once in the OTP region, Program Page and Read Page commands are used to access the information.

Once the data in the OTP region is programmed, there is an option to protect the OTP region from any further programming operations. By issuing the OTP Protection sequence 4Ch-03h-1Dh-41h-80h, the OTPEP bits in the Configuration register are set to '0b11' - OTP Area Protected from Programming (Locked).

The OTP area is mapped to the Block address shown in Table 15 when OTP AREA ENTRY command sequence is executed.

Table 15: OTP Block Address

	Address
Block 06	000180h ~ 0001BF

Firmware SLC Region

The Firmware SLC region is used for storing Firmware codes for controller management. The Firmware SLC region is accessed by entering Firmware SLC Region Entry command (DAh). To exit the Firmware SLC region, a RESET command (FFh) must be entered. Once in the Firmware SLC region, Program Page and Read Page commands are used to access the information.

Partial Programming

As mentioned before, programming is page based. However, the device does allow multiple partial page programming within the same page – a minimum of 32 bytes up to a maximum of 2176 consecutive bytes in a single program cycle. The basic programming unit is 32 bytes with an associated 1 ECC syndrome. The number of consecutive partial page programming operations (NOP) within the same page must not exceed 4. As an example, 2 programming operations for the main array (1x512 bytes) and 2 programming operations for spare array (1x32bytes). Main array data shall be stored in main array region, and the corresponding spare data in the spare array region. Both main array data and spare array data must be input for each NOP operation. It is imperative that for each NOP, column address must match up correct NOP's main array region with the NOP's spare region.

During NOP programming, random data input is used to change the column address. There are 4 spare array regions matching the number of NOPs. Main array data is also divided using NOPs. Table 16 shows the 32-byte addresses for the 4 NOPs.

Table 16: NOP Column Address table

NOP0	Column Address (Hex)	NOP1	Column Address (Hex)	NOP2	Column Address (Hex)	NOP3	Column Address (Hex)
0	000~01F	**0**	200~21F	**0**	400~41F	**0**	600~61F
1	020~03F	**1**	220~23F	**1**	420~43F	**1**	620~63F
2	040~05F	**2**	240~25F	**2**	440~45F	**2**	640~65F
3	060~07F	**3**	260~27F	**3**	460~47F	**3**	660~67F
4	080~09F	**4**	280~29F	**4**	480~49F	**4**	680~69F
5	0A0~0BF	**5**	2A0~2BF	**5**	4A0~4BF	**5**	6A0~6BF
6	0C0~0DF	**6**	2C0~2DF	**6**	4C0~4DF	**6**	6C0~6DF
7	0E0~0FF	**7**	2E0~2FF	**7**	4E0~4FF	**7**	6E0~6FF
8	100~11F	**8**	300~31F	**8**	500~51F	**8**	700~71F
9	120~13F	**9**	320~33F	**9**	520~53F	**9**	720~73F
10	140~15F	**10**	340~35F	**10**	540~55F	**10**	740~75F
11	160~17F	**11**	360~37F	**11**	560~57F	**11**	760~77F
12	180~19F	**12**	380~39F	**12**	580~59F	**12**	780~79F
13	1A0~1BF	**13**	3A0~3BF	**13**	5A0~5BF	**13**	7A0~7BF
14	1C0~1DF	**14**	3C0~3DF	**14**	5C0~5DF	**14**	7C0~7DF
15	1E0~1FF	**15**	3E0~3FF	**15**	5E0~5FF	**15**	7E0~7FF
SPARE0	800~81F	**SPARE1**	820~83F	**SPARE2**	840~85F	**SPARE3**	860~87F

Bus Interface

As mentioned above, the I/O bus on the device is multiplexed. Commands, addresses and data input/output all share the same I/O pins. Commands and addresses are always supplied on I/O[7:0]. Data uses I/O[7:0] for x8 configuration.

The read, program or erase command sequences typically consist of a command input cycle, two or five address input cycles, and one or more data cycles, either input or output.

Table 17: Device Modes Selection

Mode	CE#	CLE	ALE	WE#	RE#	WP#	I/O[x]
Standby	V_{IH}	V_{IH} / V_{IL}	V_{IH} / V_{IL}	V_{IH} / V_{IL}	V_{IH} / V_{IL}	V_{CC} / V_{SS}	V_{IH} / V_{IL}
Command Input	V_{IL}	V_{IH}	V_{IL}	↑	V_{IH}	V_{IH}	Data
Address Input	V_{IL}	V_{IL}	V_{IH}	↑	V_{IH}	V_{IH}	Data
Data Input	V_{IL}	V_{IL}	V_{IL}	↑	V_{IH}	V_{IH}	Data
Data Output	V_{IL}	V_{IL}	V_{IL}	V_{IH}	↓	V_{IH} / V_{IL}	Data
Write Protect	V_{IH} / V_{IL}	V_{IH} / V_{IL}	V_{IH} / V_{IL}	V_{IH} / V_{IL}	V_{IH} / V_{IL}	V_{IL}	V_{IH} / V_{IL}

Notes:
1. V_{IH} = High (Logic '1'), V_{IL} = Low (Logic '0')

Standby

The device enters standby when CE# pin is driven V_{IH} (High). This helps reduce power consumption. In standby mode, all I/Os are tri-stated (High-Z).

Note: The device enters standby if CE# goes High and the device is not busy (no program/erase operations in progress).

Busy

The device enters busy when program, erase or read operations are initiated. The device returns to Standby after the completion of the operation. During busy state, only RESET (FFH) and READ STATUS REGISTER (70h) commands are accepted by the device.

Table 18: Recommended Signal Selections During Busy

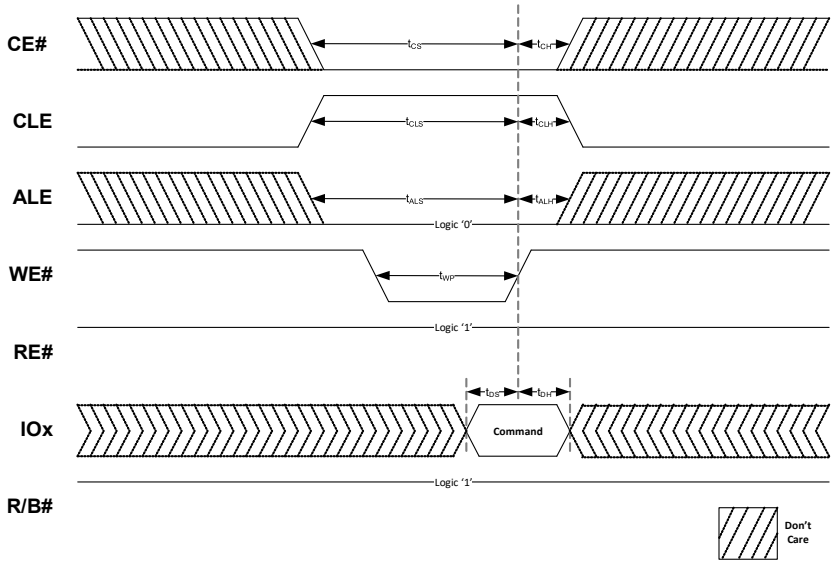
Mode	CE#	CLE	ALE	WE#	RE#	WP#	I/O[x]
Busy Period (READ)	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH} / V_{IL}	Data
Busy Period (Program)	V_{IH} / V_{IL}	V_{IH} / V_{IL}	V_{IH} / V_{IL}	V_{IH} / V_{IL}	V_{IH} / V_{IL}	V_{IH}	V_{IH} / V_{IL}
Busy Period (Erase)	V_{IH} / V_{IL}	V_{IH} / V_{IL}	V_{IH} / V_{IL}	V_{IH} / V_{IL}	V_{IH} / V_{IL}	V_{IH}	V_{IH} / V_{IL}

Notes:
1. V_{IH} = High (Logic '1'), V_{IL} = Low (Logic '0')

Command Input

A command is entered from I/O[7:0] to the command register on the rising edge of WE# when CE# is Low, ALE is Low, CLE is High, and RE# is High. Most commands are ignored if the device is busy (R/B# = 0); however, some commands, including READ STATUS (70h), are accepted.

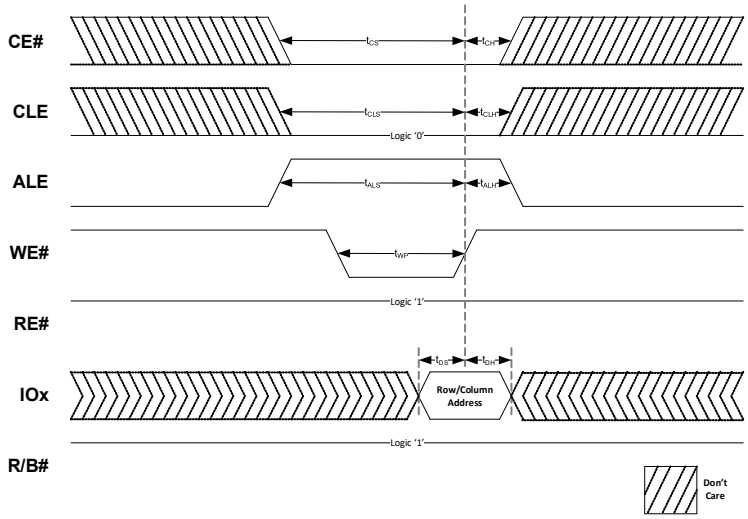
Figure 7: Command Latch Cycle



Address Input

An address is entered to the address register on the rising edge of WE# when CE# is Low, ALE is High, CLE is Low, and RE# is High. Bits that are not part of the address space must be Low (see Array Addressing Sequences). The number of address cycles required depends on the command (refer to the command descriptions to determine addressing requirements). Addresses are input on I/O[7:0] on x8 devices.

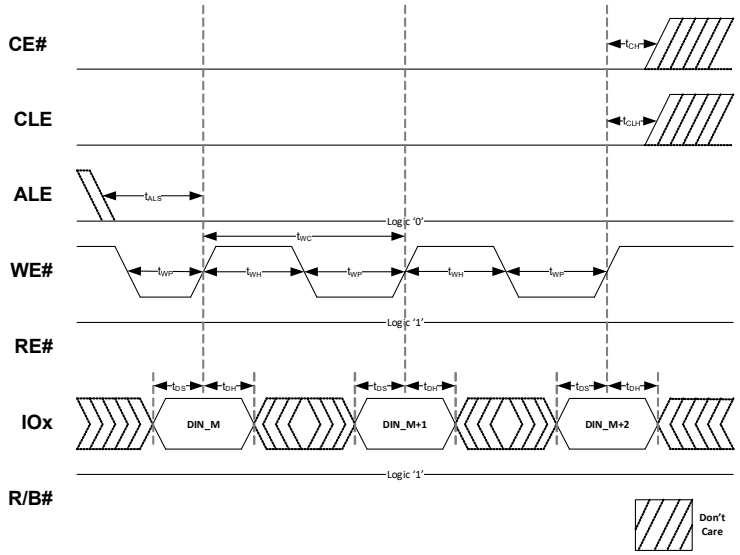
Figure 8: Address latch Cycle



Data Input

Data is entered to the page buffer on the rising edge of WE# when CE# is Low, ALE is Low, CLE is Low, and RE# is High. Data input is ignored if the device is busy (R/B# = 0). Data is input on I/O[7:0] on x8 devices.

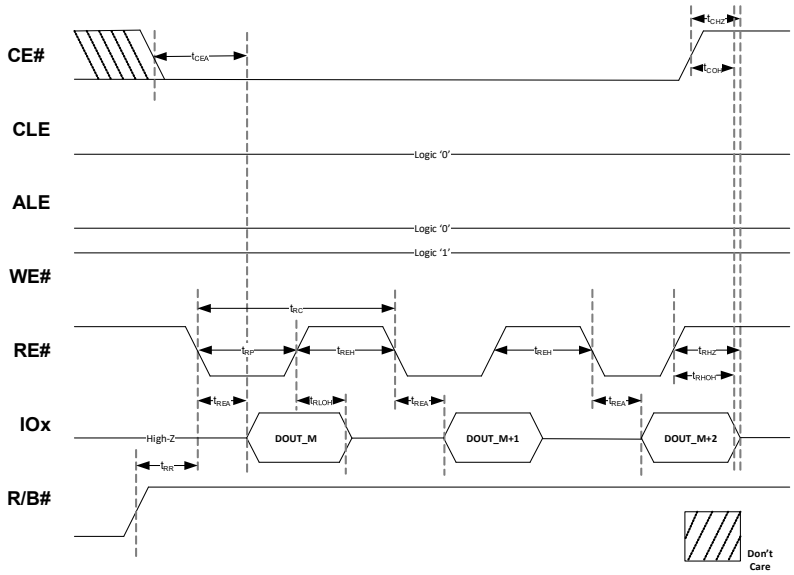
Figure 9: Data Input Cycle



Data Output

Data can only be output if the device is not busy and is in the READ state. Data output is supported following a READ operation from the NAND Flash array. Data is output from the page buffer on the falling edge of RE# when CE# is Low, ALE is Low, CLE is Low, and WE# is High. Data is output on I/O[7:0] on x8 devices.

Figure 10: Data Output Cycle



Command Set

Single Plane Commands

Table 19: Single Plane Command Set

Operation	Command Cycle #1	Address Cycles	Data Input Cycles	Command Cycle # 2	Command Accepted when Device Busy
Reset Operation					
RESET	FFh	0	0	N/A	Yes
Identification Operations					
READ ID	90h	1	0	N/A	No
READ PARAMETER PAGE	ECH	1	0	N/A	No
READ UNIQUE ID	EDh	0	0	N/A	No
Status Register Operation					
READ STATUS REGISTER	70h	0	0	N/A	Yes
Configuration Operations (Feature Set)					
READ CONFIGURATION REGISTERS (GET)	EEh	1	0	N/A	No
PROGRAM CONFIGURATION REGISTERS (SET)	EFh	1	Yes	N/A	No
Read Operations					
READ MODE	00h	0	0	N/A	No
READ PAGE	00h	5	0	30h	No
RANDOM DATA OUTPUT	05h	2	0	E0h	No
Program Operations					
PROGRAM PAGE	80h	5	Yes	10h	No
PROGRAM PAGE 2 (RE-PROGRAM)	8Bh	5	Yes	10h	No
RANDOM DATA INPUT	85h	2	Yes	N/A	No
Erase Operation					
ERASE BLOCK	60h	3	No	D0h	No
Data Move Operations (Internal)					
READ FOR DATA MOVE	00h	5	No	35h	No
PROGRAM FOR DATA MOVE	85h	5	Optional	10h	No
One-Time-Programmable Area					
OTP REGION ENTRY	29h-17h-04h-19h	0	No	N/A	No
OTP PROTECTION	4Ch-03h-1Dh-41h-80h	5 [00h, 00h, 00h, 00h, 00h]	No	10h	No
Protection Operations					
UNLOCK BLOCK LOWER	23h	3	No	N/A	No
UNLOCK BLOCK UPPER	24h	3	No	N/A	No
LOCK ALL BLOCKS VOLATILE	2Ah	0	No	N/A	No
LOCK DOWN VOLATILE	2Ch	0	No	N/A	No
PROGRAM NON-VOLATILE	4Ch-03h-1Dh-41h-80h	5 [00h, 00h, 00h, 0Yh, 00h]	No	10h	No

Operation	Command Cycle #1	Address Cycles	Data Input Cycles	Command Cycle # 2	Command Accepted when Device Busy
LOCK DOWN NON-VOLATILE	4Ch-03h-1Dh-41h-80h	5 [00h, 00h, 00h, 1Yh, 00h]	No	10h	No
READ BLOCK PROTECTION STATUS REGISTER	7Ah	3	No	N/A	No
Firmware Operations					
FIRMWARE SLC REGION ENTRY	DAh	0	No	N/A	No

Multi-Plane (MP) / Multi-Device (MD) Commands

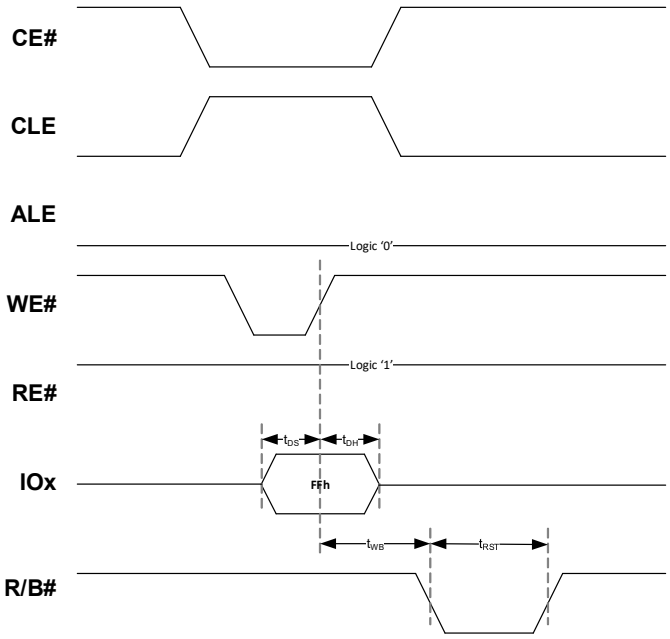
Table 20: Multi-Plane / Multi-Device Command Set

Operation	CMD Cycle #1	ADR Cycles	CMD Cycles #2	ADR Cycles	CMD Cycle #3	ADR Cycles	CAWDB
Program Operations							
PROGRAM PAGE MP	80h 80h	5 5	11h - 81h 11h - 80h	5 5	10h 10h	-	No
PROGRAM PAGE 2 MP (RE-PROGRAM)	8Bh	5	11h – 8Bh	5	10h	-	No
Erase Operations							
ERASE BLOCK MP	60h 60h	3 3	60h D1h - 60h	3 3	D0h D0h	-	No
Read Operations							
READ MP	00h	5	32h		30h	-	
Data Move Operations (Internal)							
PROGRAM FOR DATA MOVE MP	85h 85h	5 5	11h - 81h 11h - 85h	5 5	10h 10h	-	No
Status Register Operation							
READ STATUS REGISTER MP/MD	78h	3	-	-	-	-	Yes

RESET Operation (FFh)

The RESET command (FFh) places the NAND Flash device into the standby mode and aborts any command sequence in progress. READ, PROGRAM, and ERASE commands can be aborted while the device is in the busy state using the RESET command. The contents of the memory location being programmed, or the block being erased are no longer valid - the data may be partially erased or programmed and is invalid. The command register is cleared and is ready for the next command. The page buffer contents are marked invalid. The status register contains the value E0h when WP# is High; otherwise it contains the value 60h. R/B# goes Low for t_{RST} during which the device completes the reset operation.

Figure 11: RESET Operation



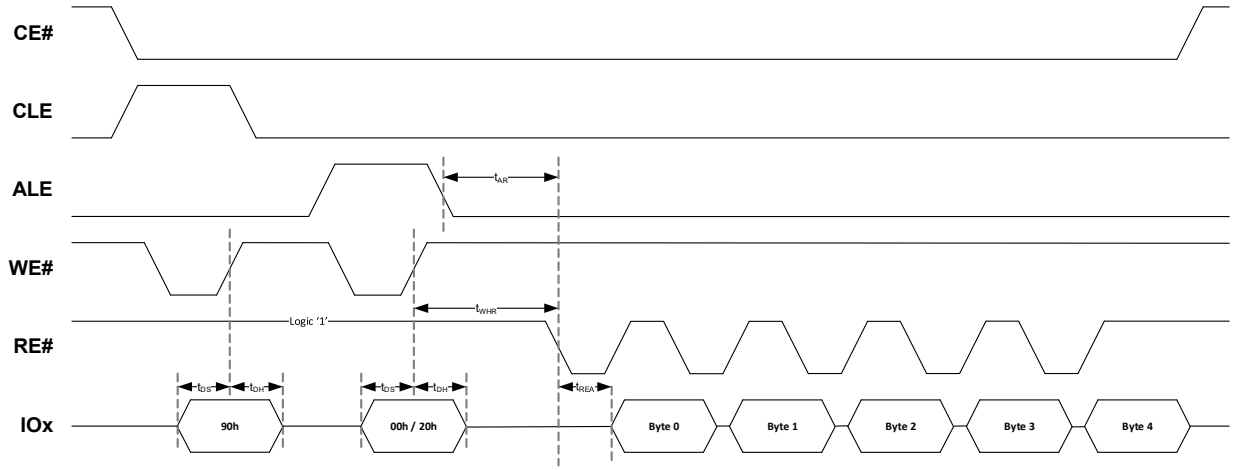
READ ID Operation (90h)

The READ ID (90h) command is used to read the product identification information programmed into the NAND Flash device. This command is accepted when the device is in Standby mode. Writing 90h to the command register puts the device in read ID mode. The device stays in this mode until another valid command is issued.

When the 90h command is followed by an 00h address cycle, the device returns a 5-byte identifier code that includes the manufacturer ID, device configuration, and part-specific information. Reading beyond the four bytes yields indeterminate data.

When the 90h command is followed by a 20h address cycle, the device returns the 4-byte ONFI identifier code. Reading beyond the four bytes yields indeterminate data.

Figure 12: READ ID Operation



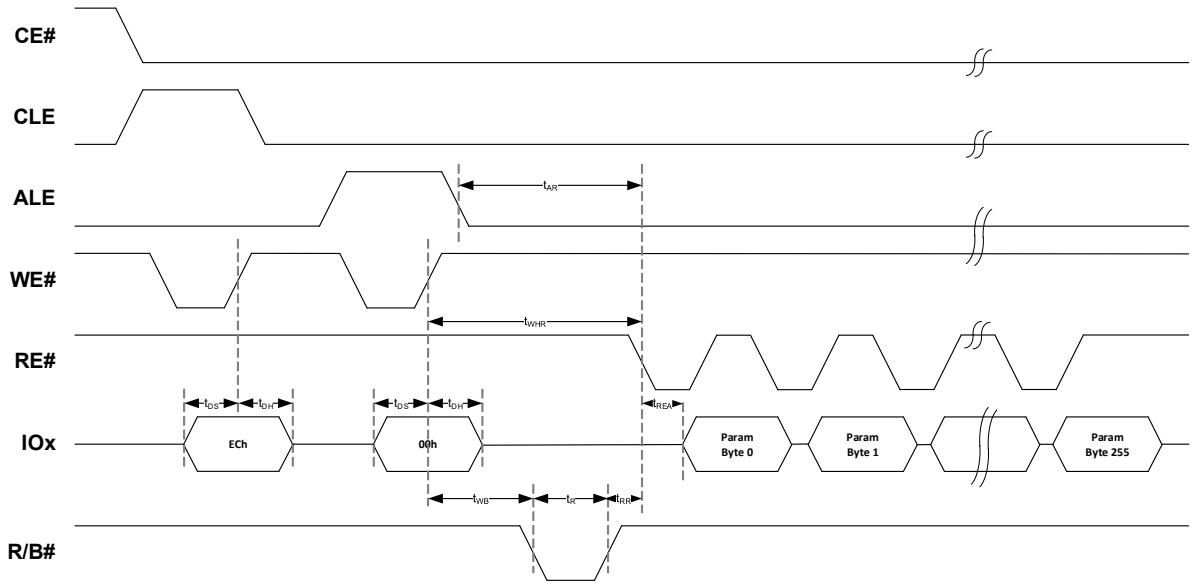
READ PARAMETER PAGE Operation (ECh)

The READ PARAMETER PAGE (ECh) command is used to read the ONFI parameter page which describes the device's organization, features, timings and other behavioral parameters. These values are static and cannot be altered by the user. The READ PARAMETER PAGE command is accepted by the device when it is in Standby mode.

Writing ECh to the command register puts the device in read parameter page mode. It stays in this mode until another valid command is issued. When the ECh command is followed by an 00h address cycle, the device goes busy for t_R. If the READ STATUS (70h) command is used to monitor for command completion, the READ MODE (00h) command must be used to re-enable data output mode.

To insure data integrity, x8 devices contain at least eight copies of the parameter page. Each parameter page is 256 bytes. If the initial READ PARAMETER PAGE (ECh) command fails to retrieve a correct copy of the parameter page, the command can be reissued until a correct copy is retrieved. If desired, the RANDOM DATA OUTPUT (05h-E0h) command can be used to change the location of data output.

Figure 13: Parameter Read Operation

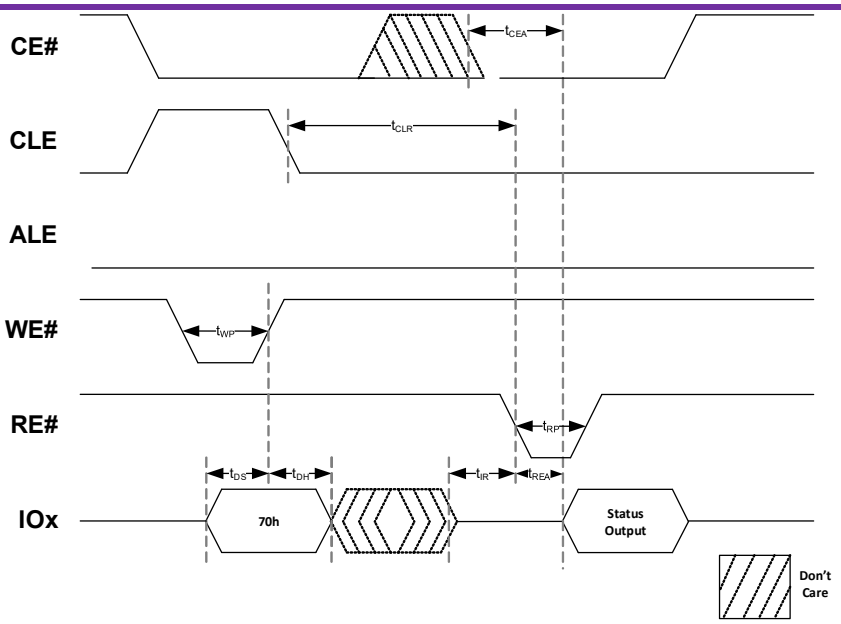


READ STATUS REGISTER Operation (70h)

The device provides its status through its 8-bit status register. After the READ STATUS REGISTER (70h) command is issued, status register output is enabled. The contents of the status register are returned on I/O[7:0] for each data output request (toggle RE#).

When the status register output is enabled, changes in the status register are seen on I/O[7:0] as long as CE# and RE# are Low; it is not necessary to toggle RE# to see the status register update. The command register remains in Status Read mode until another valid is issued to it.

Figure 14: Read Status Register Operation



READ MODE Operation (00h)

The READ MODE (00h) command enables data output and disables status output after a READ operation (00h-30h, 00-31h) has been modified with a status operation (70h). This command is accepted by the device when it is ready (RDY = 1, ARDY = 1).

READ PAGE Operation (00h – 30h)

The READ PAGE (00h–30h) command copies a page (x8: 2176 bytes) from the NAND Flash array to its page buffer and enables data output. This command is accepted by the device when it is ready (RDY = 1, ARDY = 1).

To read a page from the NAND Flash array, the host must first write the 00h command to the command register, followed by writing 5 address cycles to the address registers, and conclude with writing the 30h command. The device will go busy (RDY = 0, ARDY = 0) for t_R as data is transferred. To determine the progress of the data transfer, the host can monitor the device's R/B# signal or use the READ STATUS REGISTER operation (70h). If the READ STATUS REGISTER operation is used to monitor the progress, the host must disable status output and enable data output by issuing the READ MODE (00h) command when the device gets ready (RDY = 1, ARDY = 1).

Two types of read operations are available: random read and serial page read. During data output the READ RANDOM DATA (05h-E0h) command can be issued if random data output from the page is desired. Otherwise, the data output is sequential.

Figure 15: Read Page Operation

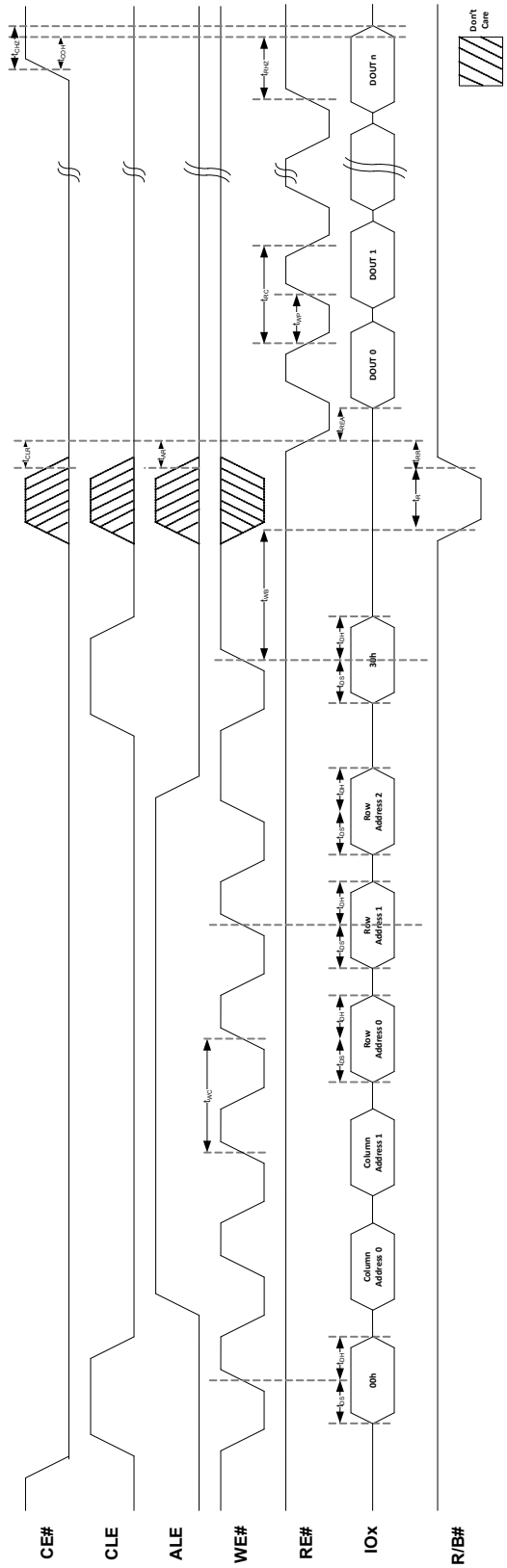
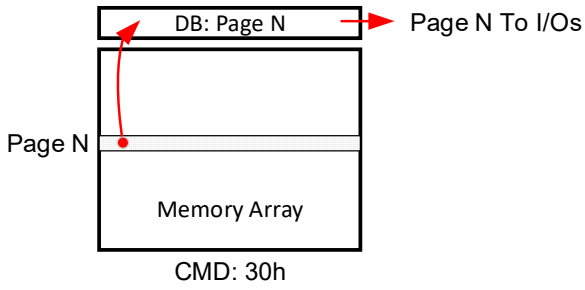


Figure 16: Read Page Operation Overview



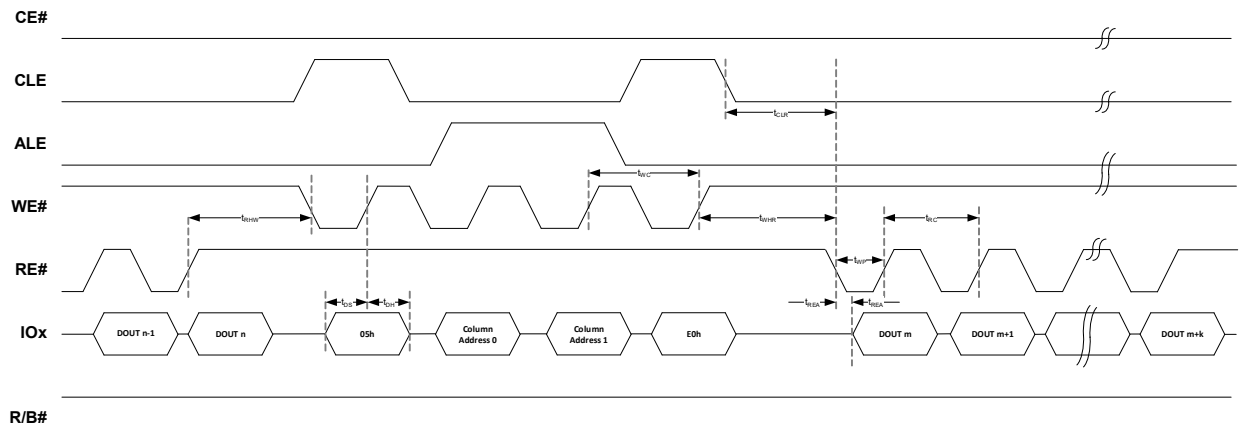
A data transfer operation from the cell array to the Data Buffer starts on the rising edge of WE# in the 30h command input cycle (after the address information has been latched in). The device will be in the Busy state during this transfer period.

READ RANDOM DATA Operation (05h – E0h)

The READ RANDOM DATA (05h-E0h) command changes the column address of the selected page buffer and enables data output from the device. This command is accepted when the device is ready (RDY = 1; ARDY = 1).

Writing 05h to the command register, followed by two column address cycles containing the column address, followed by the E0h command, puts the device into data output mode. After the E0h command cycle is issued, the host must wait at least t_{WHR} before requesting data output. The device stays in data output mode until another valid command is issued.

Figure 17: Read Random Operation



PROGRAM PAGE Operation (80h – 10h)

As mentioned in the architecture section, programming is page based. Pages must be programmed sequentially within a block. However, the device also allows multiple partial page programming in a single page program cycle.

The PROGRAM PAGE (80h-10h) command enables the host to input data to page buffer and program it to the addressed block and page in the Flash memory array. This command is accepted by the device when it is ready (RDY = 1, ARDY = 1).

To program an addressed page in the Flash array, write 80h to the command register. Write 5 address cycles containing the column address and row address. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the RANDOM DATA INPUT command can be issued. When data entry is complete, write 10h to the command register. The device will go busy (RDY = 0, ARDY = 0) for t_{PROG} as data is programmed.

To determine the progress of the data transfer, the host can either monitor the device's R/B# signal or, execute the status operation (70h). When the device is ready (RDY = 1, ARDY = 1), the host should check the status of the Program/Erase status (PES) bit.

Figure 18: Program Page Operation

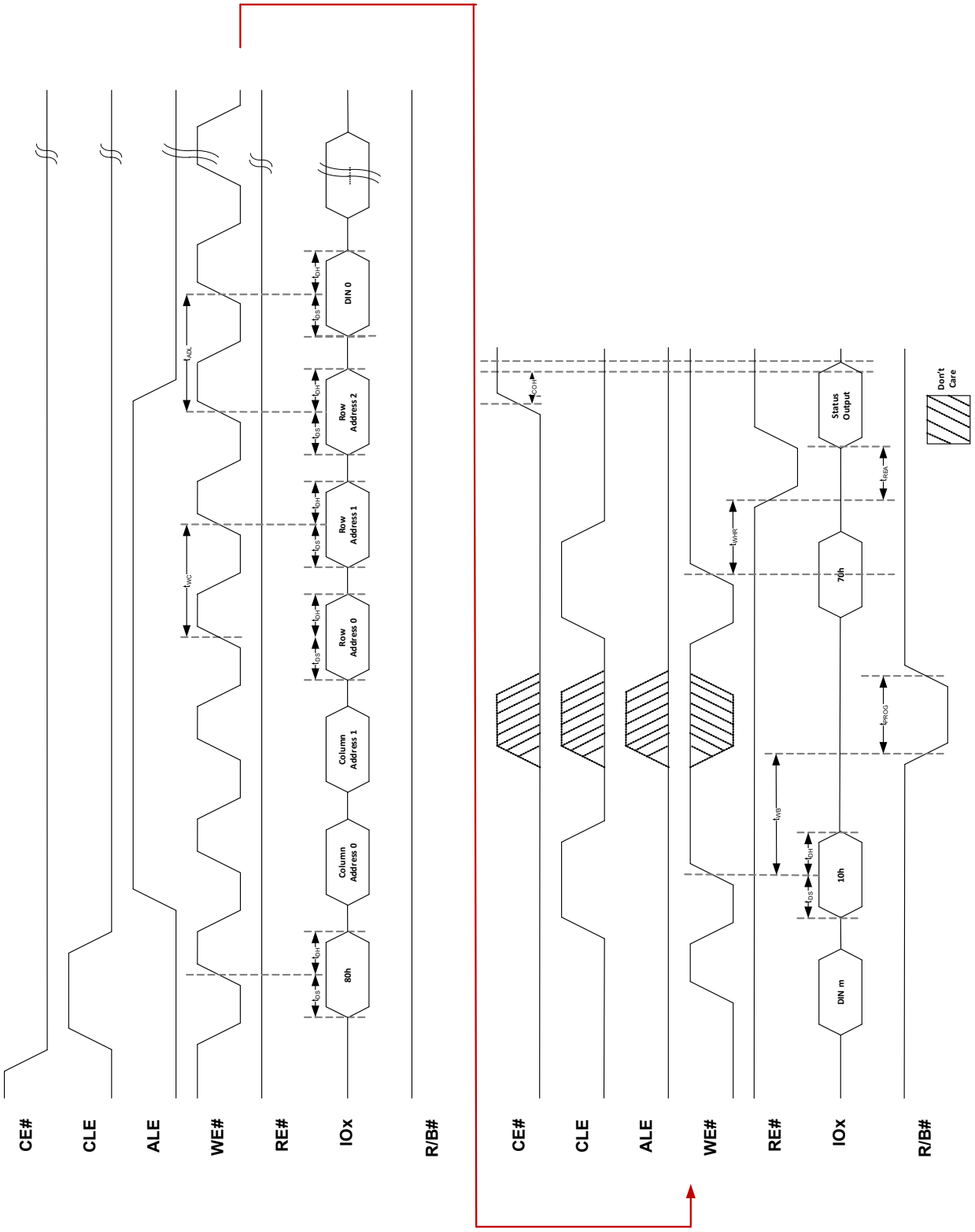
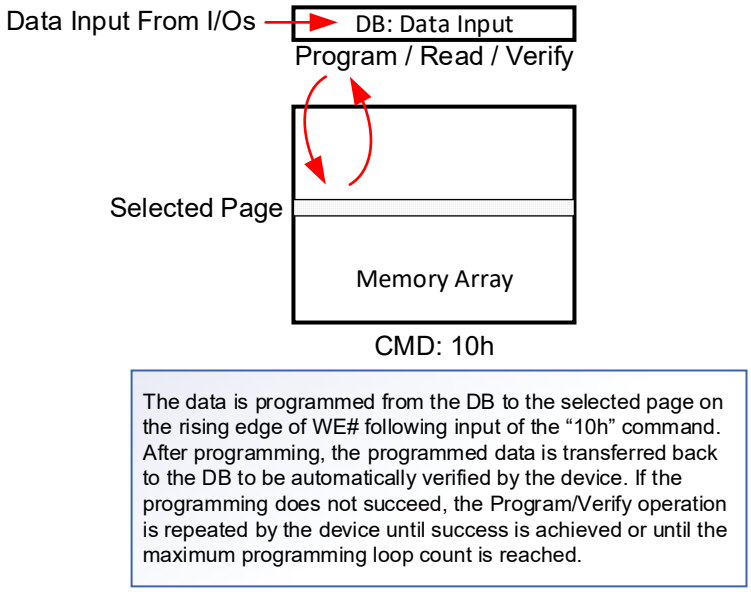


Figure 19: Program Page Operation Overview



PROGRAM PAGE 2 (RE_PROGRAM) (8Bh – 10h)

The PROGRAM PAGE 2 (8Bh-10h) command allows re-programming of the same data into a new page if the last PAGE PROGRAM (80h-10h) operation failed. This command is most efficient if the data to be programmed is not changed. However, if the data needs to be altered, data in cycles can be initiated before issuing the program confirm "10h" command.

To re-program the loaded data into a new page address in the Flash array, write 8Bh to the command register. Write 5 address cycles containing the column address and row address of the new page. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the RANDOM DATA INPUT command can be issued. When data entry is complete, write 10h to the command register. The device will go busy (RDY = 0, ARDY = 0) for t_{PROG} as data is programmed.

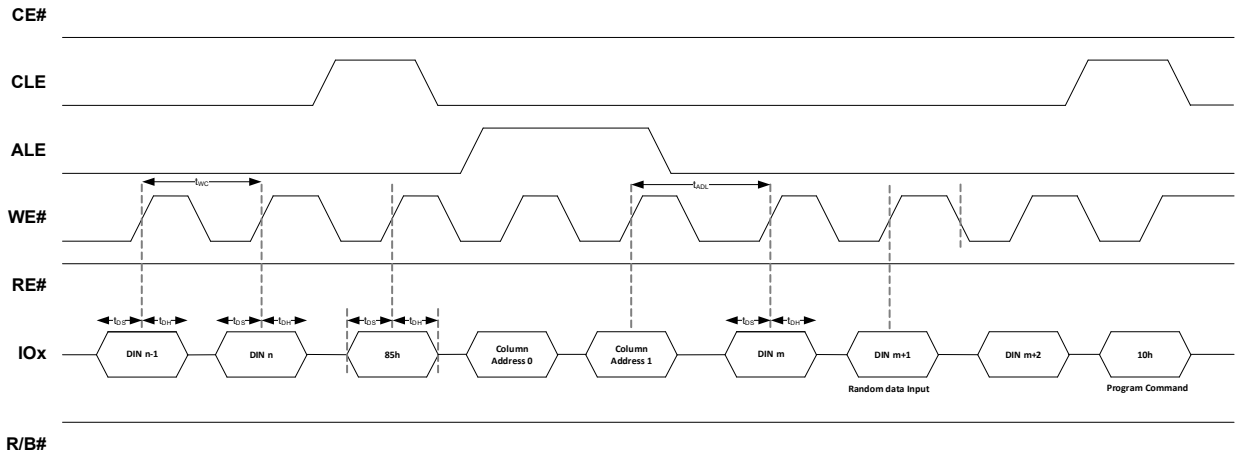
To determine the progress of the data transfer, the host can either monitor the device's R/B# signal or, execute the status operation (70h). When the device is ready (RDY = 1, ARDY = 1), the host should check the status of the Program/Erase status (PES) bits.

RANDOM DATA INPUT Operation (85h)

The RANDOM DATA INPUT (85h) command changes the column address and enables data input. This command is accepted by the device when it is ready (RDY = 1; ARDY = 1). The RANDOM DATA INPUT (85h) command is allowed after the required address cycles are specified, but prior to the final program command cycle (10h,15h) of the following commands while data input is permitted: PROGRAM PAGE (80h-10h) and PROGRAM FOR DATA MOVE (85h-10h).

Writing 85h to the command register, followed by two column address cycles containing the column address, puts the device into data input mode. After the second address cycle is issued, the host must wait at least t_{ADL} before inputting data. The device stays in data input mode until another valid command is issued.

Figure 20: Random data Input Operation



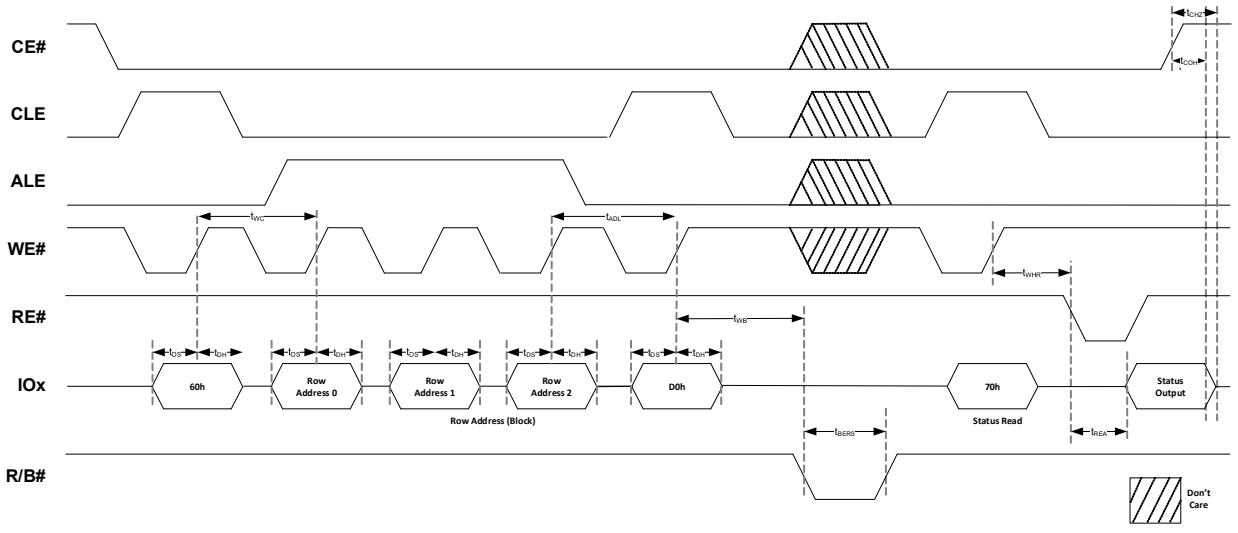
ERASE BLOCK Operation (60h – D0h)

The erase operation in the device is done on a block basis. The ERASE BLOCK (60h-D0h) command erases the specified block in the NAND Flash array. This command is accepted by the device when it is ready (RDY = 1, ARDY = 1).

To erase a block, write 60h to the command register. Then write 3 address cycles containing the row address (the page address is not required). Conclude by writing D0h to the command register. The device will go busy (RDY = 0, ARDY = 0) for t_{BERS} while the block is erased.

To determine the progress of the data transfer, the host can either monitor the device's R/B# signal or, execute the READ STATUS REGISTER (70h) command. When the device completes an ERASE Block operation, the host must check the status of the PES bit for erase completion status.

Figure 21: Erase Block Operation



READ FOR DATA MOVE Operation (00h – 35h)

The READ FOR DATA MOVE (00h-35h) operation working in conjunction with PROGRAM FOR DATA MOVE (85h-10h) operation provides a very efficient copy-back operation where data stored in one page can be written to another page without utilizing any of the host's resources. It is most efficient if loading of the data is not required (if data modifications are not needed).

The READ FOR DATA MOVE (00h-35h) command is functionally identical to the READ PAGE (00h-30h) command, except that 35h is written to the command register instead of 30h.

It is recommended that the host read the data out of the device to verify the data prior to issuing the PROGRAM FOR DATA MOVE (85h-10h) command to prevent the propagation of data errors.

PROGRAM FOR DATA MOVE Operation (85h – 10h)

The PROGRAM FOR DATA MOVE (85h-10h) command is functionally identical to the PROGRAM PAGE (80h-10h) command, except that when 85h is written to the command register.

Figure 22: Read/Program For Data Move Operation

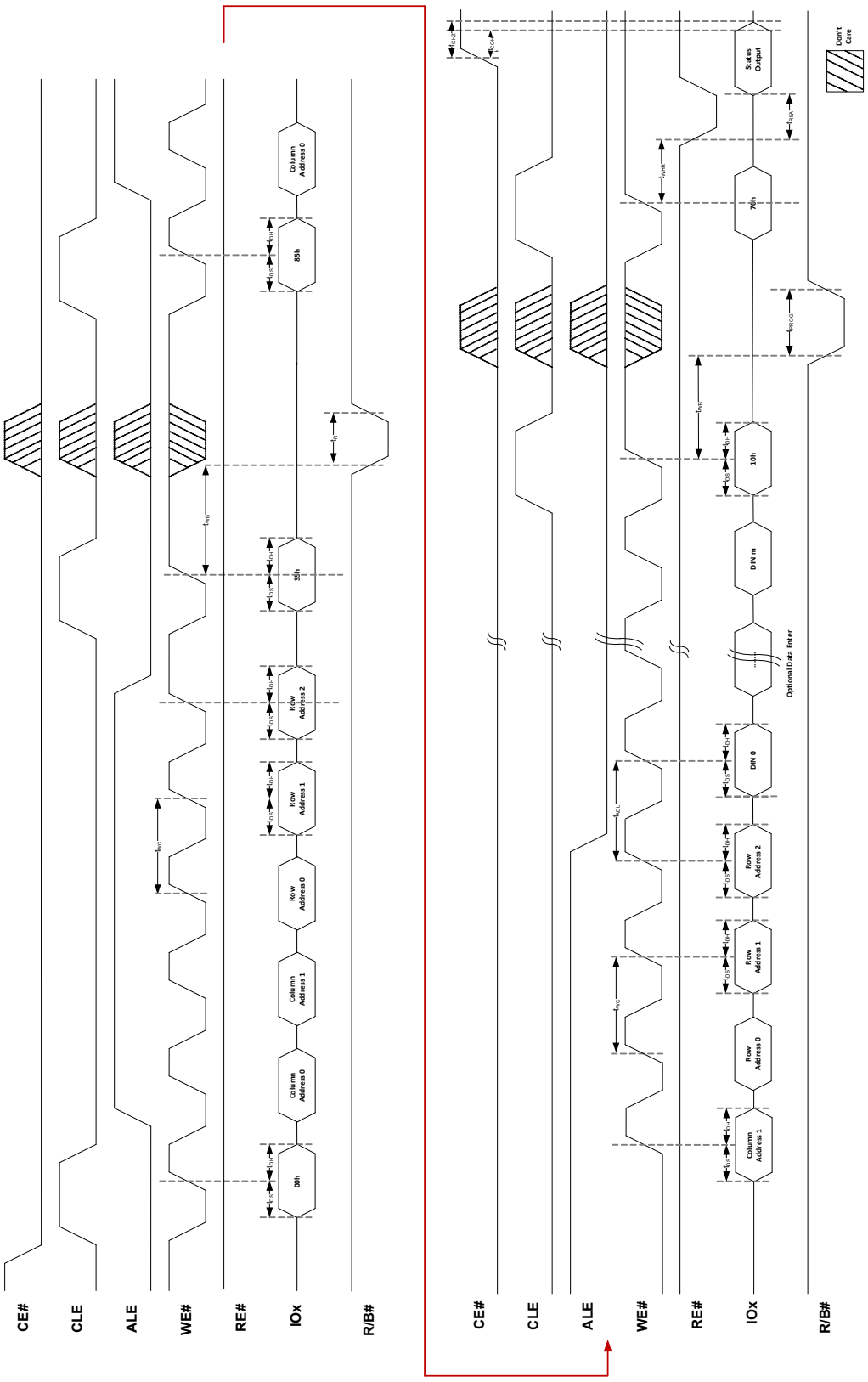
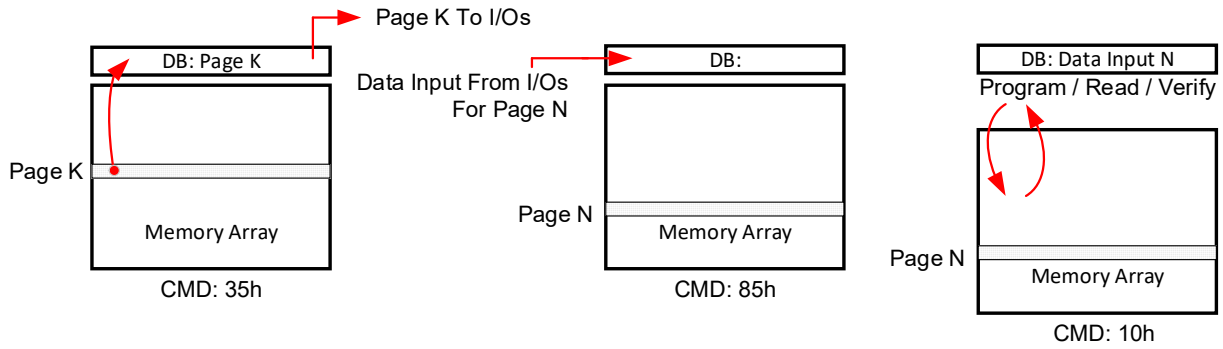


Figure 23: Read/Program For Data Move Operation Overview

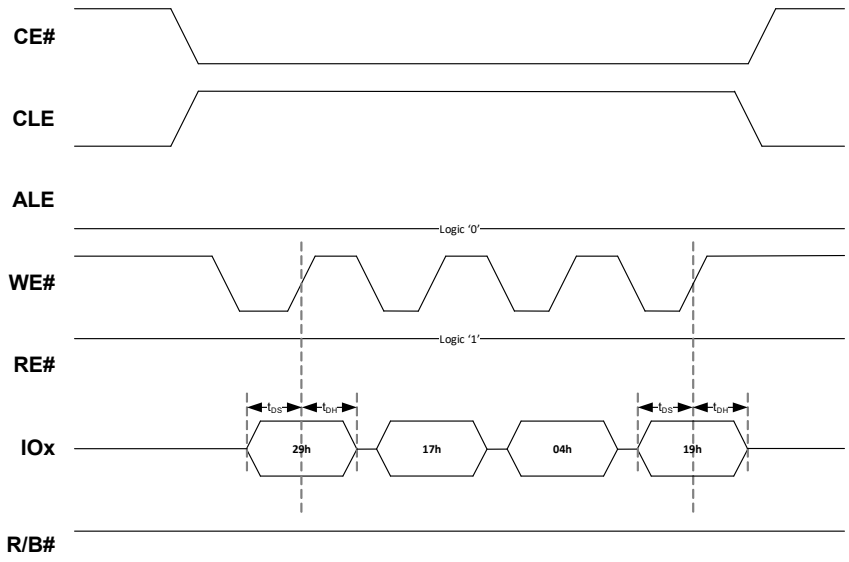


Data Move operation from Page K to Page N is as following:
1 Data for Page K is transferred to the Data Buffer (DB) - Read for Data Move.
2 Data for Page K is read out.
3 Data Move to Page address N is input and any data updates are implemented.
5 By issuing the 10h command, the data in the DB is programmed to Page N – Program for Data Move

OTP AREA ENTRY (29h-17h-04h-19h)

The OTP AREA ENTRY (29h-17h-04h-19h) command enables the host to access the One-Time-Programmable memory array. The device is then ready to accept PAGE READ (00h-30h) and PAGE PROGRAM (80h-10h) commands. The OTP area consists of a single block size (64 pages), and hence only row addresses between 00h and 3Fh are allowed. The host must issue the RESET (FFh) command to exit the OTP area and access the normal flash array.

Figure 24: OTP Area Entry Operation



MULTI-PLANE Operations

Axia's 4Gbit NAND Flash devices are divided into two physical planes. Each plane contains a page buffer independent of the other plane. The planes are addressed via the lowest block address bit (BA[6]). Specific details are provided in array addressing sequence.

Two-plane operations must be of the same type across the planes; for example, it is not possible to perform a PROGRAM operation on one plane with an ERASE operation on another.

When issuing a two-plane program or erase operation, use the READ STATUS (70h) command and check whether the previous operation(s) failed. If the READ STATUS (70h) command indicates that an error occurred (PES = 1), use the READ STATUS MP (78h) command to determine which plane's operation failed.

MULTI-PLANE Operations' Addressing Requirements

Multi-plane commands for 4Gbit devices require two, five-cycle addresses; one address per plane. For a given multi-plane operation, these addresses are subject to the following requirements:

- The plane select bit, BA[6], must be different for each issued address.
- The page address bits, PA[5:0], must be identical for each issued address.
- The READ STATUS REGISTER Multi-Plane / Multi-Device (78h) command can be used following multi-plane program page and erase block operations to check the status.

PROGRAM PAGE MP Operation

(80h – 11h – 81h – 10h) / (80h – 11h – 80h – 10h)

The PROGRAM PAGE MP (80h-11h-81h/80h-10h) command enables the host to program two pages in parallel (one in each plane). A multi-plane program cycle consists of a double serial data loading period in which up to 4224 bytes of data can be loaded into the page buffer, followed by a non-volatile programming period where the loaded data is programmed into the addressed cells.

To input a page to the page bffer and queue it to be moved to the NAND Flash array at the specified address, write 80h to the command register followed by five address cycles containing the column address and row address. Data input cycles follow where serial data is input beginning at the specified address. At any time during the data input cycle, the RANDOM DATA INPUT (85h) command can be issued. When data input is complete, write 11h to the command register. The device will go busy (RDY = 0, ARDY = 0) for t_{PBSY}.

To determine the progress of t_{PBSY}, the host can monitor the devices R/B# signal or, issue the READ STATUS REGISTER operations (70h, 78h). When the device's status shows that it is ready (RDY = 1), additional PROGRAM PAGE MULTI-PLANE (80h-11h) commands can be issued to queue additional planes for data transfer. Alternatively, the PROGRAM PAGE (80h-10h) command can be issued.

When the PROGRAM PAGE (80h-10h) command is used as the final command of a multi-plane program operation, data is transferred from the page buffer to the NAND Flash array for all addressed planes during t_{PROG}. When the device is ready (RDY = 1, ARDY = 1), the host should check the status of the PES bits for each of the planes to verify that programming was successfully.

Note that all commands are prohibited between 11h and 81h/80h except for READ STATUS REGISTER / READ STATUS REGISTER MP/MD and RESET commands.

Note that the PROGRAM PAGE MP command is available only within two paired blocks in separate planes. This is accomplished in two ways:

1. (80h – 11h – 81h – 10h) - By setting the block address bits for the first plane to all zeros and the second address issued selects the block for both planes (plane address bit must be '1' in the second address issued).
2. (80h – 11h – 80h – 10h) - Both addresses are issued in this protocol, however, the block address bits must be the same except for the bit(s) that select the planes.

Figure 25: Program Page MP Operation

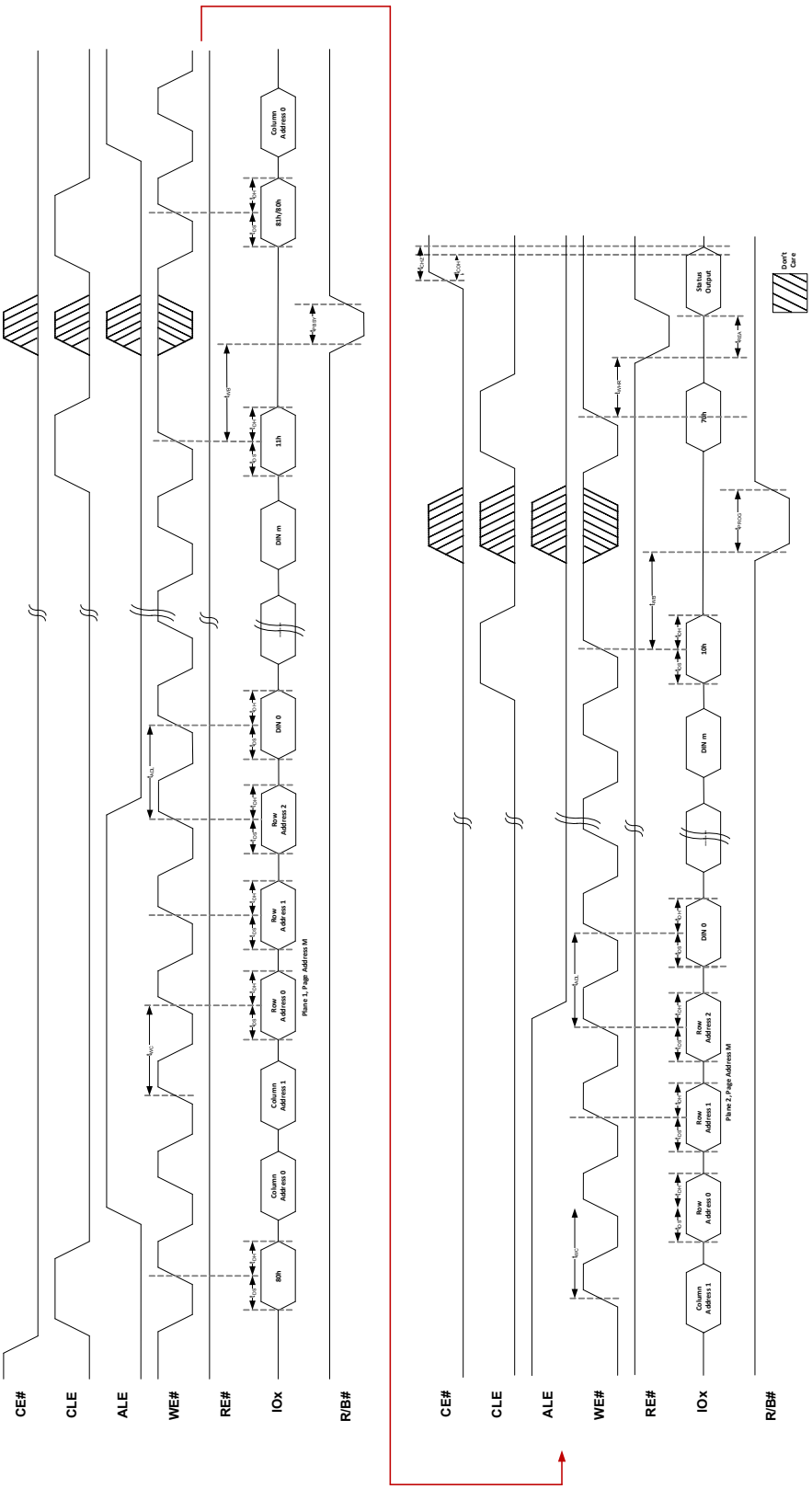
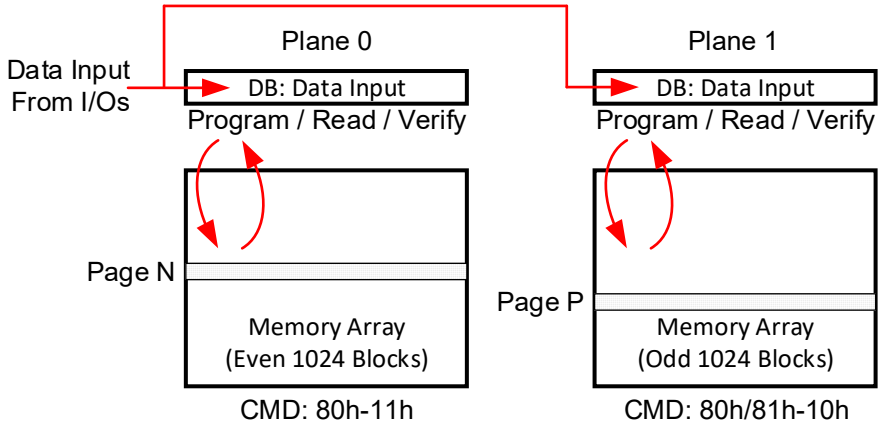


Figure 26: Program Page MP Operation Overview



The data is programmed from the DBs to the selected pages in the two planes on the rising edge of WE# following input of the "10h" command. After programming, the programmed data is transferred back to the DBs to be automatically verified by the device. If the programming does not succeed, the Program/Verify operation is repeated by the device until success is achieved or until the maximum programming loop count is reached.

PROGRAM PAGE 2 MP (RE-PROGRAM) (8Bh – 11h – 8Bh – 10h)

The PROGRAM PAGE 2 MP (8Bh-11h-8Bh-10h) command enables the host to re-program the same data into two new pages if the last PAGE PROGRAM MP (80h-10h) operation failed. This command is most efficient if the data to be programmed is not changed. However, if the data needs to be altered, data in cycles can be initiated before issuing the program confirm "10h" command.

To re-program the loaded data into new page addresses in the Flash array, write 8Bh to the command register. Write 5 address cycles containing the column address and row address of the first new page. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the RANDOM DATA INPUT command can be issued. When data entry is complete, write 11h to the command register. The device will go busy for t_{PBSY}. Following this, write 8Bh again to the command register to initiate the next new page entry. Write 5 address cycles containing the column address and row address of the second new page. Data input cycles follow. Serial data is input beginning at the column address specified. At any time during the data input cycle the RANDOM DATA INPUT command can be issued. When data entry is complete, write 10h to the command register. The device will go busy (RDY = 0, ARDY = 0) for t_{PROG} as data is programmed.

To determine the progress of the data transfer, the host can either monitor the device's R/B# signal or, execute the status operation (70h). When the device is ready (RDY = 1, ARDY = 1), the host should check the status of the Program/Erase status (PES) bits.

Note that all commands are prohibited between 11h and 8Bh except for READ STATUS REGISTER / READ STATUS REGISTER MP/MD and RESET commands.

Note that the PROGRAM PAGE 2 MP command is available only within two paired blocks in separate planes. This is accomplished by:

1. (B0h – 11h – 8Bh – 10h) - By setting the block address bits for the first plane to all zeros and the second address issued selects the block for both planes (plane address bit must be '1' in the second address issued).

.

ERASE BLOCK MP Operation

(60h – 60h – D0h) / (60h – D1h – 60h – D0h)

The ERASE BLOCK MP (60h-D1h or 60h) command queues a plane addressed block to be erased in the NAND Flash array. This command can be issued one or more times. Each time a new plane address is specified, that block in the plane is queued to be erased. To specify the final block to be erased and to begin the ERASE operation for all previously queued planes, issue the ERASE BLOCK (60h-D0h) command. This command is accepted by the device when it is ready (RDY = 1, ARDY = 1).

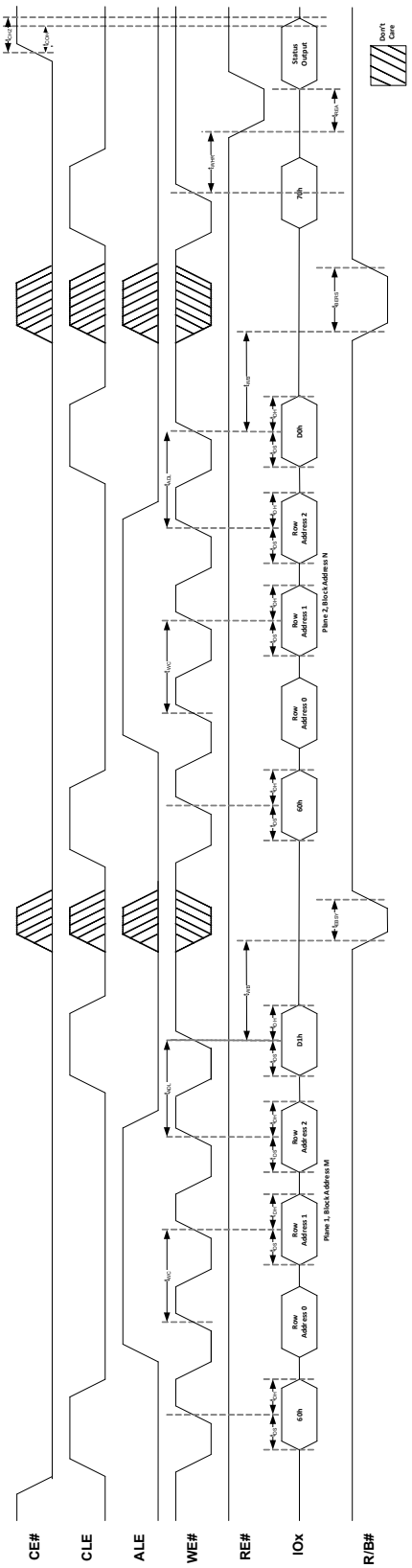
To queue a block to be erased, write 60h to the command register, then write three address cycles containing the row address; the page address is ignored. Conclude by writing D1h to the command register. The device will go busy (RDY = 0, ARDY = 0) for t_{EBSY}. Note that if D1h is omitted, the device will not go busy for t_{EBSY}.

To determine the progress of t_{EBSY}, the host can monitor the device's R/B# signal, or alternatively, the READ STATUS REGISTER operations (70h, 78h) can be used. When the device's status shows that it is ready (RDY = 1, ARDY = 1), additional ERASE BLOCK MP (60h-D1h) commands can be issued to queue additional planes for erase. Alternatively, the ERASE BLOCK (60h-D0h) command can be issued to erase all queued blocks.

Note that the ERASE BLOCK MP command is available only within two paired blocks in separate planes. This is accomplished in two ways:

1. (60h – 60h – D0h) - By setting the block address bits for the first plane to all zeros and the second address issued selects the block for both planes (plane address bit must be '1' in the second address issued).
2. (60h – D1h – 60h – D0h) - Both addresses are issued in this protocol, however, the block address bits must be the same except for the bit(s) that select the planes.

Figure 27: Erase Block MP Operation



PROGRAM FOR DATA MOVE MP Operation

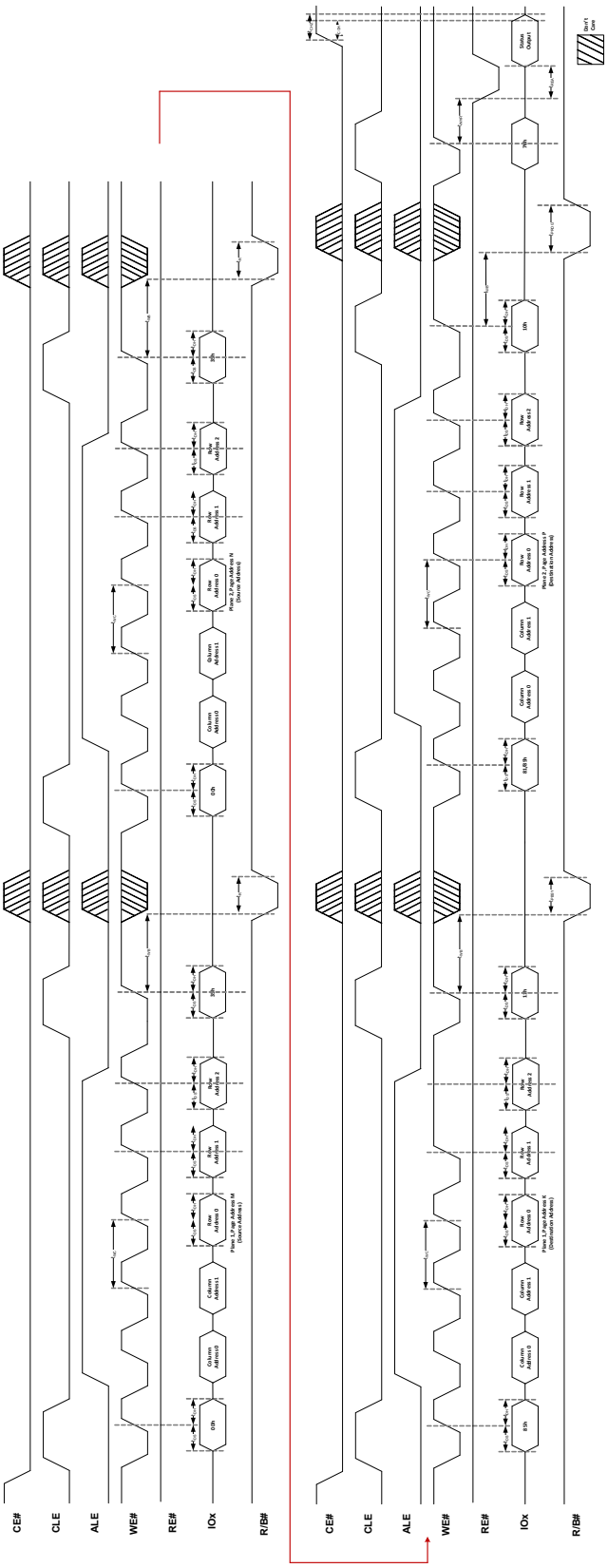
(85h – 11h - 81h – 10h) / (85h – 11h – 85h – 10h)

The PROGRAM FOR DATA MOVE MP (85h-11h) command is functionally identical to the PROGRAM PAGE MP (85h-11h) command. Program for multi-plane data move program must be preceded by 2 single page reads (1st page must be read from the 1st plane and 2nd page from the 2nd plane). Multi-plane copy back cannot cross plane boundaries: the contents of the source page of one plane can only be copied to a destination page in the same plane.

Note that the PROGRAM FOR DATA MOVE MP command is available only within two paired blocks in separate planes. This is accomplished in two ways:

1. (85h – 11h – 81h – 10h) - By setting the block address bits for the first plane to all zeros and the second address issued selects the block for both planes (plane address bit must be '1' in the second address issued).
2. (85h – 11h – 85h – 10h) - Both addresses are issued in this protocol, however, the block address bits must be the same except for the bit(s) that select the planes.

Figure 28: Program for Data Move MP Operation

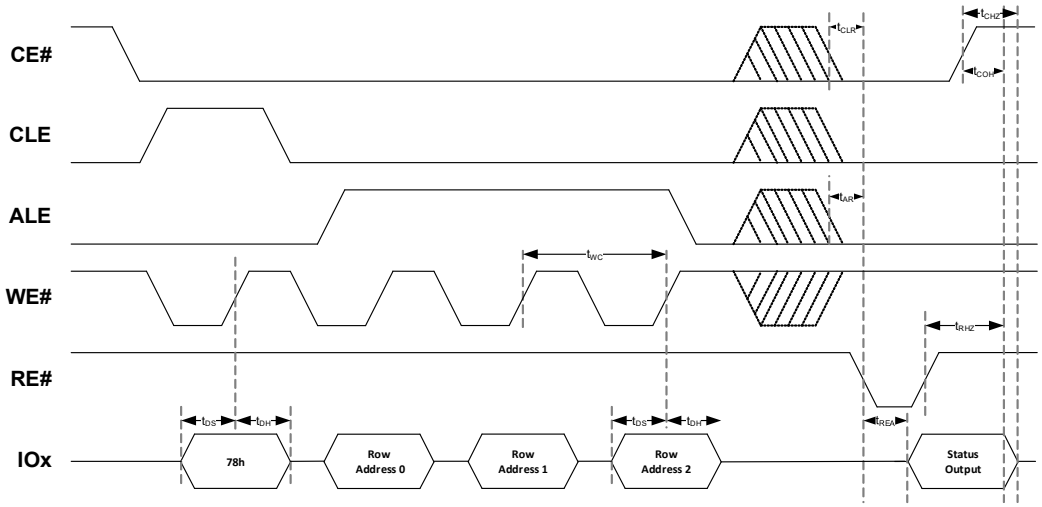


READ STATUS REGISTER MP/MD Operation (78h)

The READ STATUS REGISTER MP/MD (78h) command returns the status value on a specific plane in case of multi-plane operation on the same die or the status value in a specific die in multi-die packages.

Writing 78h to the command register, followed by three row address cycles containing the page, block, and device addresses, puts the selected device into read status mode. The selected device stays in this mode until another valid command is issued. Devices that are not addressed are deselected to avoid bus contention.

Figure 29: Read Status Register MP/MD Operation



Device Initialization

When powering up, the following procedure is required to initialize the device correctly:

- Ramp V_{CC}.
- Drive WP# Low during power-up until V_{CC} is stable
- RESET operation is required after V_{CC} ramps up and must be the first command issued. The host must wait 100µs after V_{CC} reaches V_{CC} (minimum) before issuing RESET.
- The device is now initialized and ready for normal operation (after RESET busy time t_{RST} has elapsed - this can be monitored by polling R/B# or issuing the READ STATUS (70h) command).

Figure 30: Power-On Behavior

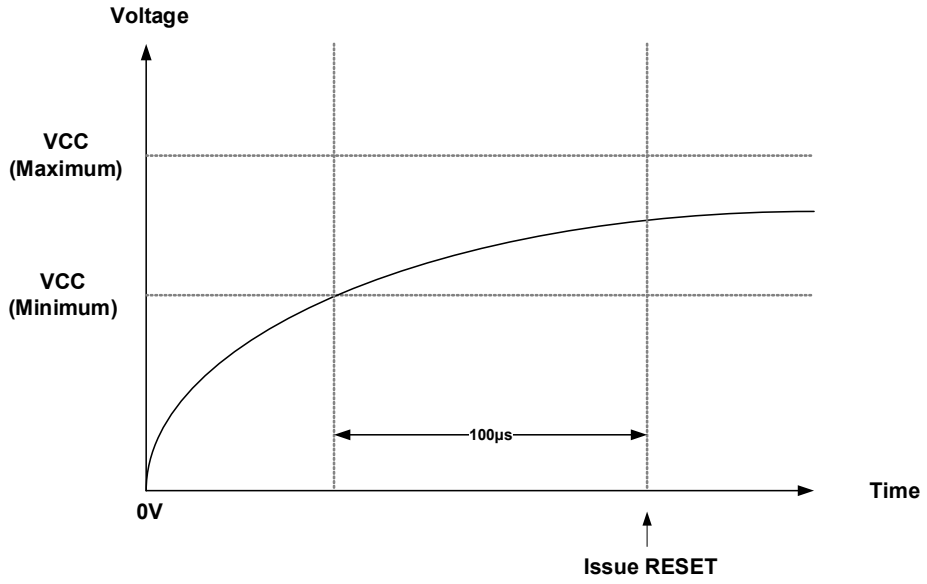
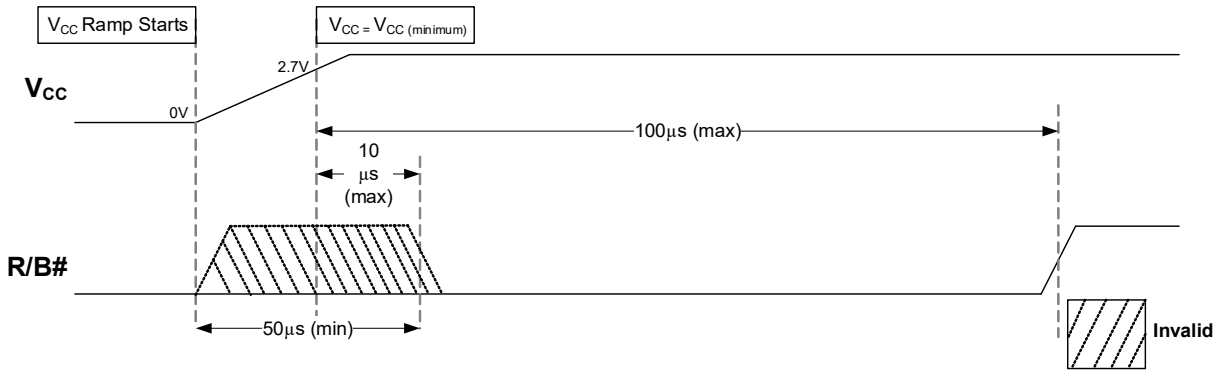


Figure 31: Power-On Behavior (Continued)



Notes:

1. During initialization, the device consumes a maximum current of I_{CC1}.
2. Once Vcc drops below 2.5V, it is recommended to drive down Vcc to below 0.5V and stay low for at least 1ms before Vcc is powered up. Floating Vcc during power-down is prohibited.

Electrical Specifications

Table 21: Absolute Maximum Ratings

Voltage on any pin with respect to V_{SS}			
Parameter / Condition	**Minimum**	**Maximum**	**Units**
Voltage Input	-0.6	4.6	V
V_{CC} Supply Voltage	-0.6	4.6	V
Storage Temperature	-65.0	150.0	°C
Short circuit output current, I/Os	-	5.0	mA

Table 22: Recommended Operating Conditions

Parameter / Condition		**Minimum**	**Maximum**	**Units**
Operating Temperature	Commercial	0.0	70.0	°C
	Industrial	-40.0	85.0	°C
V_{CC} Supply Voltage	3.3V	2.7	3.6	V
V_{SS} Supply Voltage		0.0	0.0	V

Table 23: Pin Capacitance

Parameter	**Test Conditions**	**Symbol**	**Maximum**	**Units**
Input Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V	C_{IN}	10.0	pF
Input/Output Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 0V	C_{INOUT}	10.0	pF

Table 24: DC Characteristics

Parameter	**Symbol**	**Test Conditions**	**3.0V Device (2.7V-3.6V)**			
			Minimum	**Typical**	**Maximum**	**Units**
Read Current (Seq)	I_{CC1}	t_{RC} = 50ns, CE#=V_{IL}, I_{OUT}=0mA	-	25.0	35.0	mA
Program Current	I_{CC2}		-	25.0	35.0	mA
Erase Current	I_{CC3}		-	15.0	30.0	mA
Standby Current (CMOS)	I_{SB}	CE#=V_{CC}-0.2, WP#=0/V_{CC}	-	-	100.0	µA
Power-On-Reset Current	I_{CC7}		-	-	50.0	mA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC} (max)	-	-	±10.0	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC} (max)	-	-	±10.0	µA
Input High Voltage	V_{IH}		0.8xV_{CC}	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}		-0.3	-	0.2xV_{CC}	V
Output High Voltage Level	V_{OH}	I_{OH} = -400µA	2.4	-	-	V
Output Low Voltage Level	V_{OL}	I_{OL} = 2.1mA	-	-	0.4	V
Output Low Current (R/B#)	I_{OL} (R/B#)	V_{OL}=0.4V	8.0	10.0	-	mA

Table 25: Program / Erase Characteristics

Parameter	Symbol	3.0V Device (2.7V-3.6V)			
		Minimum	Typical	Maximum	Units
Program Page Time (Array)	t_{PROG}	-	350.0	600.0	µs
Program Page Time (OTP, Non-Volatile Protection, Firmware Region)		-	550.0	800.0	µs
Block Erase Time	t_{BERS}	-	4.0	10.0	ms
Single Plane Read Time (Array)	t_R	-	45.0	250.0	µs
Single Plane Read Time (Firmware Region)		-	45.0	300.0	µs
Multiple Plane Read Time (Array)		-	55.0	450.0	µs
Multiple Plane Read Time (Firmware Region)		-	60.0	550.0	µs
Read Cycle Time	t_{RC}	-	20	-	ns
Number of Partial-Page Programs	NOP	-	-	4.0	cycles

Table 26: AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to V_{CC}
Input rise and fall times	5ns
Input and output measurement timing levels	$V_{CC}/2$
Output Load	CL = 30pF

Table 27: AC Timing Characteristics

Parameter	Symbol	3.0V Device (2.7V-3.6V)		
		Minimum	Maximum	Units
CLE Setup time	t_{CLS}	10.0	-	ns
CLE Hold time	t_{CLH}	5.0	-	ns
CE# Setup time	t_{CS}	15.0	-	ns
CE# Hold time	t_{CH}	5.0	-	ns
WE# Pulse width	t_{WP}	10.0	-	ns
ALE Setup time	t_{ALS}	10.0	-	ns
ALE Hold time	t_{ALH}	5.0	-	ns
Data Setup time	t_{DS}	7.0	-	ns
Data Hold time	t_{DH}	5.0	-	ns
Write Cycle time	t_{WC}	20.0	-	ns

Parameter	Symbol	3.0V Device (2.7V-3.6V)		
		Minimum	Maximum	Units
WE# High Hold time	t_{WH}	7.0	-	ns
Address to Data Loading time	t_{ADL}	70.0	-	ns
ALE to RE# Delay	t_{AR}	10.0	-	ns
CLE to RE# Delay	t_{CLR}	10.0	-	ns
Ready to RE# Low	t_{RR}	20.0	-	ns
RE# Pulse Width	t_{RP}	10.0	-	ns
WE# High to Busy	t_{WB}	-	100.0	ns
Read Cycle Time	t_{RC}	20.0	-	ns
RE# Access Time	t_{REA}	-	16.0	ns
CE# Access Time	t_{CEA}	-	16.0	ns
RE# High to Output Hi-Z	t_{RHZ}	-	100.0	ns
CE# High to Output Hi-Z	t_{CHZ}	-	30.0	ns
CE# High to ALE or CLE Don't care	t_{CSD}	10.0	-	ns
RE# High to Output Hold	t_{RHOH}	15.0	-	ns
RE# Low to Output Hold	t_{RLOH}	5.0	-	ns
CE# High to Output Hold	t_{COH}	15.0	-	ns
RE# High Hold Time	t_{REH}	7.0	-	ns
Output Hi-Z to RE# Low	t_{IR}	0.0	-	ns
RE# High to WE# Low	t_{RHW}	100.0	-	ns
WE# High to RE# Low	t_{WHR}	60.0	-	ns
Device Resetting Time (Read/Program/Erase)	t_{RST}	-	5.0/10.0/500.0	µs
Write protection time	t_{WW}	100.0	-	ns

Error Management

NAND Flash devices have bad blocks that are invalid when shipped from the factory. However, each NAND Flash device specifies a minimum number of valid blocks (NVB) of the total available blocks during the endurance life of the product. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Even though NAND Flash devices contain bad blocks, they can be used reliably in systems provided the systems have bad block management and error-correction algorithms.

Axia's NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by providing a bad block marker (00h to FEh) into the 1st byte in the spare area of the 1st or 2nd page (if the 1st page is Bad). This method is compliant with ONFI Factory Defect Mapping requirements.

System software should check the first spare area location on the first page of each block before performing any PROGRAM or ERASE operations on the NAND Flash device, thus creating a bad block table for the whole device.

The following recommendations should be followed to achieve maximum reliability performance:

- Always check the program/erase status bits (PS1, PES2) after a PROGRAM or ERASE operation
- Use bad block management and wear-leveling algorithms
- The first block (physical block address 00h) is guaranteed to be valid with ECC when shipped from the factory (1K program/erase cycles)

Table 28: Error Management Details

Description	Requirement
Minimum number of valid blocks (NVM)	4016
Total number of available blocks	4096
First spare area location	x8: byte 2048
Bad block mark	x8: 00h - FEh

Product Use Limitations

Axia reserves the right to make changes to the information in this document, and related hardware, software and system (collectively referred to as "**Products**") without notice. This document supersedes and replaces any and all prior or contemporaneous information or arrangement of any kind relating to the subject matter hereof. This document and any information set forth herein may not be reproduced without the prior written permission from Axia.

Critical Applications. Products are not authorized for use in applications in which failure of the Axia component could result, directly or indirectly in death, personal injury, or severe property or environmental damage ("**Critical Applications**"). Axia assumes no liability for Products if used for Critical Applications. Should customer or distributor purchase, use, or sell any Axia component for Critical Applications, customer and distributor shall indemnify and hold harmless Axia and its subsidiaries, subcontractors, and affiliates and the directors, officers, and employees of each against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, or death arising in any way out of such Critical Application, whether or not Axia or its subsidiaries, subcontractors, or affiliates were negligent in the design, manufacture, or warning of the Products.

Automotive Applications. Products are not authorized for use in automotive applications unless specified by Axia. Axia assumes no liability for Products if used for automotive applications. Distributor and customer shall assume the sole risk and liability for such use and shall indemnify and hold Axia harmless against all claims, costs, damages, and expenses and reasonable attorneys' fees arising out of, directly or indirectly, any claim of product liability, personal injury, death, or property damage resulting directly or indirectly from any use of Products in automotive applications.

Military Applications. Products are not authorized for use in military applications, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons).

Customer Responsibility. Customers are solely responsible for the design and operation of their systems using Products. It is customer's sole responsibility to determine whether Products are suited for their system. Customers are required to incorporate good safety design measures and adequate safeguards to eliminate risks of personal injury, death, or severe property or environmental damages that could result from failure of Products. **AXIA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS AND DAMAGES OR LOSSES OCCURING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**

The information contained herein is presented only as guidance for Product use. Axia assumes no responsibility for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Products. No license to any intellectual property right is granted by this document, whether expressed or implied. You may not perform compositional, structural, functional or other analysis of Products, or undertake deconvolution or reverse engineering with respect to Products.

Limited Warranty

In no event shall Axia and its representatives be liable for any indirect, incidental, punitive, special or consequential damages (including but not limited to loss of use, revenue or profit), whether or not such damages are based on tort, warranty, breach of contract or other legal theory.

In no event shall Axia's aggregate liability for any breach, warranty, indemnity or other obligation or liability arising out of or in connection with the sale of Products or the use of any Products exceed the purchase price of the particular Product(s) or services with respect to which losses or damages are claimed.

Revision History

Revision	Date	Change Summary
REV E	11/26/2018	Initial release
REV F	07/17/2019	Added BGA Removed ECC Disable Option Changed External ECC requirement to 1-bit / 544 bytes of data Corrected Parameter Page value typos for Bytes #48, #51, #52, #54, #55, #58, #254, and #255.