NTS0102-Q100

Dual supply translating transceiver; open-drain; auto direction sensing

Rev. 1.2 — 3 March 2022 Product data sheet

1 General description

The NTS0102-Q100 is a 2-bit, dual supply translating transceiver with auto direction sensing, that enables bidirectional voltage level translation. It features two 2-bit input-output ports (An and Bn), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). $V_{CC(A)}$ can be supplied at any voltage between 1.65 V and 3.6 V and $V_{CC(B)}$ can be supplied at any voltage between 2.3 V and 5.5 V, making the device suitable for translating between any of the voltage nodes (1.8 V, 2.5 V, 3.3 V, and 5.0 V). Pins An and OE are referenced to $V_{CC(A)}$ and pins Bn are referenced to $V_{CC(B)}$. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state. This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2 Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from –40 °C to +85 °C and from –40 °C to +125 °C
- Wide supply voltage range:
  - $V_{CC(A)}$: 1.65 V to 3.6 V and $V_{CC(B)}$: 2.3 V to 5.5 V
- Maximum data rates:
  - Push-pull: 50 Mbit/s
- I_{OFF} circuitry provides partial power-down mode operation
- Inputs accept voltages up to 5.5 V
- ESD protection:
  - MIL-STD-883, method 3015 Class 2 exceeds 2500 V for A port
  - MIL-STD-883, method 3015 Class 3B exceeds 8000 V for B port
  - HBM JESD22-A114E Class 2 exceeds 2500 V for A port
  - HBM JESD22-A114E Class 3B exceeds 8000 V for B port
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Multiple package options

3 Applications

- I^2C/SMBus
- UART
- GPIO

4 Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
NTS0102DP-Q100	S02	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
NTS0102GD-Q100	S02	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 3 × 2 × 0.5 mm	SOT996-2
NTS0102TL-Q100	tS2	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 3 x 2 x 0.5 mm	SOT1052-2

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method [1]	Minimum order quantity	Temperature
NTS0102DP-Q100	NTS0102DP-Q100H	TSSOP8	Reel 7" Q3 NDP	3000	–40 °C to +125 °C
NTS0102GD-Q100 [2]	NTS0102GD-Q100H	XSON8	Reel 7" Q3 NDP	3000	–40 °C to +125 °C
NTS0102TL-Q100	NTS0102TL-Q100H	XSON8	Reel 7" Q3 NDP	3000	–40 °C to +125 °C

[1] Standard packing quantities and other packaging data are available at www.nxp.com/packages/

[2] Discontinuation Notice 202111012DN - drop in replacement is NTS0102TL-Q100H.
The TL package has a center pad vs no center pad for the GD package. The TL package pad is not electrically connected to the silicon and is not required to connect to the PCB so it can drop onto the GD package PCB layout. If the existing GD package has a trace underneath the risk is low since the TL package center pad is not connected to the silicon. If there are multiple traces there could be EMI and cross talk. In both cases the customer needs to evaluate risk.

5 Functional diagram

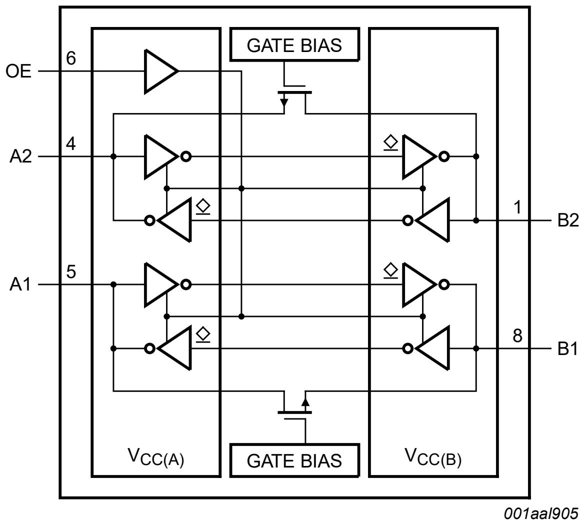


Figure 1. Logic symbol

6 Pinning information

6.1 Pinning

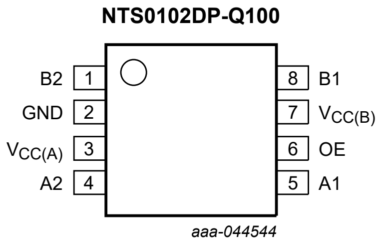


Figure 2. Pin configuration SOT505-2 (TSSOP8)

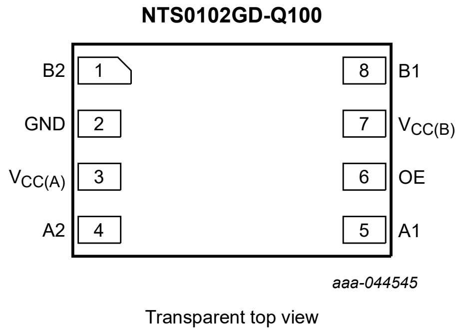


Figure 3. Pin configuration SOT996-2 (XSON8)

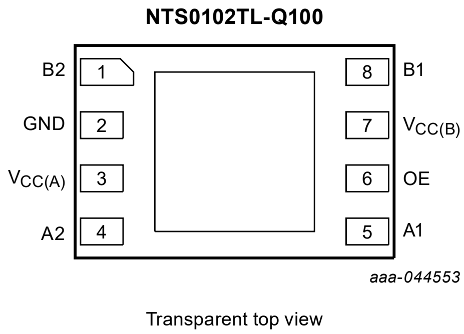


Figure 4. Pin configuration SOT1052-2

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
B2, B1	1, 8	data input or output (referenced to $V_{CC(B)}$)
GND	2	ground (0 V)
$V_{CC(A)}$	3	supply voltage A
A2, A1	4, 5	data input or output (referenced to $V_{CC(A)}$)
OE	6	output enable input (active HIGH; referenced to $V_{CC(A)}$)
$V_{CC(B)}$	7	supply voltage B
n.c.	—	not connected

7 Functional description

Table 4. Function table[1]

Supply voltage		Input	Input/output	
$V_{CC(A)}$	$V_{CC(B)}$	OE	An	Bn
1.65 V to $V_{CC(B)}$	2.3 V to 5.5 V	L	Z	Z

Table 4. Function table[1] *...continued*

Supply voltage		Input	Input/output	
$V_{CC(A)}$	$V_{CC(B)}$	OE	An	Bn
1.65 V to $V_{CC(B)}$	2.3 V to 5.5 V	H	input or output	output or input
GND[2]	GND[2]	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.
[2] When either $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into power-down mode.

8 Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{CC(A)}$	supply voltage A			–0.5	+6.5	V
$V_{CC(B)}$	supply voltage B			–0.5	+6.5	V
V_I	input voltage	A port and OE input	[1] [2]	–0.5	+6.5	V
		B port	[1] [2]	–0.5	+6.5	V
V_O	output voltage	Active mode	[1] [2]			
		A or B port		–0.5	V_{CCO} + 0.5	V
		Power-down or 3-state mode	[1]			
		A port		–0.5	+4.6	V
		B port		–0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–50	—	mA
I_{OK}	output clamping current	$V_O < 0$ V		–50	—	mA
I_O	output current	V_O = 0 V to V_{CCO}	[2]	—	± 50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$		—	100	mA
I_{GND}	ground current			–100	—	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[3]	—	250	mW

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] V_{CCO} is the supply voltage associated with the output.
[3] For TSSOP8 package: above 55 °C the value of P_{tot} derates linearly with 2.5 mW/K.
For XSON8 package: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9 Recommended operating conditions

Table 6. Recommended operating conditions[1][2]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		1.65	3.6	V
$V_{CC(B)}$	supply voltage B		2.3	5.5	V
T_{amb}	ambient temperature		–40	+125	°C
Δt/ΔV	input transition rise and fall rate	A or B port; push-pull driving			

Table 6. Recommended operating conditions[1][2] *...continued*

Symbol	Parameter	Conditions	Min	Max	Unit
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	—	10	ns/V
		OE input			
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	—	10	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.

[2] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

10 Static characteristics

Table 7. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_I	input leakage current	OE input; V_I = 0 V to 3.6 V; $V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	—	—	± 1	µA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V [1]	—	—	± 1	µA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0 V to 5.5 V	—	—	± 1	µA
		B port; V_I or V_O = 0 V to 5.5 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 3.6 V	—	—	± 1	µA
C_I	input capacitance	OE input; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V	—	1	—	pF
$C_{I/O}$	input/output capacitance	A port	—	5	—	pF
		B port	—	8.5	—	pF
		A or B port; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V	—	11	—	pF

[1] V_{CCO} is the supply voltage associated with the output.

Table 8. Typical supply current

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

$V_{CC(A)}$	$V_{CC(B)}$						Unit
	2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
1.8 V	0.1	0.5	0.1	1.5	0.1	4.6	µA
2.5 V	0.1	0.1	0.1	0.8	0.1	3.8	µA
3.3 V	—	—	0.1	0.1	0.1	2.8	µA

Table 9. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		–40 ° C to +85 ° C		–40 ° C to +125 ° C		Unit
				Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	A port						
		$V_{CC(A)}$ = 1.65 V to 1.95 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	[1]	V_{CCI} – 0.2	—	V_{CCI} – 0.2	—	V
		$V_{CC(A)}$ = 2.3 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	[1]	V_{CCI} – 0.4	—	V_{CCI} – 0.4	—	V
		B port						
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	[1]	V_{CCI} – 0.4	—	V_{CCI} – 0.4	—	V
		OE input						
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V		$0.65V_{CC(A)}$	—	$0.65V_{CC(A)}$	—	V
V_{IL}	LOW-level input voltage	A or B port						
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V		—	0.15	—	0.15	V
		OE input						
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V		—	$0.35V_{CC(A)}$	—	$0.35V_{CC(A)}$	V
V_{OH}	HIGH-level output voltage	I_O = –20 μA						
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	[2]	$0.67V_{CCO}$	—	$0.67V_{CCO}$	—	V
V_{OL}	LOW-level output voltage	A or B port; I_O = 1 mA	[2]					
		V_I ≤ 0.15 V; $V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V		—	0.4	—	0.4	V
I_I	input leakage current	OE input; V_I = 0 V to 3.6 V; $V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V		—	± 2	—	± 12	μA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	[2]	—	± 2	—	± 12	μA
I_{OFF}	power-off leakage current	A port; V_I or V_O = 0 V to 3.6 V; $V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 0 V to 5.5 V		—	± 2	—	± 12	μA
		B port; V_I or V_O = 0 V to 3.6 V; $V_{CC(B)}$ = 0 V; $V_{CC(A)}$ = 0 V to 3.6 V		—	± 2	—	± 12	μA

Table 9. Static characteristics...*continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 ° C to +85 ° C		–40 ° C to +125 ° C		Unit
			Min	Max	Min	Max	
I_{CC}	supply current	V_I = 0 V or V_{CCI}; I_O = 0 A [1]					
		$I_{CC(A)}$					
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	—	2.4	—	15	μA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	—	2.2	—	15	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V	—	–1	—	–8	μA
		$I_{CC(B)}$					
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	—	12	—	30	μA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V	—	–1	—	–5	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V	—	1	—	6	μA
		$I_{CC(A)}$ + $I_{CC(B)}$					
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	—	14.4	—	30	μA

[1] V_{CCI} is the supply voltage associated with the input.
[2] V_{CCO} is the supply voltage associated with the output.

11 Dynamic characteristics

Table 10. Dynamic characteristics for temperature range -40 °C to +85 °C[1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7; for wave forms see Figure 5 and Figure 6.

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.8 V ± 0.15 V									
t_{PHL}	HIGH to LOW propagation delay	A to B	—	4.6	—	4.7	—	5.8	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	—	6.8	—	6.8	—	7.0	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	—	4.4	—	4.5	—	4.7	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	—	5.3	—	4.5	—	0.5	ns
t_{en}	enable time	OE to A; B	—	200	—	200	—	200	ns
t_{dis}	disable time	OE to A; no external load [2]	—	25	—	25	—	25	ns
		OE to B; no external load [2]	—	25	—	25	—	25	ns
		OE to A	—	230	—	230	—	230	ns
		OE to B	—	200	—	200	—	200	ns

Table 10. Dynamic characteristics for temperature range -40 °C to +85 °C[1] *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7; for wave forms see Figure 5 and Figure 6.

Symbol	Parameter	Conditions		$V_{CC(B)}$					Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
t_{TLH}	LOW to HIGH output transition time	A port		3.2	9.5	2.3	9.3	1.8	7.6	ns
		B port		3.3	10.8	2.7	9.1	2.7	7.6	ns
t_{THL}	HIGH to LOW output transition time	A port		2.0	5.9	1.9	6.0	1.7	13.3	ns
		B port		2.9	7.6	2.8	7.5	2.8	10.0	ns
$t_{sk(o)}$	output skew time	between channels	[3]	—	0.7	—	0.7	—	0.7	ns
t_W	pulse width	data inputs		20	—	20	—	20	—	ns
f_{data}	data rate			—	50	—	50	—	50	Mbit/s
$V_{CC(A)}$ = 2.5 V ± 0.2 V									
t_{PHL}	HIGH to LOW propagation delay	A to B		—	3.2	—	3.3	—	3.4	ns
t_{PLH}	LOW to HIGH propagation delay	A to B		—	3.5	—	4.1	—	4.4	ns
t_{PHL}	HIGH to LOW propagation delay	B to A		—	3.0	—	3.6	—	4.3	ns
t_{PLH}	LOW to HIGH propagation delay	B to A		—	2.5	—	1.6	—	0.7	ns
t_{en}	enable time	OE to A; B		—	200	—	200	—	200	ns
t_{dis}	disable time	OE to A; no external load	[2]	—	20	—	20	—	20	ns
		OE to B; no external load	[2]	—	20	—	20	—	20	ns
		OE to A		—	200	—	200	—	200	ns
		OE to B		—	200	—	200	—	200	ns
t_{TLH}	LOW to HIGH output transition time	A port		2.8	7.4	2.6	6.6	1.8	6.2	ns
		B port		3.2	8.3	2.9	7.9	2.4	6.8	ns
t_{THL}	HIGH to LOW output transition time	A port		1.9	5.7	1.9	5.5	1.8	5.3	ns
		B port		2.2	7.8	2.4	6.7	2.6	6.6	ns
$t_{sk(o)}$	output skew time	between channels	[3]	—	0.7	—	0.7	—	0.7	ns
t_W	pulse width	data inputs		20	—	20	—	20	—	ns
f_{data}	data rate			—	50	—	50	—	50	Mbit/s
$V_{CC(A)}$ = 3.3 V ± 0.3 V									
t_{PHL}	HIGH to LOW propagation delay	A to B		—	—	—	2.4	—	3.1	ns
t_{PLH}	LOW to HIGH propagation delay	A to B		—	—	—	4.2	—	4.4	ns
t_{PHL}	HIGH to LOW propagation delay	B to A		—	—	—	2.5	—	3.3	ns

Table 10. Dynamic characteristics for temperature range -40 °C to +85 °C[1] *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7; for wave forms see Figure 5 and Figure 6.

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	B to A	—	—	—	2.5	—	2.6	ns
t_{en}	enable time	OE to A; B	—	—	—	200	—	200	ns
t_{dis}	disable time	OE to A; no external load [2]	—	—	—	15	—	15	ns
		OE to B; no external load [2]	—	—	—	15	—	15	ns
		OE to A	—	—	—	260	—	260	ns
		OE to B	—	—	—	200	—	200	ns
t_{TLH}	LOW to HIGH output transition time	A port	—	—	2.3	5.6	1.9	5.9	ns
		B port	—	—	2.5	6.4	2.1	7.4	ns
t_{THL}	HIGH to LOW output transition time	A port	—	—	2.0	5.4	1.9	5.0	ns
		B port	—	—	2.3	7.4	2.4	7.6	ns
$t_{sk(o)}$	output skew time	between channels [3]	—	—	—	0.7	—	0.7	ns
t_W	pulse width	data inputs	—	—	20	—	20	—	ns
f_{data}	data rate		—	—	—	50	—	50	Mbit/s

[1] t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] Delay between OE going LOW and when the outputs are actually disabled.

[3] Skew between any two outputs of the same package switching in the same direction.

Table 11. Dynamic characteristics for temperature range -40 °C to +125 °C[1]

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7; for wave forms see Figure 5 and Figure 6.

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.8 V ± 0.15 V									
t_{PHL}	HIGH to LOW propagation delay	A to B	—	5.8	—	5.9	—	7.3	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	—	8.5	—	8.5	—	8.8	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	—	5.5	—	5.7	—	5.9	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	—	6.7	—	5.7	—	0.7	ns
t_{en}	enable time	OE to A; B	—	200	—	200	—	200	ns

Table 11. Dynamic characteristics for temperature range -40 °C to +125 °C[1] *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7; for wave forms see Figure 5 and Figure 6.

Symbol	Parameter	Conditions	$V_{CC(B)}$						Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
t_{dis}	disable time	OE to A; no external load [2]	—	30	—	30	—	30	ns
		OE to B; no external load [2]	—	30	—	30	—	30	ns
		OE to A	—	250	—	250	—	250	ns
		OE to B	—	220	—	220	—	220	ns
t_{TLH}	LOW to HIGH output transition time	A port	3.2	11.9	2.3	11.7	1.8	9.5	ns
		B port	3.3	13.5	2.7	11.4	2.7	9.5	ns
t_{THL}	HIGH to LOW output transition time	A port	2.0	7.4	1.9	7.5	1.7	16.7	ns
		B port	2.9	9.5	2.8	9.4	2.8	12.5	ns
$t_{sk(o)}$	output skew time	between channels [3]	—	0.8	—	0.8	—	0.8	ns
t_W	pulse width	data inputs	20	—	20	—	20	—	ns
f_{data}	data rate		—	50	—	50	—	50	Mbit/s
$V_{CC(A)}$ = 2.5 V ± 0.2 V									
t_{PHL}	HIGH to LOW propagation delay	A to B	—	4.0	—	4.2	—	4.3	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	—	4.4	—	5.2	—	5.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	—	3.8	—	4.5	—	5.4	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	—	3.2	—	2.0	—	0.9	ns
t_{en}	enable time	OE to A; B	—	200	—	200	—	200	ns
t_{dis}	disable time	OE to A; no external load [2]	—	25	—	25	—	25	ns
		OE to B; no external load [2]	—	25	—	25	—	25	ns
		OE to A	—	220	—	220	—	220	ns
		OE to B	—	220	—	220	—	220	ns
t_{TLH}	LOW to HIGH output transition time	A port	2.8	9.3	2.6	8.3	1.8	7.8	ns
		B port	3.2	10.4	2.9	9.7	2.4	8.3	ns
t_{THL}	HIGH to LOW output transition time	A port	1.9	7.2	1.9	6.9	1.8	6.7	ns
		B port	2.2	9.8	2.4	8.4	2.6	8.3	ns
$t_{sk(o)}$	output skew time	between channels [3]	—	0.8	—	0.8	—	0.8	ns
t_W	pulse width	data inputs	20	—	20	—	20	—	ns
f_{data}	data rate		—	50	—	50	—	50	Mbit/s

Table 11. Dynamic characteristics for temperature range -40 °C to +125 °C[1] *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 7; for wave forms see Figure 5 and Figure 6.

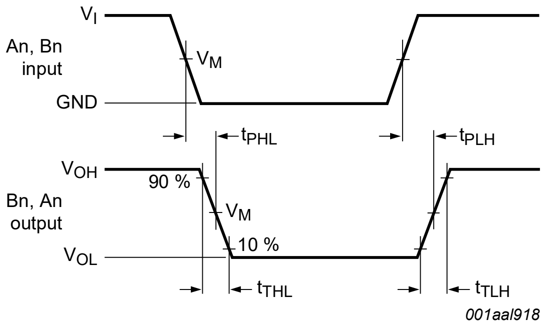
Symbol	Parameter	Conditions		$V_{CC(B)}$					Unit
			2.5 V ± 0.2 V		3.3 V ± 0.3 V		5.0 V ± 0.5 V		
			Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 3.3 V ± 0.3 V									
t_{PHL}	HIGH to LOW propagation delay	A to B	—	—	—	3.0	—	3.9	ns
t_{PLH}	LOW to HIGH propagation delay	A to B	—	—	—	5.3	—	5.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A	—	—	—	3.2	—	4.2	ns
t_{PLH}	LOW to HIGH propagation delay	B to A	—	—	—	3.2	—	3.3	ns
t_{en}	enable time	OE to A; B	—	—	—	200	—	200	ns
t_{dis}	disable time	OE to A; no external load [2]	—	—	—	20	—	20	ns
		OE to B; no external load [2]	—	—	—	20	—	20	ns
		OE to A	—	—	—	280	—	280	ns
		OE to B	—	—	—	220	—	220	ns
t_{TLH}	LOW to HIGH output transition time	A port	—	—	2.3	7.0	1.9	7.4	ns
		B port	—	—	2.5	8.0	2.1	9.3	ns
t_{THL}	HIGH to LOW output transition time	A port	—	—	2.0	6.8	1.9	6.3	ns
		B port	—	—	2.3	9.3	2.4	9.5	ns
$t_{sk(o)}$	output skew time	between channels [3]	—	—	—	0.8	—	0.8	ns
t_W	pulse width	data inputs	—	—	20	—	20	—	ns
f_{data}	data rate		—	—	—	50	—	50	Mbit/s

[1] t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] Delay between OE going LOW and when the outputs are actually disabled.

[3] Skew between any two outputs of the same package switching in the same direction.

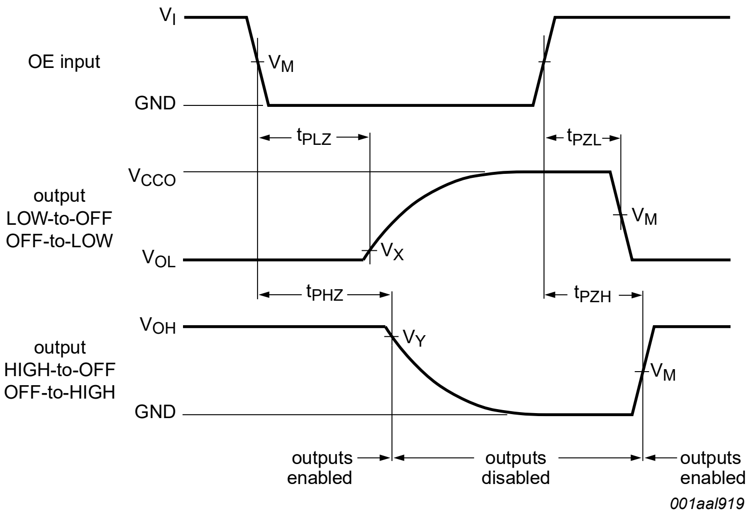
12 Waveforms



Measurement points are given in Table 12.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 5. The data input (An, Bn) to data output (Bn, An) propagation delay times



Measurement points are given in Table 12.

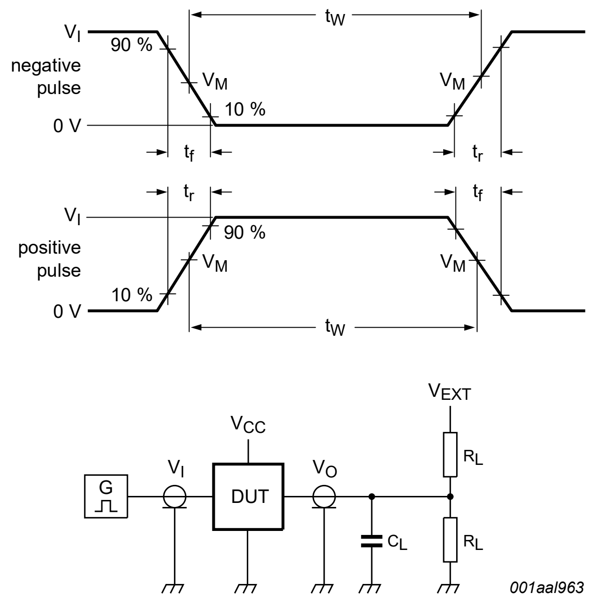
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 6. Enable and disable times

Table 12. Measurement points[1][2]

Supply voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
1.8 V ± 0.15 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} – 0.15 V
2.5 V ± 0.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} – 0.15 V
3.3 V ± 0.3 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} – 0.3 V
5.0 V ± 0.5 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} –0.3 V

[1] V_{CCI} is the supply voltage associated with the input.
[2] V_{CCO} is the supply voltage associated with the output.



Test data is given in Table 13.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_O = 50 Ω; dV/dt ≥ 1.0 V/ ns.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Figure 7. Test circuit for measuring switching times

Table 13. Test data

Supply voltage		Input		Load		V_{EXT}		
$V_{CC(A)}$	$V_{CC(B)}$	V_I[1]	Δt/ΔV	C_L	R_L[2]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}[3]
1.65 V to 3.6 V	2.3 V to 5.5 V	V_{CCI}	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the input.

[2] For measuring data rate, pulse width, propagation delay, and output rise and fall measurements, R_L = 1 MΩ; for measuring enable and disable times, R_L = 50 KΩ.

[3] V_{CCO} is the supply voltage associated with the output.

13 Application information

13.1 Applications

Voltage level-translation applications. The NTS0102-Q100 can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is primarily targeted at I^2C or 1-wire which use open-drain drivers. It may also be used in applications where push-pull drivers are connected to the ports although the NTB0102-Q100 may be more suitable.

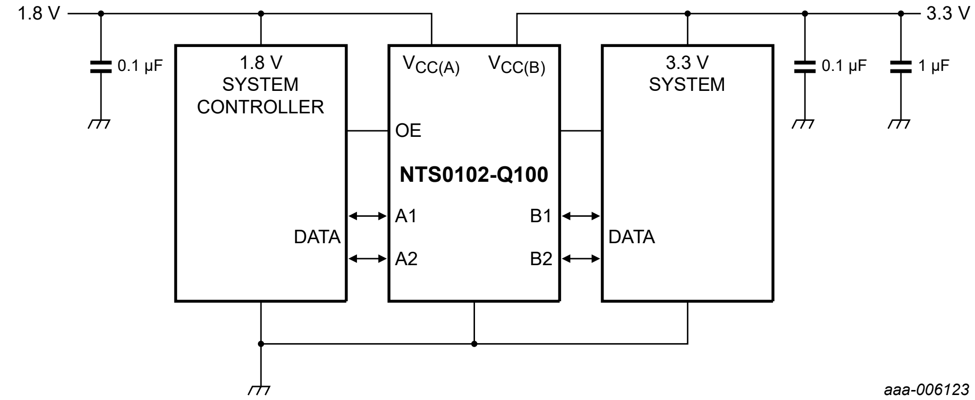


Figure 8. Typical operating circuit

13.2 Architecture

The architecture of the NTS0102-Q100 is shown in Figure 9. The device does not require an extra input signal to control the direction of data flow from A to B or B to A.

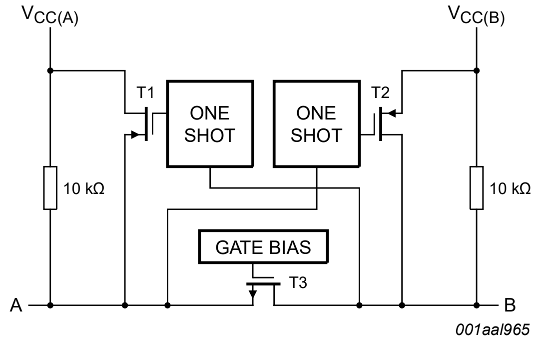


Figure 9. Architecture of NTS0102-Q100 I/O cell (one channel)

The NTS0102-Q100 is a "switch" type voltage translator, it employs two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.
2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the V_{CC} level of the low-voltage side. During a LOW-to-HIGH transition, the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2). This action bypasses the 10 kΩ pullup resistors and increases current drive capability. The one-shot is activated once the input transition reaches approximately $V_{CCI}/2$. It is de-activated approximately 50 ns after the output reaches $V_{CCO}/2$. During the acceleration time, the driver output resistance is between approximately 50 Ω and 70 Ω. To avoid signal contention and minimize dynamic I_{CC}, before applying a signal in the opposite direction, wait for the one-shot circuit to turn-off. Pullup resistors are included in the device for DC current sourcing capability.

13.3 Input driver requirements

As the NTS0102-Q100 is a switch type translator, properties of the input driver directly affect the output signal. The external open-drain or push-pull driver applied to an I/O, determines the static current sinking capability of the system. The max data rate, HIGH-to-LOW output transition time (t_{THL}), and propagation delay (t_{PHL}) are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the data sheet assume a driver with output impedance below 50 Ω is used.

13.4 Output load considerations

The maximum lumped capacitive load that can be driven is dependent upon the one-shot pulse duration. In cases with very heavy capacitive loading, there is a risk that the output does not reach the positive rail within the one-shot pulse duration.

To avoid excessive capacitive loading, and to ensure correct triggering of the one-shot, use short trace lengths and low capacitance connectors on NTS0102-Q100 PCB layouts. To ensure low impedance termination and avoid output signal oscillations and one-shot re triggering, limit the length of the PCB trace. The PCB trace should be such that the round-trip delay of any reflection is within the one-shot pulse duration (approximately 50 ms).

13.5 Power-up

During operation $V_{CC(A)}$ must never be higher than $V_{CC(B)}$, however during power-up $V_{CC(A)} \geq V_{CC(B)}$ does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The NTS0102-Q100 includes circuitry that disables all output ports when either $V_{CC(A)}$ or $V_{CC(B)}$ is switched off.

13.6 Enable and disable

An output enable input (OE) is used to disable the device. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time to allow for one one-shot circuit to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor. The current-sourcing capability of the driver determines the minimum value of the resistor.

13.7 Pull-up or pull-down resistors on I/Os lines

Each A port I/O has an internal 10 kΩ pullup resistor to $V_{CC(A)}$. Each B port I/O has an internal 10 kΩ pullup resistor to $V_{CC(B)}$. If a smaller value of pullup resistor is required, an external resistor must be added parallel to the internal 10 kΩ. The reduction in the value of the pullup resistor affects the V_{OL} level. When OE goes LOW, the internal pull-ups of the NTS0102-Q100 are disabled.

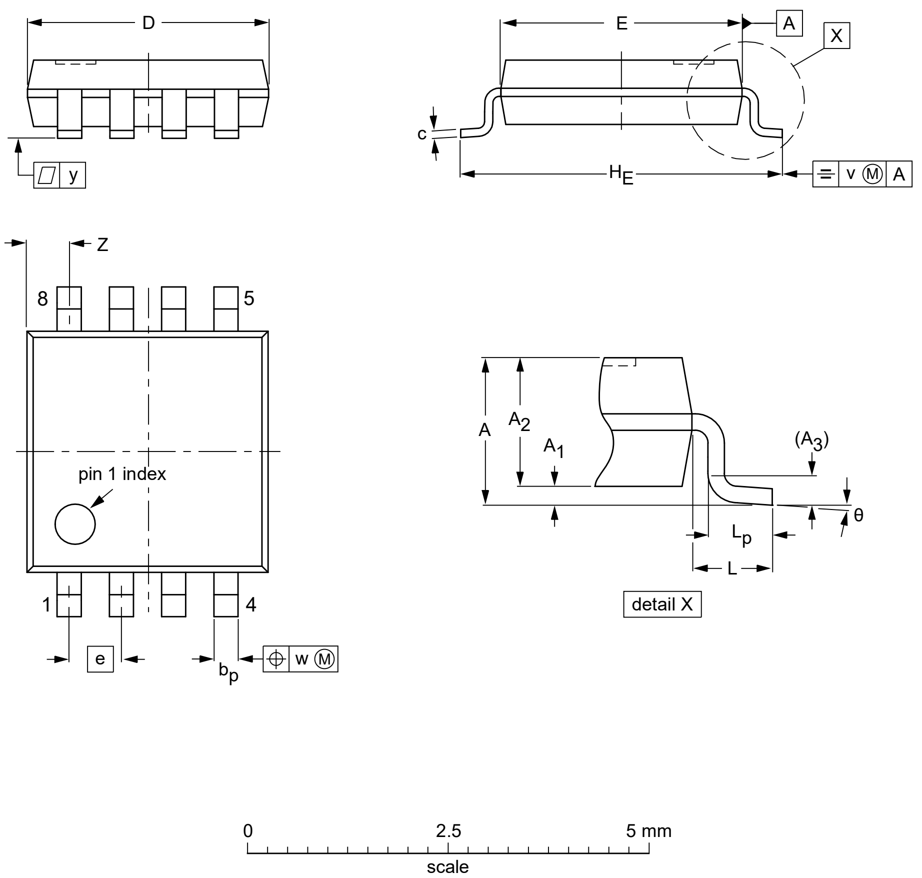
13.8 GD package vs TL package

Due to differences in package construction the TL package has a center pad vs no center pad for the GD package. The following section provides guidance in replacement vs new applications.

- **No trace under GD package**
  1. Replacement of GD package: The pad is not electrically connected to the silicon (no wire bond and epoxy is not conductive) and can be left floating. It is not required to be connected to the PCB. Simply place the TL package on the same PCB traces as the existing GD package.
  2. New use of the TL package: Place PCB trace for soldering of the center pad based on PCB layout recommendations for better mechanical connection and thermal conductivity. The PCB center pad can be connect to GND or left floating.
- **Trace under the GD package**
  1. Replacement of GD package: It is not best practice to have center pad over the trace but since the TL package center pad is not connected to the silicon the risk is low. If there are multiple traces there could be EMI and cross talk. In both cases the customer needs to evaluate risk.
  2. New use of the TL package: Do not route traces under the package

14 Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	v	w	y	Z(1)	θ
mm	1.1	0.15 0.00	0.95 0.75	0.25	0.38 0.22	0.18 0.08	3.1 2.9	3.1 2.9	0.65	4.1 3.9	0.5	0.47 0.33	0.2	0.13	0.1	0.70 0.35	8° 0°

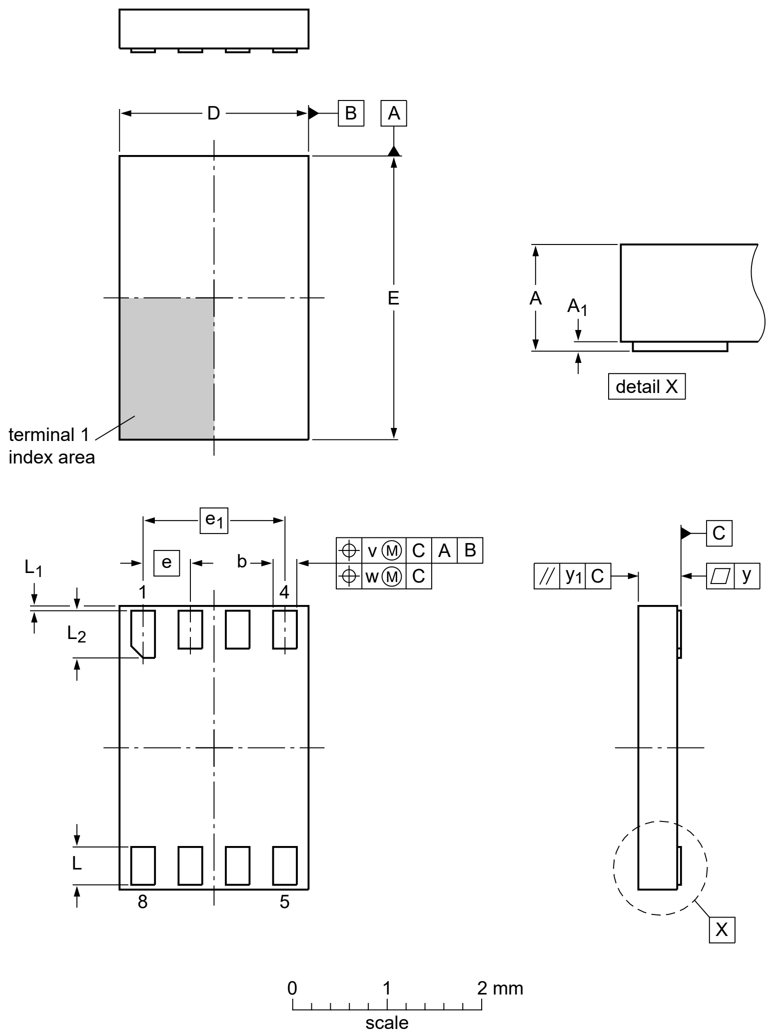
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT505-2		- - -				02-01-16

Figure 10. Package outline SOT505-2 (TSSOP8)

XSON8: plastic extremely thin small outline package; no leads;
8 terminals; body 3 x 2 x 0.5 mm **SOT996-2**



Dimensions (mm are the original dimensions)

Unit(1)		A	A_1	b	D	E	e	e_1	L	L_1	L_2	v	w	y	y_1
mm	max		0.05	0.35	2.1	3.1			0.5	0.15	0.6				
	nom	0.5					0.5	1.5				0.1	0.05	0.05	0.1
	min		0.00	0.15	1.9	2.9			0.3	0.05	0.4				

sot996-2_po

Outline version	References: IEC	References: JEDEC	References: JEITA		European projection	Issue date
SOT996-2						~~07-12-21~~ 12-11-20

Figure 11. Package outline SOT996-2 (XSON8)

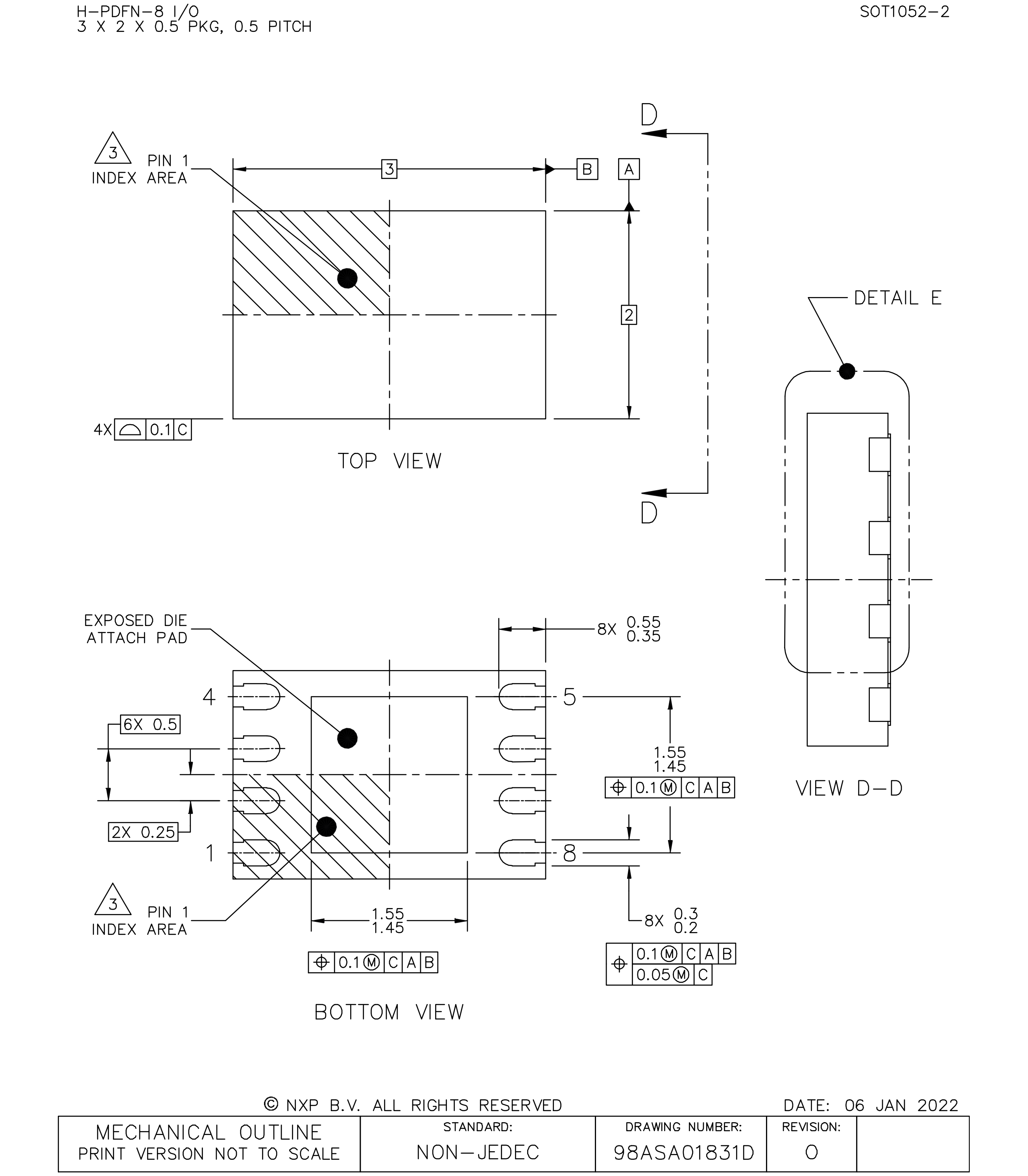
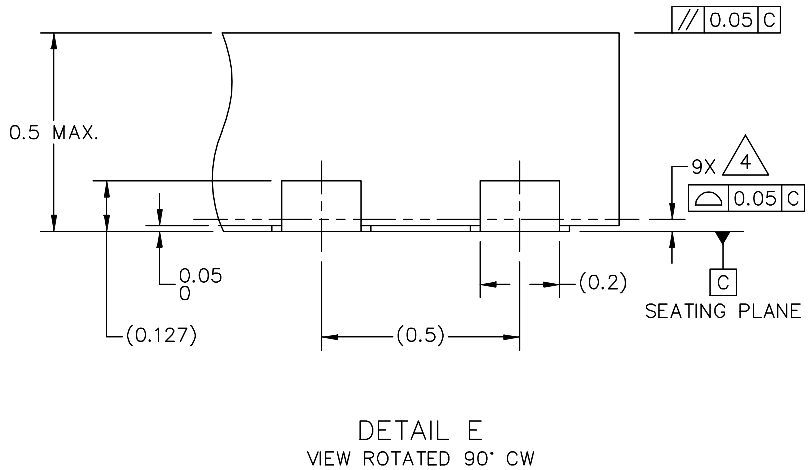


Figure 12. Package outline SOT1052-2 (XSON8)

H-PDFN-8 I/O
3 X 2 X 0.5 PKG, 0.5 PITCH

SOT1052-2



DATE: 06 JAN 2022

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01831D	REVISION: O	

Figure 13. Package outline SOT1052-2 (XSON8)

15 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

15.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

15.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

15.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

15.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 14) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 14 and Table 15

Table 14. SnPb eutectic process (from J-STD-020D)

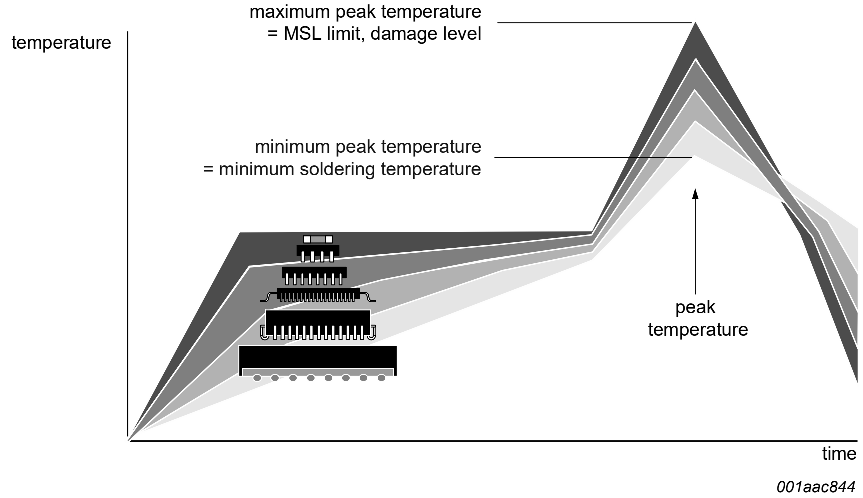
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 15. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 14.



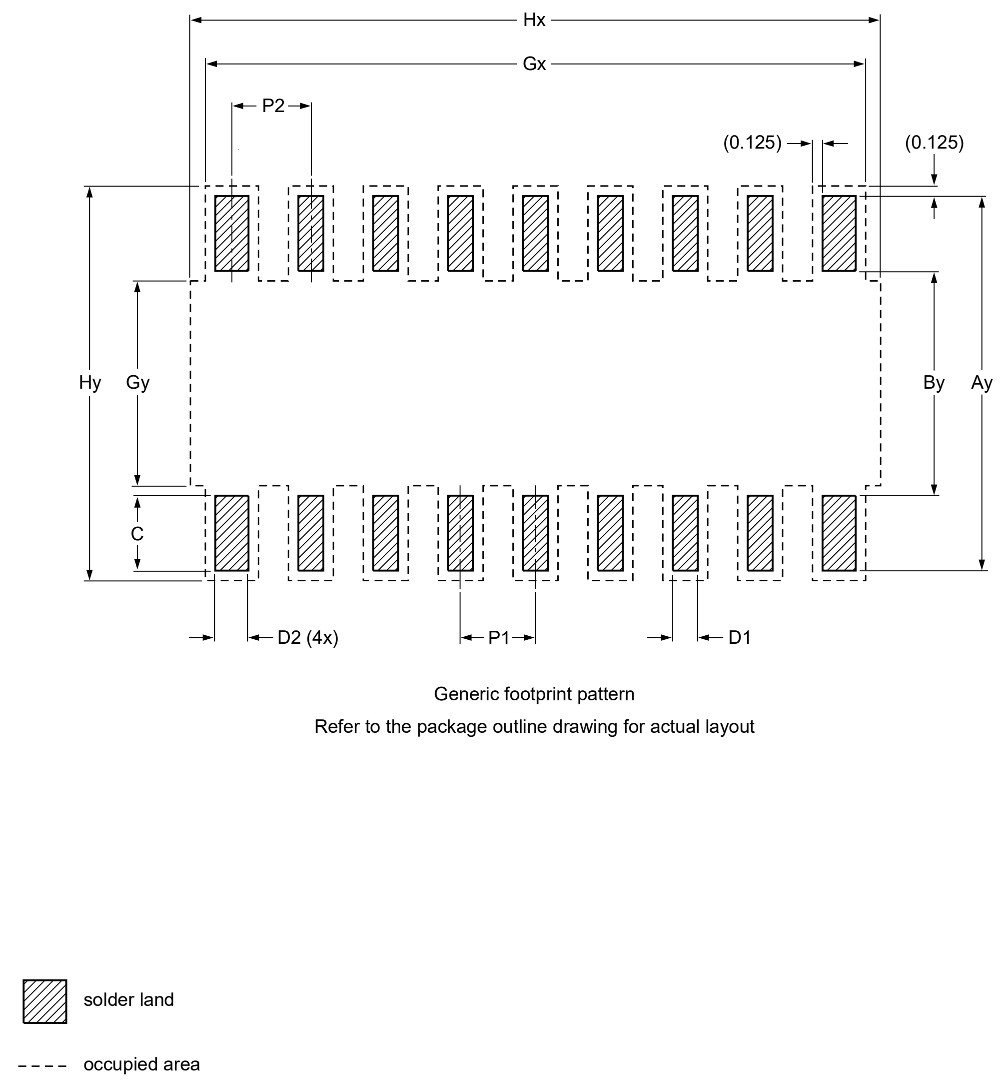
MSL: Moisture Sensitivity Level

Figure 14. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

16 Soldering: PCB footprints

Footprint information for reflow soldering of TSSOP8 package **SOT505-2**



DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.700	4.400	2.700	0.850	0.400	0.500	2.800	3.600	3.600	4.650

sot505-2_fr

Figure 15. PCB footprint for SOT505-2 (TSSOP8); reflow soldering

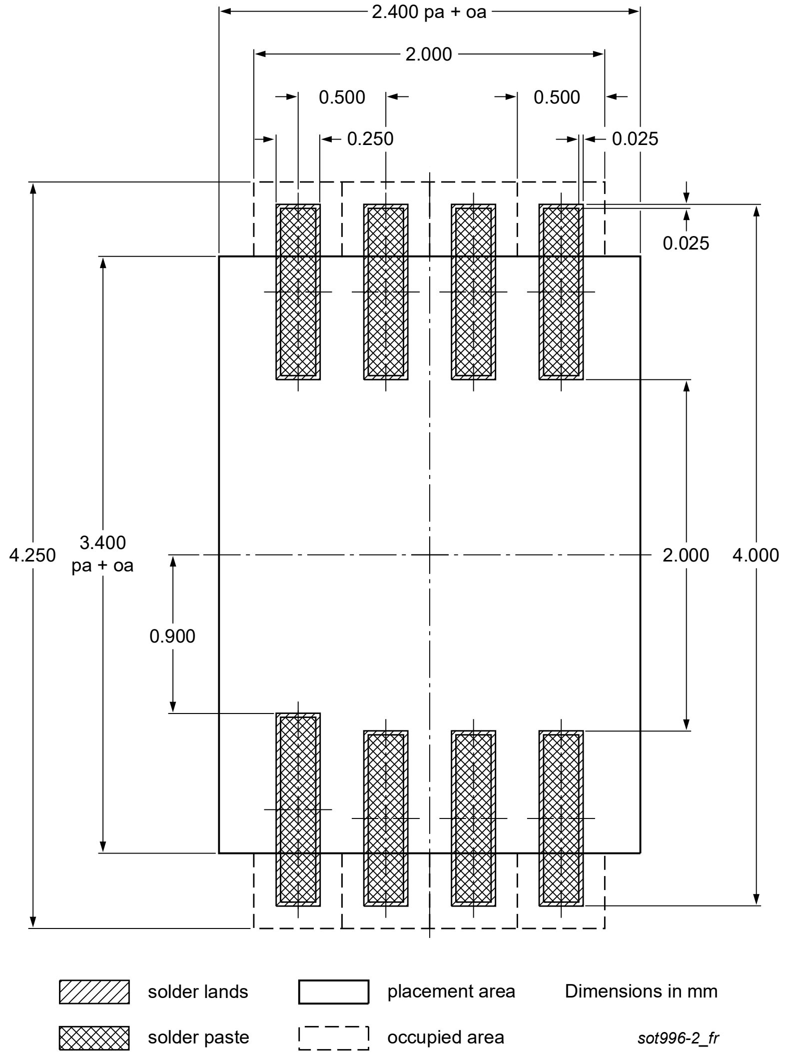
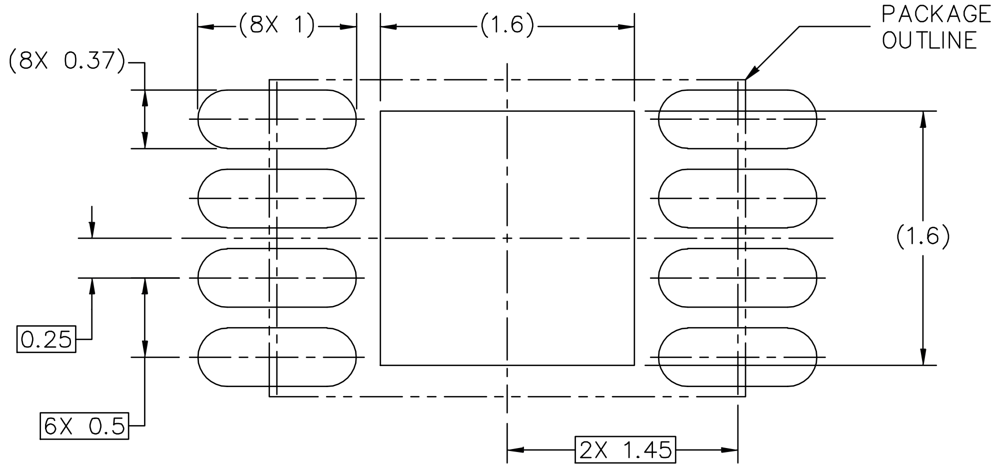


Figure 16. PCB footprint for SOT996-2 (XSON8U); reflow soldering

H-PDFN-8 I/O
3 X 2 X 0.5 PKG, 0.5 PITCH

SOT1052-2



PCB DESIGN GUIDELINES
RECOMMENDED SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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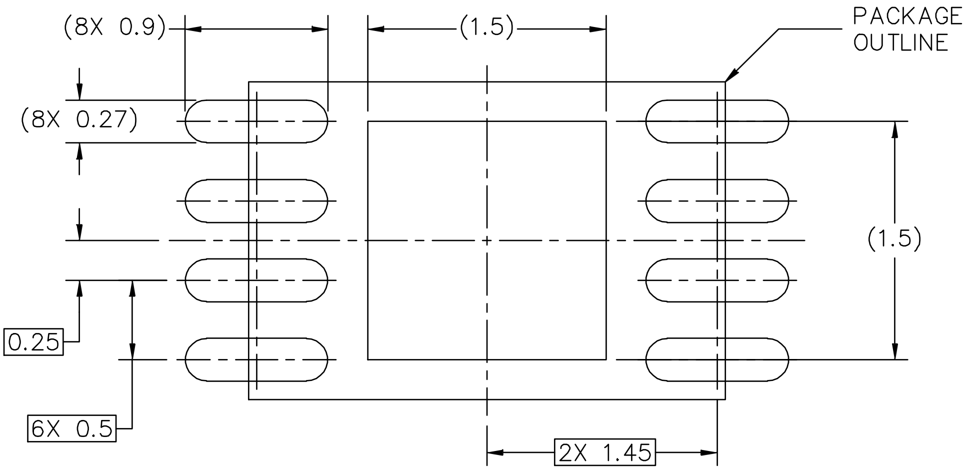
Figure 17. PCB footprint for SOT1052-2 (XSON8); recommended solder mask opening pattern

H-PDFN-8 I/O
3 X 2 X 0.5 PKG, 0.5 PITCH

SOT1052-2



PCB DESIGN GUIDELINES
RECOMMENDED I/O PADS AND SOLDERABLE AREA

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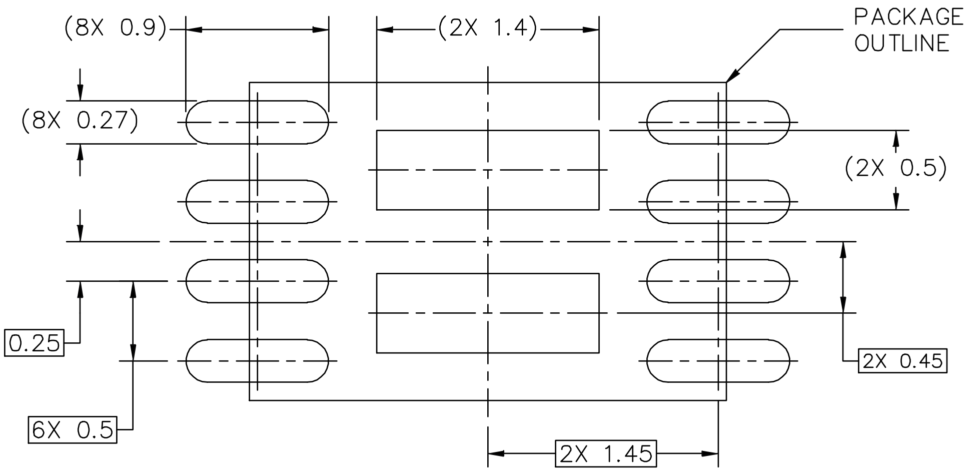
Figure 18. PCB footprint for SOT1052-2 (XSON8); recommended I/O pads and solderable area

H-PDFN-8 I/O
3 X 2 X 0.5 PKG, 0.5 PITCH

SOT1052-2



RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – RECOMMENDED SOLDER PASTE STENCIL

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DATE: 06 JAN 2022

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON–JEDEC	DRAWING NUMBER: 98ASA01831D	REVISION: O	

Figure 19. PCB footprint for SOT1052-2 (XSON8); recommended solder paste stencil

H-PDFN-8 I/O
3 X 2 X 0.5 PKG, 0.5 PITCH

SOT1052-2

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS, DIE ATTACH FLAG.
5. MIN. METAL GAP FOR LEAD TO EXPOSED PAD SHALL BE 0.2 MM.

DATE: 06 JAN 2022

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON-JEDEC	DRAWING NUMBER: 98ASA01831D	REVISION: 0	

Figure 20. PCB footprint for SOT1052-2 (XSON8); notes

17 Abbreviations

Table 16. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
GPIO	General Purpose Input Output
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
MIL	Military
MM	Machine Model
PCB	Printed-Circuit board
PMOS	Positive Metal Oxide Semiconductor
SMBus	System Management Bus
UART	Universal Asynchronous Receiver Transmitter
UTLP	Ultra Thin Leadless Package

18 Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NTS0102_Q100 v.1.2	20220303	Product data sheet	—	NTS0102_Q100 v.1.1
Modifications:	• Section 4, Table 2: Updated table note [2] • Updated SOT1052-2 (XSON8) Figure 12 and Figure 13 • Added Section 13.8, Section 15 and Section 16			
NTS0102_Q100 v.1.1	20211112	Product data sheet	—	NTS0102_Q100 v.1
NTS0102_Q100 v.1	20130227	Product data sheet	—	—

19 Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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