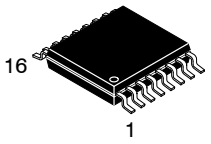
PoE-PD Interface Controller, IEEE 802.3bt

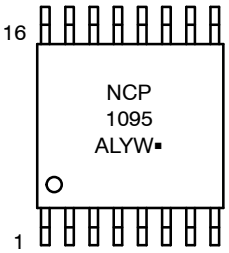
NCP1095

RELATED STANDARDS
IEEE 802.3bt−2018



TSSOP−16
CASE 948F

MARKING DIAGRAM



NCP1095	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCP1095DBR2	TSSOP−16 (Pb−Free)	2500 / Tape & Reel
NCP1095DB	TSSOP−16 (Pb−Free)	96 / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Description

The NCP1095 is a member of the ON Semiconductor Power over Ethernet Powered Device (PoE−PD) product family, and allows the device containing the NCP1095 based PD to become an IEEE 802.3af/at and −3bt compliant powered equipment.

It incorporates all the required functions for operation within a PoE system such as detection, classification and current limiting during the inrush phase. The NCP1095 supports high-power applications (up to 90 W PoE) through an external pass transistor. A power good pin guarantees proper disabling/enabling of the adjacent main DC/DC converter. The classification result pins allow for operation according to the assigned power Class (up to Class 8).

The NCP1095 also offers Autoclass support and indicates when a short Maintain Power Signature can be implemented. In addition an auxiliary supply detection pin allows NCP1095 to be used in applications where power can be supplied by either PoE or by a wall adapter.

Features

- Fully Supports IEEE 802.3af/at and −3bt Specifications
- Supports Up to 5-Event Physical Layer Classification
- Assigned Power Level Up to 90 W
- Supports Autoclass
- 110 mA Typical Inrush Current Limiting
- Open Drain Power Good Indicator
- Support for Short MPS
- Pass Switch Disabling Input for Rear Auxiliary Supply Operation
- Proprietary 100 W+ Applications
- Over Current Protection
- Over Temperature Protection
- Junction Temperature Range of −40°C to +125°C
- Available in 16-pin TSSOP
- These Devices are Pb−Free and are RoHS Compliant

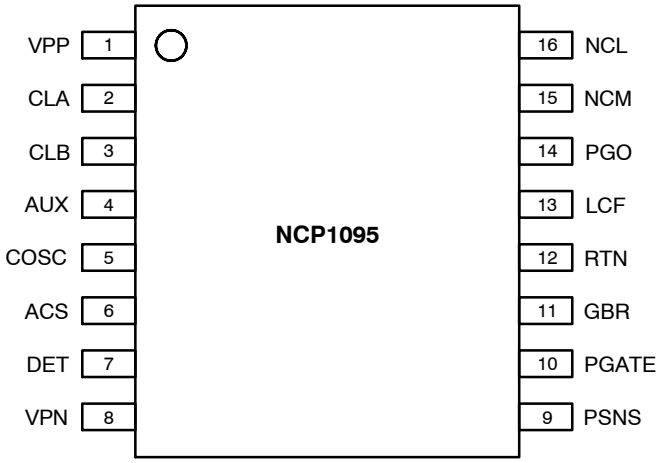


Figure 1. Pin-out NCP1095 in 16-pin TSSOP (Top View)

PIN DESCRIPTION

Signal Name	Pin No.	Type	Description
VPP	1	Power	Positive input power. Connect to the positive terminal of the rectifier bridge
CLA	2	Output	Connect a class signature programming resistor to VPN. See classification section for recommended values
CLB	3	Output	
AUX	4	Input	Auxiliary supply detection input. Referenced to VPN
COSC	5	Analog	Connect a 1 nF capacitor between COSC and VPN. This pin is pulled to VPP during the detection phase
ACS	6	Input	Autoclass enable/disable input. Pull to VPN to disable Autoclass; leave floating to enable Autoclass
DET	7	Output	Connect a 26.1 kΩ detection resistor between DET and COSC. This pin is pulled to VPN during the detection phase
VPN	8	Power, Ground	Negative input power. Connect to the negative terminal of the rectifier bridge
PSNS	9	Input	Positive current sense line. Connect to the positive side of the external sense resistor (and the source of the external pass transistor)
PGATE	10	Output	Gate driver for the external pass transistor
GBR	11	Output, Open Drain	Control output to disable the active rectifier bridge. This pin is referenced to VPN
RTN	12	Power	DC/DC controller power return. Connect to the drain of the external pass transistor
LCF	13	Output, Open Drain	Long Classification Finger Indicator. This pin is referenced to RTN. Connect with a pull-up resistor to the logic supply
PGO	14	Output, Open Drain	Power Good Indicator. This pin is left floating when the power good signal is active. Referenced to RTN. Must be used to enable/disable the main DC/DC converter adjacent to NCP1095.
NCM	15	Output, Open Drain	Class result MSB output. This pin is referenced to RTN. Connect with a pull-up resistor to the logic supply
NCL	16	Output, Open Drain	Class result LSB output. This pin is referenced to RTN. Connect with a pull-up resistor to the logic supply

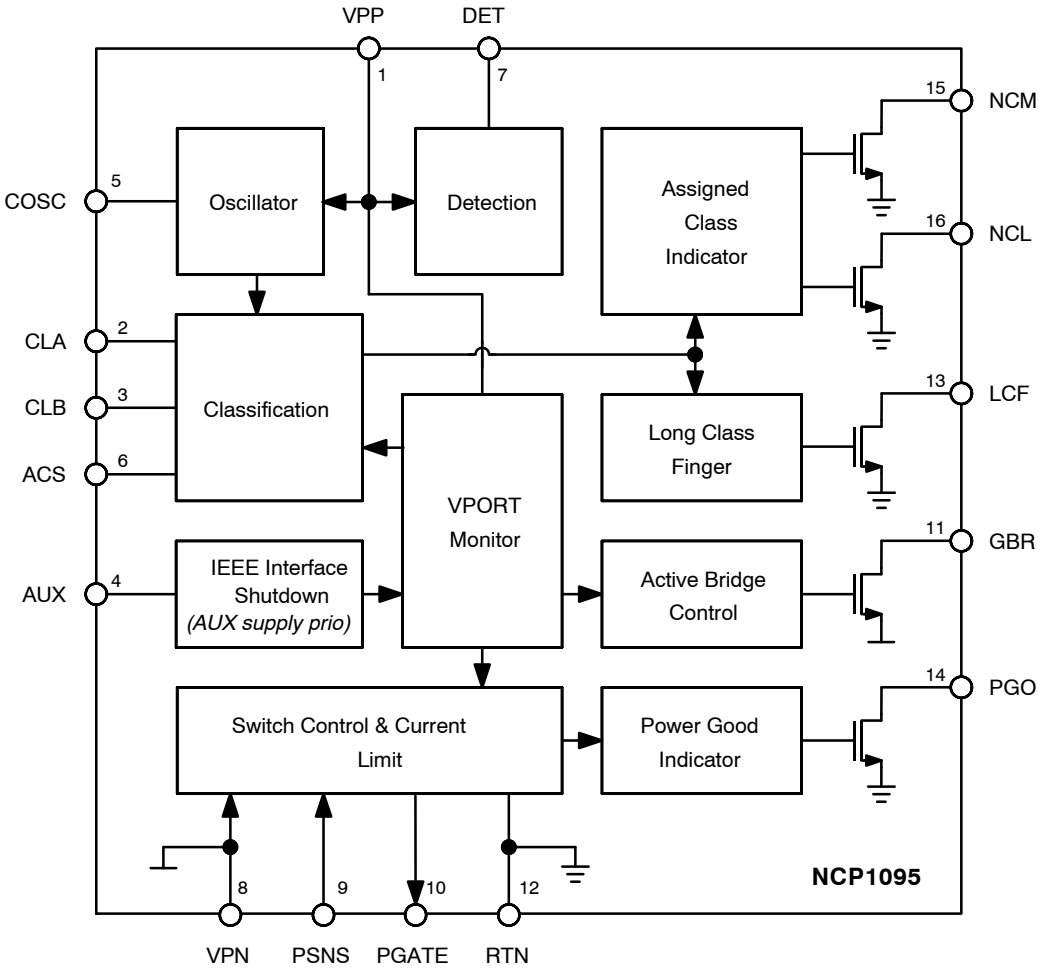


Figure 2. NCP1095 Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit	Conditions
T_J	Junction temperature	−40	+150	°C	
T_S	Storage temperature	−55	+150	°C	
VPP	Input Power Supply	−0.3	72 (Note 1)	V	Voltage with respect to VPN
RTN	Pass switch drain connection, application ground	−0.3	72 (Note 1)	V	Voltage with respect to VPN, Pass switch in the off state
PSNS	Pass switch sense resistor voltage	−0.3	3.6	V	Voltage with respect to VPN
DET	Voltage on pin DET				
PGATE	Pass switch gate drive voltage	−0.3	11	V	Voltage with respect to VPN
PGO	Power Good output	−0.3	72	V	Voltage with respect to RTN
NCM	Class result MSB output				
NCL	Class result LSB output				
LCF	Long Class Finger output				
ACS	Voltage on AUTOCLASS pin	−0.3	72	V	Voltage with respect to VPN
CLA, CLB	Voltage on CLASSA or CLASSB pins				
GBR	Active bridge control output				
COSC	Voltage on pin COSC				
AUX	Auxiliary supply detection input				
ESD−HBM	Human Body Model	2		kV	Per EIA−JESD22−A114 standard
ESD−CDM	Charged Device Model	500		V	Per ESD−STM5.3.1 standard

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. NCP1095 tolerates transient overvoltages from the capacitor and/or TVS subjected to a surge according to IEC 61000−4−5. For extremely high cable discharge and surge protection, contact ON Semiconductor.

THERMAL CHARACTERISTICS (Note 2)

Symbol	Characteristic	Typical Value	Unit
θ_{JA}	Thermal Resistance, Junction-to-Air	90.3	°C/W

2. θ_{JA} is obtained with 1S2P test board (1 signal − 2 plane) and natural convection. Refer to JEDEC JESD51 for details.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
T_J	Junction Temperature	−40	+125	°C
V_{PORT} (Note 3)	Input Power Supply ($V_{PORT} = V_{PP} - V_{PN}$)	0	57	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Refer to ABSOLUTE MAXIMUM RATINGS for Safe Operating Area.

ELECTRICAL CHARACTERISTICS

(All parameters are guaranteed for the recommended operating conditions unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
DETECTION CHARACTERISTICS						
Rdetect	Equivalent detection resistance	23.7		26.3	kΩ	R_{DET} = 26.1 kΩ ±1%; 1 V ≤ V_{PORT} ≤ 10.1 V
VoffsetIC	Detection offset voltage (IC part)	0		0.2	V	
CLASISFICATION CHARACTERISTICS						
Vcl_th	Class/Mark current switchover threshold (Note 4)	10.1		12.5	V	V_{PORT} rising or falling
Vcldis	Classification current disable threshold (Note 4)	20.5		24.5	V	V_{PORT} rising or falling
Iclsigq	Quiescent current during classification	207	327	484	μA	V_{PORT} = 12.5 V
Vcsr	CLASS driver voltage (Note 4) during class event	8.5	9.15	9.7	V	12.5 V ≤ V_{PORT} ≤ 20.5 V
Iclsig0	RclassA,B = 4.5 kΩ ±1%	1		4	mA	12.5 V ≤ V_{PORT} ≤ 20.5 V
Iclsig1	RclassA,B = 909 Ω ±1%	9		12	mA	12.5 V ≤ V_{PORT} ≤ 20.5 V
Iclsig2	RclassA,B = 511 Ω ±1%	17		20	mA	12.5 V ≤ V_{PORT} ≤ 20.5 V
Iclsig3	RclassA,B = 332 Ω ±1%	26		30	mA	12.5 V ≤ V_{PORT} ≤ 20.5 V
Iclsig4	RclassA,B = 232 Ω ±1%	36		44	mA	12.5 V ≤ V_{PORT} ≤ 20.5 V
Imark	IPP during mark event range	1	2.3	4	mA	4.9 V ≤ V_{PORT} ≤ 10.1 V
tfce	Short/Long first class event threshold	75		88	ms	R_{DET} = 26.1 kΩ ±1%; C_{OSC} = 1 nF ±2%
tacspd	Change to class signature ‘0’ current timing	75.5		87.5	ms	Autoclass enabled
RC OSCILLATOR CHARACTERISTICS						
fosc	Frequency of the oscillator		26.8		kHz	R_{DET} = 26.1 kΩ; C_{OSC} = 1 nF
duty	Oscillator duty cycle		50		%	
PASS SWITCH CURRENT CONTROL STATE CHARACTERISTICS						
Iinr	Inrush current	85	110	135	mA	25 mΩ Sense Resistor
Vdrain_pg	RTN PowerGood threshold voltage (Note 4)	0.7	0.8	0.9	V	RTN–VPN falling
Vgate_pg	PGATE PowerGood threshold voltage (Note 4)	6.9	8.5	10.0	V	PGATE–VPN rising
Vpgo_low	PGO output low voltage	–	0.15	0.50	V	Isink = 2 mA. Referenced to RTN
PASS SWITCH ON STATE CHARACTERISTICS						
Idd_on	Operating current	257	407	601	μA	V_{PORT} = 57 V
Ioc	Over current detection level	5.0	6.4	8.0	A	25 mΩ Sense Resistor
Voc	RTN overcurrent detection voltage (Note 4)	1.1	1.2	1.3	V	RTN–VPN rising
UNDER-VOLTAGE LOCK-OUT CHARACTERISTICS						
UVLO_H	VPP UVLO threshold voltage (Note 4)	33.0	35.1	37.5	V	V_{PORT} rising
UVLO_L	VPP UVLO threshold voltage (Note 4)	30.0	32.3	34.5	V	V_{PORT} falling
UVLO_hyst	UVLO threshold hysteresis	2.4	2.8	3.3	V	
RESET CHARACTERISTICS						
Vrst	VPP reset threshold voltage (Note 4)	2.81	3.85	4.9	V	V_{PORT} falling

4. Voltage referenced to VPN.
5. E.g. after overcurrent timeout

ELECTRICAL CHARACTERISTICS (continued)
(All parameters are guaranteed for the recommended operating conditions unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Unit	Condition
AUXILIARY SUPPLY DETECTION CHARACTERISTICS						
AUX_H	AUX input high level voltage (Note 4)	1.7	2.15	2.6	V	
AUX_L	AUX input low level voltage (Note 4)	0.5	0.75	1.05	V	
AUX_hyst	AUX threshold hysteresis	1.0	1.4	2.0	V	
AUX_pd	AUX internal pull down	180	265	380	kΩ	VAUX = 0.5 V
CLASSIFICATION RESULT INDICATOR CHARACTERISTICS						
Vlow	NCL, NCM or LCF output low voltage	–	0.15	0.50	V	Isink = 2 mA. Referenced to RTN
GBR CHARACTERISTICS						
Vgbr_low	GBR output low voltage (Note 4)	–	0.15	0.50	V	Isink = 2 mA
PASS SWITCH OFF STATE CHARACTERISTICS						
Idd_off_err	Poweroff current, error state (Note 5)	–	230	–	μA	V_{PORT} = 57 V, RTN = VPP
Idd_off_aux	Poweroff current, aux mode	198	315	463	μA	VPP−RTN = 57 V, AUX−VPN = 3.3 V
THERMAL PROTECTION CHARACTERISTICS						
TSD	Thermal shutdown threshold	150	–	–	°C	Junction temperature

4. Voltage referenced to VPN.
5. E.g. after overcurrent timeout

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

SIMPLIFIED APPLICATION SCHEMATIC

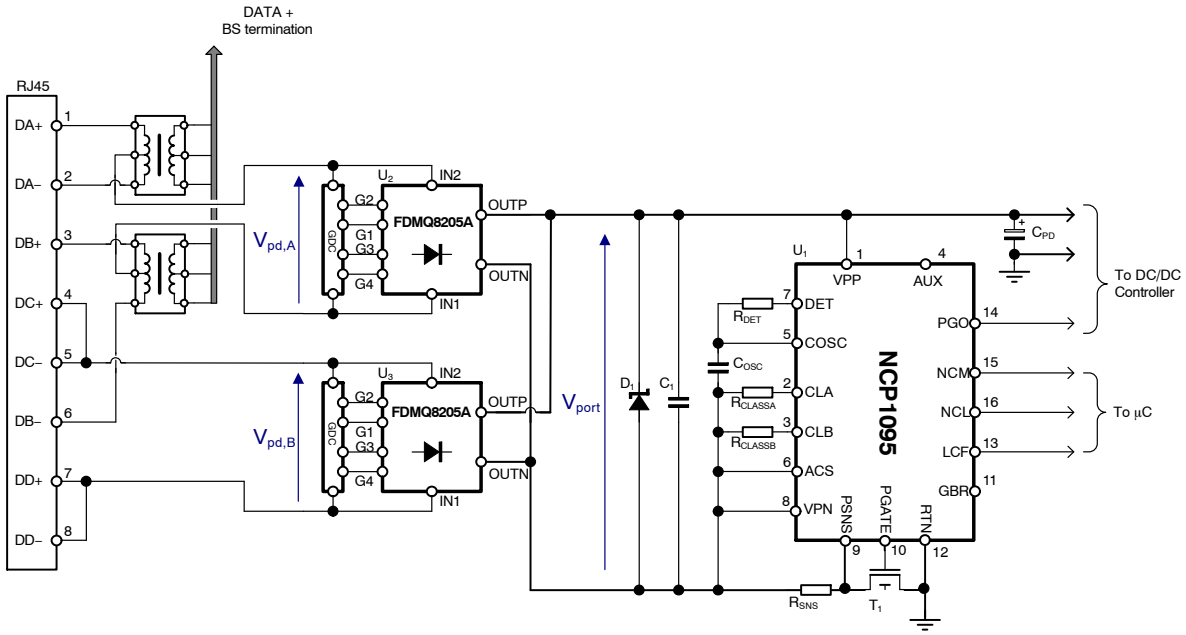


Figure 3. General Application Schematic

TYPICAL BILL OF MATERIALS

Reference Designator	Description	Value (Nominal)	Tolerance	Manufacturer	Part Number
U_1	PoE Interface	NCP1095		ON Semiconductor	NCP1095
U_2, U_3	GreenBridge™ Rectifier	FDMQ8205A		ON Semiconductor	FDMQ8205A
D1	TVS Protection	58 V		Littelfuse	SMBJ58A
C1	VPP decoupling capacitor	100 nF/100 V	±10%	Walsin	0805B104K101CT
COSC	Oscillator capacitor	1 nF	±2%	Murata	GRM1885C1H102GA01D
CPD	VPP bulk capacitor	10 µF/80 V	±20%	Panasonic	EEEFK1K100XP
RDET	Detection resistor	26.1 kΩ	±1%	Panasonic	ERJ3EKF2612V
RCLASSA	Classification resistor A	232 Ω	±1%	Panasonic	ERJ8ENF2320V
RCLASSB	Classification resistor B	332 Ω	±1%	Panasonic	ERJ6ENF3320V
RSNS	Current sense resistor	25 mΩ	±1%	Yageo	RL1206FR−070R025L
T1	Pass switch	100 V/40 mΩ		ON Semiconductor	FDMC8622

APPLICATION INFORMATION

The NCP1095 is a Power over Ethernet Powered Device (PD) interface controller with an external n-channel MOSFET load switch.

Powered Device Interface

The NCP1095 is located at the interface of the PD and will interact with the Power Sourcing Equipment (PSE) over the Ethernet cable. NCP1095 allows the device to be powered by an IEEE 802.3af/at or −3bt compliant PSE. It provides a detection signature, classification handshaking, inrush current limitation and operational overcurrent protection. A block diagram is shown in Figure 2. Each section will be explained in more detail below.

Detection

During the detection phase, the PSE will check if a valid or a non-valid detection signature is present. This will enable the PSE to differentiate between equipment supporting PoE requesting power and equipment either not supporting PoE or not requesting power. In order to be able to present a valid detection signature to the PSE, a 26.1 kΩ resistor must be inserted between the COSC and DET pins of NCP1095. During the detection phase all blocks of the chip are in power-down except for an internal reference, a comparator and two switches.

When the voltage at the PD power interface is within the detection range, the COSC pin is pulled to VPP and the DET pin is pulled to VPN, resulting in the PD presenting a valid detection signature. The offset voltage of the input rectifier bridge should be between 0 and 1.7 V in the detection range ($2.7\ V \le V_{PD} \le 10.1\ V$).

When the PSE has detected a valid detection signature and continues towards powering on the PD, the COSC and DET switches are turned off in order to reduce the current consumption of the PD.

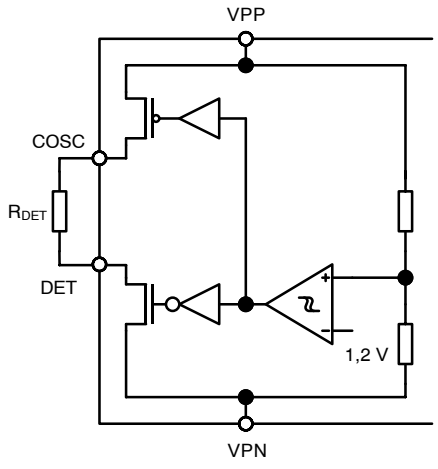


Figure 4. Detection Circuit

Classification

A PD is characterized based upon the maximum power level it requires at its power interface during operation. The IEEE 802.3bt standard supports up to 71.3 W PDs and defines 8 power Classes: Class 1 up to Class 8. The PD must conform to a Class with a power level that is at or above the maximum power the PD requires. Table 1 lists the different Classes and the corresponding power level they stand for. Based on the Class the PD conforms to, two resistance values are listed. The R_{classA} value must be inserted between CLA and VPN. Likewise, the R_{classB} value must be inserted between CLB and VPN. Eventually, when implementing a Class 1, 2, 3 or 4 PD, the CLA and CLB pins can be shorted together to the same single resistor.

Table 1. CLASSIFICATION RESISTOR VALUE

PD Class	PD Power	R_{CLASSA} (Note 7)	R_{CLASSB} (Note 7)
0 (Note 6)	13 W	4.5 kΩ	4.5 kΩ
1	3.84 W	909 Ω	909 Ω
2	6.49 W	511 Ω	511 Ω
3	13 W	332 Ω	332 Ω
4	25.5 W	232 Ω	232 Ω
5	40.0 W	232 Ω	4.5 kΩ
6	51.0 W	232 Ω	909 Ω
7	62.0 W	232 Ω	511 Ω
8	71.3…90 W	232 Ω	332 Ω

6. 3bt compliant PDs should use Class 1, 2 or 3 instead of Class 0.
7. All resistors must be 1% accurate.

Once the PSE device has detected the PD device, the classification process begins. The NCP1095 is fully capable of responding and completing classification with all PSE types described in the 802.3af/at and −3bt PoE Standard. The Class requested by NCP1095 during classification is determined by the resistors connected to the CLA and CLB pins. Depending on the power the PSE is able to deliver to the PD, the PSE will generate a different number of class-mark events. This will determine the amount of power the PD is allowed to use. Next to that, the NCP1095 is able to distinguish between a 3bt compliant PSE and a 3af/at compliant PSE. Therefor a 1 nF capacitor must be inserted between COSC and VPN. The classification results will be written to the status outputs NCL, NCM and LCF. The offset voltage of the input rectifier bridge should be between 0 and 2 V in the detection range ($14.5\ V \le V_{PD} \le 20.5\ V$).

During a class event, the power dissipation in the R_{class} resistor can be significant (V_{csr}^2/R_{class}) and its package size must be chosen properly. When the port voltage rises above V_{cldis} the class drivers will be disabled in order to limit the power dissipation.

Inrush Current Limiting

When the PSE has successfully assigned the PD to a specific Class in correspondence with the power the PSE is able to deliver, the PSE will increase the voltage at its power interface up to its internal power supply voltage. NCP1095 will enter the inrush current control state once its port voltage rises above the UVLO_H threshold.

In this state, NCP1095 will control the charging of its port capacitance C_{PD} located between VPP and RTN by operating the pass switch transistor in the active region. The current through the pass switch is regulated by monitoring the voltage over an external sense resistor R_{SNS} = 25 mΩ. NCP1095 will limit the inrush current well below the PSE inrush threshold while charging its port capacitance. The nominal level of the inrush current is 110 mA typ. The NCP1095 will exit the inrush current control state when the voltage between RTN and VPN is smaller than 0.8 V and the gate voltage rises above 8.5 V. At this stage, the port capacitance can be considered to be fully charged, and NCP1095 will enter the normal operation mode with the pass switch completely turned on.

If the port capacitance voltage remains low due to an output short error condition, the inrush current control state will be aborted to protect the pass-switch. In order not to be considered as a short, the port capacitance should be chosen not to have too high a value (above 1.5 mF).

Class 1 and 2 PDs should operate according to their power Class 50 ms after the UVLO_H threshold was crossed. Therefore it is recommended to limit the port capacitance to 59 µF for Class1 PDs and to 99 µF for Class2 PDs.

PGO Indicator

While in the inrush current control state, the PGO output will be held low by NCP1095.

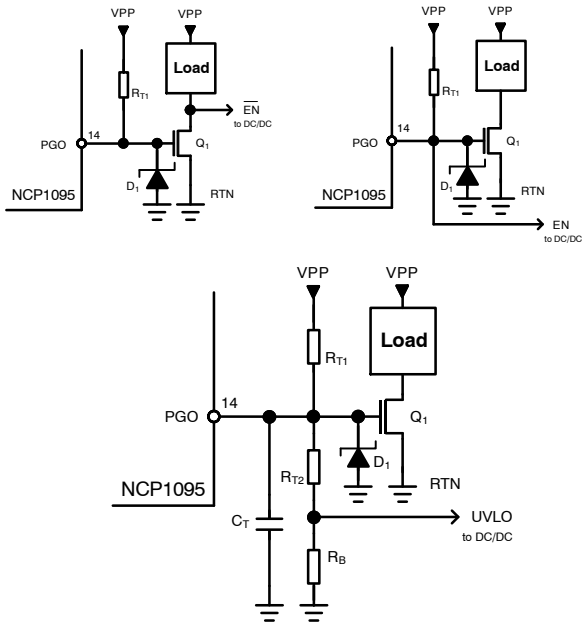


Figure 5. PGO Interfacing

This PGO output MUST be used to hold off the adjacent main DC/DC converter as well any significant load present between VPP and RTN. This is important in order not to further increase the already significant stress in the pass-switch during inrush. Figure 5 shows how to hold off a significant load and a DC/DC converter which has either an /EN, EN or UVLO input.

System Start-up

Once NCP1095 exits the inrush current control state, it will make the PGO output floating, indicating the main DC/DC converter – and eventually the system – is allowed to start. This also indicates NCP1095 will no longer actively limit the current and/or the power, as the pass switch is on and will be left turned on.

PDs requesting Class 4 or higher need to take into account that they can be underpowered and need to implement some basic functionality with Class 3 power level. Also, the microcontroller will only be able to read the classification result after system startup. Therefore the main DC/DC converter and the system must be able to start up with Class 3 power (or lower for Class 1 and Class 2 PDs) and turn on higher power loads only if this is allowed by the PSE assigned Class.

Even when being assigned to Class 4 or higher by the PSE, the PD is only allowed to use this increased power level 80 ms after the UVLO_H threshold was crossed. The nominal delay introduced to charge the port capacitance can be calculated from the formula below.

$$t_{charge}\,(ms) = \frac{C_{pd}\,(\mu F) \cdot V_{pd}\,(V)}{103} \qquad \text{(eq. 1)}$$

As an example, it typically takes 80 ms to charge a 165 µF capacitor to 50 V. Depending mainly on the chosen port capacitor value, this 80 ms delay may or may not yet have passed when the NCP1095 exits the inrush current control state.

NCM and NCL Indicators

The state of the NCM and NCL outputs provides information about the power level that the PSE has assigned to the PD during classification. These status outputs are actually only relevant for PDs requesting Class 4 or higher as those need to take into account that they can be underpowered. See Table 2 to determine the assigned power based on the NCM and NCL outputs and the requested Class. An underpowered PD can eventually be assigned to Class 3, 4 or 6.

Table 2. CLASSIFICATION RESULT OVERVIEW

Requested Class	NCM	NCL	Assigned Class	Assigned Power
4	open	open	3	13 W
	open	low	4	25.5 W
	low	X		
5	open	open	3	13 W
	open	low	4	25.5 W
	low	X	5	40 W
6	open	open	3	13 W
	open	low	4	25.5 W
	low	X	6	51 W
7	open	open	3	13 W
	open	low	4	25.5 W
	low	open	6	51 W
	low	low	7	62 W
8	open	open	3	13 W
	open	low	4	25.5 W
	low	open	6	51 W
	low	low	8	71.3…90 W

PDs assigned to Class 8 may consume greater than 71.3 W as long as they guarantee not to exceed the 90 W power limit at the PSE power interface. Operation beyond 71.3 W is, however, only possible if additional information is available to the PD regarding the actual link section DC resistance between the PSE and the PD.

The application should always operate at or below the assigned power limit. Failing to do so will result in the PSE disconnecting the PD.

LCF Indicator

The state of the LCF output provides information (retrieved during classification) about the type of PSE the PD is connected to.

- LCF is left floating:
  The PSE is categorized according to 802.3af/at (PSE Type 1 or Type 2).
- LCF is low:
  The PSE is categorized according to 802.3bt (PSE Type 3 or Type 4).

Maintain Power Signature

There is a minimum amount of current a PD needs to draw in order to allow the PSE to determine if the PD is still connected. This is called the Maintain Power Signature (MPS). If the PD no longer maintains this, the PSE may disconnect the power.

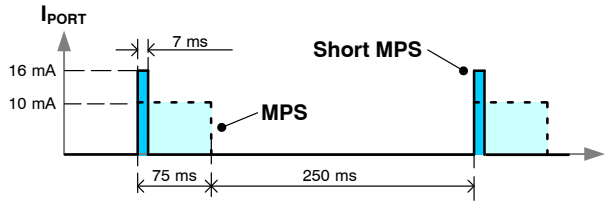


Figure 6. MPS

The current needs to be at or above a certain current threshold ($I_{Port\_MPS,Min}$) during at least a certain amount of time ($T_{MPS\_PD,Min}$). If this has been the case, the current may fall below the threshold for at most a certain dropout period ($T_{MPDO\_PD,Max}$).

Whether or not the lower power short MPS may be used depends upon the state of the LCF output.

Table 3. MPS TIMING

LCF	$T_{MPS\_PD,Min}$	$T_{MPDO\_PD,Max}$
open	75 ms	250 ms
low	7 ms	310 ms

For PDs requesting Class 4 or less the MPS current threshold will always be 10 mA.

For PDs requesting Class 5 or above the MPS current threshold will depend upon the assigned Class (which in fact can be determined by the state of the NCM output).

Table 4. MPS CURRENT

Assigned Class	$I_{Port\_MPS,Min}$
≤ 4	10 mA
≥ 5	16 mA

An important remark is that the PD load current will be low-pass filtered by its port capacitance and the actual resistance of the cable. This should be taken into account when generating current pulses for MPS.

The PD needs to maintain the MPS as soon as its port voltage rises above the UVLO_H threshold. Depending on the amount of port capacitance and the type of PSE it is connected to, the time duration of the inrush current control state might or might not be enough ($T_{MPS\_PD,Min}$) to count as the first valid current pulse. In combination with 3bt PSEs this will usually not be a problem as it typically takes 7 ms to charge just a 14.4 μF cap to 50 V. In combination with 3af/at PSEs the situation is different as it typically takes 75 ms to charge a 176 μF cap to 44 V.

Autoclass

802.3bt foresees an optional extension of classification known as Autoclass. This allows a 3bt certified PSE to better allocate its power among different PDs.

When the ACS pin is connected to VPN, Autoclass is disabled.

When the ACS pin is left floating, Autoclass is enabled and NCP1095 will request an Autoclass measurement to a 3bt type of PSE during classification. If Autoclass is enabled and the LCF output is low, the system must go to the maximum power state according to its assigned Class no later than 1.35 s after power has been applied, and keep the maximum load active until at least 3.65 s after power has been applied. During this period, the PSE will measure the maximum power draw of the PD and allocate this amount of power to the PD.

Peak Power and Transients

Although the PoE standard allows the PD to draw slightly higher peak power during a short time, making use of this is not recommended. It is best to keep this additional margin only to be able to withstand voltage transients on the PSE side. The required recovery time for transients also limits the amount of the port capacitance that can be used.

Under Voltage Lockout

If the port voltage falls below the UVLO_L threshold and remains low for a sufficient amount of time, NCP1095 will enter the poweroff state and turn off the pass switch.

Once the port voltage falls below the reset threshold Vrst, the NCP1095 will re−enter the idle state and can again be detected as a PD requesting power.

Operational Current Protection

In the normal operation mode, NCP1095 will monitor the current through the pass switch and provide protection against soft and hard shorts.

Soft shorts are detected if the current is above the short circuit threshold I_{OC} (6.4 A typ) and a time out delay of 960 μs is passed. After this time-out delay the pass switch is disabled.

A hard short is detected if the voltage across the pass-switch and sense resistor is above V_{OC} (1.2 V typ). The pass gate is switched off within 18 μs in this case.

Once an overcurrent condition is detected during the normal operation mode, the NCP1095 will transition to the offline state and remain there until the port voltage falls below the reset threshold V_{rst}.

Thermal Shutdown

The NCP1095 includes a thermal shutdown which protects the device in the case that the junction temperature is too high. An on-chip sensor monitors the temperature. Once the thermal shutdown threshold (TSD_H) is exceeded, all functions are disabled and the device goes into the offline state.

The device will remain in offline until the junction temperature drops below TSD_L and the port voltage falls below the reset threshold V_{rst}.

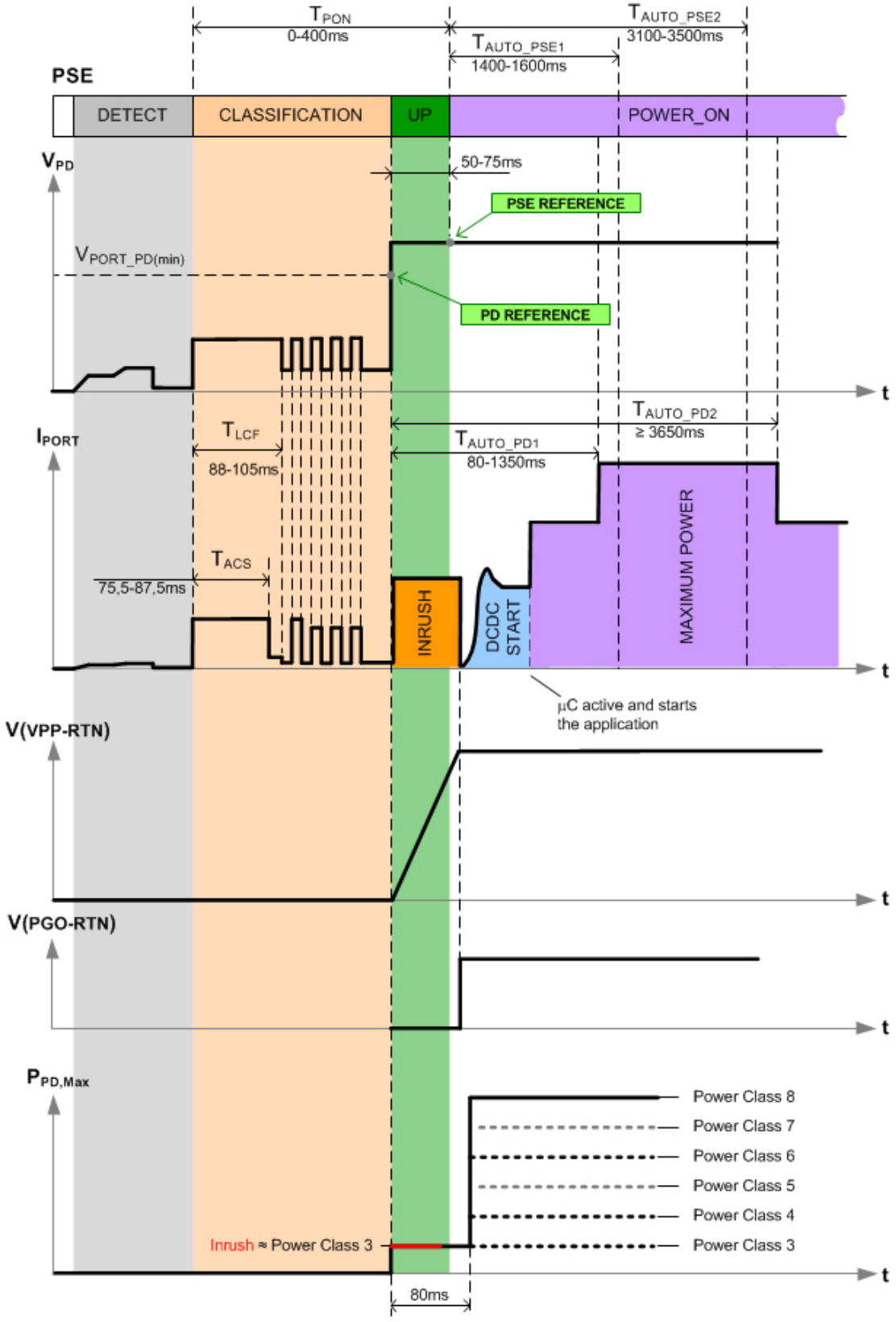


Figure 7. Complete Start-up Diagram of a Class 8 PD with Autoclass

PoE System Overview

The overall PoE standard distinguishes between four Types of PSEs and four Types of PDs.

- Type 1 PSEs and PDs behave according to 802.3af/at
- Type 2 PSEs and PDs behave according to 802.3at
- Type 3 and 4 PSEs and PDs behave according to 802.3bt

Table 5 gives an overview of the system parameters that are allowed and required for operation at a certain power level (assigned Class).

An important parameter is the cable DC resistance (determined by cable type and length).

In general a Cat 5 cable is required when using a Type 3 or Type 4 PD or PSE in the system or when both PSE and PD are of Type 2.

Operation over 4-pair is reserved for Type 3 and 4 PSEs.

Table 5. SYSTEM PARAMETERS OVERVIEW

Assigned Class	PSE Type	Minimum Cabling Type	Number of Powered Pairs	PD Type	Requested Class	Standard
1	1	Cat 3 (Note 8)	2p	1	1	802.3af/at
	2	Cat 3				
	3, 4	Cat 3	2p/4p	3		802.3bt
2	1, 2	Cat 3	2p	1	2	802.3af/at
	3	Cat 5 (Note 9)	2p/4p	3		802.3bt
	4	Cat 5				
3	1	Cat 3	2p	1	0, 3	802.3af
	1	Cat 3 (Note 10)	2p	1	0, 3	802.3at
				2	4	
	2	Cat 3		1	0, 3	802.3af/at
				2	4	802.3at
	3, 4	Cat 5	2p/4p	3	3, 4/5/6	802.3bt
				4	7/8	
4	2	Cat 5	2p	2	4	802.3at
	3, 4		2p/4p	3	4/5/6	802.3bt
				4	7/8	
5	3, 4	Cat 5	4p	3	5	802.3bt
6	3, 4	Cat 5	4p	3	6	802.3bt
				4	7, 8	
7	4	Cat 5	4p	4	7	802.3bt
8	4	Cat 5	4p	4	8	802.3bt

8. Critical for: 44 V/4 W source connected to 3.84 W load over 20 Ω.
9. Critical for: 50 V/6.7 W source connected to 6.49 W load over 12.5 Ω.
10. Critical for: 44 V/15.4 W source connected to 13 W load over 20 Ω.

Auxiliary Supply

To support applications connected to non-PoE enabled networks and to minimize the bill of materials, the NCP1095 supports drawing power from an alternate or local power source and allows a simplified design with auxiliary supply priority.

NCP1095 has a high voltage compliant AUX input pin. If the AUX pin voltage rises above the AUX_H threshold and remains high for a sufficient amount of time, the NCP1095 will turn off the pass switch and transition to the offline state (indicated by NCM, NCL and LCF being left floating). Disabling the pass switch based on the AUX input is useful for PD applications where the auxiliary supply has to be dominant over the PoE supply. When the auxiliary supply is inserted into a PoE powered application, the pass switch disconnection will move the current path from the PSE to the rear auxiliary supply. Since the current delivered from the PSE will go below the DC MPS level (as specified in the IEEE 802.3af/at, −3bt standard) the PSE will disconnect the PoE−PD. The auxiliary supply is connected between VPP and RTN with a serial diode D1 between VPP and VAUX+, as shown in Figure 8. It is recommended to use the circuit with PNP transistor in combination with an auxiliary supply.

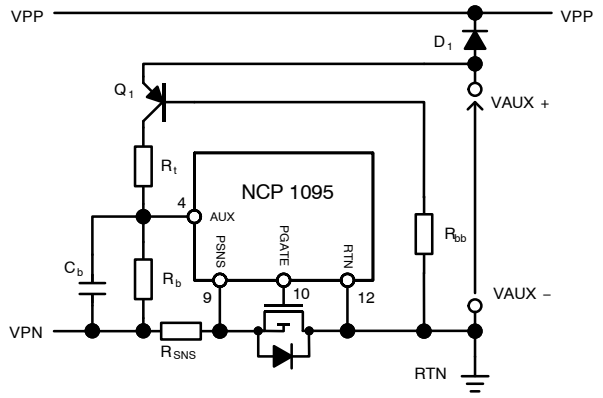


Figure 8. AUX Pin Interfacing

It is necessary that the port voltage falls below the reset threshold V_{rst} for the NCP1095 to re−enter the idle state in which it can again be detected as a PD requesting power.

If a too low aux (10.1 V…24.5 V) is inserted before the UVLO threshold was crossed by the PSE, the class driver could become unintentionally activated. The resulting large additional current draw can be easily prevented if the auxiliary supply is detected at a Vport voltage below 10.1 V. This is accomplished by taking R_t = 33 kΩ and R_b = 15 kΩ.

GBR Output

If the AUX input pin of NCP1095 is pulled high, it will immediately drive the GBR pin low. This allows the GreenBridge input rectifiers to be disabled.

The GBR pin must be used to disable the GreenBridge when a high voltage (> 30 V) auxiliary supply is used in order to be sure the PD does not source power.

Dual-signature PD

Up to now the description has been for a PD compliant to IEEE 802.3af/at or a single-signature PD compliant to IEEE 802.3bt. The IEEE 802.3bt standard also introduces the concept of a dual-signature PD. These have a separate input bridge rectifier and PD controller for each alternative or mode (A and B).

The maximum input average power is different for a Class 5 dual-signature PD (35.6…45 W) compared to a Class 5 single-signature PD. More general, a dual-signature PD uses a different class B resistance value.

Table 6. CLASSIFICATION RESISTOR VALUE

PD Class	R_{CLASSA} (Note 11)	R_{CLASSB} (Note 11)	PD Power
1	909 Ω	4.5 kΩ	3.84 W
2	511 Ω	4.5 kΩ	6.49 W
3	332 Ω	4.5 kΩ	13 W
4	232 Ω	4.5 kΩ	25.5 W
5	232 Ω	332 Ω	35.6…45 W

11. All resistors must be 1% accurate.

The NCM, NCL and LCF outputs behave in a similar way.

Table 7. CLASSIFICATION RESULT OVERVIEW

Requested Class	NCM	NCL	Assigned Class	Assigned Power
4	open	open	3	13 W
	open	low	4	25.5 W
	low	X		
5	open	open	3	13 W
	open	low	4	25.5 W
	low	X	5	35.6…45 W

The MPS timing is the same for dual-signature PDs and can be retrieved from Table 3 based on the LCF output.

The MPS current threshold however is always 10 mA for dual-signature PDs (on each pairset), even if assigned to Class 5.

Dual-signature PDs never have Autoclass implemented, so ACS should be connected to VPN.

Reference

All information regarding Power over Ethernet over 4 Pairs can be found in document IEEE 802.3bt™−2018 which is an amendment to IEEE Std 802.3™−2018.

SIMPLIFIED APPLICATION SCHEMATIC WITH AUXILIARY SUPPLY

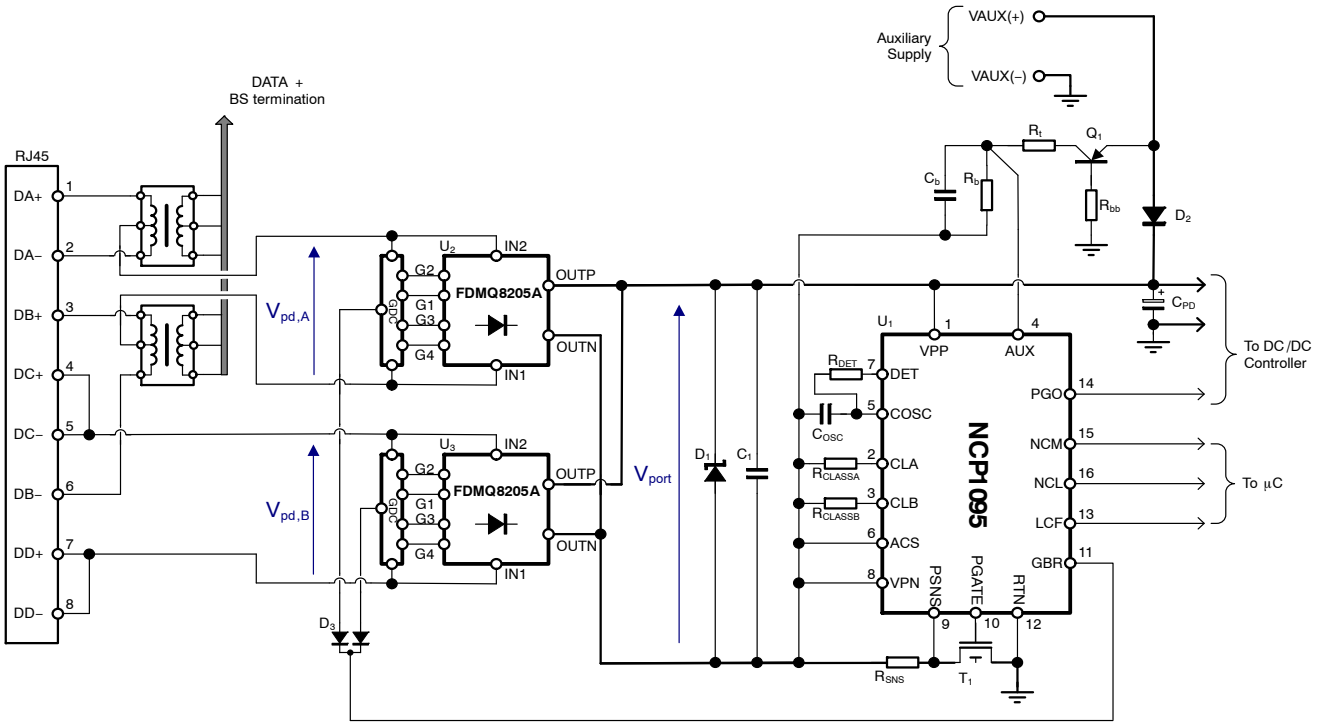


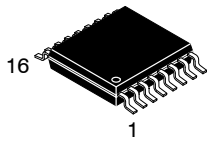
Figure 9. General Application Schematic with Auxiliary Supply

TYPICAL BILL OF MATERIALS

Reference designator	Description	Value (nominal)	Tolerance	Manufacturer	Part Number
U_1	PoE Interface	NCP1095		ON Semiconductor	NCP1095
U_2, U_3	GreenBridge™ Rectifier	FDMQ8205A		ON Semiconductor	FDMQ8205A
D1	TVS Protection	58 V		Littelfuse	SMBJ58A
C1	VPP decoupling capacitor	100 nF / 100 V	±10%	Walsin	0805B104K101CT
COSC	Oscillator capacitor	1 nF	±2%	Murata	GRM1885C1H102GA01D
CPD	VPP bulk capacitor	10 µF / 80 V	±20%	Panasonic	EEEFK1K100XP
RDET	Detection resistor	26.1 kΩ	±1%	Panasonic	ERJ3EKF2612V
RCLASSA	Classification resistor A	232 Ω	±1%	Panasonic	ERJ8ENF2320V
RCLASSB	Classification resistor B	332 Ω	±1%	Panasonic	ERJ6ENF3320V
RSNS	Current sense resistor	25 mΩ	±1%	Yageo	RL1206FR−070R025L
T1	Pass switch	100 V / 40 mΩ		ON Semiconductor	FDMC8622
D2	Schottky Rectifier	8 A / 60 V		ON Semiconductor	NRVTS860EMFS
D3	Dual Diode	100 V		ON Semiconductor	BAV70LT1G
Cb	AUX filter capacitor	47 pF	±5%	Yageo	CC0603JRNPO8BN470
Rt	AUX top resistor	33 kΩ	±1%	Panasonic	ERJ3EKF3302V
Rb	AUX bottom resistor	15 kΩ	±1%	Panasonic	ERJ3EKF1502V
Rbb	Base resistor	62 kΩ	±1%	Panasonic	ERJ3EKF6202V
Q1	PNP Transistor	80 V		ON Semiconductor	BC856BLT1G

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



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CASE 948F−01
ISSUE B

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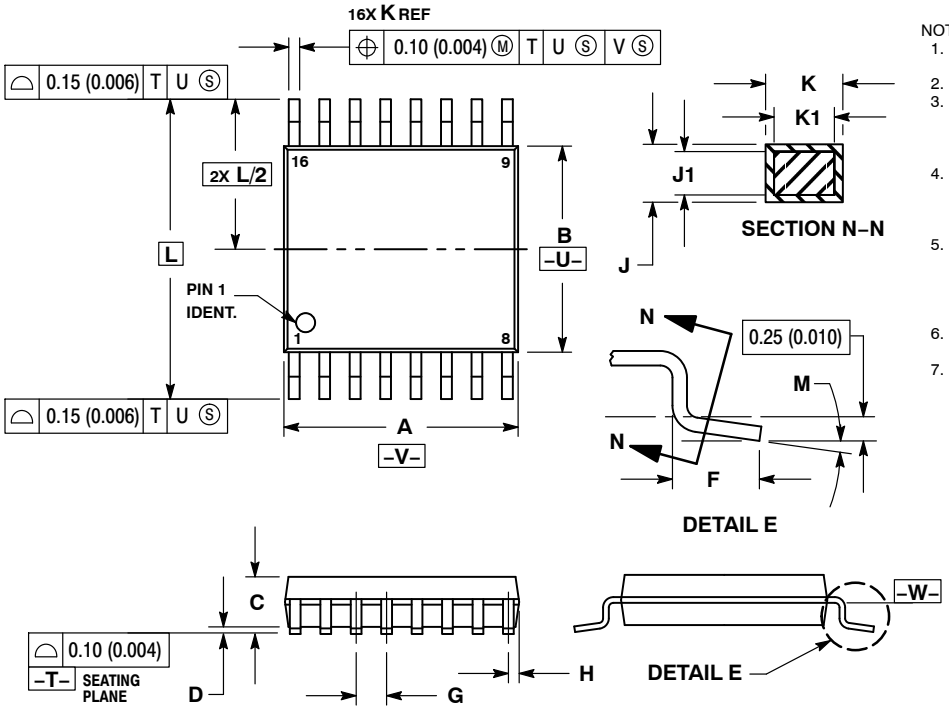
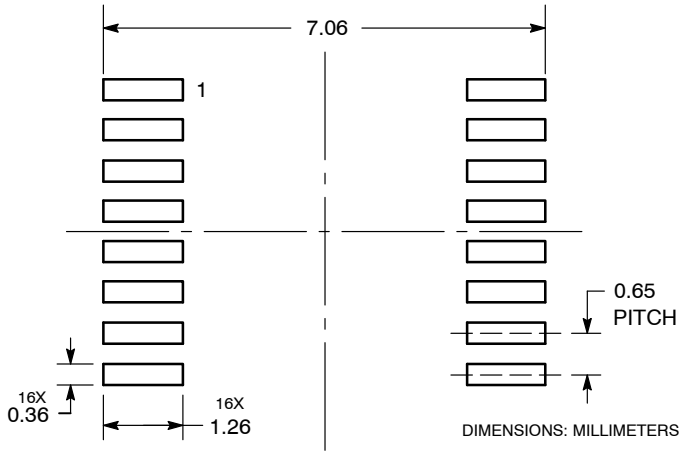


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

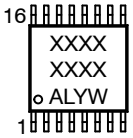
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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