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MAX77714

Complete System PMIC, Featuring 13 Regulators, 8 GPIOs, RTC, and Flexible Power Sequencing for Multicore Applications

General Description

The MAX77714 is a complete power-management IC (PMIC) for portable devices using System-on-Chip (SoC) applications processors.

Two 2A (SD2/3), one 3A (SD1), and one 4A (SD0) step-down regulator switch at 2MHz, allowing the use of small magnetic components. The output voltages for SD0 and SD1 are programmable from 0.26V to 1.52V in 10mV steps. The output voltage for SD2 is programmable from 0.6V to 2.194V in 6.5mV steps. The output voltage for SD3 is programmable from 0.6V to 3.78V in 12.5mV steps.

Nine low-dropout (LDO) linear regulators supply power to various system blocks. Each LDO features a programmable active-discharge circuit in shutdown. All LDOs feature two soft-start rates to limit inrush current during startup.

Eight programmable GPIOs can be programmed as general purpose inputs (GPI), general purpose outputs (GPO), or alternate modes for additional functionalities.

The real-time clock (RTC) with an external crystal oscillator provides time keeping and alarm wake-up functions. An internal silicon oscillator is available for systems that do not want to use the crystal oscillator. In addition, a watchdog timer is integrated for system monitoring purposes.

An integrated ON/OFF controller, in combination with flexible power sequencer (FPS), provides maximum flexibility in setting power-up/down sequences with minimal intervention from the applications processor.

The 70-bump, 4.1mm x 3.25mm x 0.7mm, 0.4mm pitch wafer-level package (WLP) is ideal for space constrained applications.

Factory-programmable options allow the MAX77714 to be tailored for many applications. Contact the factory for more information about programmable options; minimum order quantities may apply.

Applications

- Drones
- Smartphones/Tablet PCs
- Handheld Gaming Devices
- AR/VR Headsets
- Streaming Devices/Set-Top Boxes
- Home Automation Hubs
- Digital Cameras
- Automotive Aftermarket Accessories

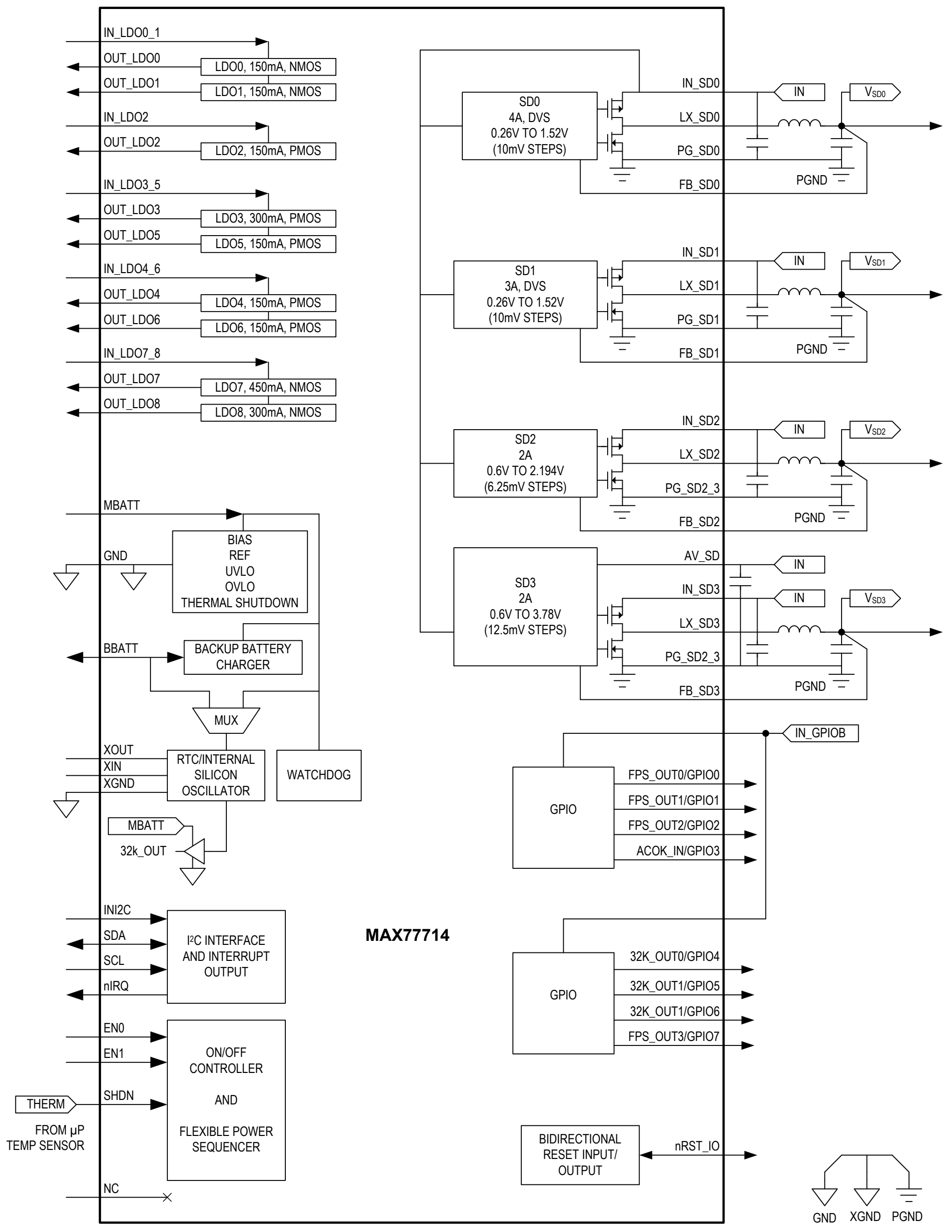
Benefits and Features

- Highly Integrated
  - 4x Buck Regulators
    - SD0/1 Peak Efficiency > 90% at $3.6V_{IN}$, $1.1V_{OUT}$
    - SD2/3 Peak Efficiency > 93% at $3.6V_{IN}$, $1.8V_{OUT}$
    - Supports LDDR4x Memory requirements
  - 9x Low-Dropout Linear Regulator
  - Eight GPIOs
  - Real-Time Clock
  - Backup Battery Charger
  - Bidirectional Reset I/O
  - Interrupt Output
  - System Watchdog Timer
- Flexible and Configurable
  - I^2C-Compatible Interface
  - Factory OTP Options Available
  - Flexible Power Sequencer
  - Configurable Power-Up/Power-Down/Sleep Mode Entry/Exit Timing
  - Highly Configurable GPIO ALT Modes
    - Three Resources Can Be Configured as 32kHz Oscillator Output
    - Four Resources Can Be Configured on FPS
    - One Resource Can Be Configured as ACOK Input
- Low Power
  - Low I_Q of 85μA in Sleep Mode
  - SD0/1 Low-Power Quiescent Current is 10μA
  - SD2/3 Low-Power Quiescent Current is 5μA
  - LDO Low-Power Quiescent Current is 1.5μA
- Small Size
  - 70-Bump, 0.4mm Pitch, 10x7 Ball Array WLP, 4.1mm x 3.25mm x 0.7mm Package Size
  - $230mm^2$ Total Solution Size

Ordering Information appears at end of data sheet.

19-100241; Rev 2; 2/22

Simplified Block Diagram



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Absolute Maximum Ratings

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- EN0 to GND .... -0.3V to V_{MBATT} + 0.3V
- EN1 to GND .... -0.3V to V_{MBATT} + 0.3V
- SHDN to GND .... -0.3V to V_{MBATT} + 0.3V
- nRST_IO to GND .... -0.3V to V_{MBATT} + 0.3V
- nIRQ to GND .... -0.3V to V_{INI2C} + 0.3V
- XOUT to XGND (Note1) .... -0.3V to VRTC + 0.3V
- XIN to XGND (Note 1) .... -0.3V to VRTC + 0.3V
- BBATT to GND .... -0.3V to +6.0V
- MBATT to GND .... -0.3V to +6.0V
- nRST_IO Sink Current 20mA
- nIRQ Sink Current 20mA
- DGND to GND .... -0.3V to +0.3V
- XGND to GND .... -0.3V to +0.3V

LDO
- IN_LDO0_1 to GND .... -0.3V to +6.0V
- OUT_LDO0 to GND .... -0.3V to V_{IN_LDO0-1} + 0.3V
- IN_LDO2 to GND .... -0.3V to +6.0V
- OUT_LDO1 to GND .... -0.3V to V_{IN_LDO0-1} + 0.3V
- IN_LDO3_5 to GND .... -0.3V to +6.0V
- OUT_LDO2 to GND .... -0.3V to V_{IN_LDO2} + 0.3V
- IN_LDO4_6 to GND .... -0.3V to +6.0V
- OUT_LDO3 to GND .... -0.3V to V_{IN_LDO3-5} + 0.3V
- IN_LDO7_8 to GND .... -0.3V to +6.0V
- OUT_LDO4 to GND .... -0.3V to V_{IN_LDO4-6} + 0.3V
- OUT_LDO5 to GND .... -0.3V to V_{IN_LDO3-5} + 0.3V
- OUT_LDO6 to GND .... -0.3V to V_{IN_LDO4-6} + 0.3V
- OUT_LDO7 to GND .... -0.3V to V_{IN_LDO7-8} + 0.3V
- OUT_LDO8 to GND .... -0.3V to V_{IN_LDO7-8} + 0.3V

Step-Down
- IN_SD0 to PG_SD0 .... -0.3V to +6.0V
- IN_SD1 to PG_SD1 .... -0.3V to +6.0V
- IN_SD2 to PG_SD2 .... -0.3V to +6.0V
- LX_SD0 to PG_SD0 (Note 1) .... -0.3V to V_{IN_SD0} + 0.3V
- LX_SD1 to PG_SD1 (Note 1) .... -0.3V to V_{IN_SD1} + 0.3V
- LX_SD2 to PG_SD2 (Note 1) .... -0.3V to V_{IN_SD2} + 0.3V
- LX_SDx RMS Current per Bump (T_J = +110°C) (RMS Current per Pin (T_J = +110°C)) 1.6A
- FB_SD0/1 to GND .... -0.3V to V_{MBATT} + 0.3V
- PG_SDx to GND .... -0.3V to +0.3V
- IN_SD3 to PG_SD3 .... -0.3V to +6.0V
- LX_SD3 to PG_SD3 (Note 1) .... -0.3V to V_{IN_SD3} + 0.3V
- FB_SD2 to GND .... -0.3V to V_{IN_SD2} + 0.3V
- FB_SD3 to GND .... -0.3V to V_{IN_SD3} + 0.3V

I^2C
- SDA, SCL to GND .... -0.3V to V_{INI2C} + 0.3V
- SDA Sink Current 25mA

GPIO
- GPIO_INB to GND .... -0.3V to +6.0V
- GPIO4-7 to GND .... -0.3V to V_{GPIO_INB} + 0.3V
- GPIO0-3 to GND .... -0.3V to V_{MBATT} + 0.3V
- GPIOx Source Current 12mA
- GPIOx Sink Current 20mA

Operating Temperature Range .... -40°C to +85°C
Junction Temperature .... +150°C
Storage Temperature Range .... -40°C to +150°C
Soldering Temperature (reflow) .... +260°C

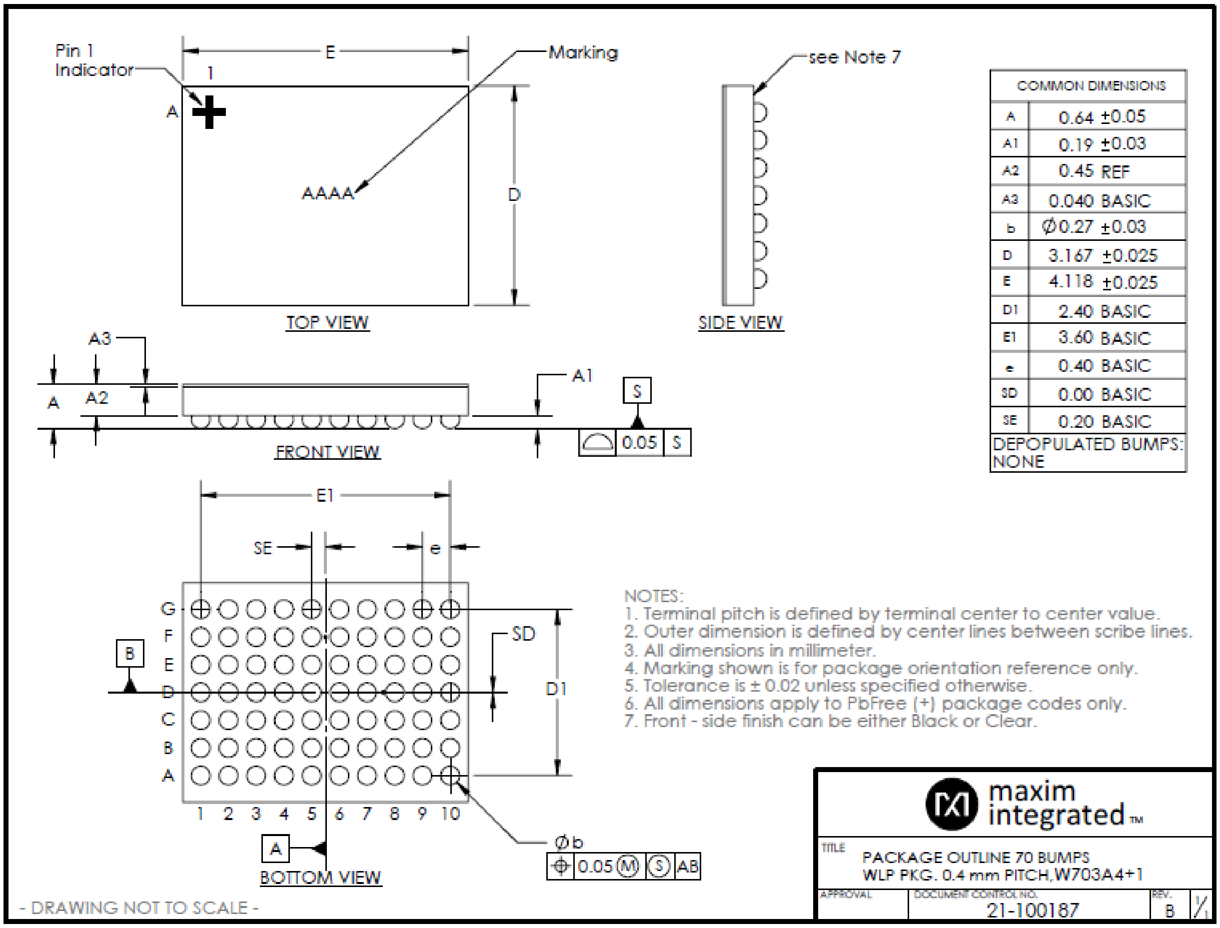
Note 1: The specified voltage limitation is for steady state conditions. Dead times of a few nano seconds exist as the dynamic step-down regulator transitions from inductor charging to inductor discharging and vice versa. These dead times allow internal clamping diodes to PGNDx and INBx to forward bias (Vf~1V). When the LXx waveform is observed on a high-bandwidth oscilloscope (≥ 100MHz), the LXx transition edges are commonly seen with 1.5V spikes. These spikes are due to (1) the internal clamping diode forward voltage and (2) the high rate of current change through the current loop's inductance (V = L x di/dt). Designs must follow the recommended printed circuit board (PCB) layout in order to minimize this current loop's inductance.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	W703A4+1
Outline Number	21-100187
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	37.43˚C/W
Junction to Case (θ_{JC})	NA



For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics—Global Resources

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +85°C) and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

<table>
<tr><th>PARAMETER</th><th>SYMBOL</th><th colspan="2">CONDITIONS</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNITS</th></tr>
<tr><td colspan="8">MAIN BATTERY POWER INPUT (MBATT)</td></tr>
<tr><td>MBATT Operating Voltage Range</td><td>V_{MBATT}</td><td colspan="2"></td><td>2.6</td><td></td><td>5.5</td><td>V</td></tr>
<tr><td>MBATT Undervoltage-Lockout Threshold</td><td>$V_{MBATTUVLO}$</td><td colspan="2">V_{MBATT} falling, 200mV hystersis</td><td></td><td>2.5</td><td></td><td>V</td></tr>
<tr><td>MBATT Overvoltage Lockout Threshold</td><td>$V_{MBATTOVLO}$</td><td colspan="2">V_{MBATT} rising, 200mV hysteresis</td><td>5.70</td><td>5.85</td><td>6.00</td><td>V</td></tr>
<tr><td rowspan="2">Quiescent Supply Current</td><td rowspan="2">I_{Q_MBATT}</td><td colspan="2">All regulators off, 32kHz oscillator in low-power mode (PWR_MD_32k = 0b1), V_{MBATT} = 3.6V, I_{BBATT} = 0μA</td><td>0.8</td><td>12</td><td>25</td><td rowspan="2">μA</td></tr>
<tr><td colspan="2">All regulators off, 32kHz oscillator in low-power mode (PWR_MD_32k = 0b1), internal reference and bias circuitry active (L_B_EN = 1), V_{MBATT} = 3.6V, I_{BBATT} = 0μA</td><td></td><td>42</td><td></td></tr>
<tr><td rowspan="2">No-Load LDO Supply Current</td><td rowspan="2"></td><td rowspan="2">Current into MBATT and all LDO power inputs, V_{MBATT} = 3.6V. All LDO power inputs are 3.6V, I_{BBATT} = 0μA, LDOs set to minimum output voltage, all step-down regulators disabled, 32kHz clock buffer disabled, 32kHz oscillator in low-power mode (PWR_MD_32k = 0b1), V_{IN_GPIOB} = 0V. This does not include any current into nRST_IO or nIRQ</td><td>Normal-power mode, all LDOs enabled</td><td></td><td>265</td><td></td><td rowspan="2">μA</td></tr>
<tr><td>Low-power mode, LDO2-LDO6 enabled (PMOS)</td><td></td><td>58</td><td></td></tr>
</table>

Electrical Characteristics—Global Resources (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +85°C) and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
No-Load Step-Down Supply Current		Current into MBATT and all step-down power inputs, V_{MBATT} = 3.6V, all regulator inputs are 3.6V, I_{BBATT} = 0µA, all step-downs enabled with their minimum output voltages, all LDOs disabled, 32kHz clock buffer disabled, 32kHz oscillator in low-power mode (PWR_MD_32k = 0b01), V_{IN_GPIOB} = 0V. This does not include any current into nRST_IO or nIRQ	Normal-power mode, all step-down regulators enabled		145		µA
			Low-power mode, all step-down regulators enabled		82.5		

Electrical Characteristics—Global Resources (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +85°C) and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
No-Load LDO and Step-Down Supply Current		Current into MBATT all step-down power inputs, and all LDO power inputs, V_{MBATT} = 3.6V, all regulator inputs are 3.6V, I_{BBATT} = 0µA, all regulators set to minimum output voltage. 32kHz clock buffer disabled, 32kHz oscillator in low-power mode (PWR_MD_32k = 0b01), V_{IN_GPIOB} = 0V. This does not include any current into nRST_IO or nIRQ	Normal-power mode, all regulators enabled		375	520	µA
		Current into MBATT all step-down power inputs, and all LDO power inputs, VMBATT = 3.6V, all regulator inputs are 3.6V, IBBATT = 0µA, all regulators set to minimum output voltage. 32kHz clock buffer disabled, 32kHz oscillator in low-power mode (PWR_MD_32k = 0b01), VIN_GPIOB = 0V. This does not include any current into nRST_IO or nIRQ	Low-power mode, all regulators except LDO0/1/7/8 (NMOS)		110	165	

Electrical Characteristics—Global Resources (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +85°C) and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MBATT RESET COMPARATOR						
Reset Falling Threshold Range	V_{MBATT_RESET}	MBATT_RESET[2:0] = 0b000		2.7		V
		MBATT_RESET[2:0] = 0b001		2.8		
		MBATT_RESET[2:0] = 0b010		2.9		
		MBATT_RESET[2:0] = 0b011	2.95	3.0	3.05	
		MBATT_RESET[2:0] = 0b100		3.1		
		MBATT_RESET[2:0] = 0b101		3.2		
		MBATT_RESET[2:0] = 0b110		3.3		
		MBATT_RESET[2:0] = 0b111		3.4		
Reset Threshold Hysteresis	$V_{MBATT\_RESET\_HYS}$	MBATT_HYS[1:0] = b00		0.1		V
		MBATT_HYS[1:0] = 0b01		0.2		
		MBATT_HYS[1:0] = 0b10		0.3		
		MBATT_HYS[1:0] = 0b11		0.4		
BIDIRECTIONAL RESET INPUT/OUTPUT (nRST_IO)						
Reset Output Deassert Delay Time	t_{RST_O}	OTP_TRSTO[1:0] = 0b00	0.8	1.0	1.2	ms
		OTP_TRSTO[1:0] = 0b01		8		
		OTP_TRSTO[1:0] = 0b10		32		
		OTP_TRSTO[1:0] = 0b11		64		
Reset Input Debounce Timer	$t_{DBNC\_nRST\_IO}$		24	30	36	ms
Input High Voltage	V_{IH}	RSO = 0	1.4			V
Input Low Voltage	V_{IL}	RSO = 0			0.4	V
Input Hysteresis	V_{HYS}	RSO = 0		50		mV
Input Leakage Current		V_{MBATT} = 5.5V, V_{nRST_IO} = 0V and 5.5V, RSO = 0, T_A = +25°C		0.001	1	µA
		V_{MBATT} = 5.5V, V_{nRST_IO} = 0V and 5.5V, RSO = 0, T_A = +85°C		0.01		
Output Voltage Low	V_{OL}	I_{SINK} = 4mA, RSO = 1			0.4	V
Output High Leakage Current		V_{MBATT} = 5.5V, V_{nRST_IO} = 0V and 5.5V, RSO = 0, T_A = +25°C		0.001	1	µA
		V_{MBATT} = 5.5V, V_{nRST_IO} = 0V and 5.5V, RSO = 0, T_A = +85°C		0.01		
DEDICATED ACTIVE-LOW OPEN-DRAIN OUTPUTS (nIRQ)						
Output Voltage Low	V_{OL}	I_{SINK} = 4mA, RSO = 1			0.4	V
Output High Leakage Current	I_{OZH}	V_{MBATT} = 5.5V, V_{nIRQ} = 0V and 5.5V, RSO = 0, T_A = +25°C		0.001	1	µA
		V_{MBATT} = 5.5V, V_{nIRQ} = 0V and 5.5V, RSO = 0, T_A = +85°C		0.01		
THERMAL ALARM AND SHUTDOWN						
Thermal Alarm 1	T_{J110}	T_J rising, +5°C hysteresis		110		°C

Electrical Characteristics—Global Resources (continued)

(Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +85°C) and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Alarm 2	T_{J130}	T_J rising, +5°C hysteresis		130		°C
Thermal Shutdown Temperature	T_{JSHDN}	T_J rising, +10°C hysteresis		145		°C
BACKUP-BATTERY POWER INPUT						
BBATT Current	I_{BBATT}	V_{MBATT} = 0V, PWR_MD_32k = 0b0; V_{BBATT} = 3.00V		4.2	8	µA

Electrical Characteristics—ON/OFF Controller

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ON/OFF CONTROLLER						
Input Voltage High	V_{IH}		1.4			V
Input Voltage Low	V_{IL}				0.4	V
Input Hysteresis	V_{HYS}			0.05		V
Manual Reset Time	t_{HRDRST}	MRT[2:0] = 0b000		2		s
		MRT[2:0] = 0b001		3		
		MRT[2:0] = 0b010		4		
		MRT[2:0] = 0b011		5		
		MRT[2:0] = 0b100		6		
		MRT[2:0] = 0b101		8		
		MRT[2:0] = 0b110		10		
		MRT[2:0] = 0b111		12		
Manual Reset Warning Time (MRWRN)	t_{MRWRN}	MRT[2:0] = 0b000		2		s
		MRT[2:0] = 0b001		2		
		MRT[2:0] = 0b010		3		
		MRT[2:0] = 0b011		4		
		MRT[2:0] = 0b100		5		
		MRT[2:0] = 0b101		6		
		MRT[2:0] = 0b110		8		
		MRT[2:0] = 0b111		10		

Electrical Characteristics—Flexible Power Supply (FPS)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FLEXIBLE POWER SEQUENCE						
Flexible Power Sequencer Enable Delay	t_{FSDON}	MAX77714 reference is already powered up prior to the enable command		91.5		µs
Flexible Power Sequencer Disable Delay	$t_{FPSDOFF}$			152		µs
Flexible Power Sequencer Event Period	t_{FST}	MSTR_PU[2:0], MSTR_PD[2:0] = 0b000		31		µs
		MSTR_PU[2:0], MSTR_PD[2:0] = 0b001		63		
		MSTR_PU[2:0], MSTR_PD[2:0] = 0b010		127		
		MSTR_PU[2:0], MSTR_PD[2:0] = 0b011		256		
		MSTR_PU[2:0], MSTR_PD[2:0] = 0b100		508		
		MSTR_PU[2:0], MSTR_PD[2:0] = 0b101		984		
		MSTR_PU[2:0], MSTR_PD[2:0] = 0b110		1936		
		MSTR_PU[2:0], MSTR_PD[2:0] = 0b111		3904		
Flexible Power Sequencer Event Period Timer Accuracy		Accuracy of the flexible power sequencer clock	-15		+15	%

Electrical Characteristics—Step-Down Regulators (SD0–4A Output)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE AND CURRENT						
Input Voltage Range	V_{INSD0}		2.6		5.5	V
OUTPUT VOLTAGE						
Output Voltage Range	V_{OUT_SD0}	I^2C programmable in 10mV steps (SD0VOUT[6:0] = 0x01 to 0x7F)	0.26		1.52	V
Output Voltage Accuracy	$V_{OUT\_ACC\_NM\_SD0}$	FPWM mode, normal-power mode, no load, T_A = +25°C, V_{OUT_SD0} = 1.0V	-2		+2	%
	$V_{OUT\_ACC\_LPM\_SD0}$	Low-power mode, no load, T_A = +25°C, V_{OUT_SD0} = 1.000V	-4		+4	
PERFORMANCE						
Switching Frequency	f_{SW}	V_{SYS} = 3.6V	1.8	2	2.2	MHz
Line Regulation		V_{INSD0} = 2.6V to 5.5V, V_{OUT_SD0} = 1.0V		0.2		%/V
Soft-Start Slew Rate		SD0_SSRAMP = 0		2.5		mV/µs
		SD0_SSRAMP = 1		10		
Output Voltage Ramp-Up/Down Slew Rate (DVS)				10		mV/µs

Electrical Characteristics—Step-Down Regulators (SD0–4A Output) (continued)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PMOS ON Resistance	R_{ON_PCH}	V_{SYS} = V_{IN_SD0} = 5V, I_{OUT} = 150mA		38	60	mΩ
		V_{SYS} = V_{IN_SD0} = 3.6V, I_{OUT} = 150mA		48	60	
NMOS ON Resistance	R_{ON_NCH}	V_{SYS} = V_{IN_SD0} = 5V, I_{OUT} = 150mA		18	40	mΩ
		V_{SYS} = V_{IN_SD0} = 3.6V, I_{OUT} = 150mA		24	40	
NMOS Zero-Crossing Threshold	I_{ZX_SKIP}	SKIP mode		20		mA
	I_{ZX_PWM}	Low-power mode		20		
LX Leakage	$I_{L\_LX\_25C}$	V_{LXSD0} = 5.5V or 0V, T_A = +25°C		0.1	1	µA
	$I_{L\_LX\_85C}$	V_{LXSD0} = 5.5V or 0V, T_A = +85°C (Note 2)		1		
Output Active Discharge Resistance	R_{DISCHG_SD0}	Resistance from FBB0 to PGND0, output disabled		100		Ω
Turn-On Delay Time	$t_{ON\_DLY\_SD0}$	EN signal to LX switching with bias on		200		µs
OUTPUT CURRENT						
Maximum Output Current	$I_{OUT\_MAX\_NM\_SD0}$	RMS, normal mode	4000			mA
PMOS Peak Current Limit	I_{LIMP}	T_A= +25°C	4825	5250	5675	mA
		T_A = -40°C to +85°C	4825	5250	5675	
NMOS Valley Current Limit	I_{LIMV}			3000		mA
NMOS (Negative) Current Limit	I_{LIMN}			2000		mA
BROWNOUT COMPARATOR						
Output-Brownout Threshold	V_{BO_SD0}	Normal-power mode, falling threshold, SD0_BO_THR[1:0] = 0b00		77		%
		Normal-power mode, falling threshold, SD0_BO_THR[1:0] = 0b01		81		
		Normal-power mode, falling threshold, SD0_BO_THR[1:0] = 0b10		85.7		
		Normal-power mode, falling threshold, SD0_BO_THR[1:0] = 0b11		91		
Output-Brownout Accuracy		Normal-power mode. V_{OUT_SD0} = 1.0V (SD0_VOUT[6:0])	-4.5		+4.5	%
Output-Brownout Threshold (Low-Power Mode)	V_{BO_SD0}	Falling threshold, low-power mode		86.0		%
Output-Brownout Accuracy		Low-power mode. V_{OUT_SD0} = 1.0V (SD0_VOUT[6:0])	-4		+4	%
Output-Brownout Hysteresis Range	$V_{BO\_HYS\_SD0}$	2-Bit control over I^2C. Max rising threshold limited to 96%	5		20	%
Brownout-Voltage Hysteresis Programming Step Size		Programmable with SD0_BO_HYS[1:0]		5		%

Electrical Characteristics—Step-Down Regulators (SD0–4A Output) (continued)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output-Brownout Hysteresis (Low-Power Mode)	$V_{BO\_HYS\_SD0\_LPM}$			5		%
OV COMPARATOR						
Output OV Trip Level	$V_{OUT\_SD0\_OV}$	Rising edge, SD0_OV_THR = 1		117.1		%
Output OV Hysteresis		SD0_OV_THR = 1		8.6		%
Output OV Trip Level	$V_{OUT\_SD0\_OV}$	Rising edge, SD0_OV_THR = 0		108.5		%
Output OV Hysteresis		SD0_OV_THR = 0		3.9		%
Output OV Trip Level (Low-Power Mode)	$V_{OUT\_SD0\_OV}$	Rising edge, low-power mode		108.3		%
Output OV Hysteresis (Low-Power Mode)		Low-power mode		3.9		%

Note 2: Design guidance only and is not production tested.

Electrical Characteristics—Step-Down Regulators (SD1–3A Output)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE AND CURRENT						
Input Voltage Range	V_{IN_SD1}		2.6		5.5	V
OUTPUT VOLTAGE						
Output Voltage Range	V_{OUT_SD1}	I^2C programmable in 10mV steps (SD1VOUT[6:0] = 0x01 to 0x7F)	0.26		1.52	V
Output Voltage Accuracy	$V_{OUT\_ACC\_NM\_SD1}$	FPWM mode, normal mode, no load, T_A = +25°C, V_{OUT_SD1} = 1.0V	-2		+2	%
	$V_{OUT\_ACC\_LPM\_SD1}$	Low-power mode, no load, T_A = +25°C, V_{OUT_SD1} = 1.000V	-4		+4	
PERFORMANCE						
Switching Frequency	f_{SW}	V_{MBATT} = 3.6V	1.8	2	2.2	MHz
Line Regulation		V_{INSD1} = 2.6V to 5.5V, V_{OUT_SD1} = 1.0V		0.2		%/V
PMOS ON Resistance	R_{ON_PCH}	V_{MBATT} = V_{INSD1} = 5V, I_{OUT} = 150mA		45	90	mΩ
		V_{MBATT} = V_{INSD1} = 3.6V, I_{OUT} = 150mA		58	90	
NMOS ON Resistance	R_{ON_NCH}	V_{MBATT} = V_{INSD1} = 5V, I_{OUT} = 150mA		28	60	mΩ
		V_{MBATT} = V_{INSD1} = 3.6V, I_{OUT} = 150mA		35	60	
NMOS Zero-Crossing Threshold	I_{ZX_SKIP}	Skip mode		20		mA
	I_{ZX_PWM}	Low-power mode		20		
LX Leakage	$I_{L\_LX\_25C}$	V_{LXSD1} = 5.5V or 0V, T_A = +25°C		0.1	1	µA
	$I_{L\_LX\_85C}$	V_{LXSD1} = 5.5V or 0V, T_A = +85°C (Note 3)		1		

Electrical Characteristics—Step-Down Regulators (SD1–3A Output) (continued)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Active Discharge Resistance	R_{DISCHG_SD1}	Resistance from FB_SD1 to PG_SD1, output disabled		100		Ω
Turn-On Delay Time	$t_{ON\_DLY\_SD1}$	EN signal to LX switching with bias on		200		µs
BROWNOUT COMPARATOR						
Output-Brownout Threshold	V_{BO_SD1}	Normal-power mode, falling threshold, SD1_BO_THR[1:0] = 0b00		77		%
		Normal-power mode, falling threshold, SD1_BO_THR[1:0] = 0b01		81		
		Normal-power mode, falling threshold, SD1_BO_THR[1:0] = 0b10		85.7		
		Normal-power mode, falling threshold, SD1_BO_THR[1:0] = 0b11		91		
Output-Brownout Accuracy		Normal-power mode. V_{OUT_SD1} = 1.0V (SD1_VOUT[6:0])	-4.5		+4.5	%
Output-Brownout Threshold (Low-Power Mode)	V_{BO_SD1}	Falling threshold, low-power mode		86.0		%
Output-Brownout Accuracy		Low-power mode, V_{OUT_SD1} = 1.0V (SD1_VOUT[6:0])	-4		+4	%
Output-Brownout Hysteresis Range	$V_{BO\_HYS\_SD1}$	2-Bit control over I^2C. Max rising threshold limited to 96%	5		20	%
Brownout-Voltage Hysteresis Programming Step Size		Programmable with SD1_BO_HYS[1:0]		5		%
Output-Brownout Hysteresis (Low-Power Mode)	$V_{BO\_HYS\_SDx\_LPM}$			5		%
OUTPUT CURRENT						
Maximum Output Current	$I_{OUT\_MAX\_NM\_SD1}$	RMS, normal mode	3000			mA
PMOS Peak Current Limit	I_{LIMP}	T_A = +25°C	3825	4250	5100	mA
		T_A = -40°C to +85°C	3825	4250	5200	
NMOS Valley Current Limit	I_{LIMV}			3000		mA
NMOS (Negative) Current Limit	I_{LIMN}			2000		mA
OV COMPARATOR						
Output OV Trip Level	V_{OUTSD1_OV}	Rising edge, SD1_OV_THR = 1		117.1		%
Output OV Hysteresis		SD1_OV_THR = 1		8.6		%
Output OV Trip Level	V_{OUTSD1_OV}	Rising edge, SD1_OV_THR = 0		108.5		%
Output OV Hysteresis		SD1_OV_THR = 0		3.9		%
Output OV Trip Level (Low-Power Mode)	V_{OUTSD1_OV}	Rising edge, low-power mode		108.3		%

Electrical Characteristics—Step-Down Regulators (SD1–3A Output) (continued)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output OV hysteresis (Low-Power Mode)		Low-power mode		3.9		%

Note 3: Design guidance only and is not production tested.

Electrical Characteristics—Step-Down Regulators (SD2/3–2A Output)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE AND CURRENT						
Input Voltage Range	V_{IN_SDx}		2.6		5.5	V
OUTPUT VOLTAGE						
Output Voltage Range	V_{OUT_SD2}	Programmable in 6.25mV steps with SD2VOUT[7:0]	0.600		2.194	V
	V_{OUT_SD3}	Programmable in 12.5mV steps with SD3VOUT[7:0]	0.600		3.78	
Output Voltage Accuracy	$V_{OUT\_ACC\_NM\_SD2}$	FPWM mode, normal-power mode, no load, V_{OUT_SD2} = 1.1V	-2		+2	%
	$V_{OUT\_ACC\_LPM\_SD2}$	Low-power mode, no load, V_{OUT_SD2} = 1.1V	-4		+4	
	$V_{OUT\_ACC\_NM\_SD3}$	FPWM mode, normal mode, no load, V_{OUT_SD3} = 1.1V	-2		+2	
	$V_{OUT\_ACC\_LPM\_SD3}$	Low-power mode, no Load, V_{OUT_SD3} = 1.1V	-4		+4	
OUTPUT CURRENT						
Maximum Output Current	$I_{OUT\_MAX\_NM\_SD2\_3}$	RMS, normal mode, L = 1µH	2000			mA
PMOS Peak Current Limit	I_{LIMP}	V_{MBATT} = 3.6V	2300	2875	4200	mA
		V_{MBATT} = 5V	2300	2875	4200	
NMOS Valley Current Limit	I_{LIMV}	V_{SYS} = 3.6V		2125		mA
		V_{SYS} = 5V		2125		
NMOS Negative Current Limit	I_{LIMN}	V_{SYS} = 3.6V		800		mA
		V_{SYS} = 5V		800		
PERFORMANCE						
Line Regulation		V_{MBATT} = $V_{IN\_SD2\_3}$ = 2.6V to 5.5V		0.2		%/V
Switching Frequency	f_{SW}	V_{MBATT} = 3.3V	1.8	2	2.2	MHz
		V_{MBATT} = 5V	1.8	2	2.2	
Soft-Start Slew Rate		Fixed for SD2		6.5		mV/µs
		Fixed for SD3		17		
Output Voltage Ramp-Up Slew Rate		Fixed for SD2, 3 (Notes 4, 7, 8), C_{OUT} = 22µF		40		mV/µs

Electrical Characteristics—Step-Down Regulators (SD2/3–2A Output) (continued)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Ramp-Down Slew Rate		Fixed for SD2, 3 (Notes 4, 7), C_{OUT} = 22µF, SDxFPWMEN = 1 (x = 1, 2), no load		18		mV/µs
PMOS ON Resistance	R_{ON_PCH}	V_{SYS} = V_{IN_SDx} = 3.6V, I_{OUT} = 150mA		100	150	mΩ
		V_{SYS} = V_{IN_SDx} = 5V, I_{OUT} = 150mA,		100	150	
NMOS ON Resistance	R_{ON_NCH}	V_{SYS} = V_{IN_SDx} = 3.6V, I_{OUT} = 150mA		60	100	mΩ
		V_{SYS} = V_{IN_SDx} = 5V, I_{OUT} = 150mA		60	100	
NMOS Zero-Crossing Threshold	I_{ZX}	SKIP mode		20		mA
LX Leakage	$I_{L\_LX\_25C}$	V_{LX2_3} = 5.5V or 0V, T_A = +25°C		0.1	1	µA
	$I_{L\_LX\_85C}$	V_{LX2_3} = 5.5V or 0V, T_A = +85°C (Note 4)		1		
Output Active Discharge Resistance	R_{DISCHG_SDx}	Resistance from FBBx to PGNDx, output disabled, (Note 6)		100		Ω
Turn-On Delay Time	$t_{ON\_DLY\_SDx}$	EN Signal to LX Switching with Bias ON		30		µs
BROWNOUT COMPARATOR						
Output-Brownout Threshold	V_{BO_SDx}	Normal-power mode, falling threshold, SDx_BO_THR[1:0] = 0b00		75		%
		Normal-power mode, falling threshold, SDx_BO_THR[1:0] = 0b01		80		
		Normal-power mode, falling threshold, SDx_BO_THR[1:0] = 0b10		85		
		Normal-power mode, falling threshold, SDx_BO_THR[1:0] = 0b11		90		
Output-Brownout Accuracy		Normal-power mode. V_{OUT_SDx} = 1.0V (SDxVOUT[7:0])	-4		+4	%
Output-Brownout Threshold (Low-Power Mode)	V_{BO_SDx}	Falling threshold, low-power mode		86.0		%
Output-Brownout Accuracy		Low-power mode. V_{OUT_SDx} = 1.0V (SDxVOUT[7:0])	-4		+4	%
Output-Brownout Hysteresis Range	$V_{BO\_HYS\_SDx}$	2-Bit control over I^2C. Max rising threshold limited to 96%	5		20	%
Brownout-Voltage Hysteresis Programming Step Size		Programmable with SDx_BO_HYS[1:0]		5		%
Output-Brownout Hysteresis (Low-Power Mode)	$V_{BO\_HYS\_SDx\_LPM}$			5		%
OV COMPARATOR						
Output OV Trip Level	V_{OUTSDx_OV}	Rising edge, SDx_OV_THR = 1, referenced to output voltage setting		116.6		%
Output OV Hysteresis		SDx_OV_THR = 1		9.1		%

Electrical Characteristics—Step-Down Regulators (SD2/3–2A Output) (continued)

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output OV Trip Level	V_{OUTSDx_OV}	Rising edge, SDx_OV_THR = 0 referenced to output voltage setting		108.3		%
Output OV Hysteresis		SDx_OV_THR = 0		2.8		%
Output OV Trip Level (Low-Power Mode)	V_{OUTSDx_OV}	Rising edge, low-power mode		108.3		%
Output OV Hysteresis (Low-Power Mode)		Low-power mode		2.8		%

Note 4: Design guidance only and is not production tested.

Note 5: Individual step-down supply current is not production tested. It is covered by a combined test by turning on all step-down regulators.

Note 6: There is an n-channel MOSFET in series with the output active discharge resistance. This NMOS requires V_{SYS} > 1.2V to be enhanced.

Note 7: The ramp-down slew rate when the output voltage is decreased via I²C is a function of the negative current limit and the output capacitance. With no load, forced PWM mode, and 22µF output capacitor, the ramp-down slew rate is dv/dt = i / C = 0.4A / 22µF = 18mV/µs.

Note 8: DVS and soft-start ramp rates can be expected to vary by up to 30%.

Note 9: The input and output voltage range of SD2/3 ensure that the 90% duty cycle limitation can never practically be reached. Additionally, SD2/3 is capable of 100% duty cycle for output voltages above 1.9V.

Electrical Characteristics—150mA PMOS LDO (LDO2, LDO4, LDO5, LDO6)

(V_{SYS} = 3.7V, V_{IN_LDO} = 3.7V, C_{IN_LDO} = 1µF, C_{OUT_LDO} = 2.2µF. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range (T_A=-40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Input Voltage Range	V_{IN_LDOx}	Guaranteed by output accuracy		1.7		5.5	V
Undervoltage Lockout	V_{UVLOxx}	Rising, 100mV hysteresis			1.6	1.7	V
Output Voltage Range	V_{OUTxx}	V_{INxx} is the maximum of 3.7 or V_{OUT}+0.3V	50mV/step (6-bit), LDO2, LDO5, LDO6	0.8		3.95	V
			50mV step from 0.4V to 0.5V and 12.5mV step (7-bit), LDO4 from 0.5 to 1.275V	0.4		1.275	
Maximum Output Current	I_{MAXxx}	Guaranteed by output accuracy	Normal mode	150			mA
			Low-power mode		5		

Electrical Characteristics—150mA PMOS LDO (LDO2, LDO4, LDO5, LDO6) (continued)

(V_{SYS} = 3.7V, V_{IN_LDO} = 3.7V, C_{IN_LDO} = 1µF, C_{OUT_LDO} = 2.2µF. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range (T_A=-40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CORE PERFORMANCE SPECIFICATIONS							
Output Voltage Accuracy		Normal mode	V_{IN} = V_{NOM}+0.3V to 5.5V with 1.7V minimum, I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage	-3		+3	%
		LDO4 Normal mode	V_{IN} = V_{NOM}+0.3V to 5.5V with 1.7V minimum, I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage	-4.5		+4.5	
		Low-power mode	V_{IN} = V_{NOM}+0.3V to 5.5V with 1.7V minimum, I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage	-5		+5	
Load Regulation (Note 15)		Normal mode	I_{OUT} = 0.1mA to I_{MAX}, VIN = V_{NOM}+0.3V with 1.7V minimum V_{NOM} set to any voltage		0.05		%
		Low-power mode	I_{OUT} = 0.1mA to 5mA, V_{IN} = V_{NOM}+0.3V with 1.7V minimum, V_{NOM} set to any voltage		0.05		
Line Regulation (Note 15)		Normal mode	V_{IN} = V_{NOM}+0.3V to 5.5V with 1.7V minimum, I_{OUT} = 0.1mA, V_{NOM} set to any voltage		0.01		%/V
Line Regulation (Note15)		Low-power mode	V_{IN} = V_{NOM}+0.3 to 5.5V with 1.7V minimum. I_{OUT} = 0.1mA, V_{NOM} set to any voltage		0.01		%/V
Dropout Voltage	V_{DOxx}	Normal mode, I_{OUT} = I_{MAX}, LDO4 not tested	V_{IN} = 3.7V		50	100	mV
			V_{IN} = 1.7V		150	300	
		Low-power mode, I_{OUT} = 5mA, V_{IN} = 3.7V			150	300	
Output Current Limit	I_{LIMxx}	V_{OUT} = 0V, % of I_{MAX}		110	180	250	%

Electrical Characteristics—150mA PMOS LDO (LDO2, LDO4, LDO5, LDO6) (continued)

(V_{SYS} = 3.7V, V_{IN_LDO} = 3.7V, C_{IN_LDO} = 1µF, C_{OUT_LDO} = 2.2µF. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range (T_A=-40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS							
Soft-Start and Dynamic Voltage Change Ramp Rate	t_{SSxx}	After enabling, SS_Lx = 1 (Note 10)			5		mV/µs
		After enabling, SS_Lx = 0 (Note 10)			100		
Active Discharge Resistance		Output disabled, V_{OUT} = 1V, resistance from OUT_LDOx to GND, active discharge enabled (Lxx_ADE = 1)			65		Ω
THERMAL SHUTDOWN							
Thermal Shutdown		Output disabled or enabled	T_J rising		165		°C
			T_J falling		150		
POWER-OK COMPARATOR							
Power-OK Threshold	V_{POKTHL}	V_{OUT} when V_{POK} switches	V_{OUT} falling	84	87		%
			V_{OUT} rising		92	96	

Note 10: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Note 11: Does not include ESR of the capacitance or trace resistance of the PCB.

Electrical Characteristics—300mA PMOS LDO (LDO3)

(V_{SYS} = 3.7V, V_{IN_LDO} = 3.7V, C_{IN_LDO} = 1µF, C_{OUT_LDO} = 2.2µF. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Input Voltage Range	V_{IN_LDOx}	Guaranteed by output accuracy		1.7		5.5	V
Undervoltage Lockout	V_{UVLOxx}	Rising, 100mV hysteresis			1.6	1.7	V
Output Voltage Range	V_{OUTxx}	V_{INxx} is the maximum of 3.7 or V_{OUT}+0.3V	50mV/step (6-bit), LDO3	0.8		3.95	V
Maximum Output Current	I_{MAXxx}	Guaranteed by output accuracy	Normal mode	300			mA
			Low-power mode		5		
CORE PERFORMANCE SPECIFICATIONS							
Output Voltage Accuracy		Normal mode	V_{IN} = V_{NOM}+0.3V to 5.5V with 1.7V minimum, I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage	-3		+3	%
		Low-power mode	V_{IN} = V_{NOM}+0.3V to 5.5V with 1.7V minimum, I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage	-5		+5	

Electrical Characteristics—300mA PMOS LDO (LDO3) (continued)

(V_{SYS} = 3.7V, V_{IN_LDO} = 3.7V, C_{IN_LDO} = 1µF, C_{OUT_LDO} = 2.2µF. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Load Regulation (Note 15)		Normal mode	I_{OUT} = 0.1mA to I_{MAX}, VIN = V_{NOM}+0.3V with 1.7V minimum V_{NOM} set to any voltage		0.05		%
		Low-power mode	I_{OUT} = 0.1mA to 5mA, V_{IN} = V_{NOM}+0.3V with 1.7V minimum, V_{NOM} set to any voltage		0.05		
Line Regulation (Note 15)		Normal mode	V_{IN} = V_{NOM}+0.3V to 5.5V with 1.7V minimum, I_{OUT} = 0.1mA, V_{NOM} set to any voltage		0.01		%/V
Line Regulation (Note15)		Low-power mode	V_{IN} = V_{NOM}+0.3 to 5.5V with 1.7V minimum. I_{OUT} = 0.1mA, V_{NOM} set to any voltage		0.01		%/V
Dropout Voltage	V_{DOxx}	Normal mode, I_{OUT} = I_{MAX}	V_{IN} = 3.7V		50	100	mV
			V_{IN} = 1.7V		150	450	
		Low-power mode, I_{OUT} = 5mA, V_{IN} = 3.7V			150	300	
Output Current Limit	I_{LIMxx}	V_{OUT} = 0V, % of I_{MAX}		110	180	250	%
DYNAMIC CHARACTERISTICS							
Soft-Start and Dynamic-Voltage-Change Ramp Rate	t_{SSxx}	After enabling (Note 12)	SS_Lx = 1		5		mV/µs
		After enabling, (Note 12)	SS_Lx = 0		100		
Active Discharge Resistance		Output disabled, V_{OUT} = 1V, resistance from OUT_LDOx to GND, active discharge enabled (ADE_LX = 1)			65		Ω
THERMAL SHUTDOWN							
Thermal Shutdown		Output disabled or enabled	T_J rising		165		°C
			T_J falling		150		
POWER-OK COMPARATOR							
Power-OK Threshold	V_{POKTHL}	V_{OUT} when V_{POK} switches	V_{OUT} falling	84	87		%
			V_{OUT} rising		92	96	

Note 12: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Note 13: Does not include ESR of the capacitance or trace resistance of the PCB.

Electrical Characteristics—150mA NMOS LDO (LDO0, LDO1)

(V_{SYS} = 3.7V, V_{IN_LDO} = 3.7V, C_{IN_LDO} = 1μF, C_{OUT_LDO} = 2.2μF. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Input Voltage Range	V_{IN_LDOx}	Guaranteed by output accuracy		V_{OUT}		5.5	V
Output Voltage Range	V_{OUTxx}	V_{INxx} is the maximum of 3.7 or V_{OUT}+0.3V	25mV/step (6-bit), LDO0, LDO1	0.8		2.375	V
Maximum Output Current	I_{MAXxx}	Guaranteed by output accuracy	Normal mode	150			mA
			Low-power mode		5		
CORE PERFORMANCE SPECIFICATIONS							
Output Voltage Accuracy		Normal mode	V_{IN} = V_{NOM}+0.3V to 5.5V, I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage, V_{MBATT} = V_{NOM}+1.5V with 2.45V minimum	-3		+3	%
		Low-power mode	V_{IN} = V_{NOM}+0.3V to 5.5V, I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage, V_{MBATT} = V_{NOM}+1.5V with 2.45V minimum	-5		+5	
Load Regulation (Note 15)		Normal mode	I_{OUT} = 0.1mA to I_{MAX}, V_{IN} = V_{NOM}+0.3V, V_{MBATT} = V_{NOM}+1.5V with 2.45V minimum		0.05		%
		Low-power mode	I_{OUT} = 0.1mA to 5mA, V_{IN} = V_{NOM}+0.3V, V_{MBATT} = V_{NOM}+1.5V with 2.45V minimum		0.05		
Line Regulation (Note 15)		Normal mode	V_{IN} = V_{NOM}+0.3V to 5.5V, I_{OUT} = 0.1mA		0.01		%/V
Line Regulation (Note15)		Low-power mode	V_{MBATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{IN} = V_{NOM}+0.3V to 5.5V, I_{OUT} = 0.1mA		0.01		%/V

Electrical Characteristics—150mA NMOS LDO (LDO0, LDO1) (continued)

(V_{SYS} = 3.7V, V_{IN_LDO} = 3.7V, C_{IN_LDO} = 1μF, C_{OUT_LDO} = 2.2μF. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Dropout Voltage	V_{DOxx}	Normal mode, I_{OUT} = I_{MAX}	$V_{MBATT\text{-}VOUT}$ = 2.5V		50	100	mV
			V_{MBATT}-V_{OUT} = 1.7V		150	300	
		Low-power mode, I_{OUT} = 5mA, V_{IN} = 3.7V			150	300	
Output Current Limit	I_{LIMxx}	V_{OUT} = 0V, % of I_{MAX}		103	180	250	%
DYNAMIC CHARACTERISTICS							
Soft-Start and Dynamic-Voltage-Change Ramp Rate	t_{SSxx}	After enabling, (Note 14)	SS_Lx = 0		100		mV/μs
		After enabling (Note 14)	SS_Lx = 1		5		
Active Discharge Resistance		Output disabled, V_{OUT} = 1V, resistance from OUT_LDOx to GND, active discharge enabled (ADE_Lx = 1)			65		Ω
THERMAL SHUTDOWN							
Thermal Shutdown		Output disabled or enabled	T_J rising		165		°C
			T_J falling		150		
POWER-OK COMPARATOR							
Power-OK Threshold	V_{POKTHL}	V_{OUT} when V_{POK} switches	V_{OUT} falling	84	87		%
			V_{OUT} rising		92	96	

Note 14: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Note 15: Does not include ESR of the capacitance or trace resistance of the PCB.

Electrical Characteristics—300mA NMOS LDO (LDO8)

(V_{SYS} = 3.7V, V_{IN_LDO} = 3.7V, C_{IN_LDO} = 1μF, C_{OUT_LDO} = 2.2μF. Limits are 100% production tested at T_A = +25°C Limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Input Voltage Range	V_{IN_LDOx}	Guaranteed by output accuracy		V_{OUT}		5.5	V
Output Voltage Range	V_{OUTxx}	V_{INxx} is the maximum of 3.7 or V_{OUT}+0.3V	50mV/step (6-bit), LDO8	0.8		3.95	V
Maximum Output Current	I_{MAXxx}	Guaranteed by output accuracy	Normal mode	300			mA
			Low-power mode		5		

Electrical Characteristics—300mA NMOS LDO (LDO8) (continued)

(V_{SYS} = 3.7V, V_{IN_LDO} = 3.7V, C_{IN_LDO} = 1µF, C_{OUT_LDO} = 2.2µF. Limits are 100% production tested at T_A = +25°C Limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CORE PERFORMANCE SPECIFICATIONS							
Output Voltage Accuracy		Normal mode	V_{IN} = V_{NOM} + 0.3V to 5.5V, I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage, V_{MBATT} = V_{NOM} + 1.5V with 2.45V minimum	-3		+3	%
		Low-power mode	V_{IN} = V_{NOM} + 0.3V to 5.5V, I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage, V_{MBATT} = V_{NOM} + 1.5V with 2.45V minimum	-5		+5	
Load Regulation (Note 15)		Normal mode	I_{OUT} = 0.1mA to I_{MAX}, V_{IN} = V_{NOM}+0.3V, V_{MBATT} = V_{NOM}+1.5V with 2.45V minimum		0.05		%
		Low-power mode	I_{OUT} = 0.1mA to 5mA, V_{IN} = V_{NOM}+0.3V, V_{MBATT} = V_{NOM}+1.5V with 2.45V minimum		0.05		
Line Regulation (Note 15)		Normal mode	V_{IN} = V_{NOM}+0.3V to 5.5V, I_{OUT} = 0.1mA		0.01		%/V
Line Regulation (Note15)		Low-power mode	V_{MBATT} = V_{NOM} + 0.3V to 5.5V with 2.45V minimum, V_{IN} = V_{NOM} + 0.3V to 5.5V, I_{OUT} = 0.1mA		0.01		%/V
Dropout Voltage	V_{DOxx}	Normal mode, I_{OUT} = I_{MAX}	$V_{MBATT-VOUT}$ = 2.5V		50	100	mV
			V_{MBATT}-V_{OUT} = 1.7V		150	450	
		Low-power mode, I_{OUT} = 5mA, V_{IN} = 3.7V			150	300	
Output Current Limit	I_{LIMxx}	V_{OUT} = 0V, % of I_{MAX}		110	180	250	%
DYNAMIC CHARACTERISTICS							
Soft-Start and Dynamic-Voltage-Change Ramp Rate	t_{SSxx}	After enabling, (Note 16)	SS_Lx = 0		100		mV/µs
		After enabling (Note 16)	SS_Lx = 1		5		

Electrical Characteristics—300mA NMOS LDO (LDO8) (continued)

(V_{SYS} = 3.7V, V_{IN_LDO} = 3.7V, C_{IN_LDO} = 1µF, C_{OUT_LDO} = 2.2µF. Limits are 100% production tested at T_A = +25°C Limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Active Discharge Resistance		Output disabled, V_{OUT} = 1V, resistance from OUT_LDOx to GND, active discharge enabled (ADE_Lx = 1)			65		Ω
THERMAL SHUTDOWN							
Thermal Shutdown		Output disabled or enabled	T_J rising		165		°C
			T_J falling		150		
POWER-OK COMPARATOR							
Power-OK Threshold	V_{POKTHL}	V_{OUT} when V_{POK} switches	V_{OUT} falling	84	87		%
			V_{OUT} rising		92	96	

Note 16: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Note 17: Does not include ESR of the capacitance or trace resistance of the PCB.

Electrical Characteristics—450mA NMOS LDO (LDO7)

(V_{SYS} = 3.7V, V_{IN_LDO} = 3.7V, C_{IN_LDO} = 1µF, C_{OUT_LDO} = 2.2µF. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL CHARACTERISTICS							
Input Voltage Range	V_{IN_LDOx}	Guaranteed by output accuracy		V_{OUT}		5.5	V
Output Voltage Range	V_{OUTxx}	V_{INxx} is the maximum of 3.7 or V_{OUT}+0.3V	50mV/step (6-bit), LDO7	0.8		3.95	V
Maximum Output Current	I_{MAXxx}	Guaranteed by output accuracy	Normal mode	450			mA
			Low-power mode		5		
CORE PERFORMANCE SPECIFICATIONS							
Output Voltage Accuracy		Normal mode	V_{IN} = V_{NOM}+0.3V to 5.5V, I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage, V_{MBATT} = V_{NOM}+1.5V with 2.45V minimum	-3		+3	%
		Low-power mode	V_{IN} = V_{NOM}+0.3V to 5.5V, I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage, V_{MBATT} = V_{NOM}+1.5V with 2.45V minimum	-5		+5	

Electrical Characteristics—450mA NMOS LDO (LDO7) (continued)

(V_{SYS} = 3.7V, V_{IN_LDO} = 3.7V, C_{IN_LDO} = 1µF, C_{OUT_LDO} = 2.2µF. Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range (T_A = -40°C to +85°C) are guaranteed by design and characterization, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Load Regulation (Note 15)		Normal mode	I_{OUT} = 0.1mA to I_{MAX}, V_{IN} = V_{NOM}+0.3V, V_{MBATT} = V_{NOM}+1.5V with 2.45V minimum		0.05		%
		Low-power mode	I_{OUT} = 0.1mA to 5mA, V_{IN} = V_{NOM}+0.3V, V_{MBATT} = V_{NOM} + 1.5V with 2.45V minimum		0.05		
Line Regulation (Note 15)		Normal mode	V_{IN} = V_{NOM}+0.3V to 5.5V, I_{OUT} = 0.1mA		0.01		%/V
		Low-power mode	V_{MBATT} = V_{NOM}+0.3V to 5.5V with 2.45V minimum, V_{IN} = V_{NOM}+0.3V to 5.5V, I_{OUT} = 0.1mA		0.01		
Dropout Voltage	V_{DOxx}	Normal mode, I_{OUT} = I_{MAX}	$V_{MBATT-VOUT}$ = 2.5V		50	100	mV
			V_{MBATT}-V_{OUT} = 1.5V		150	450	
		Low-power mode, I_{OUT} = 5mA, V_{IN} = 3.7V			150	300	
Output Current Limit	I_{LIMxx}	V_{OUT} = 0V, % of I_{MAX}		110	180	250	%
DYNAMIC CHARACTERISTICS							
Soft-Start and Dynamic-Voltage-Change Ramp Rate	t_{SSxx}	After enabling, (Note 18)	SS_Lx = 0		100		mV/µs
		After enabling (Note 18)	SS_Lx = 1		5		
Active Discharge Resistance		Output disabled, V_{OUT}=1V, resistance from OUT_LDOx to GND, active discharge enabled (ADE_Lx = 1)			65		Ω
THERMAL SHUTDOWN							
Thermal Shutdown		Output disabled or enabled	T_J rising		165		°C
			T_J falling		150		
POWER-OK COMPARATOR							
Power-OK Threshold	V_{POKTHL}	V_{OUT} when V_{POK} switches	V_{OUT} falling	84	87		%
			V_{OUT} rising		92	96	

Note 18: Does not include ESR of the capacitance or trace resistance of the PCB.

Note 19: During a soft-start event or a DVS transition, the regulators output current increases by C_{OUT} x dV/dt. In the event that the load current plus the additional current imposed by the soft-start or DVS transition reach the regulator's current limit, the current limit is enforced. When the current limit is enforced, the advertised transition rate (dV/dt) does not occur.

Electrical Characteristics—GPIO

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Power-Supply Voltage	V_{MBATT}	GPIO0-3 (Note 20)		2.6		5.5	V
	V_{GPIO_INB}	GPIO4-7 (Note 20)		1.7		5.5	
Supply Current	I_{GPIO_INB}	GPIO configured as input and connected to ground				1	µA
GPIO INPUT							
Input Voltage Low	V_{IL}	GPIO0-3, V_{MBATT} = 2.6V to 5.5V GPIO4-7, V_{IN_GPIOB} = 1.7V to 5.5V				0.5	V
Input Voltage High	V_{IH}	GPIO0-3, V_{MBATT} = 2.6V to 5.5V		0.7 x V_{MBATT}			V
		GPIO4-7, V_{IN_GPIOB} = 1.7V to 5.5V		0.7 x V_{GPIO_INB}			
Input Hysteresis	V_{HYS_GPIO}				0.25		V
Input Leakage Current	I_{LKG_GPIOx}	V_{IN_GPIOB} = V_{MBATT} = 5.5V, VGPIOx = 0V and 5.5V, internal pull-up/down disabled	T_A = +25°C		0.001	1	µA
			T_A = +85°C		0.01		
GPIO OUTPUT							
Output Voltage Low	V_{OL}	I_{SINK} = 4mA, open-drain and push-pull mode				0.08	V
		I_{SINK} = 12mA, open-drain and push-pull mode				0.25	
Output Voltage High	V_{OH}	GPIO4-7	V_{IN_GPIOB} = 1.7V, I_{SOURCE} = 4mA	0.7 x V_{IN_GPIOB}			V
		GPIO0-3	V_{MBATT} = 3.6, I_{SOURCE} = 4mA	0.7 x V_{MBATT}			
GPIO Open Leakage Current		V_{IN_GPIOB} = V_{MBATT} = 5.5V	T_A = +25°C		0.01	1	µA
			T_A = +85°C		0.1		
INTERNAL RESISTANCE							
Pullup Resistance	R_{PU_GPIO}			50	100	160	kΩ
Pulldown Resistance	R_{PD_GPIO}			50	100	160	kΩ

Note 20: Guaranteed by V_{IH} and V_{IL} tests.

Electrical Characteristics—32kHz Oscillator

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CRYSTAL OSCILLATOR						
Crystal-Oscillator Supply Voltage	V_{RTC}	(Note 21)	1.71	2.5		V
Crystal Loading		32KLOAD = 0b01 (Note 22)		6.5		pF
		32KLOAD = 0b10 (Note 22)		7.5		
		32KLOAD = 0b11 (Note 22)		12.5		
BYPASS MODE						
XIN I/O Voltage	V_{RTC}	Maximum V_{RTC} external load of 1mA		V_{RTC}		V
XIN Input Low Voltage	V_{XIN_IL}		0		0.4	V
XIN Input High Voltage	V_{XIN_IH}		V_{RTC} - 0.4		V_{RTC}	V
XIN Input Hysteresis				400		mV
XIN Input Leakage Current		T_A = +25°C	-1		+1	µA
SILICON OSCILLATOR						
Silicon-Oscillator Supply Voltage	V_{RTC}		1.71	2.5		V
Silicon Oscillator Output Frequency				32768		Hz
VALID FREQUENCY DETECTOR						
Valid XOSCOK Signal Minimum Frequency	f_{DET_MIN}			10		kHz
Valid XOSCOK Signal Maximum Frequency	f_{DET_MAX}			110		kHz
OK32K Signal Debounce (Note 23)		Primary crystal oscillator (XOSCOK)		256		cycles
		Backup silicon oscillator (XOSCOK)		32		cycles

Note 21: Minimum supply for basic functionality with reduced accuracy.

Note 22: Includes 3pF of parasitic capacitance on XIN and XOUT.

Note 23: Number of valid cycles the frequency detector needs to count before it asserts OK32K.

Electrical Characteristics—Backup Battery Charger

(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
BACKUP BATTERY CHARGER							
Programmable Output Voltage Range		I_{LOAD} = 1µA	BBCVS[1:0] = 0x00	2.420	2.500	2.580	V
			BBCVS[1:0] = 0x01	2.910	3.000	3.090	
			BBCVS[1:0] = 0x02	3.200	3.300	3.400	
			BBCVS[1:0] = 0x03	3.395	3.500	3.605	

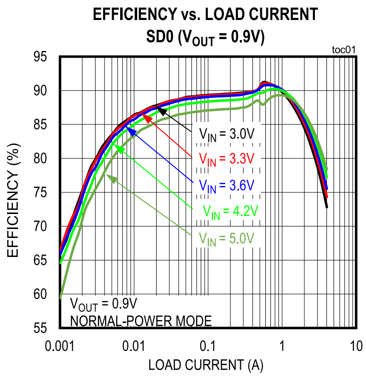
Electrical Characteristics—Backup Battery Charger (continued)

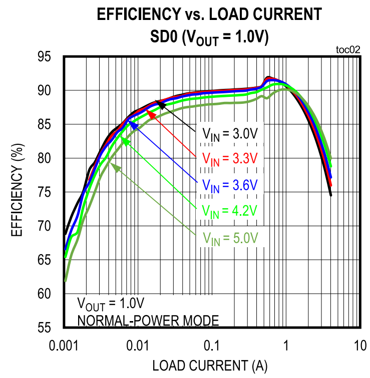
(V_{SYS} = 3.6V, T_A = -40°C to +85°C, limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked "GBD" are guaranteed by design and not production tested.)

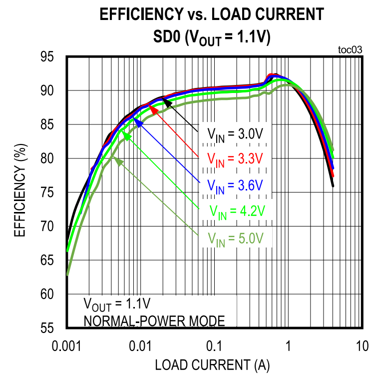
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Constant Current Limit		V_{BBATT} short to GND, BBCLOWIEN = 0	BBCCS[1:0] = 0x00, 0x01, 0x02		50		μA
			BBCCS[1:0] = 0x03		100		
		V_{BBATT} short to GND, BBCLOWIEN = 1	BBCCS[1:0] = 0x00		200		
			BBCCS[1:0] = 0x00		600		
			BBCCS[1:0] = 0x02		800		
			BBCCS[1:0] = 0x03		400		
Output Resistance		BBCRS[1:0] = 0x00			0.1		kΩ
		BBCRS[1:0] = 0x01			1		
		BBCRS[1:0] = 0x02			3		
		BBCRS[1:0] = 0x03			6		
Reverse Leakage Current from BBATT to VMBATT		Input = 0V, V_{BBATT} = 3.0V	T_A = +25°C		0.01	10	μA
			T_A = +85°C		0.1		

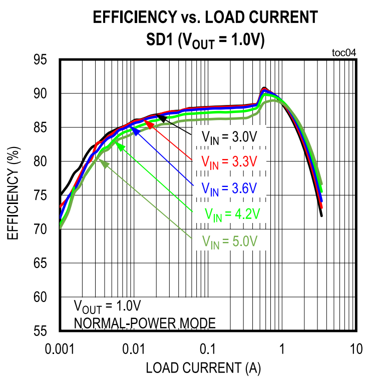
Typical Operating Characteristics

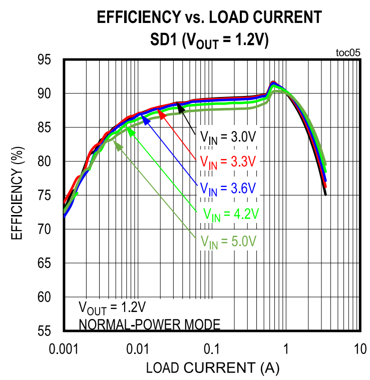
(AV_{DD} = +3.3V, V_{DDIO} = +1.8V, V_{REFP} - V_{REFN} = V_{REF} = 2.5V; No Line-Frequency Rejection, Continuous-Conversion Mode, Internal Clock; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

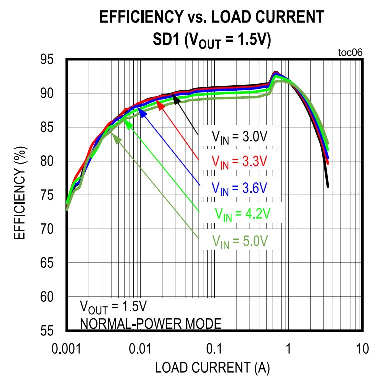


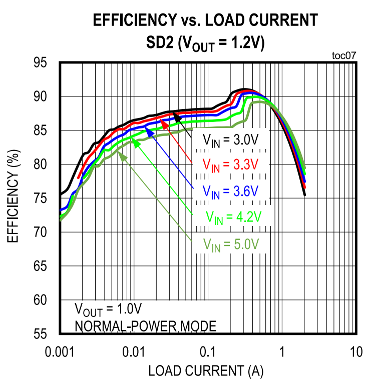


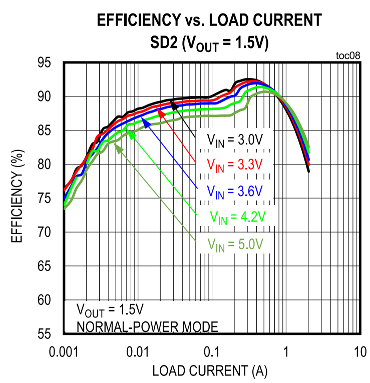


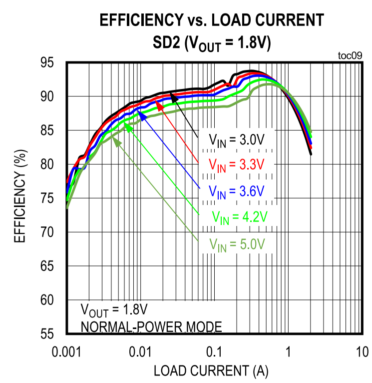






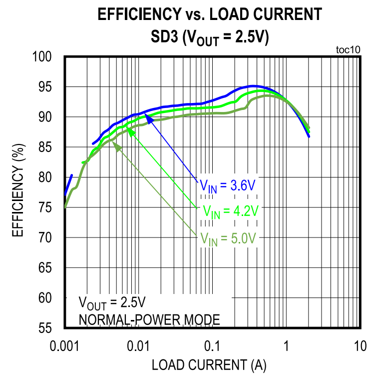


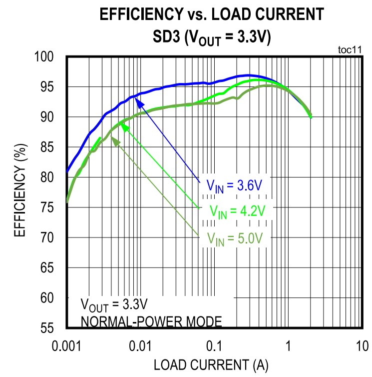


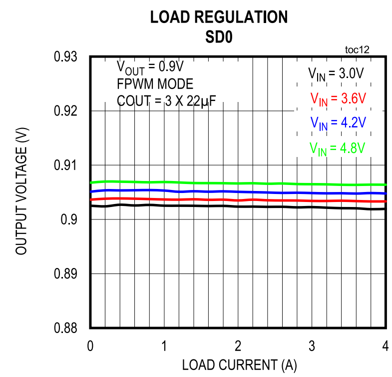


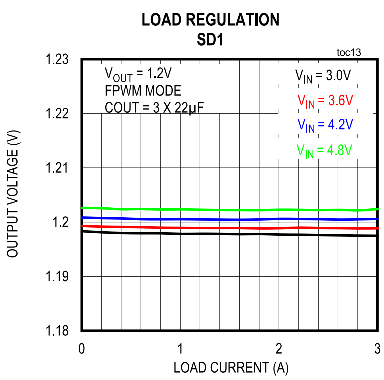
Typical Operating Characteristics (continued)

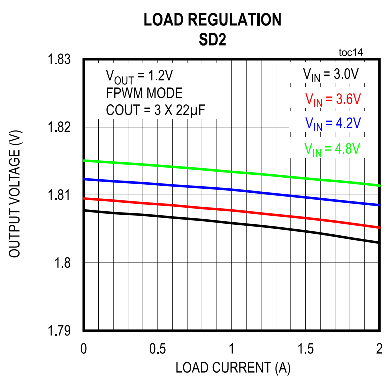
(AV_{DD} = +3.3V, V_{DDIO} = +1.8V, V_{REFP} - V_{REFN} = V_{REF} = 2.5V; No Line-Frequency Rejection, Continuous-Conversion Mode, Internal Clock; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

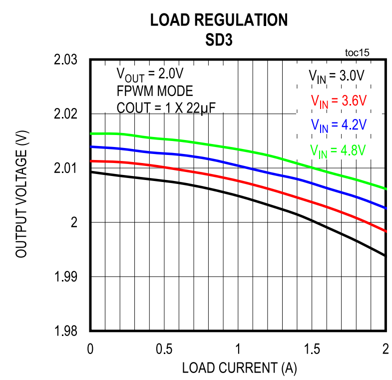


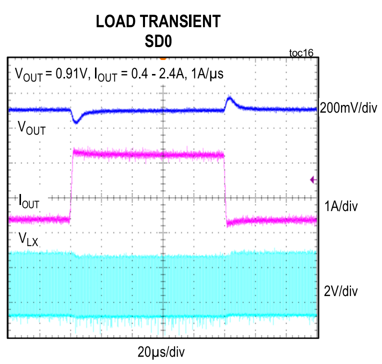


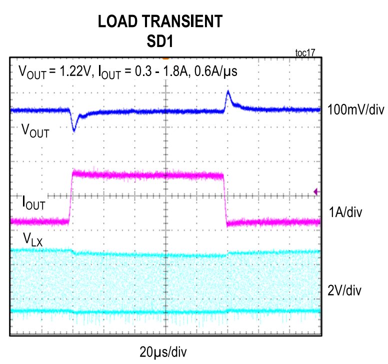


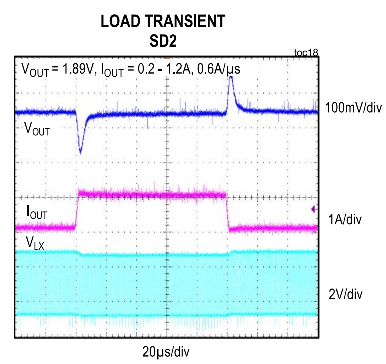






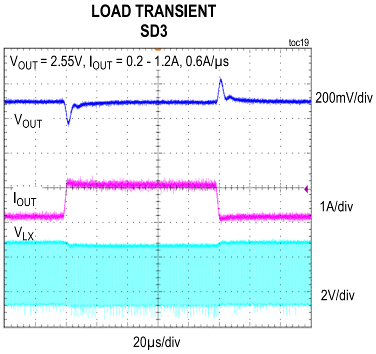


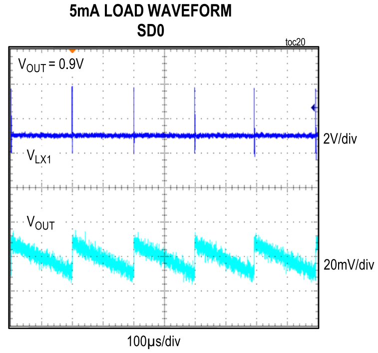


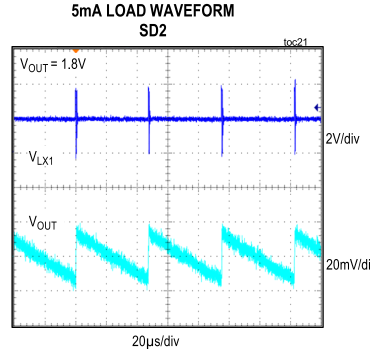


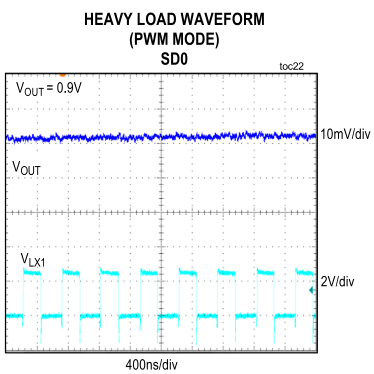
Typical Operating Characteristics (continued)

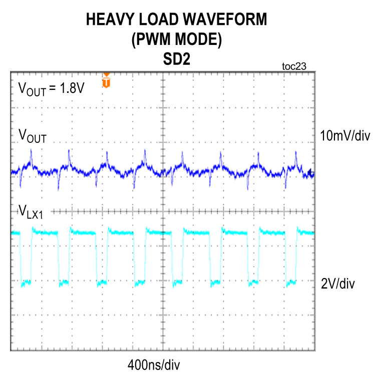
(AV_{DD} = +3.3V, V_{DDIO} = +1.8V, V_{REFP} - V_{REFN} = V_{REF} = 2.5V; No Line-Frequency Rejection, Continuous-Conversion Mode, Internal Clock; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

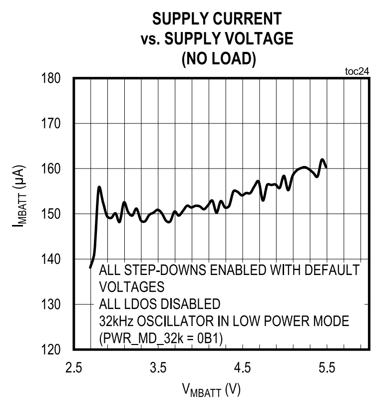


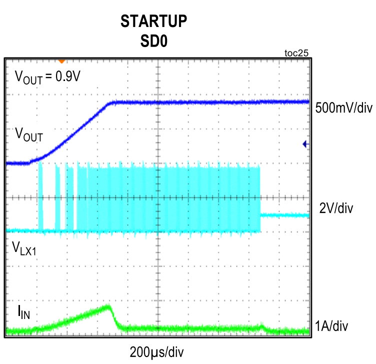


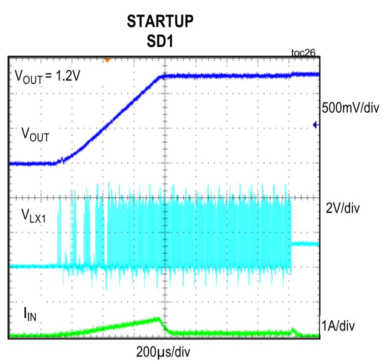


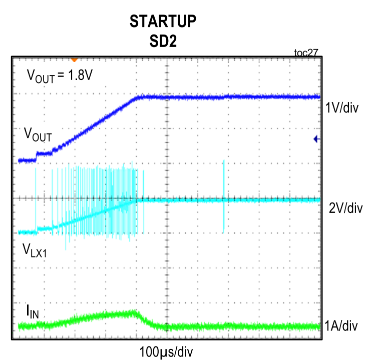








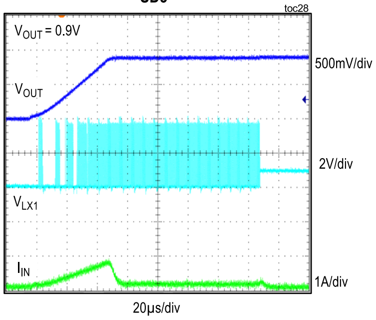




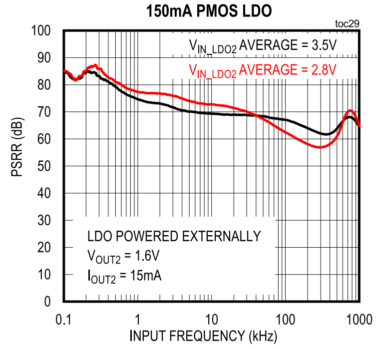
Typical Operating Characteristics (continued)

(AV_{VDD} = +3.3V, V_{DDIO} = +1.8V, V_{REFP} - V_{REFN} = V_{REF} = 2.5V; No Line-Frequency Rejection, Continuous-Conversion Mode, Internal Clock; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

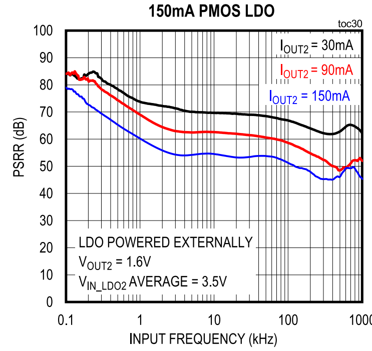
STARTUP
SD3



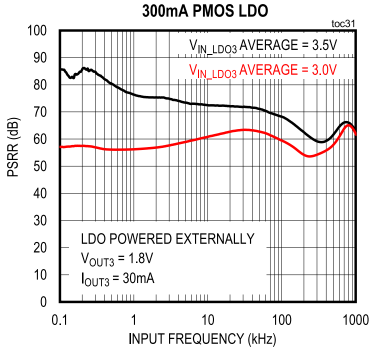
POWER-SUPPLY REJECTION RATIO
vs. INPUT FREQUENCY
150mA PMOS LDO



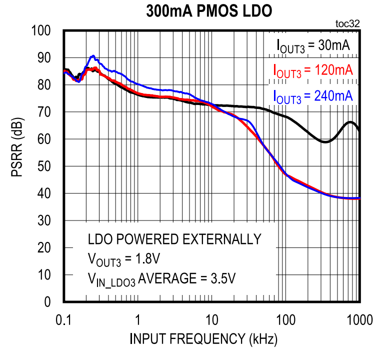
POWER-SUPPLY REJECTION RATIO
vs. INPUT FREQUENCY
150mA PMOS LDO



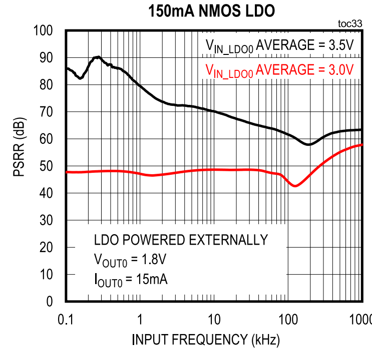
POWER-SUPPLY REJECTION RATIO
vs. INPUT FREQUENCY
300mA PMOS LDO



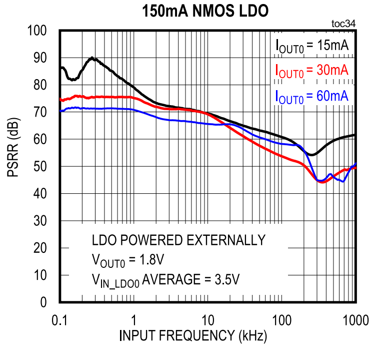
POWER-SUPPLY REJECTION RATIO
vs. INPUT FREQUENCY
300mA PMOS LDO



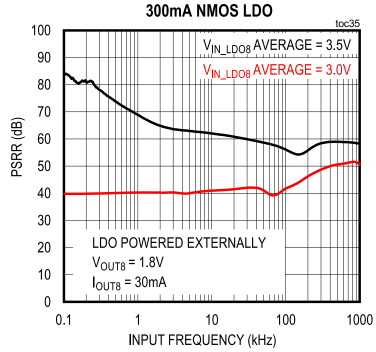
POWER-SUPPLY REJECTION RATIO
vs. INPUT FREQUENCY
150mA NMOS LDO



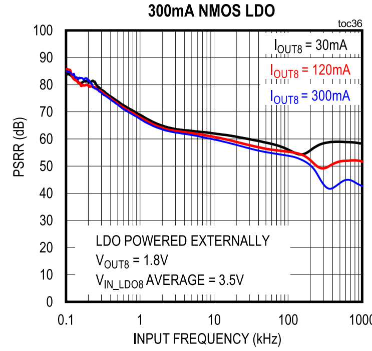
POWER-SUPPLY REJECTION RATIO
vs. INPUT FREQUENCY
150mA NMOS LDO



POWER-SUPPLY REJECTION RATIO
vs. INPUT FREQUENCY
300mA NMOS LDO

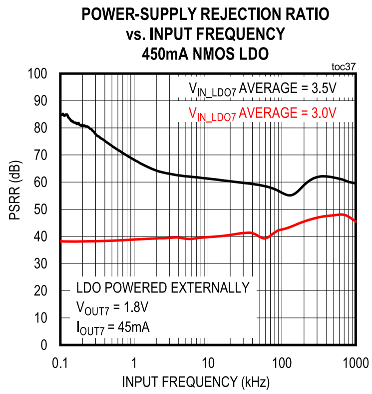


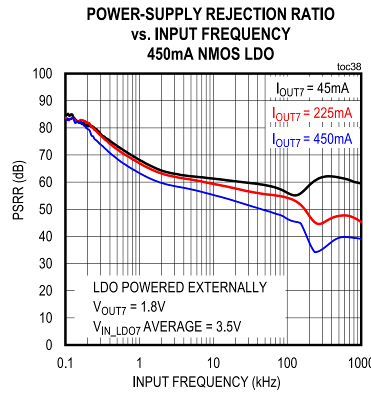
POWER-SUPPLY REJECTION RATIO
vs. INPUT FREQUENCY
300mA NMOS LDO



Typical Operating Characteristics (continued)

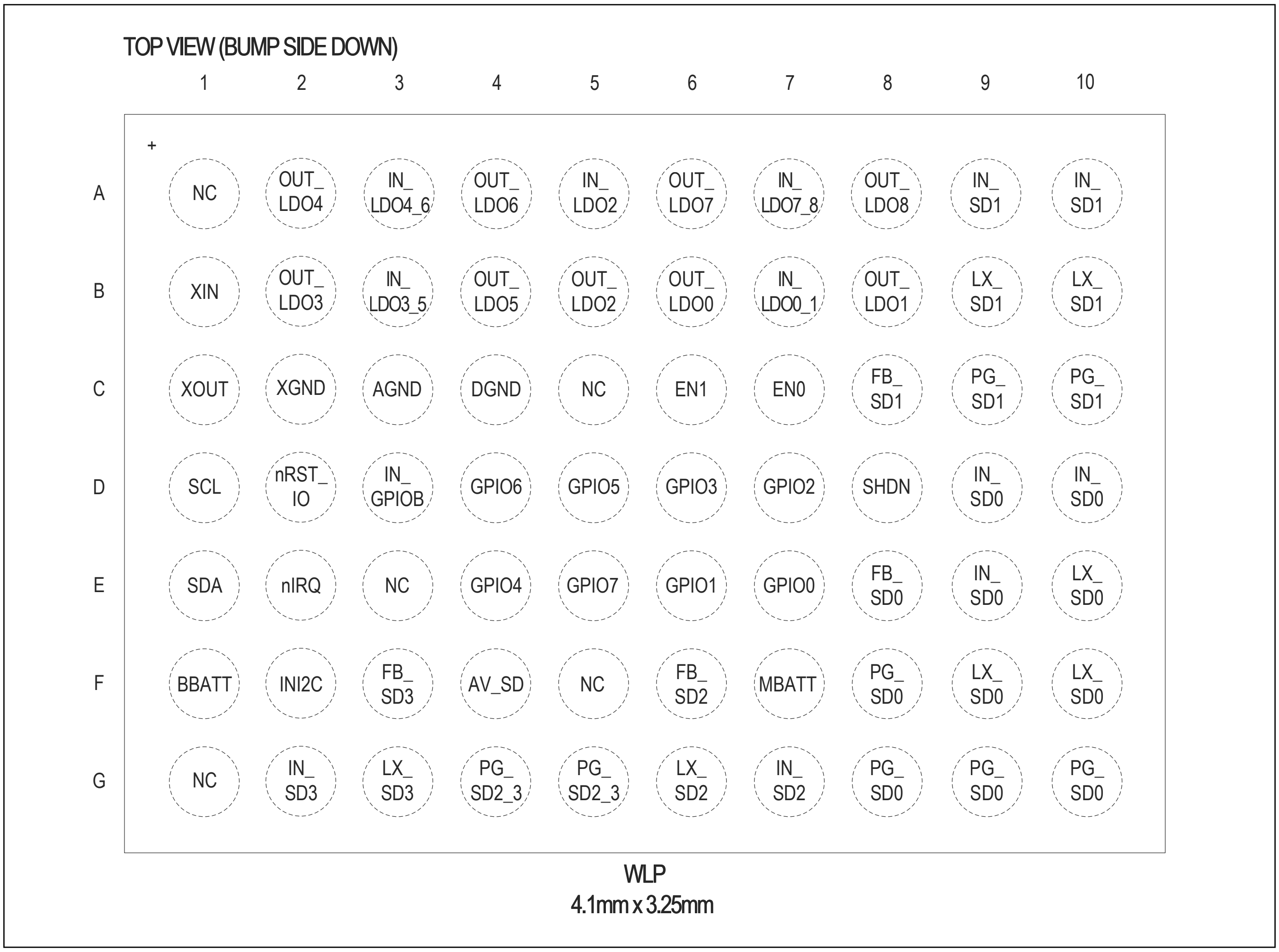
(AV_{VDD} = +3.3V, V_{DDIO} = +1.8V, V_{REFP} - V_{REFN} = V_{REF} = 2.5V; No Line-Frequency Rejection, Continuous-Conversion Mode, Internal Clock; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)





Bump Configuration

MAX77714



Bump Description

PIN	NAME	FUNCTION	TYPE
TOP			
F7	MBATT	Low-Noise PMIC Power Input. Bypass MBATT with a 0.1µF ceramic capacitor to ground.	Power Input
F1	BBATT	Backup Battery Connection. Bypass BBATT with a 0.1µF ceramic capacitor to ground.	Power Input
C1	XOUT	32.768kHz Crystal Oscillator Output. XOUT has on-chip programmable load capacitors for the crystal oscillator.	Output
B1	XIN	32.768kHz Crystal Oscillator Input. XIN has on-chip programmable load capacitors for the crystal oscillator.	Input
C2	XGND	Crystal Oscillator Ground. All XGND pins must be connected together.	Ground
E2	nIRQ	Active-Low Interrupt Output. nIRQ is an open-drain output.	Digital Output

Bump Description (continued)

PIN	NAME	FUNCTION	TYPE
C7	EN0	Enable Input 0 to the Flexible Power Sequencer. EN0 is typically connected to the system's ONKEY.	Digital Input
C6	EN1	Enable Input 1 to the Flexible Power Sequencer. EN1 is typically connected to the system's AP.	Digital Input
D8	SHDN	The shutdown input (SHDN) is a digital input to the ON/OFF controller that causes the device to reset through a global shutdown event. The signal for SHDN typically comes from a temperature sensor that measures the internal die temperature of the AP.	Digital Input
D2	nRST_IO	This is a bidirectional, active-low, open-drain, reset input/output.	Digital I/O
C3	AGND	Analog Ground. All GND pins must be connected together.	Ground
C4	DGND	Digital Ground. DGND carries ground current for digital circuits such as the I^2C.	Ground
A1, G1, E3, F5, C5	NC	No Connect. This bump is not internally connected to any node. This can be connected to GND to help improve thermal performance.	Ground
LDO			
B7	IN_LDO0_1	Linear Regulator 0 and 1 Power Input. Bypass IN_LDOx to GND with a 2.2µF ceramic capacitor.	Power Input
B6	OUT_LDO0	150mA NMOS LDO Output. If the LDO is not used, it is recommended to either ground OUT_LDO0 or leave it unconnected.	Power Output
B8	OUT_LDO1	150mA NMOS LDO1 Output. If the LDO1 is not used, it is recommended to either ground OUT_LDO1 or leave it unconnected.	Power Output
A5	IN_LDO2	Linear Regulator 2 Power Input. Bypass IN_LDO2 to GND with a 2.2µF ceramic capacitor.	Power Input
B5	OUT_LDO2	150mA PMOS LDO Output. If the LDO is not used, it is recommended to either ground OUT_LDO2 or leave it unconnected.	Power Output
B3	IN_LDO3_5	Linear Regulator 3 and 5 Power Input. Bypass IN_LDO3_5 to GND with a 2.2µF ceramic capacitor.	Power Input
B2	OUT_LDO3	300mA PMOS LDO Output. If the LDO is not used, it is recommended to either ground OUT_LDO3 or leave it unconnected.	Power Output
B4	OUT_LDO5	150mA PMOS LDO Output. If the LDO is not used, it is recommended to either ground OUT_LDO5 or leave it unconnected.	Power Output
A3	IN_LDO4_6	Linear Regulator 4 and 6 Power Input. Bypass IN_LDO4_6 to GND with a 2.2µF ceramic capacitor.	Power Input
A2	OUT_LDO4	150mA PMOS LDO Output. If the LDO is not used, it is recommended to either ground OUT_LDO4 or leave it unconnected.	Power Output
A4	OUT_LDO6	150mA PMOS LDO Output. If the LDO is not used, it is recommended to either ground OUT_LDO6 or leave it unconnected.	Power Output
A6	OUT_LDO7	450mA NMOS LDO Output. If the LDO is not used, it is recommended to either ground OUT_LDO7 or leave it unconnected.	Power Output
A7	IN_LDO7_8	Linear Regulator 7 and 8 Power Input. Bypass IN_LDO7_8 to GND with a 2.2µF ceramic capacitor.	Power Input
A8	OUT_LDO8	300mA NMOS LDO Output. If the LDO is not used, it is recommended to either ground OUT_LDO8 or leave it unconnected.	Power Output
STEP-DOWN			
D9, E9, D10	IN_SD0	SD0 Power Input. IN_SD0 is the drain connection of BUCK0's main power FET. IN_SD0 is a critical discontinuous-current node that requires careful PCB layout. See the *PCB Layout Guidelines* section for advice on how to connect IN_SD01 and its bypass capacitor.	Power Input

Bump Description (continued)

PIN	NAME	FUNCTION	TYPE
F9, F10, E10	LX_SD0	SD0 Switching Node. Connect the required inductor between LX_SD0 and the output capacitor. LX_SD0 is a critical node that requires careful PCB layout. See the *PCB Layout Guidelines* section for advice on how to connect LX_SD0 to the power inductor.	Power I/O
F8, G8, G9, G10	PG_SD0	SD0 Power Ground are internally combined. PG_SD0 is the source connection of BUCK0's synchronous rectifier. PG_SD0 is a critical discontinuous current node that requires careful PCB layout. See the *PCB Layout Guidelines* section for advice on how to connect the various ground nodes of this device.	Ground
E8	FB_SD0	SD0 Output Voltage Feedback Node. Connect FB_SD0 to the local output capacitor at the Buck output. In addition to setting the output voltage regulation threshold, FB_SD0 can also be programmed to discharges the output capacitor when the converter is shutdown. FB_SD0 is a critical analog input that requires careful PCB layout. See the *PCB Layout Guidelines* section for advice on how to connect FB_SD0 to the regulator output.	Analog Input
A9, A10	IN_SD1	SD1 Power Input. IN_SD1 is the drain connection of BUCK1's main power FET. IN_SD1 is a critical discontinuous-current node that requires careful PCB layout. See the *PCB Layout Guidelines* section for advice on how to connect IN_SD1 and its bypass capacitor.	Power Input
B9, B10	LX_SD1	SD1 Switching Node. Connect the required inductor between LX_SD1 and the output capacitor. LX_SD1 is a critical node that requires careful PCB layout. See the *PCB Layout Guidelines* section for advice on how to connect LX_SD1 to the power inductor.	Power I/O
C9, C10	PG_SD1	SD1 Power Ground are internally combined. PG_SD1 is the source connection of BUCK1's synchronous rectifier. PG_SD1 is a critical discontinuous-current node that requires careful PCB layout. See the *PCB Layout Guidelines* section for advice on how to connect the various ground nodes of this device.	Ground
C8	FB_SD1	SD1 Output Voltage Feedback Node. Connect FB_SD1 to the local output capacitor at the Buck output. In addition to setting the output voltage regulation threshold, FB_SD1 can also be programmed to discharge the output capacitor when the converter is shutdown. FB_SD1 is a critical analog input that requires careful PCB layout. See the *PCB Layout Guidelines* section for advice on how to connect FB_SD1 to the regulator output.	Analog Input
G7	IN_SD2	SD2 Power Input. IN_SD2 is the drain connection of BUCK2's main power FET. IN_SD2 is a critical discontinuous-current node that requires careful PCB layout. See the *PCB Layout Guidelines* section for advice on how to connect IN_SD2 and its bypass capacitor.	Power Input
G6	LX_SD2	SD2 Switching Node. Connect the required inductor between LX_SD2 and the output capacitor. LX_SD2 is a critical node that requires careful PCB layout. See the *PCB Layout Guidelines* section for advice on how to connect LX_SD2 to the power inductor.	Power I/O
G4, G5	PG_SD2_3	SD2 and SD3 Power Ground are internally combined. PG_SD2_3 is the source connection of SD2 and 3's synchronous rectifier. PG_SD2_3 is a critical discontinuous-current node that requires careful PCB layout. See the *PCB Layout Guidelines* section for advice on how to connect the various ground nodes of this device.	Ground
F6	FB_SD2	SD2 Output Voltage Feedback Node. Connect FB_SD2 to the local output capacitor at the Buck output. In addition to setting the output voltage regulation threshold, FB_SD2 can also be programmed to discharge the output capacitor when the converter is shutdown. FB_SD2 is a critical analog input that requires careful PCB layout. See the *PCB Layout Guidelines* section for advice on how to connect FB_SD2 to the regulator output.	Analog Input

Bump Description (continued)

PIN	NAME	FUNCTION	TYPE
G2	IN_SD3	SD3 Power Input. IN_SD3 is the drain connection of BUCK1's main power FET. IN_SD3 is a critical discontinuous-current node that requires careful PCB layout. See the *PCB Layout Guidelines* section for advice on how to connect IN_SD3 and its bypass capacitor.	Power Input
G3	LX_SD3	SD3 Switching Node. Connect the required inductor between LX_SD3 and the output capacitor. LX_SD3 is a critical node that requires careful PCB layout. See the *PCB Layout Guidelines* section for advice on how to connect LX_SD3 to the power inductor.	Power I/O
F3	FB_SD3	SD3 Output Voltage Feedback Node. Connect FB_SD3 to the local output capacitor at the Buck output. In addition to setting the output voltage regulation threshold, FB_SD3 can also be programmed to discharge the output capacitor when the converter is shutdown. FB_SD3 is a critical analog input that requires careful PCB layout. See the *PCB Layout Guidelines* section for advice on how to connect FB_SD3 to the regulator output.	Analog Input
F4	AV_SD	SD3 Analog Power input. Connect AV_SD to the local output capacitor at the Buck Input. This supply powers the internal analog circuit.	Analog Input
I^2C			
E1	SDA	Serial Interface Data Bidirectional Open-Drain.	Digital I/O
D1	SCL	Serial Interface Clock Input. Open-Drain Output.	Digital Input
F2	INI2C	Internal Logic Supply for SDA and SCL.	Power Input
GPIO			
E7	GPIO0	General Purpose Input Output resource can be controlled using the Flexible Power Sequencer.	Digital I/O
E6	GPIO1	General Purpose Input Output resource can be controlled using the Flexible Power Sequencer.	Digital I/O
D7	GPIO2	General Purpose Input Output resource can be controlled using the Flexible Power Sequencer.	Digital I/O
D6	GPIO3	General Purpose Input Output resource and can be configured as an ACOK input when configured in ALT mode.	Digital I/O
E4	GPIO4	General Purpose Input Output resource and can be confirgure to output 32kHz clock when configured in ALT mode.	Digital I/O
D5	GPIO5	General Purpose Input Output resource and can be configured to output 32kHz clock when configured in ALT mode.	Digital I/O
D4	GPIO6	General Purpose Input Output resource and can be configured to output 32kHz clock when configured in ALT mode.	Digital I/O
E5	GPIO7	General Purpose Input Output resource can be controlled using the Flexible Power Sequencer.	Digital I/O
D3	IN_GPIOB	Input for the General Purpose Input Output resource 4-7.	Digital I/O

Detailed Description

OTP Options

Refer to Table 1 for the default register settings.

Table 1. OTP Options

RESOURCE	MAX77714EWC+	MAX77714FEWC+
CID4	0x01	0x06
MSTR_PU[2:0]	3904µs	984µs
MSTR_PD[2:0]	3904µs	31µs
MSTR_SLPENTY[2:0]	3904µs	984µs
MSTR_SLPEXT[2:0]	3904µs	31µs
SD0	0.90V, FPS0, UPSLT1, DNSLT1	1.20V, FPS1, UPSLT1, DNSLT0
SD1	1.29V, FPS0, UPSLT3, DNSLT3	0.90V, FPS1, UPSLT3, DNSLT0
SD2	1.80V, FPS0, UPSLT5, DNSLT5	0.625V, FPS0, UPSLT5, DNSLT0
SD3	0.90V, FPS0, UPSLT4, DNSLT4	3.6V, NOT CONFIGURED IN FPS, OUTPUT DISABLED
LDO0	1.80V, FPS0, UPSLT6, DNSLT6	0.8V, FPS1, UPSLT6, DNSLT0, OUTPUT DISABLED
LDO1	0.90V, FPS0, UPSLT6, DNSLT6	0.8V, FPS1, UPSLT6, DNSLT0, OUTPUT DISABLED
LDO2	3.30V, FPS0, UPSLT6, DNSLT6	2.5V, FPS1, UPSLT2, DNSLT0, NORMAL-POWER MODE
LDO3	2.90V, FPS0, UPSLT6, DNSLT6	3.3V, FPS1, UPSLT6, DNSLT0, GLOBAL LOW-POWER MODE
LDO4	0.90V, FPS0, UPSLT6, DNSLT6	0.4V, FPS1, UPSLT6, DNSLT0, OUTPUT DISABLED
LDO5	3.30V, FPS0, UPSLT6, DNSLT6	0.8V, FPS1, UPSLT6, DNSLT0, OUTPUT DISABLED
LDO6	1.80V, FPS0, UPSLT4, DNSLT4	0.8V, FPS1, UPSLT6, DNSLT0, OUTPUT DISABLED
LDO7	3.30V, FPS0, UPSLT6, DNSLT6	0.8V, FPS1, UPSLT6, DNSLT0, OUTPUT DISABLED
LDO8	2.90V, FPS0, UPSLT7, DNSLT7	0.8V, FPS1, UPSLT6, DNSLT0, OUTPUT DISABLED
GPIO0	FPS0, UPSLT0, DNSLT0	NOT CONFIGURED IN FPS
RSTIO	FPS0, UPSLT7, DNSLT7	FPS0, UPSLT4, DNSLT7
32KSOURCE_OTP	0b1 (Silicon Oscillator)	0b1 (Silicon Oscillator)
OTP_EN0[1:0]	0b10 (ON/OFF Software)	0b01 (Slide Switch)
OTP_MR	0b0 (Manual reset with no wakeup)	0b0 (Manual reset with no wakeup)
OTP_I2CADDR[1:0]	0b00 PMIC 7-bit address = 0x38 RTC 7-bit slave address = 0x90	0b00 PMIC 7-bit address = 0x38 RTC 7-bit slave address = 0x90
OTP_MBATT	0b0 (MBATT wakeup signal disabled)	0b0 (MBATT wakeup signal disabled)
OTP_TRSTO[1:0]	0b10 (32ms)	0b00 (1ms)
OTP_SHDNAL	0b0 (Active-high)	0b0 (Active-high)
OTP_BBATT	0b0 (BBCVS[0] will always reset to 1b0	0b0 (BBCVS[0] will always reset to 1b0
OTP_ACOKAL	0b0 (Active-high)	0b0 (Active-high)
OTP_EN1AL	0b0 (Active-high)	0b0 (Active-high)
OTP_EN0AL	0b0 (Active-high)	0b0 (Active-high)
OTP_WDTEN	0b0 (Watchdog default off, can be enabled with I^2C)	0b0 (Watchdog default off, can be enabled with I^2C)

Detailed Description—Global Resources

Voltage References, Bias Currents, and Timing References

Centralized voltage references, bias current, and timing references support all of the functional blocks within the MAX77714. These resources are automatically enabled when any of the peripheral functions within the device require them. The supply current associated with the minimum set of these resources make up the quiescent current (I_{Q_MBATT}).

Voltage Monitors

The MBATT undervoltage lockout (UVLO) and MBATT overvoltage lockout (OVLO) comparators force the entire device off when the supply voltage (V_{MBATT}) is not within the acceptable window of operation (2.6V to 5.5V). Disabling the device when the supply is outside of its acceptable range ensures reliable consistent behavior when the supply voltage is removed/applied and prevents overvoltage stress to the device. The main-battery low signal is also available through the nRST_IO signal when LBRSTEN = 1. With all peripheral blocks of the device disabled, the quiescent current of the device is 12μA (I_{Q_MBATT}).

Thermal Monitors

Several on-chip thermal sensors force the device to shutdown if the junction temperature exceeds +165°C (T_{JSHDN}). In addition to the +165°C shutdown threshold, these thermal sensors also provide interrupts when the temperature exceeds +120°C (thermal alarm 1) and +140°C (thermal alarm 2).

Bidirectional Reset Input/Output

The device has a bidirectional, active-low, open-drain, reset input/output (nRST_IO). The RSO signal within the bidirectional reset IO logic is asserted by the device when it needs to drive nRST_IO low. If the device is not driving nRST_IO low (i.e., RSO is low), and an external device such as a reset button pulls nRST_IO low, then the RSI signal within the bidirectional reset IO logic is asserted. If RSI is asserted for longer than t_{DBNC}, then a global shutdown event is triggered (GLBALSHDN). A global shutdown due to RSI is recorded in the POERC register such that when the system's microprocessor recovers from the reset it can recognize that the cause of the power down was due to RSI. If a global shutdown event is triggered by RSI, then the deviceautomatically generates a wakeup event after the global shutdown event has completed.

The reset output is a programmable slave to the flexible power sequencer. Allowing the RSO to respond to the flexible power sequencer gives it the capability to drive the nRST_IO line low as the first action in the power down sequence. The RSTIOFPS register configures how nRST_IO behaves with respect to the flexible power sequencer.

Once all conditions for allowing the reset output to go high-impedance have been met, a reset delay timer is initiated before RSO is deasserted (t_{RST_O}).

The following bulleted list summarizes all the conditions required for the device to set RSO low and allow nRST_IO to go high-impedance.

- The device must not be in a global shutdown state.
- The 32kHz oscillator must be stable (32K_OK).
- The flexible power sequencer (FPS_RSO) must be satisfied.
- Reset timer has expired (t_{RST_O}).

An example configuration that allows nRST_IO to go high-impedance is:

- No global shutdown events.
- The main-battery voltage is within the valid region.
- The 32kHz clock is stable.
- FPS0 (flexible power sequencer 0) has gotten past power-up cycle 4 (FPS_RSO).
- t_{RST_O} expired.
- No external device such as a reset button are pulling nRST_IO low.

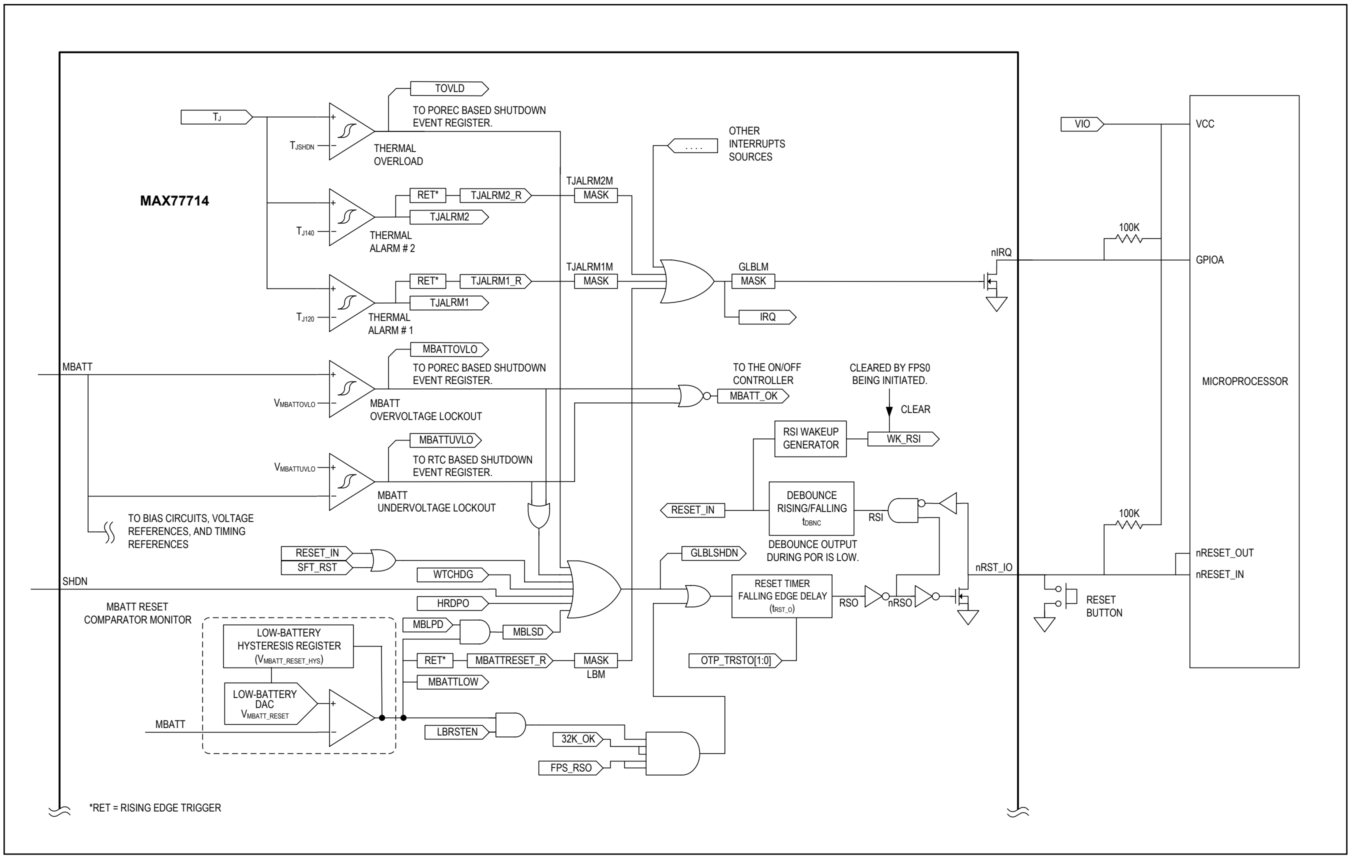


Figure 1. Global Resource Logic

Global Shutdown

This document uses the term "global shutdown" to refer to any event that causes a shutdown of all regulators and a reset for most of the registers within the device. The POERC register records the source of a "global shutdown" event. The various conditions which cause a global shutdown are as follows:

- The battery voltage is low (MBATT < MBATT_RESET falling)
- Hardware reset input (RSI) event detected
- Manual Reset event detected
- Watchdog timer expires
- SFT_RST = 1
- PWR_OFF = 1
- The junction temperature is too high ($T_J > T_{JSHDN}$)
- SHDN pin is asserted (SHDN = 1)
- SRCFPS0 = 1 and ENFPS0 register transitions from HIGH to LOW

After a global shutdown occurs, the device can be powered up normally as long as the main-battery voltage and the die temperature are within their valid ranges. Although all regulators are forced off in response to a global shutdown, the RTC remains powered and continues to record the calendar.

From any state in the device, there are three ways of implementing a "global shutdown". The source of the global shutdown event determines how a global shutdown is implemented as described in the following:

Global Shutdown Events with Sequenced Shutdown and Automatic Wakeup

The events in this category are associated with faulty system states where the software may not be working properly but the system could potentially recover by powering down the microprocessor, resetting all the global shutdown registers, and then powering up the microprocessor again. The following events initiate a sequenced shutdown followed by automatic wakeup:

- RSI event (hardware reset input)
- SFT_RST event if SFT_RST_WK = 1 (software reset input)
- Watchdog timer expires if WD_RST_WK = 1
- Manual reset event if OTP_MR = 1

Global Shutdown Events with Sequenced Shutdown to the OFF State

Six events initiate "sequenced global shutdown to the off state." With the exception of PWR_OFF, which is a normal system function, the events in this category are associated with undesirable system states that may occur in a normally functioning product. Powering down the microprocessor and resetting all the global shutdown registers helps the system resolve these undesirable events. In general, a wakeup event such as an onkey press is required to power-up the microprocessor again.

In the case of a software reset input (SFT_RST) with SFT_RST_WK = 0, the global shutdown state machine results in the default state with the device off and waiting for a wakeup event. It is possible for the system software to program a wakeup event based on an RTC alarm. For example, once the state machine lands in the default state it waits there until the RTC alarm generates the wakeup event.

The following six conditions fall into this category:

- Watchdog timer expires if WD_RST_WK = 0
- Manual reset event if OTP_MR = 0
- SFT_RST event if SFT_RST_WK = 0 (software reset input)
- PWR_OFF = 1
- $T_J > T_{JSHDN}$ (thermal overload)
- SHDN input event

Global Shutdown Events with Immediate Shutdown

Four events initiate an “immediate shutdown.” The events in this category are associated with potentially hazardous system events. Powering down the microprocessor and resetting all the registers helps mitigate any issues that may occur due to these potentially hazardous system events.

The following four events fall in this category:

- $V_{MBATT} < V_{MBATTUVLO}$ (main-battery undervoltage)
- $V_{MBATT} > V_{MBATTOVLO}$ (main-battery overvoltage)
- OK32K = 0 (in or after standby state)
- BRDY = 0 (in or after ready state)

System Watchdog Timer

The MAX77714 contains a system watchdog timer to ensure safe and reliable operation. The system watchdog timer prevents the device from powering a system in the event that the system controller (processor) hangs or otherwise isn’t communicating correctly. The default state of the system watchdog timer enable bit (WDTEN) can be factory programmed with an OTP bit (OTP_WDTEN). To use the watchdog timer feature, enable the feature by setting WDTEN. While enabled, the system controller must reset the system watchdog timer within the timer period (t_{WD}) for the charger to operate normally. Reset the system watchdog timer by programming WDTC[1:0] = 0b01. t_{WD} is programmable from 2s to 128s with TWD[1:0].

With WDTEN set, an internal counter is incremented with the internal oscillator. When the internal counter matches a value programmed by TWD[1:0], the device asserts nRST_IO, powers down all of its regulators with a global shutdown condition, and sets the WDT bit in the non-volatile event recorder.

To prevent the system watchdog timer from initiating a global shutdown event and disabling the device, a properly operating processor clears the system watchdog timer within the timer period programmed by TWD[1:0]. The system watchdog time is cleared by setting WDTC[1:0] = 0b01.

The system watchdog timer can be set to automatically clear when the AP enters its sleep or off states. The device interprets the AP sleep state as FPS1 being disabled. The device interprets the off state as FPS1 being disabled.

Note that the device contains both a system watchdog timer and an I^2C watchdog timer.

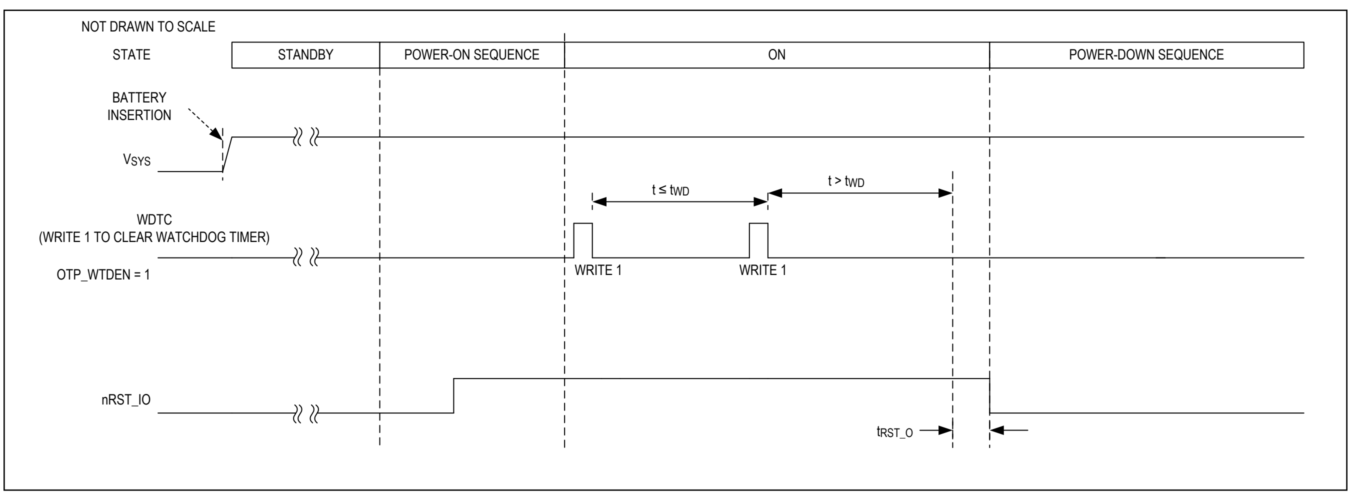


Figure 2. System Watchdog Timer

EN0 Functionality

The EN digital input can be configured to work with a push-button switch, a slide-switch, or a ON/OFF logic signal (e.g., PGOOD). (Figure 3) shows EN's functionality for power-on sequencing and manual reset. The default configuration of the device is pushbutton mode and no additional programming is necessary. Applications that use a slide-switch on-key or ON/OFF logic signal configuration must set OTP_EN0[1:0]. The polarity of EN0 can be controlled using the OTP_EN0AL bit. The default is active high.

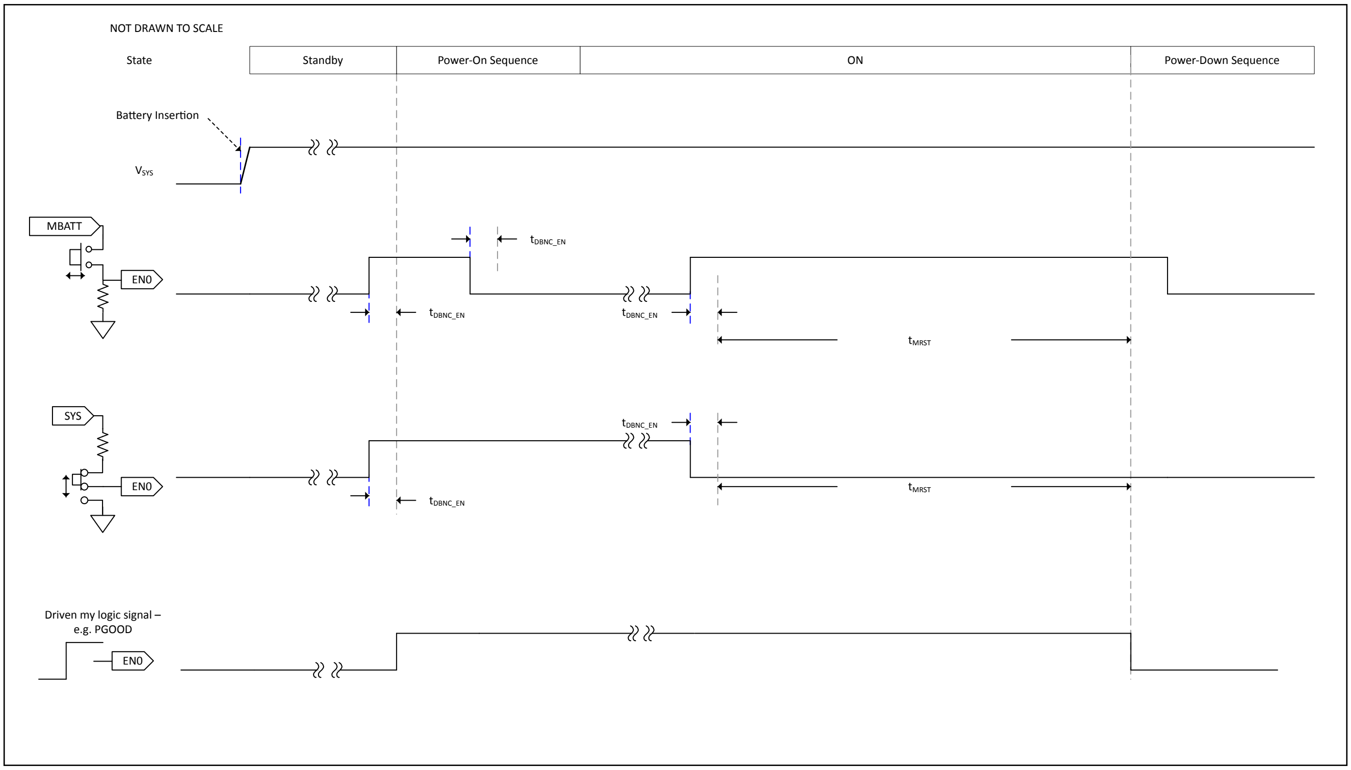


Figure 3. EN0 Functionality Options

Interrupt Logic

Several interrupt and interrupt mask registers monitor key information and assert the nIRQ output signal when an interrupt event has occured. nIRQ is an active-low, open-drain output that is typically routed to the processor's interrupt input to allow for quick notification of interrupt events. A pullup resistor is require for this signal. This pullup resistor is typically found inside the processor that interprets the interrupt signal, but a board-mounted pullup resistor is required if one is unavailable.

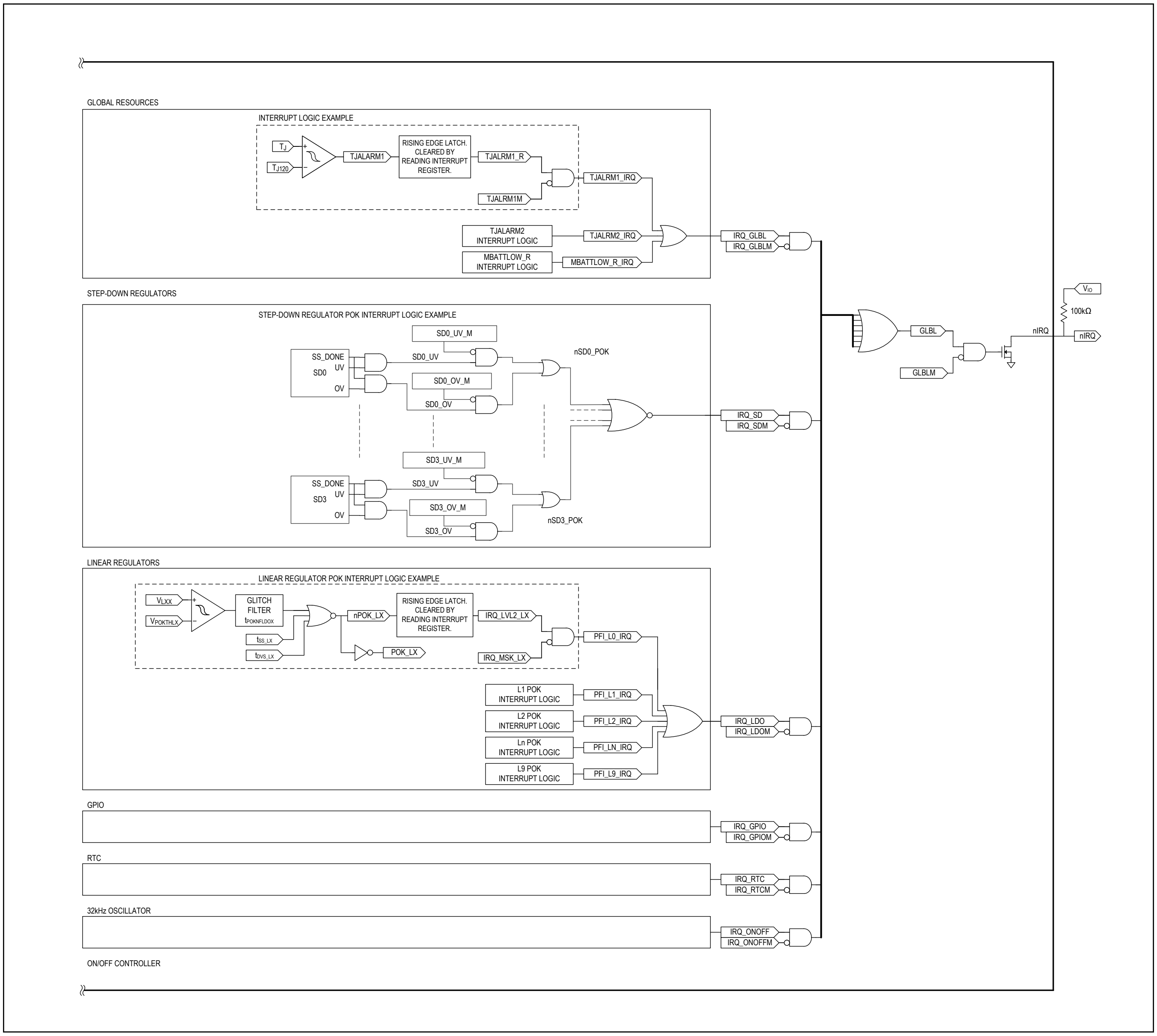


Figure 4. Simplified Interrupt Status and Mask Logic

Detailed Description—ON/OFF Controller

ON/OFF Controller

The ON/OFF controller monitors multiple wakeup sources to intelligently enable all resources that are necessary for the AP to boot (i.e., FPS0 and FPS1). The ON/OFF controller monitors wakeup events on the EN0, EN1, ACOK, and nRST_IO hardware inputs. Additionally, internal wakeup events are also monitored: SMPL, ALARM1, and ALARM2 internal signals. Wakeup events go through logic to affect flexible power sequencers 0 and 1 (FPS0, FPS1). Many wakeup signals can be masked (WK_ACOK, WK_ALARM1, WL_ALARM2, WK_EN0).

Many signals within the ON/OFF controller generate interrupts and are recorded in the status registers.

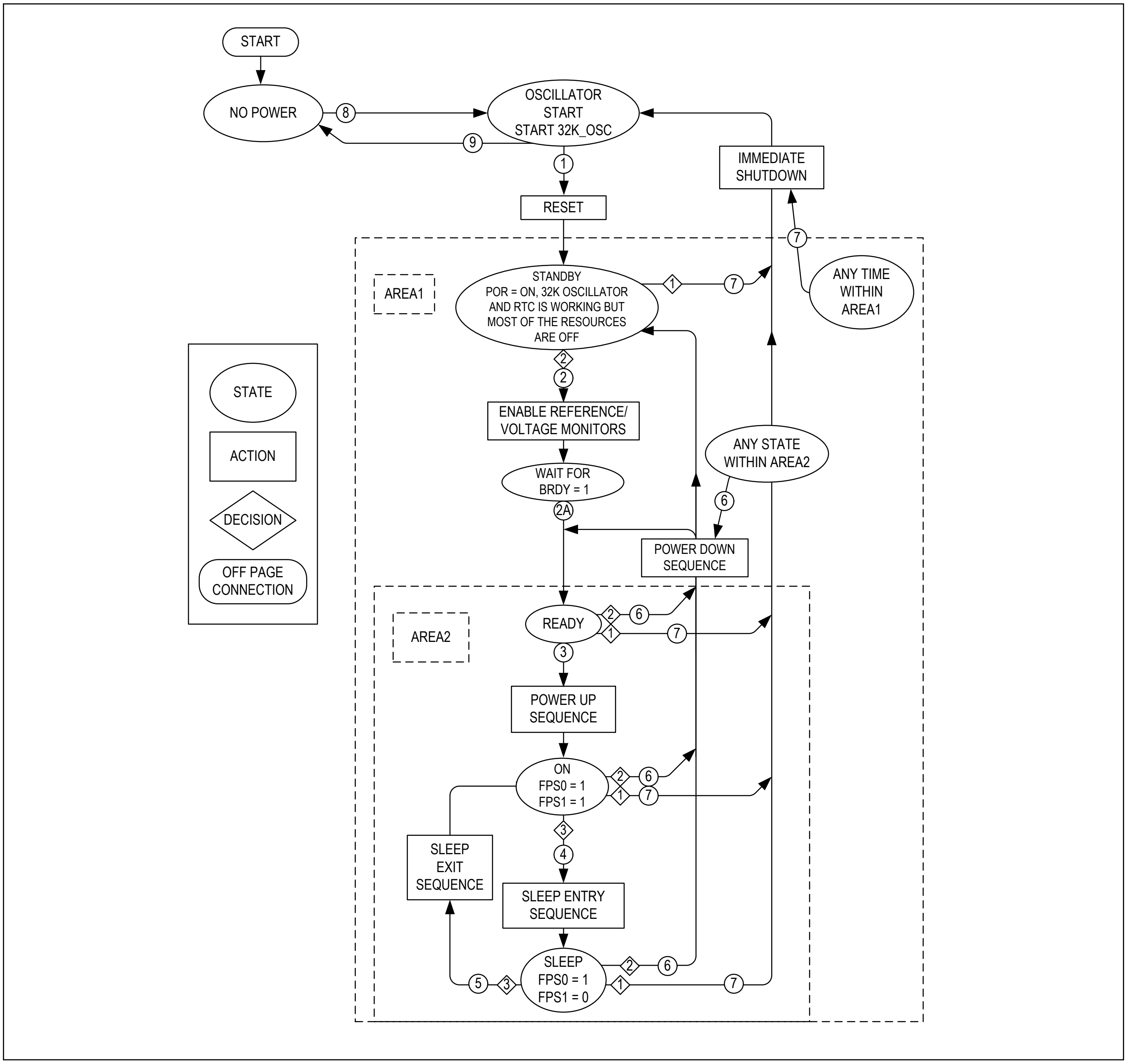


Figure 5. State Diagram: ON/OFF Controller Top Level

Table 2. ON/OFF Controller Transition Conditions

TRANSITION	CONDITION
1	The fundamental system voltages and resources are available. Move to the standby state. ● 32kHz oscillator is OK (OK32K = 1) OR ● The battery voltage is undervoltage ($V_{MBATT} > V_{MBATTUVLO}$) OR ● The battery voltage is overvoltage ($V_{MBATT} < V_{MBATTOVLO}$)

Table 2. ON/OFF Controller Transition Conditions (continued)

2	I^2C Bias Enable Command OR A wakeup signal has been received from one of the following sources: ● A debounced EN0 press (i.e., edge) and WK_EN0 is SET has been detected OR ● ALARM1_R event occurs and WK_ALRM1R is set OR ● ALARM2_R event occurs and WK_ALRM2R is set OR ● SMPL_EVENT occurs and SMPL_EN is set OR ● ACOK event (i.e., level) occurs and WK_ACOK is set OR ● MBATT > MBATTUVLO rising and WK_MBATT is set OR ● WAKEUP flag is set by the previous sequenced shutdown (starts at STANDBY state post power-down event) ● SRCFPS0 = 1 and ENFPS0 register transitions from LOW to HIGH
2A	The basic system resources are okay ● BRDY = 1 and t_{BRDY_TMR} not expired
3	If a wakeup signal was initiated at transition "2" then proceed to powerup sequence, else stay in Ready state and wait for wakeup
4	Enter Sleep Mode ● Sleep mode is enabled (SLPEN = 1) and EN1 transitions from high to low (OTP_EN1AL = 1) OR ● SRCFPS1 = 1 and ENFPS1 register transitions from HIGH to LOW
5	Exit Sleep Mode ● Sleep mode is enabled (SLPEN = 1) and EN1 transitions from low to high OR ● A debounced EN0 press and WK_EN0 is SET has been detected OR ● ALARM1_R event occurs and WK_ALRM1R is set OR ● ALARM2_R event occurs and WK_ALRM2R is set OR ● ACOK event (i.e. level) occurs and WK_ACOK is set OR ● SRCFPS0 = 1 and ENFPS0 register transitions from LOW to HIGH ● SRCFPS1 = 1 and ENFPS1 register transitions from LOW to HIGH
6	Enter the Power-Down Sequence with Register Reset ● The battery voltage is low (MBATT < MBATT_RESET falling) OR ● Hardware reset input (RSI) event detected OR ● Manual reset event detected OR ● SFT_RST = 1 OR ● PWR_OFF = 1 OR ● The junction temperature is too high ($T_J > T_{JSHDN}$) OR ● SHDN pin is asserted (SHDN = 1) ● SRCFPS0 = 1 and ENFPS0 register transitions from HIGH to LOW
7	Immediate Shutdown ● The battery voltage is undervoltage ($V_{MBATT} < V_{MBATTUVLO}$) OR ● The battery voltage is overvoltage ($V_{MBATT} > V_{MBATTOVLO}$) OR ● OK32K = 0 OR ● BRDY = 0 t_{BRDY_TMR} expired
8	Oscillator Start ● $V_{MBATT} > V_{MBATTPOR}$
9	No Power ● $V_{MBATT} < V_{MBATTPOR}$

Power-Up/Down Sequence

The device integrated a flexible power sequencer (FPS) that controls the power-up and power-down timing of the system. The functionality of the FPS is described as follows:

- The power-up/down sequence consists of two FPS masters (FPS0 and FPS1) each contains 8 slots.
- The 8 slots count sequentially in time during both power-up and power-down.
- During the power-up sequence (Figure 6), the slots count upwards from 0 to 7.
- During the power-down sequence (Figure 7), the slots count downwards from 7 to 0.
    - The events in this category are associated with faulty system states where the software may not be working properly but the system could potentially recover by powering down the microprocessor, resetting all the global shutdown registers, and then powering up the microprocessor again.
- Regulators enable in their assigned slots in the power-up sequence. Regulators disabled in their assigned slots in the power-down sequence.
- GPIOs assert logic-high in their assigned slot in the power-up sequence. GPIOs assert logic-low in their assigned slot in the power-down sequence.
- Three dedicated bits are available to program the slot pitch (t_{FPST}, time between slots) and are programmable between 31µs to 3904µs in eight binary weighted steps.
    - FPS0 power-up sequence (MSTR_PU[2:0]), power-down sequence (MSTR_PD[2:0]).
    - FPS1 sleep exit power-up sequence (MSTR_SLPEXT[2:0]), Sleep entry power-down sequence (MSTR_SLPENTY[2:0]).

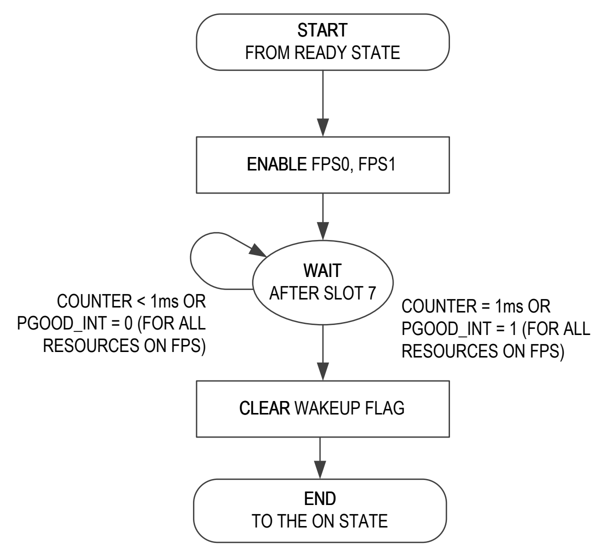


Figure 6. Flow Chart—Power-Up Sequence

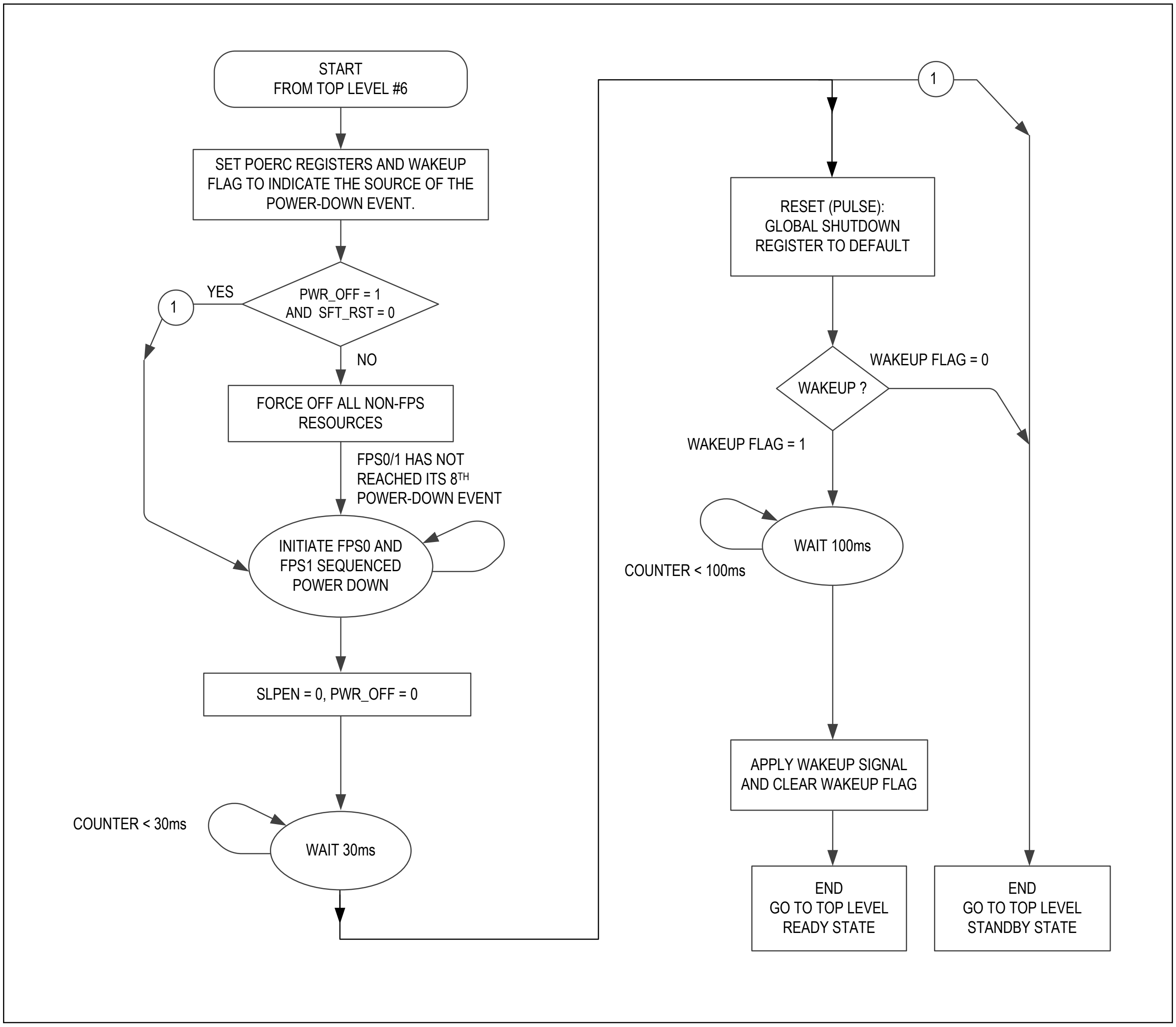


Figure 7. Flow Chart—Power-Down Sequence

Immediate Shutdown

The events in this category are associated with potentially hazardous system events. Powering down the microprocessor and resetting all the device registers helps mitigate any issues that may occur due to these potentially hazardous system events.

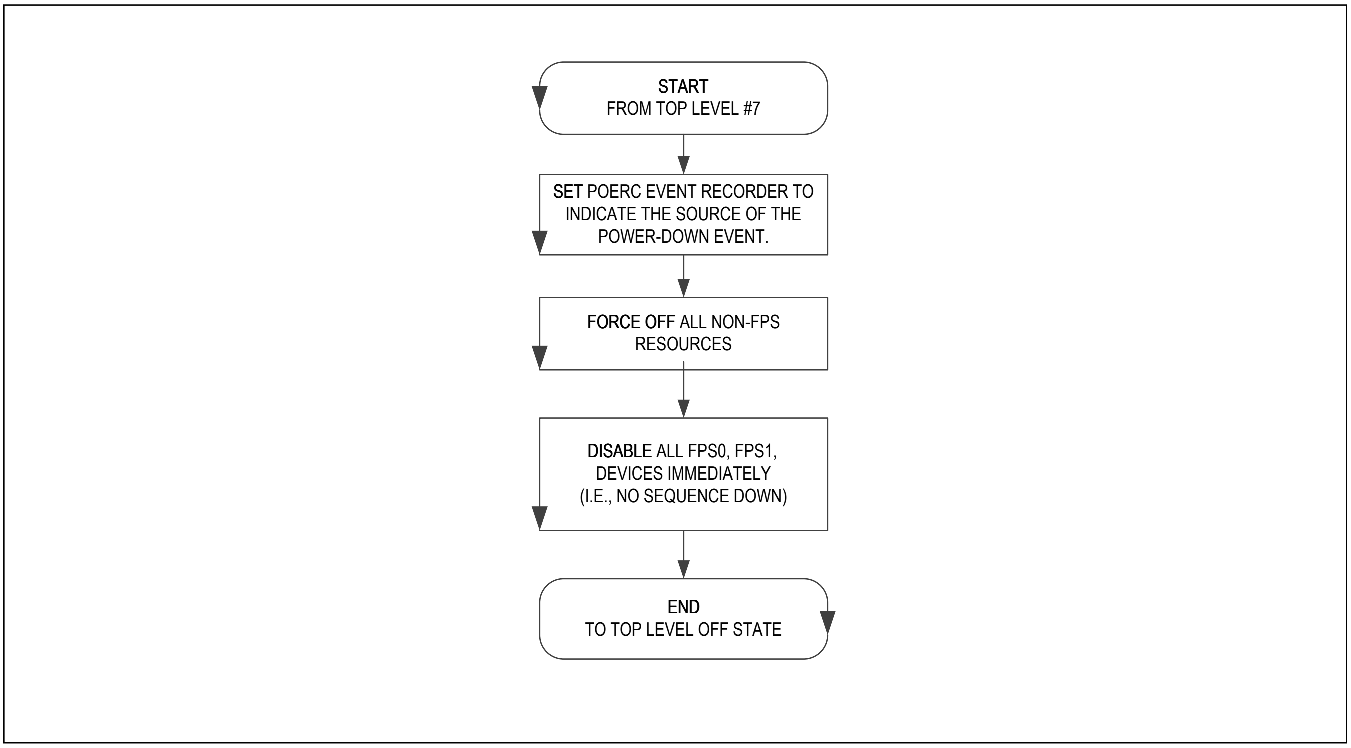


Figure 8. Flow Diagram: Immediate Shutdown

RESET

The reset state puts the PMIC in an initial known state by following the flow in (Figure 9).

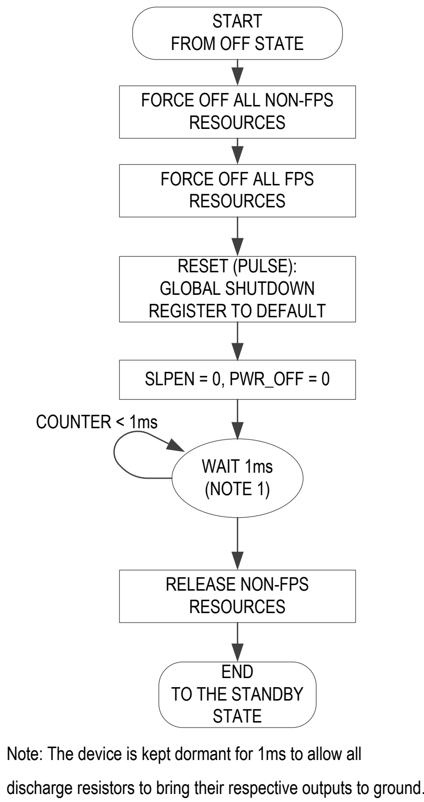


Figure 9. Reset Flow Diagram

EN0

EN0 is a digital input to the ON/OFF controller that typically comes from the system’s on-key. The EN0 polarity is factory-programmable with OTP (OTP_EN0AL) to be active-high or active-low

EN1

EN1 is a digital input to the ON/OFF controller that typically comes from the system’s AP. EN1 is used to control sleep modes. The EN1 polarity is factory-programmable with OTP (OTP_EN1AL) to be active-high or active-low.

ACOK

ACOK is a digital input (GPIO3 ALT mode) to the ON/OFF controller that typically comes from the system’s battery charger. ACOK indicates the presence/absence of the external charge adapter. The ACOK polarity is factory-programmable with OTP (OTP_ACOKAL) to be active-high or active-low with the appropriate internal pull-up/down.

SHDN

The shutdown input (SHDN) is a digital input to the ON/OFF controller that causes the device to reset through a global shutdown event. The signal for SHDN typically comes from a temperatures sensor such as the MAX6642 that measures the internal die temperature of the AP. The SHDN polarity is factory-programmable with OTP (OTP_SHDNAL) to be active high or active low with the appropriate internal pull-up/down. A system shutdown based on SHDN is recorded in the non-volatile power-off event recorder.

SMPL, ALARM1, and ALARM2

SMPL, ALARM1, and ALARM2 are signal generated from the RTC and used by the ON/OFF controller. See the *RTC* section for more information on these signals.

MBATT_OK and MBATTLOW

MBATT_OK and MBATTLOW are digital signals that come from the systems' main-battery monitor. MBATT_OK gates several wakeup sources so that they cannot enable FPS0 and FPS1 until the battery is above the system undervoltage-lockout threshold ($V_{MBATTUVLO}$). MBATTLOW prevents FPS0 and FPS1 from being enabled when the main-battery is below a programmed minimum voltage.

Resource Power Mode

Table 3. LDO and Step-Down Resource Power Mode

#	REGISTER BIT	INTERNAL SIGNAL	REGISTER BIT	REGISTER BIT	REGISTER BIT	ON/ OFF	POWER MODE
#	FPSSRC_Lx = 0b11 or FPSSRC_SDx = 0b11	FPS_EN_SDx or FPS_EN_LDO	PWR_MD_SDx[1] or PWR_MD_LDOx[1]	PWR_MD_SDx[0] or PWR_MD_LDOx[0]	GLBL_LPM		
1	Y	x	0	0	x	OFF	OFF
2	Y	x	0	1	1	ON	Low power
3	Y	x	0	1	0	ON	Normal
4	Y	x	1	0	x	ON	Low power
5	Y	x	1	1	x	ON	Normal
6	N	1	0	0	x	OFF	OFF
7	N	1	0	1	1	ON	Low power
8	N	1	0	1	0	ON	Normal
9	N	1	1	0	x	ON	Low power
10	N	1	1	1	x	ON	Normal
11	N	0	x	x	x	OFF	OFF

Table 4. 32k Resource Power Mode

#	REGISTER BIT	REGISTER BIT	REGISTER BIT	ON/OFF	POWER MODE
#	PWR_MD_32K[1]	PWR_MD_32K[0]	GLBL_LPM		

Table 4. 32k Resource Power Mode (continued)

1	0	0	x	OFF	OFF
2	0	1	1	ON	Low-power mode
3	0	1	0	ON	Low-jitter mode (Normal mode)
4	1	0	x	ON	Low-power mode
5	1	1	x	ON	Low-jitter mode (Normal mode)

Detailed Description—Flexible Power Supply (FPS)

Power-Off Event Recorder

Several events within a MAX77714 based system can autonomously cause a power-off (i.e., global shutdown). The source of the power-down event is recorded in a register so that when the system's microprocessor powers on again it can determine the source of the previous power-off condition. Maxim recommends that as part of the software's initialization code, it checks the POERC register. This power-off event recorder register is non-volatile as long as the RTC's coin cell (BBATT) remains within its valid voltage range. Unlike most interrupt registers, the POERC register does not have a corresponding interrupt mask and status register. Additionally, it does not affect the nIRQ pin. No status register is provided since all POERC events result in a global shutdown which would subsequently reset any related status. Once a bit is set, the controller has to write a 1 to clear it.

Flexible Power Sequencer (FPS)

The FPS allows each regulator to power-up under hardware or software control. Additionally, each regulator can power on independently or among a group of other regulators with an adjustable power-up and power-down delays (sequencing). GPIO0, GPIO1, GPIO2, and GPIO7 can be programmed to be part of a sequence allowing external regulators to be sequenced along with internal regulators. nRST_IO can be programmed to be part of a sequence.

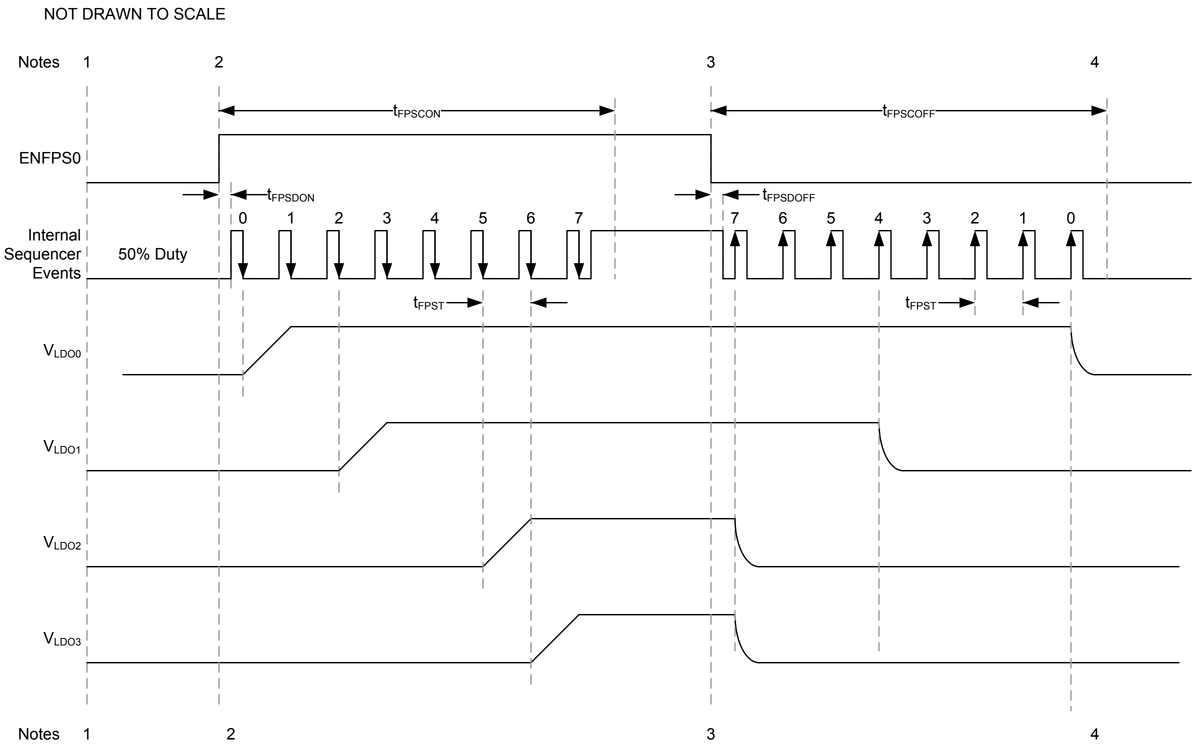
(Figure 10) shows LDO0, LDO1, LDO2, and LDO3 powering up under the control of flexible power sequencer 2.

The time period between each sequencer event for power-up, power-down, sleep entry, and sleep exit can be configured by setting MSTR_PU[2:0], MSTR_PD[2:0], MSTR_SLPENTY[2:0], and MSTR_SLPEXT[2:0] respectively.

The flexible sequencing structure consists of two hardware enable inputs (EN0, EN1), and three master sequencing timers. Each master-sequencing timer is programmable through its configuration register to have a hardware enabled source or a software enabled source (CNFG_GLBLx). When enabled/disabled the master-sequencing timer generates eight sequencing events. The time period between each event is programmable within the configuration register.

Each regulator, GPIO0, GPIO1, GPIO2, GPIO7 and nRST_IO has a flexible-power-sequence slave register (FPS_x) which allows its enable source to be specified as a flexible-power-sequence timer or a software bit. When a FPSSRCx specifies the enable source to be a flexible power sequencer, the power-up and power-down delays are configured by MSTR_PU[2:0] and MSTR_PD[2:0] and can be specified in that regulator's flexible-power-sequencer configuration register.

If any of the FPS hardware inputs (EN0, EN1) are not needed, connect them to ground. Grounding these inputs when they are not needed ensures that they do not accidentally turn on any voltage regulators—furthermore it improves the thermal impedance of the MAX77714 package.



1) LDO0, LDO1, LDO2, and LDO3 are off. Each LDO's enable register selects active discharge enabled and FPS0 as the enable source. Each LDO's flexible sequencer configuration register is programmed with the power-up and power-down timing delays as shown in the figure. The CNFGFPS2 register selects the ENFPS0 bit as the enable source.
2) The ENFPS0 bit is set high which initiates eight internal power-up sequencing events. Each regulator is enabled at the sequencing event that corresponds to its flexible sequencer configuration register.
3) The ENFPS0 bit is cleared to low which initiates eight internal power-down sequencing events. Each regulator is disabled at the sequencing event that corresponds to its flexible sequencer configuration register.
4) LDO0, LDO1, LDO2, and LDO3 are off.

Figure 10. Flexible Power Sequencer

Features

- Two Sequencers
- Power-Up/Down Sequencing Control
- Eight Power-Up Sequence Time Slots
- Eight Power-Down Sequence Time Slots
- Adjustable Time Period Between Time Slots from 31μs to 3,904μs in Eight Binary Weighted Steps
- Sequence Enable/Disable can be Controlled by Hardware and Software
- Capable of Controlling:
  - All Regulators
  - GPIO0, GPIO1, GPIO2, and GPIO7
  - nRST_IO

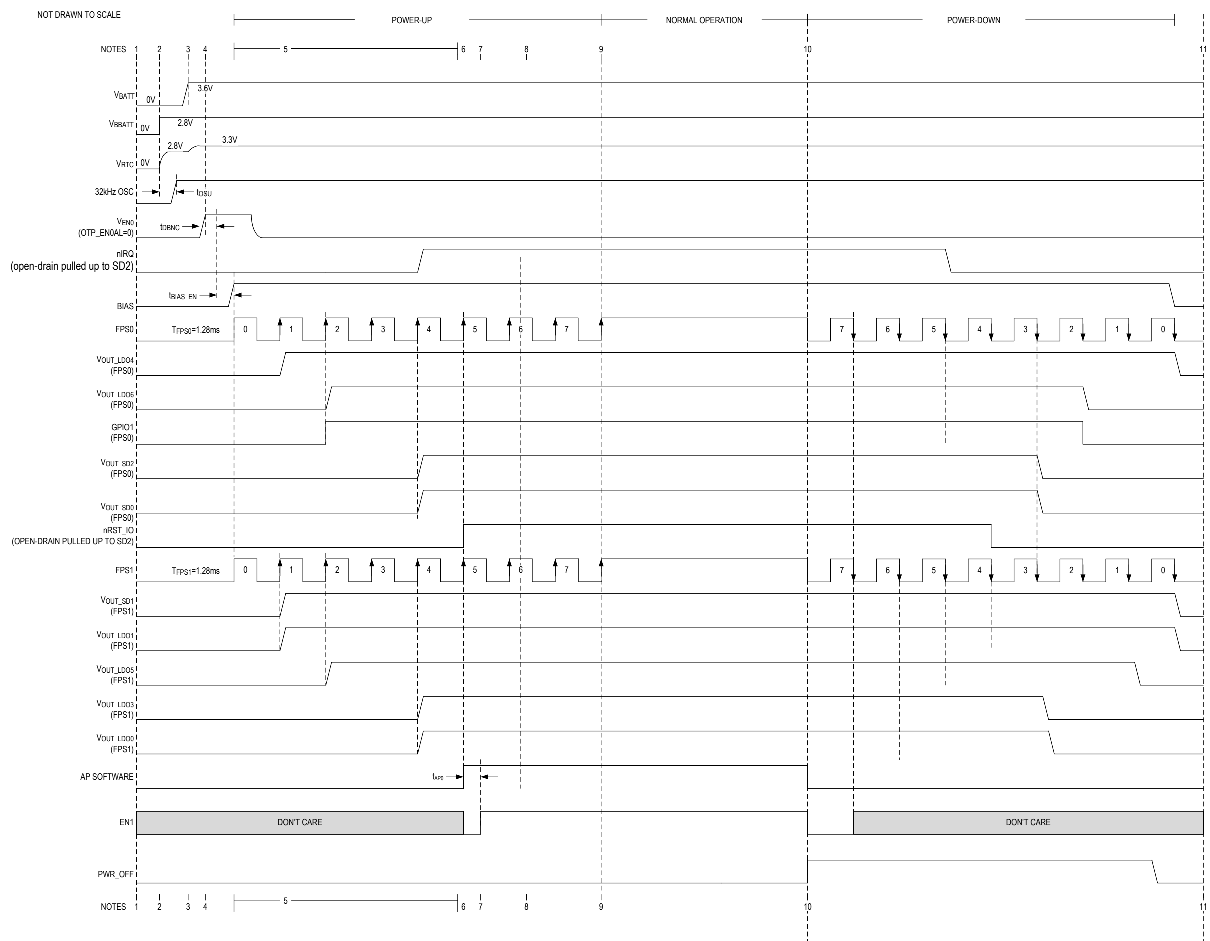
FPS0

Flexible Power Sequencer 0 is the enable signal for the resources that need to be enabled when the AP is in its normal operating mode and its sleep mode. When the AP is in normal operating mode, both FPS0 and FPS1 are enabled.

FPS1

Flexible Power Sequencer 1 is the enable signal for the resources that need to be enabled when the AP is in its normal operating mode **and disabled when the AP is in sleep mode.** When the AP is in normal operating mode, both FPS0 and FPS1 are enabled.

FPS Sequence Power-Up/Down



1) THE AP AND ENTIRE SYSTEM IS OFF WITH NO BACKUP BATTERY AND NO MAIN BATTERY INSTALLED.
2) A HALF-CHARGED LITHIUM MANGANESE CELL IS INSTALLED FROM BBATT TO GND. V_{RTC} RISES TO ~V_{BBATT}. THE RTC RELATED PORTION OF THE I²C REGISTER MAP POWERS UP TO ITS DEFAULT VALUE. THE OSCILLATOR STARTS TO FUNCTION AND THE RTC BLOCK BEGINS TO FUNCTION.
3) THE MAIN BATTERY IS CONNECTED. V_{RTC} RISES UP TO ITS 3.3V REGULATION LEVEL. THE BACKUP-BATTERY CHARGER DEFAULTS TO "ON" WITH A 2.5V REGULATION THRESHOLD. THE NON-RTC RELATED I²C REGISTERS GO TO THEIR DEFAULT VALUES.
4) AN EXTERNAL EVENT PULLS EN0 HIGH. THE DEVICE DEBOUNCES EN0 AND STARTS THE BIAS FOLLOWED BY FPS0 AND FPS1.
5) FPS0 STARTS THE FUNDAMENTAL REGULATORS AT THE SAME TIME AS FPS1 STARTS THE SECONDARY REGULATORS.
6) FPS0 DEASSERTS NRST_IO ON ITS RISING EDGE #4. WITH NRST_IO HIGH, THE AP STARTS RUNNING SOFTWARE.
7) AP ASSERTS EN1. EN1 KEEPS THE FPS1 REGULATORS ENABLED.
8) WITH SD0 ENABLED, THE AP CONTINUES TO RUN SOFTWARE. IT CHECKS THE NIRQ INTERRUPT CAUSING NIRQ TO GO HIGH. IT POWERS UP THE "OTHER" RESOURCES OF THE DEVICE AS REQUIRED.
9) THE AP AND ENTIRE SYSTEM ARE ON IN NORMAL OPERATING MODE.
10) WITH ALL THE OPTIONAL RESOURCES POWERED DOWN, THE AP SETS TO "OFF" BIT AND PULLS EN1. THE OFF BIT STARTS THE POWER DOWN SEQUENCE OF FPS0 AND EN1 LOW STARTS THE POWER DOWN SEQUENCE OF FPS1.
11) AFTER THE FPS0 AND FPS1 POWER DOWN SEQUENCES ARE FINISHED, THE BIAS TURNS OFF AND THE AP IS OFF.

Figure 11. FPS Sequence Power-Up/Down

FPS Sequence Sleep Entry/Exit

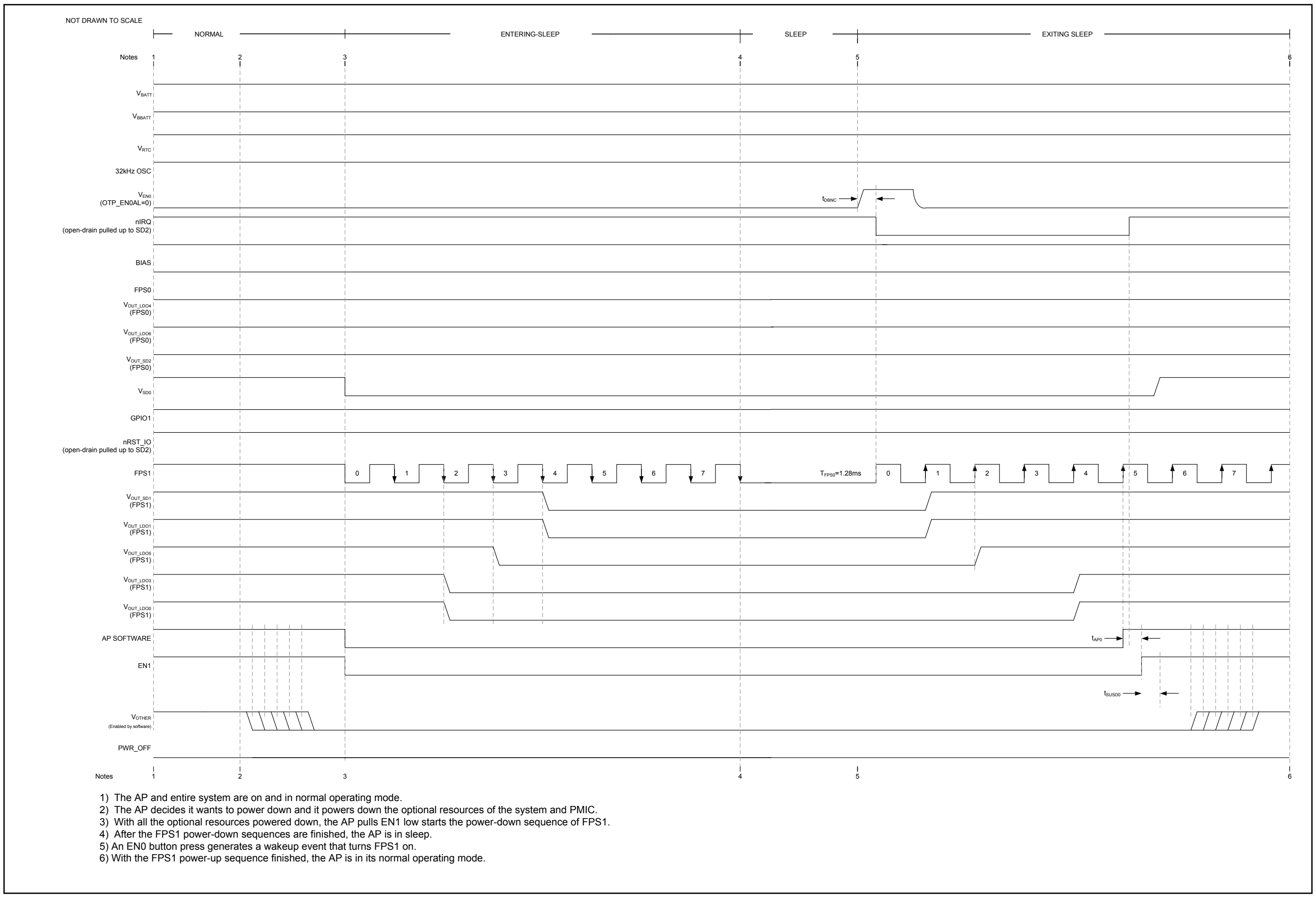


Figure 12. FPS Sleep Entry/Exit

Detailed Description—Step-Down Regulators (SD0–4A Output)

SD0 is a step-down converter with the following features:

- Programmable output voltage from 0.26V to 1.52V in 10mV steps.
- ±2% Initial output accuracy.
- Capable of 4A continuous output current.
- Capable of powering up into a prebiased output.
- Automatic transition from pulse-skipping mode to fixed-frequency mode to provide high efficiency across load range.
- Programmable low-power-mode (LPM) to enable efficient low-power PMIC states.
- Programmable soft-start to minimize inrush current.
- Inductor current limits to limit power output to a short circuit or overload.
- Capable of active discharge.
- Programmable brownout and over-voltage comparators.

Active Discharge

- When the active discharge feature is enabled (SD0ADDIS = 0) and the step-down is disabled (either through I^{2}C or by the sequencer), there is a 100Ω active discharge resistance that is enabled from the output to ground.

Output Monitoring

SD0 has multiple ways of ensuring the health of its output.

- There is a programmable brownout monitor that sets an interrupt flag (SD0_UV_I) when the output voltage falls below the programmed brownout threshold.
  - If the SD0_UV_M mask bit is unmasked, this allows the brownout on the output of the step-down to initiate a power-down sequence.
  - When the step-down is first enabled, either through I^2C or by the sequencer, the brownout condition is not be asserted until the soft-start is complete. However, if the output capacitance is large enough, the soft-start process completes before the output reaches the rising UV threshold and thereby the UV interrupt would get set, although the output would eventually rise above the UV threshold.
  - However, when the output voltage target is increased through I^2C (write to SD0VOUT[6:0]) and the step-down converter is in the process of performing the controlled ramp to the new target, a brownout condition is not triggered until the controlled ramp is complete.
- There is a programmable overvoltage monitor that sets an interrupt flag (SD0_OV_I) when the output voltage rises above the programmed overvoltage threshold.
  - If the SD0_OV_M mask bit is unmasked, this allows the overvoltage on the output of the step-down to initiate a power-down sequence and assert the nIRQ output.
  - However, when the output voltage target is decreased through I^2C (write to SD0VOUT[6:0]) and the step-down converter is in the process of performing the controlled ramp to the new target (if SD0FSREN = 1), an overvoltage condition is not triggered until the controlled ramp is complete. Note that if the controlled ramp for decreasing output voltage target is disabled (SD0FSREN = 0), then the over-voltage condition triggers and causes a power down sequence if unmasked (SD0_OV_M = 0). If this situation is expected, it is recommended to mask it by setting SD0_OV_M to 1.
  - When the step-down is first enabled, either through I^2C or by the sequencer, it is possible that the combination of the programmed soft-start ramp rate (SD0SSRAMP) and the output capacitance is such that it can cause the inductor current to reach the PMOS peak current limit.
  - Similarly, when the output voltage target is increased (by a write to SD0VOUT[6:0]) and the slew rate for dynamic voltage scaling is high enough (SD0SSRAMP), it can cause the inductor current to reach the PMOS peak current limit.
- All of the above conditions have associated status bits that provide a real-time status of the condition.

Enable and Power Mode Control

- SD0 can be enabled and disabled either by the flexible power sequencer or by I^2C.
- The SD0FPS register configures if it is part of the sequence, and the master and slots numbers that it is assigned to.
- The bits PWR_MD_SD0[1:0] control whether the step-down is in normal-power mode or low-power mode.
  - The step-down can be configured to dynamically transition to low-power mode when the PMIC transitions to the DevSlp state.
  - The step-down can also be forced to transition to low-power mode through an I^2C command. See (Table 3) in the Resource Power Mode section for additional information.

PCB Layout Guidelines

Careful circuit board layout is critical to achieve low-switching power losses and clean, stable operation.

When designing the PCB, follow these guidelines:

1. Place the inductor and output capacitor close to the device and keep the loop area of switching current small.
2. When wiring the high current paths, short and wide traces should be used. For example, the trace between LX and the inductor. The voltage on this node is switching very quickly and additional area creates more radiated emissions.
3. The ground loop for the input and output capacitor should be as small as possible.
4. AGND should be connected to PGND through a via. Connect DGND and AGND together at the return terminal of the output capacitor. Do not connect them anywhere else.
5. Keep the power traces and load connections short and wide. This practice is essential for high-efficiency.
6. The feedback pin should be routed away from the switching node to increase noise immunity. This pin is a high-impedance input which is highly noise sensitive.
7. When possible, ground planes and traces should be used to help shield the feedback signal and minimize noise and magnetic interference.

Detailed Description—Step-Down Regulators (SD1–3A Output)

SD1 is a step-down converter with the following features:

- Programmable output voltage from 0.26V to 1.52V in 10mV steps.
- ±2% Initial output accuracy.
- Capable of 3A continuous output current.
- Capable of powering up into a prebiased output.
- Automatic transition from pulse-skipping mode to fixed-frequency mode to provide high-efficiency across load range.
- Programmable low-power mode (LPM) to enable efficient low-power PMIC states.
- Programmable soft-start to minimize inrush current.
- Inductor current limits to limit power output to a short circuit or overload.
- Capable of active discharge.
- Programmable brownout and over-voltage comparators.

Active Discharge

- When the active discharge feature is enabled (SD1ADDIS = 0) and the step-down is disabled (either through I^2C or by the sequencer), there is a 100Ω active discharge resistance that is enabled from the output to ground.

Output Monitoring

SD1 has multiple ways of ensuring the health of its output.

- There is a programmable brownout monitor that sets an interrupt flag (SD1_UV_I) when the output voltage falls below the programmed brownout threshold.
  - If the SD1_UV_M mask bit is unmasked, this allows the brownout on the output of the step-down to initiate a power-down sequence.
  - When the step-down is first enabled, either through I^2C or by the sequencer, the brownout condition is not asserted until the soft-start is complete. However, if the output capacitance is large enough, the soft-start process completes before the output reaches the rising UV threshold and thereby the UV interrupt would get set, although the output would eventually rise above the UV threshold.
  - However, when the output voltage target is increased through I^2C (write to SD1VOUT[6:0]) and the step-down converter is in the process of performing the controlled ramp to the new target, a brownout condition is not triggered until the controlled ramp is complete.
- There is a programmable overvoltage monitor that sets an interrupt flag (SD_OV_I) when the output voltage rises above the programmed overvoltage threshold.
  - If the SD1_OV_M mask bit is unmasked, this allows the overvoltage on the output of the step-down to initiate a power-down sequence and assert the nIRQ output.
  - However, when the output voltage target is decreased through I^2C (write to SDVOUT[6:0]) and the step-down

converter is in the process of performing the controlled ramp to the new target (if SD1FSREN = 1), an overvoltage condition is not triggered until the controlled ramp is complete. Note that if the controlled ramp for decreasing output voltage target is disabled (SD1FSREN = 0), then the over-voltage condition triggers and could cause a power-down sequence if unmasked (SD1_OV_M = 0). If this situation is expected, it is recommended to mask it by setting SD1_OV_M to 1.
  - When the step-down is first enabled, either through I²C or by the sequencer, it is possible that the combination of the programmed soft-start ramp rate (SD1SSRAMP) and the output capacitance is such that it can cause the inductor current to reach the PMOS peak current limit.
  - Similarly, when the output voltage target is increased (by a write to SD1VOUT[6:0]) and the slew rate for dynamic voltage scaling is high enough (SD1SSRAMP), it can cause the inductor current to reach the PMOS peak current limit.
- All of the above conditions have associated status bits that provide a real-time status of the condition.

Enable and Power Mode Control

- SD1 can be enabled and disabled either by the flexible power sequencer or by I²C.
- The SD1FPS register configures if it is part of the sequence, and the master and slots numbers that it is assigned to.
- The bits PWR_MD_SD1[1:0] control whether the step-down is in normal-power mode or low-power mode.
  - The step-down can be configured to dynamically transition to low-power mode when the PMIC transitions to the DevSlp state.
  - The step-down can also be forced to transition to low-power mode through an I²C command. See (Table 3) in the *Resource Power Mode* section for additional information.

Detailed Description—Step-Down Regulators (SD2/3–2A Output)

SD2 and SD3 are step-down converters with the following features:

- Programmable output voltage from 0.600V to 2.194V in 6.25mV steps for SD2.
- Programmable output voltage from 0.600V to 3.78V in 12.5mV steps for SD3.
- ±2% Initial output accuracy.
- Capable of 2A continuous output current.
- Capable of powering up into a prebiased output.
- Automatic transition from pulse-skipping mode to fixed-frequency mode to provide high-efficiency across load range.
- Programmable low-power mode (LPM) to enable efficient low-power PMIC states.
- Soft-start to minimize inrush current.
- Inductor current limits to limit power output to a short circuit or overload.
- Programmable brownout and over-voltage comparators.

Output Monitoring

SD2 and SD3 have multiple ways of ensuring the health of their output.

- There is a programmable brownout monitor that sets an interrupt flag (SD2_UV_I/SD3_UV_I) when the output voltage falls below the programmed brownout threshold.
  - If the SD2_UV_M/SD_UV_M mask bit is unmasked, this allows the brownout on the output of the step-down to initiate a power-down sequence.
  - When the step-down is first enabled, either through I²C or by the sequencer, the step-down's control circuit attempts to ramp the output voltage as fast as possible to the target output (programmed by SDVOUT[7:0]/SD3VOUT[7:0]) limited only by the PMOS peak current limit. During this process of output voltage ramp, the brownout output is prevented from being triggered until the end of the soft-start period (determined by the specified ramp-up slew rate). However, if the output capacitance is large enough, the soft-start process completes before the output reaches the rising UV threshold and thereby the UV interrupt would get set, although the output would eventually rise above the UV threshold.
  - When the output voltage for SD2 or SD3 is increased through I²C (programmed by SD2VOUT[7:0]/SD3VOUT[7:0]) after they have been enabled, the step-down control circuit changes the

output voltage target directly to the final value. In such a case, the brownout comparator provides an undervoltage assertion. If the undervoltage assertion is not masked by SD2_UV_M/SD3_UV_M, a power-down sequence occurs. If such a use case is foreseen, it is recommended to set the mask bits first and then change the output voltage. Alternatively, the change in output voltage should be done in small steps. Note that even if the mask bit is set, the corresponding interrupt bit is still set.
    - Note that a load transient on the output of the step-down at a fast slew rate and a large magnitude has the capability to cause an output voltage droop that can cause the UV comparator to trip and flag an undervoltage event, if the brownout threshold is set high (such as 90%).
- There is a programmable overvoltage monitor that sets an interrupt flag (SD2_OV_I/SD3_OV_I) when the output voltage rises above the programmed overvoltage threshold.
    - If the SD2_OV_M/SD3_OV_M mask bit is unmasked, this allows the overvoltage on the output of the step-down to initiate a power-down sequence.
    - When the step-down is first enabled, either through I^2C or by the sequencer, the step-down control circuit attempts to ramp the output voltage as fast as possible to the target output (programmed by SD2VOUT[7:0]/SD3VOUT[7:0]) limited only by the PMOS peak current limit. During this process of output voltage ramp, the over-voltage output is prevented from being triggered until the end of the soft-start period (determined by the specified ramp-up slew rate).
    - When the output voltage for SD2 or SD3 is increased through I^2C (programmed by SD2VOUT[7:0]/SD3VOUT[7:0]) after they have been enabled, the step-down's control circuit changes the output voltage target directly to the final value. The step-down output voltage increases as a function of the output capacitance and load. In such a case, the over-voltage comparator provides an over-voltage assertion. If the overvoltage assertion is not masked by SD1_OV_M/SD1_OV_M, a power-down sequence occurs. If such a use case is foreseen, it is recommended to set the mask bits first and then change the output voltage. Alternatively, the change in output voltage should be done in small steps. Note that even if the mask bit is set, the corresponding interrupt bit is still set.
    - Note that a sudden load release with a high slew rate and magnitude has the potential to cause a momentary over-shoot on the output of the step-down that can trip the OV comparator output. If such use cases are expected, the OV threshold should be set as high as allowed.
- All of the above conditions have associated status bits that provide a real-time status of the condition.

Enable and Power Mode Control

- SD2/3 can be enabled and disabled either by the flexible power sequencer or by I^2C.
- The SD2FPS/SD3FPS registers configure if it they are part of the sequence, and the master and slots numbers that they are assigned to.
- The bits PWR_MD_SD2[1:0]/PWR_MD_SD3[1:0] control whether the step-down is in normal-power mode or low-power mode.
    - The step-down can be configured to dynamically transition to low-power mode when the PMIC transitions to the DevSlp state.
    - The step-down can also be forced to transition to low-power mode through an I^2C command. See (Table 3) in the *Resource Power Mode* section for additional information.

Active Discharge Resistor

SD2/3 have an active-discharge resistance that can be enabled and disabled with SDxADDIS. Enabling the active discharge feature helps ensure a complete and timely power-down of all system peripherals. The default condition of the active-discharge resistor feature is enabled, such that when the step-down converter is disabled, an internal 100Ω discharge resistor is connected to the output to discharge the energy stored in the output capacitor. When the step-down converter is enabled, the discharge resistor is disconnected from the output.

Soft-Start

The SD2/3 regulators have a soft-start feature to limit the inrush current during startup. The soft-start feature is achieved by limiting the slew rate of the output voltage during startup (dV_{OUT_SDx}/dt).

During soft-start the output voltage for the regulator ramps at a fixed rate of 17mV/µs to its final value. The soft-start time(µs) is calculated by V_{OUT_SDx}/17mV.

If V_{OUT_SDx} = 1.8V, the startup time is 105µs.

Register and Reset Conditions

See the *PMIC Register* section for additional information.

Detailed Description—150mA PMOS LDO (LDO2, LDO4, LDO5, LDO6)

The MAX77714 has nine linear regulators (LDOs).

The four NMOS regulators are capless designs that are stable with or without an output decoupling capacitor. Additionally, the PMOS regulators have adjustable compensation that allows for the use of remote output capacitors.

All regulators can be operated in low-power mode, where the no-load quiescent current drops to 1.5mA. In low-power mode, each output supports a maximum load of 5mA.

All regulators have an output voltage power-OK interrupt signal that is integrated into the MAX77714 interrupt architecture.

Features and Benefits

- Nine Linear Regulators
  - General Performance
    - ±3% Output Accuracy LDOx and ±4.5% for LDO4 (0.4V) Over Load/Line/Temperature
    - 50mV Dropout at Full Load
    - 63dB PSRR at 10kHz
    - 1.5mA Low-Power Mode
    - Short-Circuit and Thermal-Overload Protection
    - Dynamically Programmable Output Voltage
    - Power-OK Interrupt
    - Programmable Soft-Start Rate: 100mV/µs or 5mV/µs
  - Soft-Start into Prebiased Output
  - Four N-Channel Regulators (LDO0/1/7/8)
    - 0.8V to 5.5V Input Range
    - 29mA Quiescent Supply Current
    - No Output Capacitor Required in Normal Operating Mode (cap required for low-power mode)
  - Five Standard P-Channel Regulators (LDO2/3/4/5/6)
    - 1.7V to 5.5V Input Range
    - 20mA Quiescent Supply Current
    - Remote Capacitor Design with Register Adjustable Compensation to Optimize Transient Performance

Simplified Block Diagram

The nine LDOs of the MAX77714 are derived of five basic topologies as shown in (Table 5).

The PMOS regulators (PDRVx) operate and draw power from their power inputs (IN_LDOxx), which have a minimum operating supply voltage of 1.7V (V_{IN_LDOx}). The control registers and some input circuitry operate from the main system supply (MBATT) and hold their contents when the regulator input voltage (V_{IN_LDOx}) drops to 0V.

The NMOS regulators (NDRVx) gate drive operates from the main system supply (MBATT), while the load current is provided by the regulator input (IN_LDOxx). The input voltage (V_{IN_LDOx}) for the NMOS regulators extends down to 0.8V. To provide adequate gate drive for the NMOS output device, the NMOS output voltage should be more than 1.5V lower than the main system supply voltage (V_{MBATT}). The control registers are also powered from MBATT.

NMOS regulators works into dropout with the V_{IN_LDOx} to V_{OUT_LDOx} voltage determined by I_{LOAD} x R_{DO} where R_{DO} is the dropout resistance (typically 200mW). As dropout voltage decreases (by reducing load) below 0.3V, the PSRR and load regulation degrades.

All PMOS regulators are compensated at their output and require a remote output capacitance large enough to prevent oscillation. The NMOS regulators are internally compensated, but an additional output capacitor can be added to improve immunity to high-frequency noise and allow stable low-power mode operation. See the *Output Capacitor Selection* section for additional information.

Table 5. Basic LDO Topologies

NAME	DESCRIPTION	LDO
PDRV1	Power Device: PMOS Output Current: 150mA	LDO2, LDO4, LDO5, LDO6
PDRV2	Power Device: PMOS Output Current: 300mA	LDO3
NDRV1	Power Device: NMOS Output Current: 150mA	LDO0, LDO1
NDRV2	Power Device: NMOS Output Current: 300mA	LDO8
NDRV3	Power Device: NMOS Output Current: 450mA	LDO7

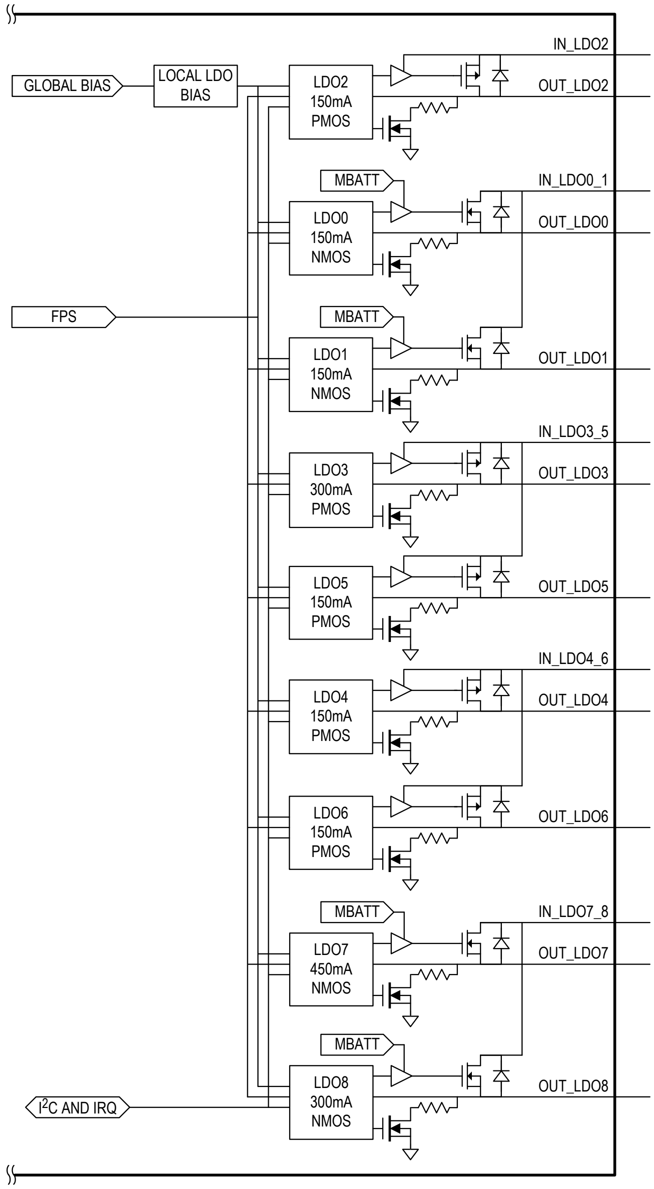


Figure 13. Linear Regulator Functional Diagram

Active-Discharge Resistor

Each linear regulator has an active-discharge resistor feature that can be enabled/disabled with ADE_Lx_. Enabling the active discharge feature helps ensure a complete and timely power-down of all system peripherals. The default condition of the active-discharge resistor feature is enabled so that whenever V_{MBATT} is below $V_{MBATTUVLO}$ all regulators are disabled with their active-discharge resistors turned on. When V_{MBATT} is less than 1.0V, the NMOS transistors that control the active-discharge resistors lose their gate drive and become open.

Input Capacitor Selection

Sufficient input bypass capacitance is required for stable operation of the LDO. Choose an effective input bypass capacitance (C_{IN_LDO}) of at least 1μF after derating. A 2.2μF ceramic capacitor is sufficient for most use cases. Larger values of C_{IN_LDO} improve the decoupling for the LDO regulator.

C_{IN_LDO} reduces the current peaks drawn from the battery or input power source during LDO regulator operation. The impedance of the input capacitor should be very low (i.e., ≤ 5mΩ + ≤ 500pH) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

As the case sizes of ceramic surface-mount capacitors decrease, their capacitance verses DC bias voltage characteristic becomes poor. Due to this characteristic, it is possible for 0603 case size capacitors to perform well while 0402 case size capacitors of the same value perform poorly. Consider the input capacitance value after initial tolerance, bias voltage, aging, and temperature derating. Maxim recommends a nominal capacitance value of 1μF which, in 0402 case size, can derate to 0.4μF.

Output Capacitor Selection

Choose the output bypass capacitance (C_{OUT_LDO}) to be 2.2μF. Larger values of C_{OUT_LDO} improve PSRR and load transient performance but increases the input surge currents during soft-start and output voltage changes.

C_{OUT_LDO} is required to keep the LDO stable. The impedance of the output capacitor should be very low (i.e., ≤ 5mΩ + ≤ 500pH) for frequencies up to 2MHz. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients.

As the case sizes of ceramic surface-mount capacitors decrease, their capacitance verses DC bias voltage characteristic becomes poor. Due to this characteristic, it is possible for 0603 case size capacitors to perform well while 0402 case size capacitors of the same value perform poorly. Consider the output capacitance value after initial tolerance, bias voltage, aging, and temperature derating. Maxim recommends a nominal capacitance value of 2.2μF which, in 0402 case size, can derate to 1.1μF.

P-Channel Linear Regulator Output Capacitor

P-channel LDOs require an output capacitor to maintain stable output voltage regulation. Adjustable compensation allows for flexibility when designing the PCB and placing the output capacitor. The default compensation is factory programmable; additionally, the compensation is register adjustable when the LDO is off.

In many LDO designs, there is little-to-no flexibility in the physical placement of the output capacitor on the PCB. However, the LDO implementation within the device provides adjustable compensation for the p-channel LDOs. This adjustable compensation allows flexibility in the placement of the output capacitor on the PCB. However, as the output capacitor is placed farther from the device, slower compensation values are required to maintain stability; these slower compensation values decrease performance.

For optimum p-channel LDO performance, place the output capacitor as close to the LDO output as possible and program COMP_Lx = 0b00. In situations were the full LDO performance is not required, the output capacitor can be place farther away from the LDO output with slower compensation values. This option becomes especially useful when the LDO output capacitor can be eliminated and the load's local input capacitor becomes the only capacitance on the LDO output node.

Warning: The COMP_Lx bits should only be changed when the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.

N-Channel Linear Regulator Output Capacitor

N-channel LDOs technically do not require and output capacitor to maintain stable output voltage regulation if they are in normal mode (i.e., they can be capless). However, a n-channel LDO does require an output capacitor to maintain stable output voltage regulation in low-power mode. In either mode (normal or low-power), the LDO performs best with an output capacitor (C_{OUTx}) as recommended in the *Output Capacitor Selection* section of the datasheet.

Note that the COMP_Lx[1:0] bits for n-channel LDOs must be set to 0b00.

Bias

A small section of bias circuitry is required to be on when any of the LDOs are enabled. LDO enable signal from the FPS OR the L_B_EN from I^2C enables the LDO bias circuits. In addition, whenever the LDO bias is enabled, the global bias for the MAX77714 is also enabled. The LDO bias circuitry takes t_{LBIAS} to turn on. If the LDO bias circuit is off and an LDO is enabled, the total time before the output starts slewing up is t_{LBIAS} + t_{LON}. If the LDO bias is on and an LDO is enabled, the total time before the output starts slewing is t_{LON}.

If the sequencing of a group of regulators is particularly important, it may be desirable to force the LDO bias to be on with the L_B_EN bit to ensure that the LDOs enables in a consistent manner with the shortest latency. Note that whenever L_B_EN is set, the global bias circuits and LDO bias circuits are enabled. The combined bias circuitry current is I_{QBIAS}. To ensure that the system always operates with the lowest quiescent current possible, it is a good idea to clear L_B_EN when it is not needed.

LDO Power Modes

Linear regulators and step-down regulators have very similar power mode controls. Each linear regulator is independently controlled with PWR_MD_Lx[1:0] and each step-down regulator is independently controlled with PWR_MD_SDx[1:0]. In addition to enable and disable control, each linear regulator has a special low-power mode that reduced the quiescent current to 1.5µA. In low-power mode, each regulator supports a load of up to 5mA ($I_{.MAXxx}$). The load regulation performance degrades proportionally with the reduced load current.

Several usage options are available for low-power mode. To force individual regulators to low-power mode, set PWR_MD_Lx to 0b10. To force a group of regulators to enter and exit low-power mode in unison, set their individual PWR_MD_Lx_ bits to 0b10. When set for this “group and/or dynamic” low-power mode, the low-power mode is enabled when the global low-power mode signal is high. The global low-power mode signal is driven by the GLBL_LPM bit or though a GPIO0.

When a linear regulator is configured to be part of a flexible power sequence (FPSSRC_Lx), the power mode bits (PWR_MD_Lx) are still used to configure low-power mode and normal-power mode, but the flexible power sequencer itself controls weather the regulator is enabled or disabled.

Soft-Start and Dynamic Voltage Scaling (DVS)

The linear regulators have a programmable soft-start rate. When a linear regulator is enabled, the output voltage ramps to its final voltage at a slew rate of either 5mV/ms or 100mV/ms, depending on the state of the SS_Lx bit. The 5mV/ms ramp rate limits the input inrush current to around 10mA on a 300mA regulator with a 2.2µF output capacitor and no load. The 100mV/ms ramp rate results in a 200mA inrush current on a 300mA regulator with a 2.2µF output capacitor and no load, but achieves regulation within 50ms. The soft-start ramp rate is also the rate of change at the output when changing dynamically between two output voltages while enabled (DVS). This includes both positive and negative output voltage transitions.

The LDO soft-start circuitry supports starting into a prebiased output. For example, if the output capacitor has an initial voltage of 0.4V when the regulator is enabled, the regulator gracefully increases the capacitor voltage to the required target voltage such as 1.2V. This is unlike other regulators without the start into prebias feature where they can force the output capacitor voltage to 0V before the soft-start ramp begins.

During a soft-start event or a DVS transition, the regulators output current increases by C_{OUT} x dV/dt. In the event that the load current plus the additional current imposed by the soft-start or DVS transition, reach the regulator’s current limit, the current limit is enforced. When the current limit is enforced, the advertised transition rate (dV/dt) does not occur.

Power-OK (POK) Comparators for Linear Regulators

Each linear regulator includes a POK comparator. The POK comparator signals (POK_Lx) indicate when each output has lost regulation (i.e., the output voltage is below V_{POKTHL}). The POK signal has a 25µs noise immunity filter ($t_{POKNFLDO}$).

When any of the POK signals (POK_Lx) go low, a maskable interrupt is generated. POK is the only interrupt available for the device's LDOs. The block level LDO interrupt register is IRQ_LVL2_Lx and the top level LDO interrupt is IRQ_LDO.

Overvoltage Clamp

Each LDO has an overvoltage clamp that allows it to sink current when the output voltage is above its target voltage. This overvoltage clamp for a given LDO is disabled when that LDO is in low-power mode. If an LDO is in normal-power mode, then the overvoltage clamp is enabled/disabled with OVCLMP_EN_Lx (default enabled). The following bulleted list briefly describes three typical application scenarios that pertain to the overvoltage clamp.

Warning: If an LDO's overvoltage clamp is disabled (OVCLMP_EN_Lx = 0), the output loading is very low (<10μA), and the junction temperature of the device is hot (>70°C) the output voltage may rise above its regulation point.

Typical application scenarios for the overvoltage clamp:

- LDOs Load Leaking Current into the LDOs Output. Some LDO loads leak current into an LDO output during certain operating modes. This is typically seen with microprocessor loads. For example, a microprocessor with 3.3V, 2.5V, 1.8V, and 1.0V supply rails is running in standby mode. In this mode the higher voltage rails can leak currents of several milliamps into the lower voltage rails. If the 1.0V rail is supplied by an LDO, the LDO output voltage rises based on the amount of leakage current. With the LDO overvoltage clamp enabled, when the output voltage rises above its target regulation voltage, the overvoltage clamp sinks current from the output capacitor, which brings the output voltage back within regulation.
- Negative Load Transient to 0A: When the LDO load current quickly ramps to 0A (i.e., 300mA to 0A load transient with 1μs transition time), the output voltage can overshoot (i.e., sore). Since the LDO cannot turn off its pass device with an intently fast load transition, the LDO output voltage overshoots. In this instance, when the output voltage sores above target regulation voltage, the overvoltage clamp sinks current from the output capacitor, which brings the output voltage back within regulation.
- Negative Dynamic Voltage Transition: When the LDO output target voltage is decreased (i.e., 1.2V to 0.8V) when the system loading is light, the energy in the output capacitor tends to hold the output voltage up. When the output voltage is above its target regulation voltage, the overvoltage clamp sinks current from the output capacitor, which brings the output voltage back within regulation.

Nontypical Applications:

There are some nontypical applications for this overvoltage clamp that are not discussed.

- Two LDO outputs can be connected together to give one output with more current capability. In this case, you typically want one LDOs output voltage to be set 1LSB higher than the other LDO. The LDO with the lower output voltage should deactivate its overvoltage clamp.
- Similar to the above, a step-down and LDO output can be connected together to give more current. In this case, the LDO output should be set lower than the step-down so that the step-down delivers the bulk of the load current (i.e., step-down is more efficient). The LDO would only become active during transient conditions or high load condiditons. In this case, the LDO overvoltage clamp should be disabled.

Detailed Description—GPIO

GPIO

The MAX77714 has eight GPIO channels. It can be configure as GPO, GPI, and also has an ALT mode.

When configured as a general purpose output (GPO), the GPO is programmable to be push-pull or open-drain. When a GPIO is configured as a general purpose output, do not enable the internal pull-up or internal pull-down resistors which corresponds with that GPO.

When configured as a general pupose input (GPI), the GPI is programmable to have either a high-impedance, 100kΩ pulldown, or 100kΩ pullup. Additionally, interrupt inputs with programmable debounce timers are available.

The GPI edge(s) that triggers interrupts are selectable with REFE_IRQx. When a GPI interrupt is enabled and the selected edge(s) are detected, EDGEx is set in the INT_LVL2_GPIO register and IRQ_GPIO is set in the top-level interrupt register. If the top-level interrupt mask is cleared (IRQ_GPIOM), the external interrupt signal nIRQ is asserted.

Alternate Mode

In addition to the GPO and GPI configurations, each GPIO has an alternate mode.

When a GPIO is in an alternate mode device may internally force the direction (i.e., output or input) and/or logic level of the GPIO. However, other options such as debounce times and rising/falling edge triggered interrupt settings are still valid in alternate mode.

Table 6. GPIO Alternate Modes

GPIOx	ALTERNATE MODES
GPIO0	Active-High, Open-Drain, Flexible Power Sequencer Output
GPIO1	Active-High, Open-Drain, Flexible Power Sequencer Output
GPIO2	Active-High, Open-Drain, Flexible Power Sequencer Output
GPIO3	ACOK input
GPIO4	32kHz Output (32K_OUT0)
GPIO5	32kHz Output (32K_OUT1)
GPIO6	32kHz Output (32K_OUT2)
GPIO7	Active-High, Open-Drain, Flexible Power Sequencer Output

Features and Benefits

- Eight GPIO
- MBATT and GPIO_INB Input Power Sources
  - Four GPIOs per input
  - Input Voltage Range from 1.7V to 5.5V
- GPI
  - GPI to ACOK
  - GPI
  - Flexible Edge Trigger Support
  - Selectable Debounce Time
  - Optional pullup/pulldown
- GPO
  - Push-Pull
  - Open-Drain
  - Four GPO programmable to Flexible Power Sequencer
  - Three GPO to 32kHz Output Option
  - 12mA Sink Current Allows for LED Drive

GPIO Programming Matrix

Table 7. GPIO Programming Matrix

GPIOx GPI									
Comment	DBNCx[1:0]	REFE_IRQx[1:0]	DOx	DIx	DIRx	PPDRVx	PUEx	PDEx	AMEx
GPI	Debounce Times	Interrupt Options	0	Input Logic Level	1 = GPI	0	0	0	0
GPI with Internal Pullup	Debounce Times	Interrupt Options	0	Input Logic Level	1 = GPI	0	1	0	0
GPI with Internal Pulldown	Debounce Times	Interrupt Options	1	Input Logic Level	1 = GPI	0	0	1	0
GPIOx GPO									
GPO Push-Pull	0	0	Output Logic Level	0	0 = GPO	1 = push-pull	0	0	0
GPO Open-Drain	0	0	Output Logic Level	0	0 = GPO	0 = open-drain	0	0	0
GPIO0/1/2/7 Alternative Mode Active-High Flexible Power Sequencer Output									
Comment	DBNCx[1:0]	REFE_IRQx[1:0]	DOx	DIx	DIRx	PPDRVx	PUEx	PDEx	AMEx
GPO Flexible Power Sequencer Output, Push-Pull	0	0	set by FPS	0	0	1 = push-pull	0	0	1
GPO Flexible Power Sequencer Output, Open-Drain	0	0	set by FPS	0	0	0 = open-drain	0	0	1
GPIO4/5/6 Alternative Mode 32kHz Output (32K_OUT1)									
Comment	DBNCx[1:0]	REFE_IRQx[1:0]	DOx	DIx	DIRx	PPDRVx	PUEx	PDEx	AMEx
GPO 32kHz Output, Push-Pull	0	0	set by XIN	0	0	1 = push-pull	0	0	1
GPO 32kHz Output, Open-Drain	0	0	set by XIN	0	0	0 = open-drain	0	0	1
GPIO3 Alternative Mode ACOK (Level Triggered)									
Comment	DBNC3[1:0]	REFE_IRQx[1:0]	DO3	DI3	DIR3	PPDRV3	PUE3	PDE3	AME3
GPI	Debounce Times	Interrupt Options	0	Input Logic Level	1 = GPI	0	0	0	1
GPI with Internal Pullup	Debounce Times	Interrupt Options	0	Input Logic Level	1 = GPI	0	1	0	1
GPI with Internal Pulldown	Debounce Times	Interrupt Options	1	Input Logic Level	1 = GPI	0	0	1	1

Detailed Description—32kHz Oscillator

The MAX77714 provides a 32kHz clock signal for the real-time clock and the central state machine. The 32kHz clock signal is derived from either an external 32kHz crystal or an external 32kHz clock source.

Features: 32kHz Oscillator

- Low-jitter mode reduces cycle-to-cycle jitter to 15ns
- Low-power mode lowers power consumption
- Dedicated clock output, additional outputs selectable as GPIO alternate modes
- Allows use of board-mounted crystal ballast capacitors or on-chip crystal ballast capacitors
- Internal ballast capacitor options support 6.5pF, 7.5pF, and 12.5pF crystals
- Bypass mode supports external clock input
- Backup silicon oscillator allows continued functionality if crystal fails

Operation Modes

The MAX77714 32kHz oscillator supports two hardware configurations, selectable by an OTP option. In normal mode, the oscillator drives an external crystal to derive a 32kHz clock signal. In bypass mode, the oscillator accepts a 32kHz square wave from an external clock source. CRYSTAL_CONFIG indicates the active operation mode.

In bypass mode, the oscillator buffers and passes through the input clock. The frequency detector detects abnormally low or high frequencies (below fDET_MIN and above fDET_MAX), but does not consider duty cycle or jitter.

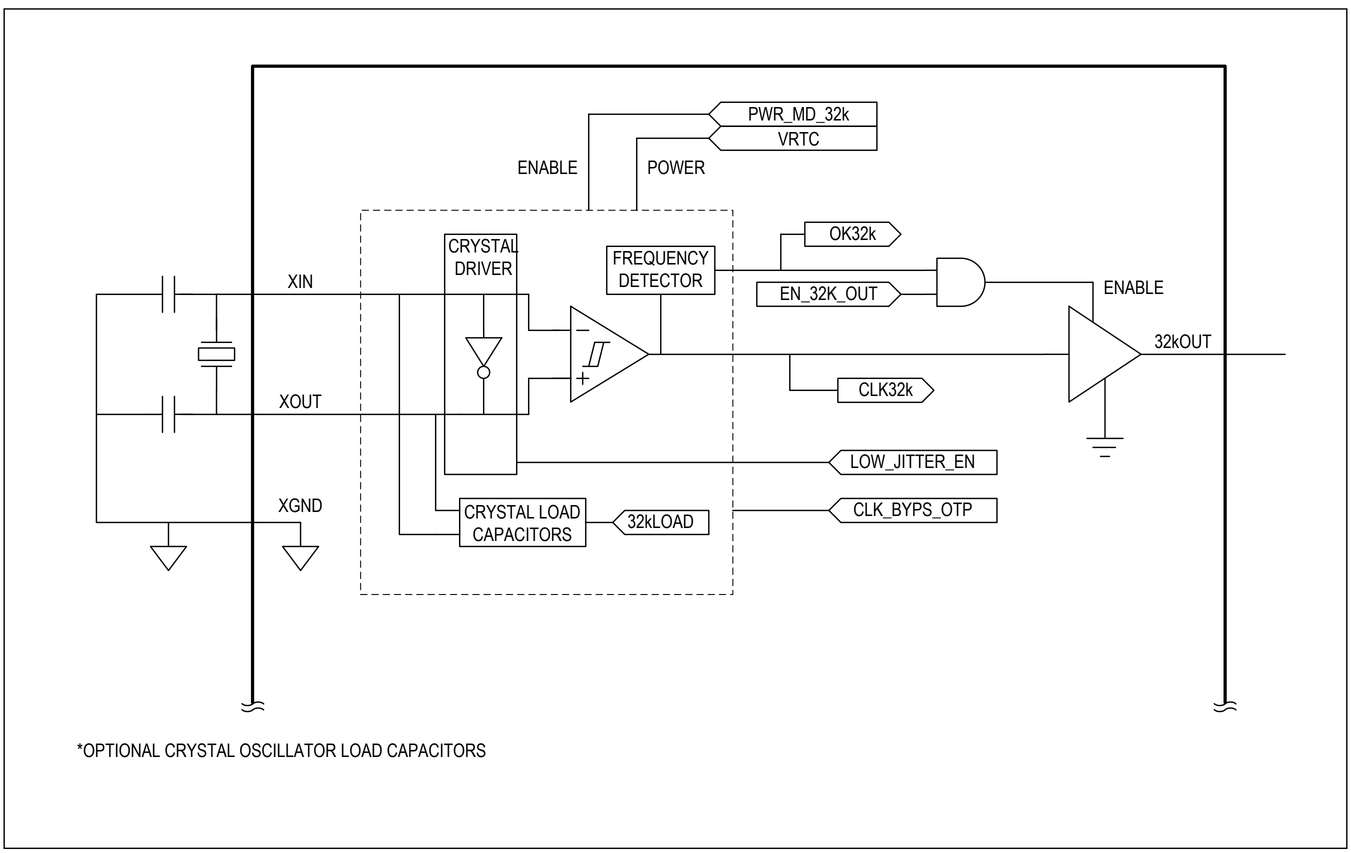


Figure 14. Block Diagram—32kHz Normal-Mode Operation

Low-Jitter Mode and Low-Power Mode

The crystal driver features two modes of operation: low-power mode and low-jitter mode. In low-jitter mode, the crystal driver current consumption is 24µA which allows for 15ns cycle-to-cycle jitter (tJIT_LPM) and duty cycle to between 45% and 55%. In low-power mode, the crystal driver current consumption is low (IOSC_LPM, 1.5µA) which corresponds to an increased cycle-to-cycle jitter and wider duty cycle (40% to 60%).

Power mode control is independently managed by the ON/OFF Controller based on the system state (ACTIVE, HIBERNATE, and STANDBY). When a system state transition occurs, the crystal driver automatically changes power mode as configured with 32K_LJ_x.

Internal Ballast Capacitors

The crystal driver has four options for internal ballast capacitance, selectable with an OTP option (32KLOAD_OTP). (Table 8) shows the total crystal load capacitance (internal and external) for common configurations. XIN and XOUT typically have 3pf of parasitic capacitance each (C_{PAR}) which factors in the total load capacitance calculation. For any internal and external load capacitance configuration, C_{LOAD} can be calculated using the formula $C_{LOAD} = (C_{INT} + C_{EXT} + C_{PAR}) / 2$.

For prototyping purposes, the internal load capacitance can be changed using test register access. Changing the internal load capacitance while the system is in operation is not recommended.

Table 8. 32kHz Crystal Oscillator Load Capacitance

32KLOAD	PARASITIC CAPACITANCE FROM XIN TO GND and XOUT TO GND (C_{PAR})	INTERNAL LOAD CAPACITANCE FROM XIN TO GND AND XOUT TO GND (C_{INT})	EXTERNAL LOAD CAPACITANCE FROM XIN TO GND AND XOUT TO GND (C_{EXT})	TOTAL LOAD CAPACITANCE ON THE CRYSTAL (C_{LOAD})
0b00	3pF	None	10pF	6.5pF
0b00	3pF	None	12pF	7.5pF
0b00	3pF	None	22pF	12.5pF
0b01	3pF	10pF	None	6.5pF
0b10	3pF	12pF	None	7.5pF
0b11	3pF	22pF	None	12.5pF

Buffered Output

The oscillator clocks a dedicated 32kHz buffered output (32KOUT) which provides a low-jitter 32kHz clock source to the system. The buffer is configurable to be either a push-pull, or open-drain output stage. The supply for the push-pull output stage is configurable to be one of three voltage rails: LDO12, BUCK3 or LSW1 (V32KOUT). For the buffered output to meet the low-jitter spec (t-JIT_LPM), the following conditions must be satisfied:

- The primary oscillator must generate the 32kHz clock (32KSOURCE = 0).
- If a crystal is used (normal mode), the oscillator must be configured for low-jitter operation.
- If an external clock is used (bypass mode), the external clock must meet the low-jitter spec.
- The buffer must be configured for the push-pull output stage.

Additional 32kHz outputs are available from GPIO alternative modes; see the GPIO section for more information.

The FBB3 and LSW1 supply inputs to the buffer can be unpowered when their respective inputs are disabled. In such cases, the unpowered inputs are not backpowered from the powered inputs. Before enabling the buffer (EN32KOUT = 1), the selected supply must have reached its programmed output voltage; otherwise, runt pulses may appear at 32KOUT.

Silicon Oscillator

The MAX77714 includes a silicon oscillator which permits continued system operation in the event that the crystal oscillator fails. The silicon oscillator has reduced accuracy and higher jitter than a crystal oscillator and is not suitable for timekeeping or applications requiring low jitter; however, it offers greater reliability than the crystal oscillator and is sufficiently accurate for continued operation of device's core functionality.

During normal operation, the device derives its 32kHz clock from the crystal oscillator or internal silicon oscillator depending on the oscillator OTP selection. There are two conditions that cause it to use the silicon oscillator instead: if the crystal oscillator fails to start up in a timely manner, or if it fails during operation. The latter case results in an asynchronous reset of all registers in the device. In both cases, the device generates an interrupt (XTAL_FAIL_I) to notify the AP that a crystal fault caused the device to start up and operate using the silicon oscillator.

Once the system is operating with the silicon oscillator, software can periodically check XOSCOK to see if the crystal has restabilized. If software determines that the crystal is stable enough to use, it can set XOSC_RETRY to initiate a glitchless transition back to the crystal oscillator. If the crystal oscillator is not OK (XOSCOK = 0), the transition does not occur.

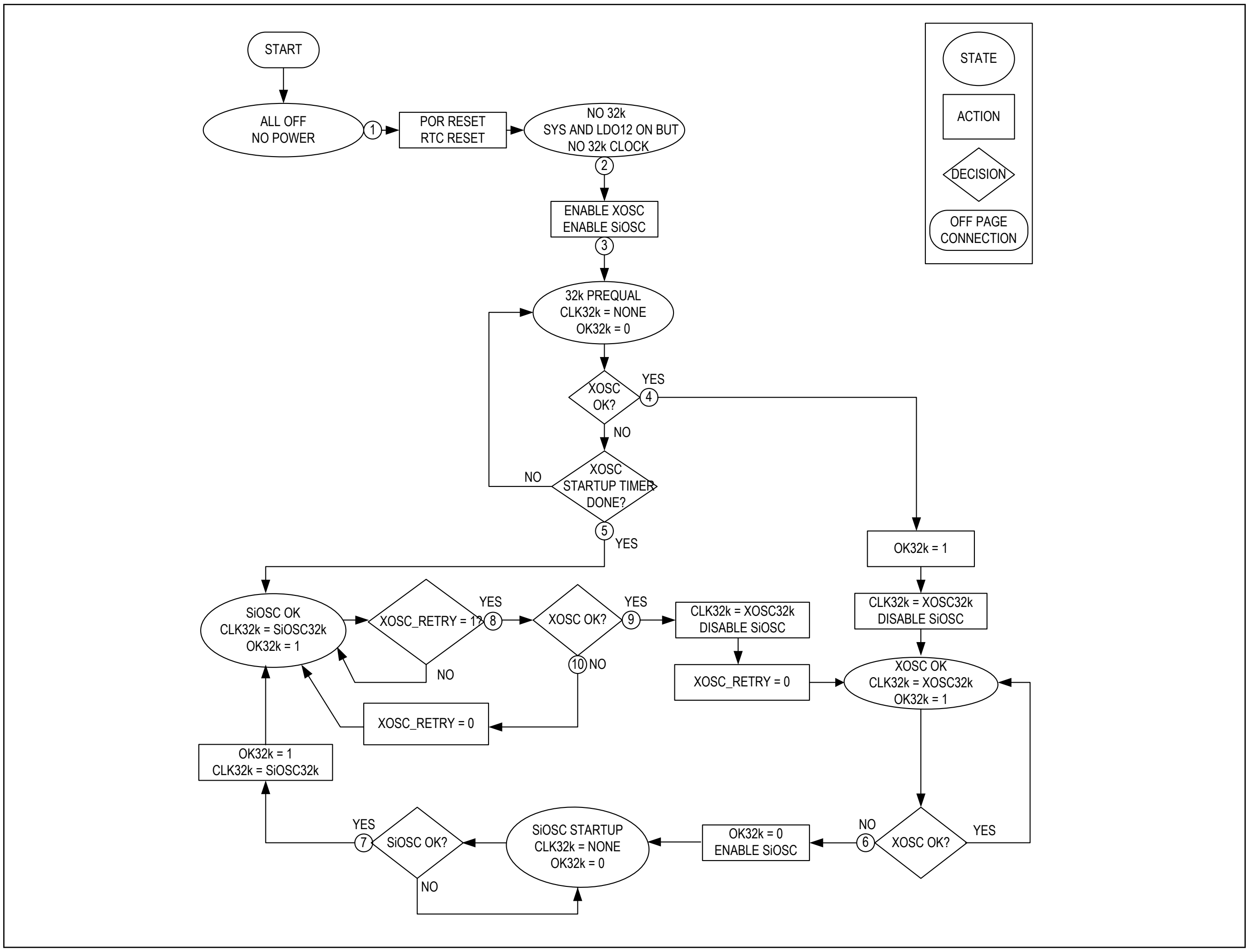


Figure 15. Flow Chart—Silicon Oscillator

Detailed Description—Backup Battery Charger

The backup battery charger is a constant voltage (CV) and constant current (CC) style charger with a series output resistance. The backup battery charger is enabled and disabled with BBCEN. The charge current, charger voltage, output current, and output resistance are adjustable with the CNFG_BBC register. The backup battery charger is suitable for the following types of backup cells:

- Super capacitor (a.k.a., gold cap, double-layer electrolytic)

- Standard capacitors (tantalum, electrolytic, ceramic)
- Rechargeable lithium manganese cells

Features

- 800μA maximum CC-CV backup battery charger.
- 2.5V to 3.5V adjustable backup battery setting with ± 3% tolerance.
- Seamless transition of RTC supply from V_{MBATT} to V_{BBATT} when V_{MBATT} drops below V_{MBATT_UVLO} threshold.

Detailed Description—Real-Time Clock (RTC)

The real-time clock (RTC) is responsible for keeping track of the time. It records seconds, minutes, hours, days, months, and years with a calendar structure that accounts for leap years. The RTC is further equipped with two alarms and has a host of maskable capabilities.

Through a set of configuration registers, various modes of operation are possible. RTC supports both “Binary”, and “Binary Coded Decimal”, and supports features such as AM/PM, and 24/12 modes of operation. Additional sudden momentary power loss (SMPL) is available.

Features

- Gregorian Calendar with Leap Year Correction
- Two Alarms
- Maskable Interrupts
  - 1s and 60s
  - Alarm 1 & 2
  - SMPL
- Binary and BCD Modes
- 12/24 Hour Modes
- Sudden Momentary Power Loss (SMPL)
- Double Buffered Read/Write Registers Allows Asynchronous Register Access
- Operates down to 1.71V

Writing to RTC

In order to safely write to various registers on-board the RTC, all RTC registers (except RTCINT register, bit 0 of UPDATE0 register, and bit 4 of UPDATE0 register) have a corresponding “Write Buffer”. When the user writes to the RTC, the user is actually performing a write to these “Write Buffers”. Therefore, in writing to RTC there are two steps needed to update a particular register or set of registers:

1. User writes desired value(s) to the register(s) located between 0x01 and 0x24. Behind the scene, only the “Write Buffers” are updated with these new values.
2. The user then writes a 1 to UDR bit 0 of the “UPDATE0 Register” at address 0x04 to transfer the modified “Write Buffers” to the corresponding time registers.

The logic subsequently would perform a transfer of data from Write Buffers to the actual registers and then clears the “UDR” bit automatically as well as clearing the Write Buffers (marking them as not modified).

Under the hood, the logic first does a double synchronization of the UDR bit to the 32.768kHz clock before using it as an enable bit to transfer from Write buffers to the actual registers thus allowing a safe update of these two unsynchronized clock events.

Example 1. Pseudo code for setting clock to Saturday, Jan 01, 2011, 1:00:00 PM

```
Set RTCCNTL to 0x01        //12hr mode, BCD mode
Set RTCUPDATE0 to 0x01  //transfer RTCCNTL modification to RTC
Set RTCSEC to 0x00       //0 second
Set RTCMIN to 0x00        //0 minute
Set RTCHOUR to 0x41      //1 PM
```

Set RTCDOW to 0x40 //Saturday

Set RTCMONTH to 0x01 //January

Set RTCYEAR to 0x11 //11

Set RTCDOM to 0x01 //First

Set RTCUPDATE0 to 0x01 //transfer write buffers to counters

Wait 16 ms for write to complete

Set RTCSEC to 0x… //new write

Example 2. Pseudo code for setting ALARM1 to every Wednesday at 7:30:00 AM:

Set RTCCNTL to 0x01 //12hr mode, BCD mode

Set RTCUPDATE0 to 0x01 //transfer RTCCNTL modification to RTC

Set RTCSECA1 to 0x80 //0 sec, enabled

Set RTCMINA1 to 0xB0 //30 minute, enabled

Set RTCHOURA1 to 0x87 //7 AM, enabled

Set RTCDOWA1 to 0x08 //Wednesday, enabled

Set RTCMONTHA1 to 0x00 //Disabled

Set RTCYEARA1 to 0x00 //Disabled

Set RTCDOMA1 to 0x00 //Disabled

Set RTCUPDATE0 to 0x01 //transfer write buffers to counters

Wait 16ms for write to complete

Set RTCSEC to 0x… //new write

Reading from RTC

Corresponding to most timing registers are a series of Read Buffers.

In order to safely read from various registers on-board the RTC, all RTC registers (except RTCINT register and bit 0 and 4 of UPDATE0 Register) have a corresponding Read Buffer. When the user reads from the RTC, the user is actually performing a read from the Read Buffers. Therefore, there are two steps needed to read a particular register or set of registers:

1. The user writes a 1 to RBUDR bit 4 of the UPDATE0 Register at address 0x04 to transfer most timing registers to the Read Buffers. Behind the scene, the Read Buffers are updated.
2. The user then reads from the desired register location.

After step 1, the logic subsequently performs a transfer of data from the actual registers to the Read Buffers and then clears the RBUDR bit.

The logic first does a double synchronization of the RBUDR bit to the 32.768 kHz clock before using it as a clock (RBUDR_sync) to transfer from the actual registers to the Read Buffers, thus allowing a safe update of these 2 unsynchronized clock events.

Example 3. Pseudo code for reading the time:

Set RTCUPDATE0 to 0x10 //transfer timekeeper counters to read buffers

Wait 16ms for read to complete

Read RTCSEC //second

Read RTCMIN //minute

Read RTCHOUR //hour

Read RTCDOW //Day of Week

Read RTCMONTH //Month

Read RTCYEAR //Year

Read RTCDOM //Day of Month

Example 4. Pseudo code for reading ALARM1 setting:

Set RTCUPDATE0 to 0x10 // transfer timekeeper counters to read buffers

Wait 16ms for read to complete

Read RTCSECA1 //sec

Read RTCMINA1 //minute

Read RTCHOURA1 //hour

Read RTCDOWA1 //Day of Week

Read RTCMONTHA1 //Month

Read RTCYEARA1 //Year

Read RTCDOMA1 //Day of Month

Sudden Momentary Power Loss (SMPL)

The SMPL function allows the system to recover if power is briefly lost due to a poor battery connection. If V_{MBATT} falls below and returns above the UVLO threshold within the SMPL timer threshold (SMPLT[1:0]) and SMPL is enabled (SMPL_EN = 1), SMPL initiates a power-up sequence and the SMPL interrupt bit is set. If the SMPL timer expires before V_{MBATT} returns, the SMPL enable bit is automatically cleared in order to prevent power-up on subsequent SMPL events.

To ensure proper operation of the SMPL state machine, initialization software should clear and set SMPL_EN after each power on event.

Detailed Description—I^{2}C Interface

I^{2}C Slave Address

The device implements 7-bit slave addressing. An I^{2}C bus master initiates communication with a slave device by issuing a START condition followed by the slave address. The device responds to its two slave addresses; all other slave addresses are not acknowledged by the device, (optional) with the exception of the General Call address (Software Reset option).

Table 9. MAX77714 Slave Addresses

OTP_I2CADDR[1:0]	RTC SLAVE ADDRESS WRITE	RTC SLAVE ADDRESS READ	PMIC/GPIO SLAVE ADDRESS WRITE	PMIC/GPIO SLAVE ADDRESS READ
0b00	0x90, 0b1001_0000	0x91, 0b1001_0001	0x38, 0b0011_1000	0x39, 0b0011_1001
0b01	0x94, 0b1001_0100	0x95, 0b1001_0101	0x3C, 0b0011_1100	0x3D, 0b0011_1101
0b10	0x0D, 0b1101_0000	0xD1, 0b1101_0001	0x78, 0b0111_1000	0x79, 0b0111_1001
0b11	0xD4, 0b1101_0100	0xD5, 0b1101_0101	0x7C, 0b0111_1100	0x7D, 0b0111_1101

Register Map

RTC

ADDRESS	NAME	MSB							LSB
RTC_FUNC									
0x00	RTCINT[7:0]	RSVD	RSVD	RSVD	RTC1S	SMPL	RTCA2	RTCA1	RTC60S
0x01	RTCINTM[7:0]	RSVD	RSVD	RSVD	RTC1SM	SMPLM	RTCA2M	RTCA1M	RTC60SM
0x02	RTCCNTLM[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	HRMODEM	BCDM
0x03	RTCCNTL[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	HRMODE	BCD
0x04	RTCUPDATE0[7:0]	RSVD	RSVD	RSVD	RBUDR	RSVD	FREEZE_SEC	FCUR	UDR
0x05	RTCUPDATE1[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RBUDF	UDF
0x06	RTCSMPL[7:0]	SMPL_EN	RSVD	RSVD	RSVD	SMPLT[1:0]		RSVD	RSVD
0x07	RTCSEC[7:0]	RSVD	SEC[6:0]						
0x08	RTCMIN[7:0]	RSVD	MIN[6:0]						
0x09	RTCHOUR[7:0]	RSVD	AMPM	HOUR[5:0]					
0x0A	RTCDOW[7:0]	RSVD	SAT	FRI	THU	WED	TUE	MON	SUN
0x0B	RTCMONTH[7:0]	RSVD	RSVD	RSVD	MONTH[4:0]				
0x0C	RTCYEAR[7:0]	YEAR[7:0]							
0x0D	RTCDOM[7:0]	RSVD	RSVD	DAY[5:0]					
0x0E	RTCSECA1[7:0]	AESECA1	SECA1[6:0]						
0x0F	RTCMINA1[7:0]	AEMINA1	MINA1[6:0]						
0x10	RTCHOURA1[7:0]	AEHOURA1	AMPMA1	HOURA1[5:0]					
0x11	RTCDOWA1[7:0]	AEDOWA1	SATA1	FRIA1	THUA1	WEDA1	TUEA1	MONA1	SUNA1
0x12	RTCMONTHA1[7:0]	AEMONA1	RSVD	RSVD	MONTHA1[4:0]				
0x13	RTCYEARA1[7:0]	AEYEARA1	YEARA1[6:0]						
0x14	RTCDOMA1[7:0]	AEDOMA1	RSVD	DAYA1[5:0]					
0x15	RTCSECA2[7:0]	AESECA2	SECA2[6:0]						
0x16	RTCMINA2[7:0]	AEMINA2	MINA2[6:0]						
0x17	RTCHOURA2[7:0]	AEHOURA2	AMPMA2	HOURA2[5:0]					
0x18	RTCDOWA2[7:0]	AEDOWA2	SATA2	FRIA2	THUA2	WEDA2	TUEA2	MONA2	SUNA2

ADDRESS	NAME	MSB							LSB
0x19	RTCMONTHA2[7:0]	AEMON A2	RSVD	RSVD	MONTHA2[4:0]				
0x1A	RTCYEARA2[7:0]	AEYEAR A2	YEARA2[6:0]						
0x1B	RTCDOMA2[7:0]	AEDOM A2	RSVD	DAYA2[5:0]					
0x25	RTC_TIME_OK[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RTC_TIME_OK

Register Details

RTCINT (0x00)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RTC1S	SMPL	RTCA2	RTCA1	RTC60S
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0x0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	There is no physical bit at this location. Write to 0. Reads are don't care.	
RSVD	6	There is no physical bit at this location. Write to 0. Reads are don't care.	
RSVD	5	There is no physical bit at this location. Write to 0. Reads are don't care.	
RTC1S	4	RTC Periodic 1 Second Timer Expired Interrupt 0b0 = 1s Timer did not expire 0b1 = 1s Time expired	
SMPL	3	SMPL Event Interrupt	0: No Interrupt 1: Interrupt
RTCA2	2	RTC Alarm 2 Interrupt 0b0 = No interrupt 0b1 = Interrupt	
RTCA1	1	RTC Alarm 1 Interrupt 0b0 = No interrupt 0b1 = Interrupt	
RTC60S	0	RTC 60 Second Timer Expired Interrupt 0b0 = 60s Timer did not expire 0b1 = 60s Timer expired	

RTCINTM (0x01)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RTC1SM	SMPLM	RTCA2M	RTCA1M	RTC60SM
Reset	0b0	0b0	0x0	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RSVD	7	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	6	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	5	There is no physical bit at this location. Write to 0. Reads are don't care.
RTC1SM	4	RTC Periodic 1 Second Timer Expired Interrupt MASK 0b0 = Not Masked 0b1 = Masked
SMPLM	3	SMPL Event Interrupt 0b0 = Not Masked 0b1 = Masked
RTCA2M	2	RTC Alarm 2 Interrupt 0b0 = Not Masked 0b1 = Masked
RTCA1M	1	RTC Alarm 1 Interrupt 0b0 = Not Masked 0b1 = Masked
RTC60SM	0	RTC 60 Second Timer Expired Interrupt 0b0 = Not Masked 0b1 = Masked

RTCCNTLM (0x02)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	HRMODEM	BCDM
Reset	0b0	0b0	0x0	0b0	0b0	0b0	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	There is no physical bit at this location. Write to 0. Reads are don't care.	
RSVD	6	There is no physical bit at this location. Write to 0. Reads are don't care.	
RSVD	5	There is no physical bit at this location. Write to 0. Reads are don't care.	
RSVD	4	There is no physical bit at this location. Write to 0. Reads are don't care.	
RSVD	3	There is no physical bit at this location. Write to 0. Reads are don't care.	
RSVD	2	There is no physical bit at this location. Write to 0. Reads are don't care.	
HRMODEM	1	Access Control of HRMODE Bit in Register RTCCNTL 0b0 = Writes to Bit 1 (HRMODE) of register address 0x03 (RTCCNTL) is not allowed. 0b1 = Writes to Bit 1 (HRMODE) of register address 0x03 (RTCCNTL) is allowed.	0 1: Writes to Bit 0 (HRMODE) of register address 0x03 (RTCCNTL) is allowed.

BITFIELD	BITS	DESCRIPTION	DECODE
BCDM	0	Access Control of BCD Bit in Register RTCCNTL 0b0 = Writes to Bit 0 (BCD) of register address 0x03 (RTCCNTL) is not allowed. 0b1 = Writes to Bit 0 (BCD) of register address 0x03 (RTCCNTL) is allowed.	0: Writes to Bit 0 (BCD) of register address 0x03 (RTCCNTL) is not allowed. 1: Writes to Bit 0 (BCD) of register address 0x03 (RTCCNTL) is allowed.

RTCCNTL (0x03)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	HRMODE	BCD
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	There is no physical bit at this location. Write to 0. Reads are don't care.	
RSVD	6	There is no physical bit at this location. Write to 0. Reads are don't care.	
RSVD	5	There is no physical bit at this location. Write to 0. Reads are don't care.	
RSVD	4	There is no physical bit at this location. Write to 0. Reads are don't care.	
RSVD	3	There is no physical bit at this location. Write to 0. Reads are don't care.	
RSVD	2	There is no physical bit at this location. Write to 0. Reads are don't care.	
HRMODE	1	Hour Format Control Note that AMPM bit defined for the HOUR or HOURA register only makes sense for the 12-hour mode as the 24-hour mode already has AM/PM implied. 0b0 = 12-Hour mode 0b1 = 24-Hour mode If HRMODEM = 0, writes to HRMODE are not allowed. When switching between 12-hour and 24-hour mode, the registers do not automatically update. User must reprogram all registers.	

BITFIELD	BITS	DESCRIPTION	DECODE
BCD	0	Data Mode for Time and Calendar Updates 0b0 = Binary 0b1 = Binary Coded Decimal (BCD) If BCDM = 0 writes to BCD are not allowed. When switching between binary and BCD, the time contents are no longer valid and must be reinitialized.	0: Binary 1: Binary Coded Decimal (BCD)

RTCUPDATE0 (0x04)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RBUDR	RSVD	FREEZE_SEC	FCUR	UDR
Reset	0b0	0b0	0b0	0b0	0b1	0b0	0b1	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RSVD	7	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	6	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	5	There is no physical bit at this location. Write to 0. Reads are don't care.
RBUDR	4	Access control to update RTC registers by transferring data from the actual registers to the Read Buffers. 0b0 = No action 0b1 = Update Read Buffers Typical transfer time from timekeeper counters to read is 15ms after RBUDR is set. RBUDR is internally cleared after the registers data has been transferred.
RSVD	3	There is no physical bit at this location. Write to 0. Reads are don't care.
FREEZE_SEC	2	This bit freezes the SEC counter from incrementing. 0b0 = SEC counter increments normally 0b1 = SEC counter stops incrementing, which stops all subsequent registers in the timer string (MIN, HOUR, DAY, etc.). This setting effectively stops the clock.
FCUR	1	Flags Cleared Upon Read Control Bit 0b0 = User must write 0 to clear UDF and RBUDF 0b1 = UDF and RBUDF cleared upon read
UDR	0	Access control to update RTC registers by transferring data from the Write Buffers to the actual registers. 0b0 = No action 0b1 = Update register Typical transfer time from Write Buffers to the timekeeper counters is 15ms after UDR is set. UDR is internally cleared after the registers data has been transferred.

RTCUPDATE1 (0x05)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RBUDF	UDF
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b1	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
RSVD	7	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	6	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	5	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	4	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	3	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	2	There is no physical bit at this location. Write to 0. Reads are don't care.
RBUDF	1	This bit is an Update Flag that indicates when an actual transfer of data from the actual registers to Read Buffers occurs. When this bit is 1, then the user can initiate a new read operation, otherwise it is not safe to do so. 0b0 = Update not done 0b1 = Update done Typical update time is 15ms after the RBUDR bit is set. If FCUR bit (RTCUPDATE0 register) is 1, this bit is automatically cleared after a read operation. If FCUR is 0, the user must write a 0 to clear it.
UDF	0	This bit is an Update Flag that indicates when an actual transfer of data from the Write Buffers to the corresponding register occurs. When this bit is 1, then the user can initiate a new write operation, otherwise it is not safe to do so. 0b0 = Update not done 0b1 = Update done Typical update time is 15ms after the UDR bit is set. If FCUR bit (RTCUPDATE0 register) is 1, this bit is automatically cleared after a read operation. If FCUR is 0, the user must write a 0 to clear it.

RTCSMPL (0x06)

BIT	7	6	5	4	3	2	1	0
Field	SMPL_EN	RSVD	RSVD	RSVD	SMPLT[1:0]		RSVD	RSVD
Reset	0b0	0b0	0b0	0b0	0b00		0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
SMPL_EN	7	SMPL Feature Enable Control 0b0 = SMPL Disabled 0b1 = SMPL Enabled
RSVD	6	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	5	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	4	There is no physical bit at this location. Write to 0. Reads are don't care.

BITFIELD	BITS	DESCRIPTION
SMPLT	3:2	Sets the SMPL Timer Threshold 0b00 = 0.5s 0b01 = 1.0s 0b10 = 1.5s 0b11 = 2.0s
RSVD	1	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	0	There is no physical bit at this location. Write to 0. Reads are don't care.

RTCSEC (0x07)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	SEC[6:0]						
Reset	0b0	0b00000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RSVD	7	There is no physical bit at this location. Write to 0. Reads are don't care.
SEC	6:0	RTC Seconds Counter Register In Binary format (BCD = 0), valid values for B6 through B0 are 0 through 59. In BCD format, valid data for B6 through B4 are 0 through 5, and valid data for B3 through B0 are 0 through 9.

RTCMIN (0x08)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MIN[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RSVD	7	There is no physical bit at this location. Write to 0. Reads are don't care.
MIN	6:0	RTC Minutes Counter Register In Binary format (BCD = 0), valid values for B6 through B0 are 0 through 59. In BCD format, valid data for B6 through B4 are 0 through 5, and valid data for B3 through B0 are 0 through 9.

RTCHOUR (0x09)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	AMPM	HOUR[5:0]					
Reset	0b0	0b0	0b000000					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
RSVD	7	There is no physical bit at this location. Write to 0. Reads are don't care.

BITFIELD	BITS	DESCRIPTION
AMPM	6	AM/PM Selection. AMPM is only valid when the clock is set for 12-hour mode (HRMODE = 0). When the clock is set for 24-hour mode, this bit is a don't care. 0b0 = AM 0b1 = PM
HOUR	5:0	RTC Hours Counter Register Note that there are two possibilities for values chosen for B5 through B0 depending on current status of HRMODE Bit: If HRMODE = 1 (24-Hour Mode) • Binary mode (BCD = 0): B5 is zero, and B4 through B0 valid values are 0 through 23. • BCD mode (BCD = 1): Valid values for B5 through B4 are 0 through 2, and valid values for B3 through B0 are 0 through 9 (the full number does not exceed 23). If HRMODE = 0 (12-Hour Mode) • Binary mode (BCD = 0): B5 and B4 are 0, and valid values for B3 through B0 are 1 through 12. • BCD mode (BCD = 1): Valid values for B5 through B4 are 0 through 1, and valid values for B3 through B0 are 0 through 9 (the full number does not exceed 12).

RTCDOW (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	SAT	FRI	THU	WED	TUE	MON	SUN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RSVD	7	There is no physical bit at this location. Write to 0. Reads are don't care.
SAT	6	Bits B6 through B0 each represent one day of the week. As such, only one bit is set at a time. B[6:0] = 100_0000 represents Saturday
FRI	5	B[6:0] = 010_0000 represents Friday
THU	4	B[6:0] = 001_0000 represents Thursday
WED	3	B[6:0] = 000_1000 represents Wednesday
TUE	2	B[6:0] = 000_0100 represents Tuesday
MON	1	B[6:0] = 000_0010 represents Monday
SUN	0	B[6:0] = 000_0001 represents Sunday

RTCMONTH (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	MONTH[4:0]				
Reset	0b0	0b0	0b0	0b00001				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION
RSVD	7	There is no physical bit at this location. Write to 0. Reads are don't care.

BITFIELD	BITS	DESCRIPTION
RSVD	6	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	5	There is no physical bit at this location. Write to 0. Reads are don't care.
MONTH	4:0	RTC Months Counter Register In Binary format (BCD = 0), valid values for B4 through B0 are 1 through 12. In BCD format (BCD = 1), valid data for B4 is either 0 or 1, and valid data for B3 through B0 are 0 through 9 (the full value in BCD format does not exceed 12 and must be greater than zero).

RTCYEAR (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	YEAR[7:0]							
Reset	0b00000000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
YEAR	7:0	RTC Years Counter Register In Binary format (BDC = 0), valid values for B7 through B0 are 0 through 99. In BCD format (BCD = 1), valid data for B7 through B4 are 0 through 9, and similarly valid data for B3 through B0 are 0 through 9.

RTCDOM (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	DAY[5:0]					
Reset	0b0	0b0	0b000001					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
RSVD	7	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	6	There is no physical bit at this location. Write to 0. Reads are don't care.
DAY	5:0	RTC Days in a Month Register In Binary format (BCD = 0), valid values for B5 through B0 are 1 through 31. In BCD format (BCD = 1), valid data for B4 through B5 are 0 through 3, and valid data for B3 through B0 are 0 through 9 (the full value should be greater than 0 but not exceed 31). Furthermore, there is a restriction on choosing number of days in a month according to the selected month and year as shown below: • For months 1, 3, 5, 7, 8, 10, and 12 the selected value for B5 through B0 must be 1 through 31. • For months 4, 6, 9, and 11 the selected value for B5 through B0 must be 1 through 30. • For month 2, or month of Feb., the selected value for B5 through B0 must be 1 through 28 for normal years, or must be 1 through 29 for leap years. Does not account for solar years. Leap years are those that are evenly divisible by 4. 0, 4, 8, . . . 24, 28, . . .72, 76 . . . 92, 96.

RTCSECA1 (0x0E)

BIT	7	6	5	4	3	2	1	0
Field	AESECA1	SECA1[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
AESECA1	7	Alarm Enable Control	0: Alarm disable 1: Alarm enable
SECA1	6:0	RTC Seconds Counter Register In Binary format (BCD = 0), valid values for B6 through B0 are 0 through 59. In BCD format, valid data for B6 through B4 are 0 through 5, and valid data for B3 through B0 are 0 through 9.	

RTCMINA1 (0x0F)

BIT	7	6	5	4	3	2	1	0
Field	AEMINA1	MINA1[6:0]						
Reset	0b0	0x0000001						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
AEMINA1	7	Alarm Enable Control	0: Alarm disable 1: Alarm enable
MINA1	6:0	RTC Minutes Alarm Register If the value of MINA1 is equal to the value of MIN and AEMINA1 is 1, an RTCA1 alarm interrupt is generated. RTC Minutes Counter Register In Binary format (BCD = 0), valid values for B6 through B0 are 0 through 59. In BCD format, valid data for B6 through B4 are 0 through 5, and valid data for B3 through B0 are 0 through 9.	

RTCHOURA1 (0x10)

BIT	7	6	5	4	3	2	1	0
Field	AEHOURA1	AMPMA1	HOURA1[5:0]					
Reset	0b0	0b0	0b000001					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
AEHOURA1	7	Alarm Enable Control 0b0 = Alarm disabled 0b1 = Alarm enabled

BITFIELD	BITS	DESCRIPTION
AMPMA1	6	AM/PM Selection AMPM is only valid when the clock is set for 12-hour mode (HRMODE = 0). When the clock is set for 24-hour mode, this bit is a don't care. 0b0 = AM 0b1 = PM
HOURA1	5:0	RTC Hours Alarm Register If the value of HOURA1 is equal to the value of HOUR and AEHOURA1 is 1, an RTCA1 alarm interrupt is generated. RTC Hours Counter Register Note that there are two possibilities for values chosen for B5 through B0 depending on current status of HRMODE Bit: If HRMODE = 1 (24-Hour Mode) • Binary mode (BCD = 0): B5 is zero, and B4 through B0 valid values are 0 through 23. • BCD mode (BCD = 1): Valid values for B5 through B4 are 0 through 2, and valid values for B3 through B0 are 0 through 9 (the full number does not exceed 23). If HRMODE = 0 (12-Hour Mode) • Binary mode (BCD = 0): B5 and B4 are 0, and valid values for B3 through B0 are 1 through 12. • BCD mode (BCD = 1): Valid values for B5 through B4 are 0 through 1, and valid values for B3 through B0 are 0 through 9 (the full number does not exceed 12).

RTCDOWA1 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	AEDOWA1	SATA1	FRIA1	THUA1	WEDA1	TUEA1	MONA1	SUNA1
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
AEDOWA1	7	Alarm Enable Control 0b0 = Alarm disabled 0b1 = Alarm enabled
SATA1	6	RTC Day Of Week Alarm Register If the value of RTCDOWA1 is equal to the value of DOW and AEDOWA1 is 1, an RTCA1 alarm interrupt is generated. Bits B6 through B0 each represent one day of the week. As such, only one bit is set at a time. B[6:0] = 100_0000 represents Saturday
FRIA1	5	B[6:0] = 010_0000 represents Friday
THUA1	4	B[6:0] = 001_0000 represents Thursday
WEDA1	3	B[6:0] = 000_1000 represents Wednesday
TUEA1	2	B[6:0] = 000_0100 represents Tuesday
MONA1	1	B[6:0] = 000_0010 represents Monday
SUNA1	0	B[6:0] = 000_0001 represents Sunday

RTCMONTHA1 (0x12)

BIT	7	6	5	4	3	2	1	0
Field	AEMONA1	RSVD	RSVD	MONTHA1[4:0]				
Reset	0b0	0b0	0b0	0b00000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION
AEMONA1	7	Alarm Enable Control 0b0 = Alarm disabled 0b1 = Alarm enabled
RSVD	6	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	5	There is no physical bit at this location. Write to 0. Reads are don't care.
MONTHA1	4:0	RTC Month Alarm Register If the value of MONTHA1 is equal to the value of MONTH and AEMONTHA1 is 1, an RTCA1 alarm interrupt is generated.

RTCYEARA1 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	AEYEARA1	YEARA1[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
AEYEARA1	7	Alarm Enable Control 0b0 = Alarm disabled 0b1 = Alarm enabled
YEARA1	6:0	RTC Year Alarm Register If the value of YEARA1 is equal to the value of YEAR and AEYEARA1 is 1, an RTCA1 alarm interrupt is generated. RTC Years Counter Register In Binary format (BDC = 0), valid values for B7 through B0 are 0 through 99. In BCD format (BCD = 1), valid data for B7 through B4 are 0 through 9, and similarly valid data for B3 through B0 are 0 through 9.

RTCDOMA1 (0x14)

BIT	7	6	5	4	3	2	1	0
Field	AEDOMA1	RSVD	DAYA1[5:0]					
Reset	0b0	0b0	0b000000					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
AEDOMA1	7	Alarm Enable Control 0b0 = Alarm disabled 0b1 = Alarm enabled
RSVD	6	There is no physical bit at this location. Write to 0. Reads are don't care.

BITFIELD	BITS	DESCRIPTION
DAYA1	5:0	RTC Day Of Month Alarm 1 Register If the value of DAYA1 is equal to the value of DAY and AEDAYA1 is 1, an RTCA1 alarm interrupt is generated.

RTCSECA2 (0x15)

BIT	7	6	5	4	3	2	1	0
Field	AESECA2	SECA2[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
AESECA2	7	Alarm Enable Control 0b0 = Alarm disabled 0b1 = Alarm enabled
SECA2	6:0	RTC Seconds Counter Register In Binary format (BCD = 0), valid values for B6 through B0 are 0 through 59. In BCD format, valid data for B6 through B4 are 0 through 5, and valid data for B3 through B0 are 0 through 9.

RTCMINA2 (0x16)

BIT	7	6	5	4	3	2	1	0
Field	AEMINA2	MINA2[6:0]						
Reset	0b0	0b0000001						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
AEMINA2	7	Alarm Enable Control 0b0 = Alarm disabled 0b2 = Alarm enabled
MINA2	6:0	RTC Minutes Alarm Register If the value of MINA2 is equal to the value of MIN and AEMINA2 is 1, an RTCA2 alarm interrupt is generated. RTC Minutes Counter Register In Binary format (BCD = 0), valid values for B6 through B0 are 0 through 59. In BCD format, valid data for B6 through B4 are 0 through 5, and valid data for B3 through B0 are 0 through 9.

RTCHOURA2 (0x17)

BIT	7	6	5	4	3	2	1	0
Field	AEHOURA2	AMPMA2	HOURA2[5:0]					
Reset	0b0	0b0	0b000000					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
AEHOURA2	7	Alarm Enable Control 0b0 = Alarm disabled 0b1 = Alarm enabled
AMPMA2	6	AM/PM Selection. AMPM is only valid when the clock is set for 12-hour mode (HRMODE = 0). When the clock is set for 24-hour mode, this bit is a don’t care. 0b0 = AM 0b1 = PM
HOURA2	5:0	RTC Hours Alarm Register If the value of HOURA2 is equal to the value of HOUR and AEHOURA2 is 1, an RTCA2 alarm interrupt is generated. RTC Hours Counter Register Note that there are two possibilities for values chosen for B5 through B0 depending on current status of HRMODE Bit: If HRMODE = 1 (24-Hour Mode) • Binary mode (BCD = 0): B5 is zero, and B4 through B0 valid values are 0 through 23. • BCD mode (BCD = 1): Valid values for B5 through B4 are 0 through 2, and valid values for B3 through B0 are 0 through 9 (the full number does not exceed 23). If HRMODE = 0 (12-Hour Mode) • Binary mode (BCD = 0): B5 and B4 are 0, and valid values for B3 through B0 are 1 through 12. • BCD mode (BCD = 1): Valid values for B5 through B4 are 0 through 1, and valid values for B3 through B0 are 0 through 9 (the full number does not exceed 12).

RTCDOWA2 (0x18)

BIT	7	6	5	4	3	2	1	0
Field	AEDOWA2	SATA2	FRIA2	THUA2	WEDA2	TUEA2	MONA2	SUNA2
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
AEDOWA2	7	Alarm Enable Control 0b0 = Alarm disabled 0b1 = Alarm enabled
SATA2	6	RTC Day Of Week Alarm Register If the value of RTCDOWA2 is equal to the value of DOW and AEDOWA2 is 1, an RTCA2 alarm interrupt is generated. Bits B6 through B0 each represent one day of the week. As such, only one bit is set at a time. B[6:0] = 100_0000 represents Saturday
FRIA2	5	B[6:0] = 010_0000 represents Friday
THUA2	4	B[6:0] = 001_0000 represents Thursday
WEDA2	3	B[6:0] = 000_1000 represents Wednesday
TUEA2	2	B[6:0] = 000_0100 represents Tuesday
MONA2	1	B[6:0] = 000_0010 represents Monday
SUNA2	0	B[6:0] = 000_0001 represents Sunday

RTCMONTHA2 (0x19)

BIT	7	6	5	4	3	2	1	0
Field	AEMONA2	RSVD	RSVD	MONTHA2[4:0]				
Reset	0b0	0b0	0b0	0b00000				
Access Type	Write, Read	Write, Read	Write, Read	Write, Read				

BITFIELD	BITS	DESCRIPTION	DECODE
AEMONA2	7	Alarm Enable Control 0b0 = Alarm disabled 0b1 = Alarm enabled	0: Alarm disable 1: Alarm enable
RSVD	6	There is no physical bit at this location. Write to 0. Reads are don't care.	
RSVD	5	There is no physical bit at this location. Write to 0. Reads are don't care.	
MONTHA2	4:0	RTC Month Alarm Register If the value of MONTHA2 is equal to the value of MONTH and AEMONTHA2 is 1, an RTCA2 alarm interrupt is generated.	

RTCYEARA2 (0x1A)

BIT	7	6	5	4	3	2	1	0
Field	AEYEARA2	YEARA2[6:0]						
Reset	0b0	0b0000000						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
AEYEARA2	7	Alarm Enable Control 0b0 = Alarm disabled 0b1 = Alarm enabled
YEARA2	6:0	RTC Year Alarm Register If the value of YEARA2 is equal to the value of YEAR and AEYEARA2 is 1, an RTCA2 alarm interrupt is generated. RTC Years Counter Register In Binary format (BDC = 0), valid values for B7 through B0 are 0 through 99. In BCD format (BCD = 1), valid data for B7 through B4 are 0 through 9, and similarly valid data for B3 through B0 are 0 through 9.

RTCDOMA2 (0x1B)

BIT	7	6	5	4	3	2	1	0
Field	AEDOMA2	RSVD	DAYA2[5:0]					
Reset	0b0	0b0	0b000000					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
AEDOMA2	7	Alarm Enable Control 0b0 = Alarm disabled 0b1 = Alarm enabled
RSVD	6	There is no physical bit at this location. Write to 0. Reads are don't care.
DAYA2	5:0	RTC Day Of Month Alarm 2 Register If the value of DAYA2 is equal to the value of DAY and AEDAYA2 is 1, an RTCA2 alarm interrupt is generated.

RTC_TIME_OK (0x25)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RTC_TIME_OK
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RSVD	7	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	6	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	5	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	4	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	3	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	2	There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	1	There is no physical bit at this location. Write to 0. Reads are don't care.
RTC_TIME_OK	0	RTC_TIME_OK bit can be used by the customer to use as a RTC data validity bit. This bit is by default 0, communicating that the RTC time keeping register data is either holding RESET default or holding a value which is not current. In the application, when the customer updates the time keeping register, they should write 1 to this bit and every time this bit is read and holds "1" implies that the RTC data is current/valid. If the VRTC < VRTCUVLO, then this bit is reset to 0.

PMIC-GPIO

ADDRESS	NAME	MSB							LSB
CLOGIC									
0x00	INT_TOP[7:0]	IRQ_GLBL	IRQ_SD	IRQ_LDO	IRQ_GPIO	IRQ_RTC	RSVD	IRQ_ONOFF	IRQ
0x01	INT_MBATTRST_TEMP[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	MBATTRESET_R	TJALRM1_R	TJALRM2_R
0x02	INT_LVL2_ONOFF[7:0]	RSVD	RSVD	ACOK_R	ACOK_F	EN0_R	EN0_F	EN0_1SEC	MRWRN
0x03	INT_LVL2_SD0_3[7:0]	SD0_OV_I	SD0_UV_I	SD1_OV_I	SD1_UV_I	SD2_OV_I	SD2_UV_I	SD3_OV_I	SD3_UV_I
0x04	INT_LVL2_L0_7[7:0]	IRQ_LVL2_7	IRQ_LVL2_6	IRQ_LVL2_5	IRQ_LVL2_4	IRQ_LVL2_3	IRQ_LVL2_2	IRQ_LVL2_1	IRQ_LVL2_0

ADDRESS	NAME	MSB							LSB
0x05	INT_LVL2_L8[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	IRQ_LVL2_8
0x06	INT_LVL2_GPIO[7:0]	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0
0x07	INT_TOPM[7:0]	IRQ_GLBLM	IRQ_SDM	IRQ_LDOM	IRQ_GPIOM	IRQ_RTCM	RSVD	IRQ_ONOFFM	GLBLM
0x08	INTM_MBATTRST_TEMP[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	MBATTRESETM	TJALRM1M	TJALRM2M
0x09	INTM_ONOFF[7:0]	RSVD	RSVD	ACOK_HIGHM	ACOK_LOWM	EN0_RM	EN0_FM	EN0_1SECM	MRWRNM
0x0A	INTM_SD0_3[7:0]	SD0_OV_M	SD0_UV_M	SD1_OV_M	SD1_UV_M	SD2_OV_M	SD2_UV_M	SD3_OV_M	SD3_UV_M
0x0B	INT_MSK_L0_7[7:0]	IRQ_MSK_L7	IRQ_MSK_L6	IRQ_MSK_L5	IRQ_MSK_L4	IRQ_MSK_L3	IRQ_MSK_L2	IRQ_MSK_L1	IRQ_MSK_L0
0x0C	INT_MSK_L8[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	IRQ_MSK_L8
0x0D	STAT_MBATTRST_TEMP[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	MBATTRESET_S	TJALRM1	TJALRM2
0x0E	STAT_ONOFF[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	EN0	ACOK
0x10	POERC0[7:0]	RSTIN	MBU	MBO	MBLSD	TOVLD	HDRST	WTCHDG	SHDN
0x11	POERC1[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	32K_OK	BRDY_OK
0x20	STAT_SD0_3[7:0]	SD0_OV_S	SD0_UV_S	SD1_OV_S	SD1_UV_S	SD2_OV_S	SD2_UV_S	SD3_OV_S	SD3_UV_S
0x30	32K_STATUS[7:0]	RSVD	RSVD	SIOSCOK	XOSCOK	32KSOURCE	32KLOAD[1:0]		CRYSTAL_CONFIG
0x31	32K_CONFIG[7:0]	RSVD	RSVD	RSVD	XOSC_RETRY	RSVD	PWR_MD_32k[1:0]		32KSOURCE_OTP
0x90	CNFG_GLBL1[7:0]	RSVD	MBLPD	MBATT_RESET_HYS[1:0]		MBATT_RESET[2:0]			MBATT_RSTEN
0x91	CNFG_GLBL2[7:0]	RSVD	RSVD	RSVD	GLBL_LPM	WDTSLPC	WDTEN	TWD[1:0]	
0x92	CNFG_GLBL3[7:0]	RSVD	RSVD	RSVD	SRCFPS0	ENFPS0	SRCFPS1	ENFPS1	WDTC
0x93	CNFG1_ONOFF[7:0]	RSVD	SFT_RST	MRT[2:0]			SLPEN	PWR_OFF	EN0DLY
0x94	CNFG2_ONOFF[7:0]	MR_RST_WK	SFT_RST_WK	WD_RST_WK	WK_ACOK	WK_MBATT	WK_ALARM1R	WK_ALARM2R	WK_EN0
0x95	MSTR_PU_PD[7:0]	RSVD	MSTR_PU[2:0]			RSVD	MSTR_PD[2:0]		
0x96	MSTR_SLPENTRY_EXIT[7:0]	RSVD	MSTR_SLPENTY[2:0]			RSVD	MSTR_SLPEXT[2:0]		
0x97	BUCK_PWR_MD[7:0]	PWR_MD_SD3[1:0]		PWR_MD_SD2[1:0]		PWR_MD_SD1[1:0]		PWR_MD_SD0[1:0]	
0x98	LDO_PWR_MD0_3[7:0]	PWR_MD_L0[1:0]		PWR_MD_L1[1:0]		PWR_MD_L2[1:0]		PWR_MD_L3[1:0]	
0x99	LDO_PWR_MD4_7[7:0]	PWR_MD_L4[1:0]		PWR_MD_L5[1:0]		PWR_MD_L6[1:0]		PWR_MD_L7[1:0]	
0x9A	LDO_PWR_MD8[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	PWR_MD_L8[1:0]	
0x9B	LDO0FPS[7:0]	FPSSRC_L0[1:0]		LDO0UPSLT[2:0]			LDO0DNSLT[2:0]		

ADDRESS	NAME	MSB							LSB
0x9C	LDO1FPS[7:0]	FPSSRC_L1[1:0]		LDO1UPSLT[2:0]			LDO1DNSLT[2:0]		
0x9D	LDO2FPS[7:0]	FPSSRC_L2[1:0]		LDO2UPSLT[2:0]			LDO2DNSLT[2:0]		
0x9E	LDO3FPS[7:0]	FPSSRC_L3[1:0]		LDO3UPSLT[2:0]			LDO3DNSLT[2:0]		
0x9F	LDO4FPS[7:0]	FPSSRC_L4[1:0]		LDO4UPSLT[2:0]			LDO4DNSLT[2:0]		
0xA0	LDO5FPS[7:0]	FPSSRC_L5[1:0]		LDO5UPSLT[2:0]			LDO5DNSLT[2:0]		
0xA1	LDO6FPS[7:0]	FPSSRC_L6[1:0]		LDO6UPSLT[2:0]			LDO6DNSLT[2:0]		
0xA2	LDO7FPS[7:0]	FPSSRC_L7[1:0]		LDO7UPSLT[2:0]			LDO7DNSLT[2:0]		
0xA3	LDO8FPS[7:0]	FPSSRC_L8[1:0]		LDO8UPSLT[2:0]			LDO8DNSLT[2:0]		
0xA4	SD0FPS[7:0]	FPSSRC_SD0[1:0]		SD0UPSLT[2:0]			SD0DNSLT[2:0]		
0xA5	SD1FPS[7:0]	FPSSRC_SD1[1:0]		SD1UPSLT[2:0]			SD1DNSLT[2:0]		
0xA6	SD2FPS[7:0]	FPSSRC_SD2[1:0]		SD2UPSLT[2:0]			SD2DNSLT[2:0]		
0xA7	SD3FPS[7:0]	FPSSRC_SD3[1:0]		SD3UPSLT[2:0]			SD3DNSLT[2:0]		
0xA8	GPIO0FPS[7:0]	FPSSRC_GPIO0[1:0]		GPIO0UPSLT[2:0]			GPIO0DNSLT[2:0]		
0xA9	GPIO1FPS[7:0]	FPSSRC_GPIO1[1:0]		GPIO1UPSLT[2:0]			GPIO1DNSLT[2:0]		
0xAA	GPIO2FPS[7:0]	FPSSRC_GPIO2[1:0]		GPIO2UPSLT[2:0]			GPIO2DNSLT[2:0]		
0xAB	GPIO7FPS[7:0]	FPSSRC_GPIO7[1:0]		GPIO7UPSLT[2:0]			GPIO7DNSLT[2:0]		
0xAC	RSTIOFPS[7:0]	FPSSRC_RSTIO[1:0]		RST7UPSLT[2:0]			RST7DNSLT[2:0]		
OVERLAP									
BUCK									
0x40	SD0_CNFG1[7:0]	RSVD	SD0VOUT[6:0]						
0x41	SD1_CNFG1[7:0]	RSVD	SD1VOUT[6:0]						
0x42	SD2_CNFG1[7:0]	SD2VOUT[7:0]							
0x43	SD3_CNFG1[7:0]	SD3VOUT[7:0]							
0x44	SD0_CNFG2[7:0]	RSVD	RSVD	SD0_SS RAMP	RSVD	RSVD	SD0FSREN	SD0ADDIS	SD0FPWMEN
0x45	SD0_CNFG3[7:0]	SD0_BO_THR[1:0]		SD0_BO_HYS[1:0]		RSVD	SD0_BO_PR[1:0]		SD0_OV_THR
0x46	SD1_CNFG2[7:0]	RSVD	RSVD	SD1_SS RAMP	RSVD	RSVD	SD0FSREN	SD0ADDIS	SD0FPWMEN
0x47	SD1_CNFG3[7:0]	SD1_BO_THR[1:0]		SD1_BO_HYS[1:0]		RSVD	SD1_BO_PR[1:0]		SD1_OV_THR
0x48	SD2_CNFG2[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	SD2ADDIS	SD2FPWMEN
0x49	SD2_CNFG3[7:0]	SD2_BO_THR[1:0]		SD2_BO_HYS[1:0]		RSVD	SD2_BO_PR[1:0]		SD2_OV_THR
0x4A	SD3_CNFG2[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	SD3ADDIS	SD3FPWMEN
0x4B	SD3_CNFG3[7:0]	SD3_BO_THR[1:0]		SD3_BO_HYS[1:0]		RSVD	SD3_BO_PR[1:0]		SD3_OV_THR
OVERLAP									

ADDRESS	NAME	MSB							LSB
LDO									
0x50	LDO_CNFG1_L0[7:0]	RSVD	RSVD	VOUT_LDO_L0[5:0]					
0x51	LDO_CNFG2_L0[7:0]	OVCLMP_EN_L0	ALPM_EN_L0	RSVD	RSVD	POK_L0	RSVD	ADE_L0	SS_L0
0x52	LDO_CNFG1_L1[7:0]	RSVD	RSVD	VOUT_LDO_L1[5:0]					
0x53	LDO_CNFG2_L1[7:0]	OVCLMP_EN_L1	ALPM_EN_L1	RSVD	RSVD	POK_L1	RSVD	ADE_L1	SS_L1
0x54	LDO_CNFG1_L2[7:0]	RSVD	RSVD	VOUT_LDO_L2[5:0]					
0x55	LDO_CNFG2_L2[7:0]	OVCLMP_EN_L2	ALPM_EN_L2	COMP_L2[1:0]		POK_L2	RSVD	ADE_L2	SS_L2
0x56	LDO_CNFG1_L3[7:0]	RSVD	RSVD	VOUT_LDO_L3[5:0]					
0x57	LDO_CNFG2_L3[7:0]	OVCLMP_EN_L3	ALPM_EN_L3	COMP_L3[1:0]		POK_L3	RSVD	ADE_L3	SS_L3
0x58	LDO_CNFG1_L4[7:0]	RSVD	RSVD	VOUT_LDO_L4[5:0]					
0x59	LDO_CNFG2_L4[7:0]	OVCLMP_EN_L4	ALPM_EN_L4	COMP_L4[1:0]		POK_L4	RSVD	ADE_L4	SS_L4
0x5A	LDO_CNFG1_L5[7:0]	RSVD	RSVD	VOUT_LDO_L5[5:0]					
0x5B	LDO_CNFG2_L5[7:0]	OVCLMP_EN_L5	ALPM_EN_L5	COMP_L5[1:0]		POK_L5	RSVD	ADE_L5	SS_L5
0x5C	LDO_CNFG1_L6[7:0]	RSVD	RSVD	VOUT_LDO_L6[5:0]					
0x5D	LDO_CNFG2_L6[7:0]	OVCLMP_EN_L6	ALPM_EN_L6	COMP_L6[1:0]		POK_L6	RSVD	ADE_L6	SS_L6
0x5E	LDO_CNFG1_L7[7:0]	RSVD	RSVD	VOUT_LDO_L7[5:0]					
0x5F	LDO_CNFG2_L7[7:0]	OVCLMP_EN_L7	ALPM_EN_L7	COMP_L7[1:0]		POK_L7	RSVD	ADE_L7	SS_L7
0x60	LDO_CNFG1_L8[7:0]	RSVD	RSVD	VOUT_LDO_L8[5:0]					
0x61	LDO_CNFG2_L8[7:0]	OVCLMP_EN_L8	ALPM_EN_L8	RSVD[1:0]		POK_L8	RSVD	ADE_L8	SS_L8
0x62	LDO_CNFG3[7:0]	RSVD[6:0]							L_B_EN
OVERLAP									
GPIO									
0x70	CNFG_GPIO0[7:0]	DBNC0[1:0]		REFE_IRQ[1:0]		DO0	DI0	DIR0	PPDRV0
0x71	CNFG_GPIO1[7:0]	DBNC1[1:0]		REFE_IRQ[1:0]		DO1	DI1	DIR1	PPDRV1
0x72	CNFG_GPIO2[7:0]	DBNC2[1:0]		REFE_IRQ[1:0]		DO2	DI2	DIR2	PPDRV2
0x73	CNFG_GPIO3[7:0]	DBNC3[1:0]		REFE_IRQ[1:0]		DO3	DI3	DIR3	PPDRV3
0x74	CNFG_GPIO4[7:0]	DBNC4[1:0]		REFE_IRQ[1:0]		DO4	DI4	DIR4	PPDRV4
0x75	CNFG_GPIO5[7:0]	DBNC5[1:0]		REFE_IRQ[1:0]		DO5	DI5	DIR5	PPDRV5
0x76	CNFG_GPIO6[7:0]	DBNC6[1:0]		REFE_IRQ[1:0]		DO6	DI6	DIR6	PPDRV6
0x77	CNFG_GPIO7[7:0]	DBNC7[1:0]		REFE_IRQ[1:0]		DO7	DI7	DIR7	PPDRV7

ADDRESS	NAME	MSB							LSB
0x78	PUE_GPIO[7:0]	PUE7	PUE6	PUE5	PUE4	PUE3	PUE2	PUE1	PUE0
0x79	PDE_GPIO[7:0]	PDE7	PDE6	PDE5	PDE4	PDE3	PDE2	PDE1	PDE0
0x7A	AME_GPIO[7:0]	AME7	AME6	AME5	AME4	AME3	AME2	AME1	AME0
OVERLAP									
SBIAS									
0xB0	CID0[7:0]	SR[7:0]							
0xB1	CID1[7:0]	SR[15:8]							
0xB2	CID2[7:0]	SR[23:16]							
0xB3	CID3[7:0]	DIDM[3:0]				DIDO[3:0]			
0xB4	CID4[7:0]	DRV[7:0]							
BBC									
0x80	CNFG_BBC[7:0]	BBCRS[1:0]		BBCLO WIEN	BBCVS[1:0]		BBCCS[1:0]		BBCEN
I2C									
0xC0	I2C_CTRL1[7:0]	RSVD	RSVD	RSVD	PAIR	RSVD	RSVD	WD_EN	HS_EXT
0xC1	I2C_CTRL2[7:0]	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	I2CWP

Register Details

INT_TOP (0x00)

BIT	7	6	5	4	3	2	1	0
Field	IRQ_GLBL	IRQ_SD	IRQ_LDO	IRQ_GPIO	IRQ_RTC	RSVD	IRQ_ONOF F	IRQ
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
IRQ_GLBL	7	0 = No unmasked interrupts pending in the INT_MBATTRST_TEMP register. 1 = There are unmasked interrupts pending in the INT_MBATTRST_TEMP register.
IRQ_SD	6	0 = No unmasked interrupts pending in the INT_LVL2_SD0_3 register. 1 = There are unmasked interrupts pending in the INT_LVL2_SD0_3 register.
IRQ_LDO	5	0 = No unmasked interrupts pending in the INT_LVL2_L0_7 and INT_LVL2_L8 register. 1 = There are unmasked interrupts pending in the INT_LVL2_L0_7 and INT_LVL2_L8 register.
IRQ_GPIO	4	0 = No unmasked interrupts pending in the IRQ_LVL2_GPIO register 1 = There are unmasked interrupts pending in the IRQ_LVL2_GPIO register
IRQ_RTC	3	0 = No unmasked interrupts pending in the RTCINT register. 1 = There are unmasked interrupts pending in the RTCINT register.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don't care.
IRQ_ONOFF	1	0 = No unmasked interrupts pending in the INT_LVL2_ONOFF register. 1 = There are unmasked interrupts pending in the INT_LVL2_ONOFF register.
IRQ	0	0 = Unmasked gate drive is logic low. 1 = Unmasked gate drive is logic high.

INT_MBATTRST_TEMP (0x01)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	MBATTRESET_R	TJALRM1_R	TJALRM2_R
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	5	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	4	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
MBATTRESET_R	2	0 = MBATT has not fallen below programmed MBATTRESET since the last time this bit was read. 1 = MBATT has fallen below programmed MBATTRESET since the last time this bit was read.
TJALRM1_R	1	0 = T_J has not risen above TJALRM1 since the last time this bit was read. 1 = T_J has risen above TJALRM1 since the last time this bit was read.
TJALRM2_R	0	0 = T_J has not risen above TJALRM21 since the last time this bit was read. 1 = T_J has risen above TJALRM2 since the last time this bit was read.

INT_LVL2_ONOFF (0x02)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	ACOK_R	ACOK_F	EN0_R	EN0_F	EN0_1SEC	MRWRN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
ACOK_R	5	0 = No ACOK rising edges have occurred since the last time this bit was read. 1 = An ACOK rising edge has occurred since the last time this bit was read.
ACOK_F	4	0 = No ACOK falling edges have occurred since the last time this bit was read. 1 = An ACOK falling edge has occurred since the last time this bit was read.
EN0_R	3	0 = No EN0 rising edges have occurred since the last time this bit was read. 1 = An EN0 rising edge has occurred since the last time this bit was read.
EN0_F	2	0 = No EN0 rising edges have occurred since the last time this bit was read. 1 = An EN0 rising edge has occurred since the last time this bit was read.
EN0_1SEC	1	0 = EN0 has not been active for 1 second since the last time this bit was read. 1 = EN0 has been active for 1 second since the last time this bit was read.

BITFIELD	BITS	DESCRIPTION
MRWRN	0	The time for the hard power off warning is one setting shorter than what is programmed by MRT[2:0]. When MRT[2:0] = 0b000, MRWRN is essentially a don't care. 0 = EN0 has not been active for MRT[2:0]-1 since the last time this bit was read. 1 = EN0 has been active for MRT[2:0]-1 since the last time this bit was read.

INT_LVL2_SD0_3 (0x03)

BIT	7	6	5	4	3	2	1	0
Field	SD0_OV_I	SD0_UV_I	SD1_OV_I	SD1_UV_I	SD2_OV_I	SD2_UV_I	SD3_OV_I	SD3_UV_I
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION
SD0_OV_I	7	0 = SD0 output HAS NOT risen above the rising OV threshold since the last time this bit was read. 1 = SD0 output HAS risen above the rising OV threshold since the last time this bit was read.
SD0_UV_I	6	0 = SD0 was enabled and SD0 output HAS NOT fallen below the falling UV threshold since the last time this bit was read, OR, SD1 was disabled. 1 = SD0 was enabled and SD0 output HAS fallen below the falling UV threshold since the last time this bit was read.
SD1_OV_I	5	0 = SD1 output HAS NOT risen above the rising OV threshold since the last time this bit was read. 1 = SD1 output HAS risen above the rising OV threshold since the last time this bit was read.
SD1_UV_I	4	0 = SD1 was enabled and SD1 output HAS NOT fallen below the falling UV threshold since the last time this bit was read, OR, SD1 was disabled. 1 = SD1 was enabled and SD1 output HAS fallen below the falling UV threshold since the last time this bit was read.
SD2_OV_I	3	0 = SD2 output HAS NOT risen above the rising OV threshold since the last time this bit was read. 1 = SD2 output HAS risen above the rising OV threshold since the last time this bit was read.
SD2_UV_I	2	0 = SD2 was enabled and SD2 output HAS NOT fallen below the falling UV threshold since the last time this bit was read, OR, SD2 was disabled. 1 = SD2 was enabled and SD2 output HAS fallen below the falling UV threshold since the last time this bit was read.
SD3_OV_I	1	0 = SD3 output HAS NOT risen above the rising OV threshold since the last time this bit was read. 1 = SD3 output HAS risen above the rising OV threshold since the last time this bit was read.
SD3_UV_I	0	0 = SD3 was enabled and SD3 output HAS NOT fallen below the falling UV threshold since the last time this bit was read, OR, SD3 was disabled. 1 = SD3 was enabled and SD3 output HAS fallen below the falling UV threshold since the last time this bit was read.

INT_LVL2_L0_7 (0x04)

BIT	7	6	5	4	3	2	1	0
Field	IRQ_LVL2_7	IRQ_LVL2_6	IRQ_LVL2_5	IRQ_LVL2_4	IRQ_LVL2_3	IRQ_LVL2_2	IRQ_LVL2_1	IRQ_LVL2_0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
IRQ_LVL2_7	7	1: An interrupt has occurred. Cleared when read. 0: No interrupt has occurred since the last time this register was read.
IRQ_LVL2_6	6	1: An interrupt has occurred. Cleared when read. 0: No interrupt has occurred since the last time this register was read.
IRQ_LVL2_5	5	1: An interrupt has occurred. Cleared when read. 0: No interrupt has occurred since the last time this register was read.
IRQ_LVL2_4	4	1: An interrupt has occurred. Cleared when read. 0: No interrupt has occurred since the last time this register was read.
IRQ_LVL2_3	3	1: An interrupt has occurred. Cleared when read. 0: No interrupt has occurred since the last time this register was read.
IRQ_LVL2_2	2	1: An interrupt has occurred. Cleared when read. 0: No interrupt has occurred since the last time this register was read.
IRQ_LVL2_1	1	1: An interrupt has occurred. Cleared when read. 0: No interrupt has occurred since the last time this register was read.
IRQ_LVL2_0	0	1: An interrupt has occurred. Cleared when read. 0: No interrupt has occurred since the last time this register was read.

INT_LVL2_L8 (0x05)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	IRQ_LVL2_8
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	5	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	4	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	1	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
IRQ_LVL2_8	0	1: An interrupt has occurred. Cleared when read. 0: No interrupt has occurred since the last time this register was read.

INT_LVL2_GPIO (0x06)

BIT	7	6	5	4	3	2	1	0
Field	EDGE7	EDGE6	EDGE5	EDGE4	EDGE3	EDGE2	EDGE1	EDGE0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
EDGE7	7	GPIOx Edge Detection Interrupt 0 = No edges have been detected on GPIOx since the last time this bit was read. 1 = An edge corresponding to REFE_IRQx has been detected on GPIOx since the last time this bit was read. Note that REFE_IRQx = 0b00 sets an interrupt mask which forces EDGEx to 0.
EDGE6	6	GPIOx Edge Detection Interrupt 0 = No edges have been detected on GPIOx since the last time this bit was read. 1 = An edge corresponding to REFE_IRQx has been detected on GPIOx since the last time this bit was read. Note that REFE_IRQx = 0b00 sets an interrupt mask which forces EDGEx to 0.
EDGE5	5	GPIOx Edge Detection Interrupt 0 = No edges have been detected on GPIOx since the last time this bit was read. 1 = An edge corresponding to REFE_IRQx has been detected on GPIOx since the last time this bit was read. Note that REFE_IRQx = 0b00 sets an interrupt mask which forces EDGEx to 0.
EDGE4	4	GPIOx Edge Detection Interrupt 0 = No edges have been detected on GPIOx since the last time this bit was read. 1 = An edge corresponding to REFE_IRQx has been detected on GPIOx since the last time this bit was read. Note that REFE_IRQx = 0b00 sets an interrupt mask which forces EDGEx to 0.
EDGE3	3	GPIOx Edge Detection Interrupt 0 = No edges have been detected on GPIOx since the last time this bit was read. 1 = An edge corresponding to REFE_IRQx has been detected on GPIOx since the last time this bit was read. Note that REFE_IRQx = 0b00 sets an interrupt mask which forces EDGEx to 0.
EDGE2	2	GPIOx Edge Detection Interrupt 0 = No edges have been detected on GPIOx since the last time this bit was read. 1 = An edge corresponding to REFE_IRQx has been detected on GPIOx since the last time this bit was read. Note that REFE_IRQx = 0b00 sets an interrupt mask which forces EDGEx to 0.
EDGE1	1	GPIOx Edge Detection Interrupt 0 = No edges have been detected on GPIOx since the last time this bit was read. 1 = An edge corresponding to REFE_IRQx has been detected on GPIOx since the last time this bit was read. Note that REFE_IRQx = 0b00 sets an interrupt mask which forces EDGEx to 0.

BITFIELD	BITS	DESCRIPTION
EDGE0	0	GPIOx Edge Detection Interrupt 0 = No edges have been detected on GPIOx since the last time this bit was read. 1 = An edge corresponding to REFE_IRQx has been detected on GPIOx since the last time this bit was read. Note that REFE_IRQx = 0b00 sets an interrupt mask which forces EDGEx to 0.

INT_TOPM (0x07)

BIT	7	6	5	4	3	2	1	0
Field	IRQ_GLBLM	IRQ_SDM	IRQ_LDOM	IRQ_GPIOM	IRQ_RTCM	RSVD	IRQ_ONOFFM	GLBLM
Reset	0b1	0b1	0b1	0b1	0b1	0b0	0b1	0b1
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
IRQ_GLBLM	7	IRQ_GLBLM blocks the interrupts from the global resources (INTLBT register) from affecting the nIRQ pin. Be careful not to confuse IRQ_GLBLM with GLBLM. GLBLM blocks all interrupts from affecting the nIRQ pin. 0 = Unmasked 1 = Masked
IRQ_SDM	6	0 = Unmasked 1 = Masked
IRQ_LDOM	5	0 = Unmasked 1 = Masked
IRQ_GPIOM	4	0 = Unmasked 1 = Masked
IRQ_RTCM	3	0 = Unmasked 1 = Masked
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don't care.
IRQ_ONOFFM	1	0 = Unmasked 1 = Masked
GLBLM	0	IRQ_GLBLM blocks the interrupts from the global resources (INT_MBATTRST_TEMP register) from affecting the nIRQ pin. Be careful not to confuse IRQ_GLBLM with GLBLM. GLBLM blocks all interrupts from affecting the nIRQ. 0 = Unmasked 1 = Masked

INTM_MBATTRST_TEMP (0x08)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	MBATTRESETM	TJALRM1M	TJALRM2M
Reset	0b0	0b0	0b0	0b0	0b0	0b1	0b1	0b1
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don't care.

BITFIELD	BITS	DESCRIPTION
RSVD	5	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	4	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
MBATTRESETM	2	0 = Unmasked 1 = Masked
TJALRM1M	1	0 = Unmasked 1 = Masked
TJALRM2M	0	0 = Unmasked 1 = Masked

INTM_ONOFF (0x09)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	ACOK_HIGHM	ACOK_LOWM	EN0_RM	EN0_FM	EN0_1SECM	MRWRNM
Reset	0b0	0b0	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
ACOK_HIGHM	5	0 = Unmasked 1 = Masked
ACOK_LOWM	4	0 = Unmasked 1 = Masked
EN0_RM	3	0 = Unmasked 1 = Masked
EN0_FM	2	0 = Unmasked 1 = Masked
EN0_1SECM	1	0 = Unmasked 1 = Masked
MRWRNM	0	0 = Unmasked 1 = Masked

INTM_SD0_3 (0x0A)

BIT	7	6	5	4	3	2	1	0
Field	SD0_OV_M	SD0_UV_M	SD1_OV_M	SD1_UV_M	SD2_OV_M	SD2_UV_M	SD3_OV_M	SD3_UV_M
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
SD0_OV_M	7	0 = During an output over-voltage event, SD0_OV_I is set to 1. nIRQ is driven low due to an output over-voltage event. 1 = During an output over-voltage event, SD0_OV_I is set to 1. nIRQ is not driven low due to an output over-voltage event.

BITFIELD	BITS	DESCRIPTION
SD0_UV_M	6	0 = During an output under-voltage event, SD0_UV_I is set to 1. nIRQ is driven low due to an output under-voltage event. 1 = During an output under-voltage event, SD0_UV_I is set to 1. nIRQ is not driven low due to an output under-voltage event.
SD1_OV_M	5	0 = During an output over-voltage event, SD1_OV_I is set to 1. nIRQ is driven low due to an output over-voltage event. 1 = During an output over-voltage event, SD1_OV_I is set to 1. nIRQ is not driven low due to an output over-voltage event.
SD1_UV_M	4	0 = During an output under-voltage event, SD1_UV_I is set to 1. nIRQ is driven low due to an output under-voltage event. 1 = During an output under-voltage event, SD1_UV_I is set to 1. nIRQ is not driven low due to an output under-voltage event.
SD2_OV_M	3	0 = During an output over-voltage event, SD2_OV_I is set to 1. nIRQ is driven low due to an output over-voltage event. 1 = During an output over-voltage event, SD2_OV_I is set to 1. nIRQ is not driven low due to an output over-voltage event.
SD2_UV_M	2	0 = During an output under-voltage event, SD2_UV_I is set to 1. nIRQ is driven low due to an output under-voltage event. 1 = During an output under-voltage event, SD2_UV_I is set to 1. nIRQ is not driven low due to an output under-voltage event.
SD3_OV_M	1	0 = During an output over-voltage event, SD3_OV_I is set to 1. nIRQ is driven low due to an output over-voltage event. 1 = During an output over-voltage event, SD3_OV_I is set to 1. nIRQ is not driven low due to an output over-voltage event.
SD3_UV_M	0	0 = During an output under-voltage event, SD3_UV_I is set to 1. nIRQ is driven low due to an output under-voltage event. 1 = During an output under-voltage event, SD3_UV_I is set to 1. nIRQ is not driven low due to an output under-voltage event.

INT_MSK_L0_7 (0x0B)

BIT	7	6	5	4	3	2	1	0
Field	IRQ_MSK_L7	IRQ_MSK_L6	IRQ_MSK_L5	IRQ_MSK_L4	IRQ_MSK_L3	IRQ_MSK_L2	IRQ_MSK_L1	IRQ_MSK_L0
Reset	0b1	0b1	0b1	0b1	0b1	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
IRQ_MSK_L7	7	1: Interrupt is masked and nIRQ is not driven low due to an LDO event. 0: Interrupt is unmasked.
IRQ_MSK_L6	6	1: Interrupt is masked and nIRQ is not driven low due to an LDO event. 0: Interrupt is unmasked.
IRQ_MSK_L5	5	1: Interrupt is masked and nIRQ is not driven low due to an LDO event. 0: Interrupt is unmasked.
IRQ_MSK_L4	4	1: Interrupt is masked and nIRQ is not driven low due to an LDO event. 0: Interrupt is unmasked.
IRQ_MSK_L3	3	1: Interrupt is masked and nIRQ is not driven low due to an LDO event. 0: Interrupt is unmasked.

BITFIELD	BITS	DESCRIPTION
IRQ_MSK_L2	2	1: Interrupt is masked and nIRQ is not driven low due to an LDO event. 0: Interrupt is unmasked.
IRQ_MSK_L1	1	1: Interrupt is masked and nIRQ is not driven low due to an LDO event. 0: Interrupt is unmasked.
IRQ_MSK_L0	0	1: Interrupt is masked and nIRQ is not driven low due to an LDO event. 0: Interrupt is unmasked.

INT_MSK_L8 (0x0C)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	IRQ_MSK_L8
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	5	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	4	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	1	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
IRQ_MSK_L8	0	1: Interrupt is masked and nIRQ is not driven low due to an LDO event. 0: Interrupt is unmasked.

STAT_MBATTRST_TEMP (0x0D)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	MBATTRESET_S	TJALRM1	TJALRM2
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	5	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	4	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
MBATTRESET_S	2	0 = $V_{MBATT} > V_{MBATTRESET}$ 1 = $V_{MBATT} < V_{MBATTRESET}$
TJALRM1	1	0 = T_J < TJ120 1 = T_J > TJ120

BITFIELD	BITS	DESCRIPTION
TJALRM2	0	0 = T_J < TJ140 1 = T_J > TJ140

STAT_ONOFF (0x0E)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	EN0	ACOK
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	5	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	4	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
EN0	1	For OTP_EN0AL = 0 0 = EN0 is not active (logic low). 1 = EN0 is active (logic high). For OTP_EN0AL = 1 0 = EN0 is not active (logic high). 1 = EN0 is active (logic low).
ACOK	0	For OTP_ACOKAL = 0 0 = ACOK is not active (logic low). 1 = ACOK is active (logic high). For OTP_ACOKAL = 1 0 = ACOK is not active (logic high). 1 = ACOK is active (logic low).

POERC0 (0x10)

BIT	7	6	5	4	3	2	1	0
Field	RSTIN	MBU	MBO	MBLSD	TOVLD	HDRST	WTCHDG	SHDN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
RSTIN	7	0 = The reset input signal (RSI) did not cause a global shutdown. 1 = The reset input signal (RSI) caused a global shutdown.
MBU	6	0 = Main battery undervoltage event did not cause a global shutdown. 1 = The main battery caused a global shutdown by falling below its UVLO threshold (V_{MBATT} < $V_{MBATTUVLO}$). If the sudden momentary power loss (SMPL) function is enabled, the PMIC can automatically recover from a momentary power loss.

BITFIELD	BITS	DESCRIPTION
MBO	5	0 = Main battery overvoltage event did not cause a global shutdown. 1 = The main battery caused a global shutdown by rising above its OVLO threshold (V_{MBATT} < $V_{MBATTOVLO}$).
MBLSD	4	0 = Main battery low did not cause a global shutdown. 1 = Main battery low caused a global shutdown because MBLPD is set and V_{MBATT} < $V_{MBATTRESET}$.
TOVLD	3	0 = The junction temperature did not cause a global shutdown. 1 = The junction temperature caused a global shutdown by rising above T_JSHDN.
HDRST	2	0 = The hard-reset function did not cause a global shutdown. 1 = The hard-reset function caused a global shutdown.
WTCHDG	1	0 = The system watchdog timer did not cause a global shutdown. 1 = The system watchdog timer caused a global shutdown.
SHDN	0	0 = The shutdown pin did not cause a global shutdown. 1 = The shutdown pin caused a global shutdown.

POERC1 (0x11)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	32K_OK	BRDY_OK
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write Clears All, Read	Write Clears All, Read	Write Clears All, Read	Write Clears All, Read	Write Clears All, Read	Write Clears All, Read	Write Clears All, Read	Write Clears All, Read

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	5	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	4	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
32K_OK	1	Write 1 to clear 0 = The 32kHz oscillator did not cause a global shutdown. 1 = The 32kHz oscillator caused a global shutdown.
BRDY_OK	0	Write 1 to clear 0 = The BRDY did not cause a global shutdown. 1 = The BRDY caused a global shutdown.

STAT_SD0_3 (0x20)

BIT	7	6	5	4	3	2	1	0
Field	SD0_OV_S	SD0_UV_S	SD1_OV_S	SD1_UV_S	SD2_OV_S	SD2_UV_S	SD3_OV_S	SD3_UV_S
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
SD0_OV_S	7	0 = SD0 output HAS NOT risen above the rising OV threshold. 1 = SD0 output HAS risen above the rising OV threshold.

BITFIELD	BITS	DESCRIPTION
SD0_UV_S	6	0 = SD0 is enabled and SD1 output HAS NOT fallen below the falling UV threshold OR, SD0 is disabled. 1 = SD0 is enabled and SD1 output HAS fallen below the falling UV threshold.
SD1_OV_S	5	0 = SD1 output HAS NOT risen above the rising OV threshold. 1 = SD1 output HAS risen above the rising OV threshold.
SD1_UV_S	4	0 = SD1 is enabled and SD1 output HAS NOT fallen below the falling UV threshold OR, SD1 is disabled. 1 = SD1 is enabled and SD1 output HAS fallen below the falling UV threshold.
SD2_OV_S	3	0 = SD2 output HAS NOT risen above the rising OV threshold. 1 = SD2 output HAS risen above the rising OV threshold.
SD2_UV_S	2	0 = SD2 is enabled and SD2 output HAS NOT fallen below the falling UV threshold OR, SD2 is disabled. 1 = SD2 is enabled and SD2 output HAS fallen below the falling UV threshold.
SD3_OV_S	1	0 = SD3 output HAS NOT risen above the rising OV threshold. 1 = SD3 output HAS risen above the rising OV threshold.
SD3_UV_S	0	0 = SD3 is enabled and SD3 output HAS NOT fallen below the falling UV threshold OR, SD3 is disabled. 1 = SD3 is enabled and SD3 output HAS fallen below the falling UV threshold.

32K_STATUS (0x30)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	SIOSCOK	XOSCOK	32KSOURCE	32KLOAD[1:0]		CRYSTAL_CONFIG
Reset	0b0	0b0	0b0	0b0	0b0	0b10		0b0
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only		Read Only

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
SIOSCOK	5	Silicon Oscillator OK Indicator 0 = The silicon oscillator is disabled or the clock is not yet stable. 1 = The silicon oscillator is enabled and is generating a clock. During normal operation this bit is interchangeable with 32KSOURCE. The values may differ when transitioning between silicon and crystal oscillators.
XOSCOK	4	Crystal Oscillator OK Indicator 0 = The crystal oscillator is not generating a valid clock. 1 = The crystal oscillator is generating a valid clock.
32KSOURCE	3	Primary Source of Internal Oscillator 0 = XOSC is the primary source for 32kHz oscillator (silicon oscillator is used initially to get the PMIC up and running while the XOSC is settling). 1 = Silicon oscillator is used as the primary source for 32K oscillator.
32KLOAD	2:1	Internal Crystal Load Capacitance 0b00 = None 0b01 = 10pF 0b10 = 12pF 0b11 = 22pF

BITFIELD	BITS	DESCRIPTION
CRYSTAL_CONFIG	0	Primary Oscillator Clock Source Indicator 0 = Normal mode. Oscillator is generating the clock from a crystal on XIN and XOUT or silicon oscillator. 1 = Bypass mode. Oscillator is deriving the clock from an external clock driving XIN.

32K_CONFIG (0x31)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	XOSC_RETRY	RSVD	PWR_MD_32k[1:0]		32KSOURCE_OTP
Reset	0b0	0b0	0b0	0b1	0b0	OTP		OTP
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	5	Reserved. Unutilized bit. Write to 0. Reads are don't care.
XOSC_RETRY	4	Crystal Oscillator Retry When the system is operating with the backup silicon oscillator and the crystal oscillator is stable (XOSCOK = 1), setting this bit causes the system to switch back to the crystal oscillator. If the crystal oscillator is not stable (XOSCOK = 0) or the system is already using the crystal oscillator, setting this bit has no effect. This bit clears after the operation is complete.
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don't care.
PWR_MD_32k	2:1	32kHz Oscillator Mode of Operation 0b00 = Low-power mode 0b01 = Global low-power mode. The oscillator operates in low-jitter mode when the global low-power mode signal is low. When the global low-power mode signal is high, the oscillator operates in low-power mode. 0b10 = Same as 0b00 0b11 = Low-jitter mode
32KSOURCE_OTP	0	Primary Source of Internal Oscillator 0 = XOSC is the primary source for 32kHz oscillator (silicon oscillator is used initially to get the PMIC up and running while the XOSC is settling) 1 = Silicon oscillator is used as the primary source for 32kHz oscillator

CNFG_GLBL1 (0x90)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MBLPD	MBATT_RESET_HYS[1:0]		MBATT_RESET[2:0]			MBATT_RSTEN
Reset	0b0	OTP	OTP		OTP			OTP
Access Type	Write, Read	Write, Read	Write, Read		Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don't care.

BITFIELD	BITS	DESCRIPTION
MBLPD	6	0 = MBATT < MBATT_RESET falling (MBATTLOWB) does not cause a global shutdown. 1 = MBATT < MBATT_RESET falling (MBATTLOWB) forces a global shutdown.
MBATT_RESET_HYS	5:4	0x00 = 100mV 0x02 = 300mV 0x01 = 200mV 0x03 = 400mV
MBATT_RESET	3:1	0b000 = 2.7V 0b100 = 3.1V 0b001 = 2.8V 0b101 = 3.2V 0b010 = 2.9V 0b110 = 3.3V 0b011 = 3.0V 0b111 = 3.4V
MBATT_RSTEN	0	0 = The low-battery monitor only generates the MBATT < MBATT_RESET status bit and the MBATTRESET_R interrupt bit. 1 = In addition to the bits mentioned above, the low-battery monitor also pulls nRST_IO low.

CNFG_GLBL2 (0x91)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	GLBL_LPM	WDTSLPC	WDTEN	TWD[1:0]	
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b11	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	5	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
GLBL_LPM	4	0 = The global low-power mode signal is logic low. Devices that have been programmed to follow the global low-power mode signal operates in their normal power modes. 1 = The global low-power mode signal is logic high. Devices that have been programmed to follow the global low-power mode signal operates in their low-power modes.
WDTSLPC	3	0 = The system watchdog timer does not automatically clear in the sleep state. 1 = The system watchdog timer automatically clears in the sleep state.
WDTEN	2	0 = System watchdog timer disabled 1 = System watchdog timer enabled If OTP_WDTEN = 0, then WDTEN can be changed at any time. If OTP_WDTEN = 1, then once WDTEN is set, the watchdog timer cannot be disabled by clearing WDTEN. Once enabled, the system watchdog timer runs until a global shutdown occurs.

BITFIELD	BITS	DESCRIPTION
TWD	1:0	0b00 = 2s 0b01 = 16s 0b10 = 64s 0b11 = 128s If OTP_WDTT = 0, then TWD can be changed at any time. If the value of TWD needs to be changed, clear the system watchdog timer first (WDTC[1:0] = 0b01), then change the value of TWD. If OTP_WDTT = 1, then TWD can only be changed when WDTEN = 0.

CNFG_GLBL3 (0x92)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	SRCFPS0	ENFPS0	SRCFPS1	ENFPS1	WDTC
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	5	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
SRCFPS0	4	0b0 = EN0 hardware input 0b1 = ENFPS0 software bit
ENFPS0	3	0 = Disable FPS0 1 = Enable FPS0 ENFPS0 is a don’t care if SRCFPS0 = 0
SRCFPS1	2	0b0 = EN1 hardware input 0b1 = ENFPS1 software bit
ENFPS1	1	0 = Disable FPS1 1 = Enable FPS1 ENFPS1 is a don’t care if SRCFPS1 = 0
WDTC	0	Writing 0b1 to these bits clears the watchdog timer. These bits automatically reset to 0b0 after they are written to 0b1. 0b0 = The system watchdog timer is not cleared. 0b1 = The system watchdog timer is cleared.

CNFG1_ONOFF (0x93)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	SFT_RST	MRT[2:0]			SLPEN	PWR_OFF	EN0DLY
Reset	0b0	0x0	OTP			0b0	0b0	OTP
Access Type	Write, Read	Write, Read	Write, Read			Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.

BITFIELD	BITS	DESCRIPTION
SFT_RST	6	0 = No action 1 = Generates a global shutdown event that initiates the FPS0 and FPS1 power-down event and generates a reset. If both SFT_RST and PWR_OFF are set, the resulting action is SFT_RST. This bit self clears at the end of the global shutdown event.
MRT	5:3	3b000 = 2s 3b001 = 3s 3b010 = 4s 3b011 = 5s 3b100 = 6s 3b101 = 8s 3b110 = 10s 3b111 = 12s
SLPEN	2	0 = Pulling EN1 low does not place the AP into sleep mode. 1 = Pulling EN1 low places the AP into sleep mode.
PWR_OFF	1	0 = No action 1 = Generates a global shutdown event that initiates the FPS0 and FPS1 power-down event but does not generate a reset. Note that PWR_OFF is cleared at the end of any global shutdown event that it generates.
EN0DLY	0	0 = The only delay for EN0 is the debounce circuit. 1 = In addition to the debounce circuit, there is an addition 1 second delay for EN0.

CNFG2_ONOFF (0x94)

BIT	7	6	5	4	3	2	1	0
Field	MR_RST_WK	SFT_RST_WK	WD_RST_WK	WK_ACOK	WK_MBATT	WK_ALARM1R	WK_ALARM2R	WK_EN0
Reset	OTP	0b1	0b0	0b0	OTP	0b1	0b1	0b1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
MR_RST_WK	7	0 = An MR_RST event does not generate a wakeup signal (device resides in standby state). 1 = An MR_RST event generates a wakeup signal (device moves to ON state)".
SFT_RST_WK	6	0 = An SFT_RST event does not generate a wakeup signal (device resides in standby state). 1 = An SFT_RST event generates a wakeup signal (device moves to ON state).
WD_RST_WK	5	0 = An WD_RST event does not generate a wakeup signal (device resides in standby state). 1 = An WD_RST event generates a wakeup signal (device moves to ON state).
WK_ACOK	4	0 = An ACOK event does not generate a wakeup signal. 1 = An ACOK event generates a wakeup signal.
WK_MBATT	3	0 = A valid MBATT event does not generate a wakeup signal. 1 = A valid MBATT event generates a wakeup signal.
WK_ALARM1R	2	0 = An ALARM1_R event does not generate a wakeup signal. 1 = An ALARM1_R event generates a wakeup signal.
WK_ALARM2R	1	0 = An ALARM2_R event does not generate a wakeup signal. 1 = An ALARM2_R event generates a wakeup signal.

BITFIELD	BITS	DESCRIPTION
WK_EN0	0	0 = An EN0 event does not generate a wakeup signal. 1 = An EN0 event generates a wakeup signal.

MSTR_PU_PD (0x95)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MSTR_PU[2:0]			RSVD	MSTR_PD[2:0]		
Reset	0b0	OTP			0b0	OTP		
Access Type	Write, Read	Write, Read			Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
MSTR_PU	6:4	3'b000 = 31μs 3'b001 = 63μs 3'b010 = 127μs 3'b011 = 253μs 3'b100 = 508μs 3'b101 = 984μs 3'b110 = 1936μs 3'b111 = 3904μs
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
MSTR_PD	2:0	3'b000 = 31μs 3'b001 = 63μs 3'b010 = 127μs 3'b011 = 253μs 3'b100 = 508μs 3'b101 = 984μs 3'b110 = 1936μs 3'b111 = 3904μs

MSTR_SLPENTRY_EXIT (0x96)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	MSTR_SLPENTY[2:0]			RSVD	MSTR_SLPEXT[2:0]		
Reset	0b0	OTP			0b0	OTP		
Access Type	Write, Read	Write, Read			Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
MSTR_SLPENTY	6:4	3'b000 = 31μs 3'b001 = 63μs 3'b010 = 127μs 3'b011 = 253μs 3'b100 = 508μs 3'b101 = 984μs 3'b110 = 1936μs 3'b111 = 3904μs
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don’t care.

BITFIELD	BITS	DESCRIPTION
MSTR_SLPEXT	2:0	3'b000 = 31μs 3'b001 = 63μs 3'b010 = 127μs 3'b011 = 253μs 3'b100 = 508μs 3'b101 = 984μs 3'b110 = 1936μs 3'b111 = 3904μs

BUCK_PWR_MD (0x97)

BIT	7	6	5	4	3	2	1	0
Field	PWR_MD_SD3[1:0]		PWR_MD_SD2[1:0]		PWR_MD_SD1[1:0]		PWR_MD_SD0[1:0]	
Reset	OTP		OTP		OTP		OTP	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
PWR_MD_SD3	7:6	0b00 = Output disabled 0b01 = Global low-power mode 0b10 = Forced low-power mode 0b11 = Forced normal-mode
PWR_MD_SD2	5:4	0b00 = Output disabled 0b01 = Global low-power mode 0b10 = Forced low-power mode 0b11 = Forced normal-mode
PWR_MD_SD1	3:2	0b00 = Output disabled 0b01 = Global low-power mode 0b10 = Forced low-power mode 0b11 = Forced normal-mode
PWR_MD_SD0	1:0	0b00 = Output disabled 0b01 = Global low-power mode 0b10 = Forced low-power mode 0b11 = Forced normal-mode

LDO_PWR_MD0_3 (0x98)

BIT	7	6	5	4	3	2	1	0
Field	PWR_MD_L0[1:0]		PWR_MD_L1[1:0]		PWR_MD_L2[1:0]		PWR_MD_L3[1:0]	
Reset	OTP		OTP		OTP		OTP	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
PWR_MD_L0	7:6	When FPSSRC_Lx[1:0] = 0b11 0b00 = Output disabled. LDOx is off. 0b01 = Group low-power mode. LDOx operates in normal mode when the global low-power mode signal is low. When the global low-power mode signal is high, LDOx operates in low-power mode. 0b10 = Low-power mode. LDOx is forced into low-power mode. The maximum load current is 5mA and the quiescent supply current is 1.5mA. 0b11 = Normal Mode. LDOx is forced into its normal operating mode. When FPSSRC_Lx[1:0] ≠ 0b11 0b00 = Output disabled. LDOx is off. 0b01 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled when the flexible power sequencer is enabled. When LDOx is enabled, it operates in normal mode when the global low-power mode signal is low, and it operates in low-power mode when the global low-power mode signal is logic high. 0b10 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in low-power mode when the flexible power sequencer is enabled. 0b11 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in normal-power mode when the flexible power sequencer is enabled.
PWR_MD_L1	5:4	When FPSSRC_Lx[1:0] = 0b11 0b00 = Output disabled. LDOx is off. 0b01 = Group low-power mode. LDOx operates in normal mode when the global low-power mode signal is low. When the global low-power mode signal is high, LDOx operates in low-power mode. 0b10 = Low-Power Mode. LDOx is forced into low-power mode. The maximum load current is 5mA and the quiescent supply current is 1.5mA. 0b11 = Normal mode. LDOx is forced into its normal operating mode. When FPSSRC_Lx[1:0] ≠ 0b11 0b00 = Output disabled. LDOx is off. 0b01 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled when the flexible power sequencer is enabled. When LDOx is enabled, it operates in normal mode when the global low-power mode signal is low, and it operates in low-power mode when the global low-power mode signal is logic high. 0b10 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in low-power mode when the flexible power sequencer is enabled. 0b11 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in normal-power mode when the flexible power sequencer is enabled.

BITFIELD	BITS	DESCRIPTION
PWR_MD_L2	3:2	When FPSSRC_Lx[1:0] = 0b11 0b00 = Output disabled. LDOx is off. 0b01 = Group low-power mode. LDOx operates in normal mode when the global low-power mode signal is low. When the global low-power mode signal is high, LDOx operates in low-power mode. 0b10 = Low-Power Mode. LDOx is forced into low-power mode. The maximum load current is 5mA and the quiescent supply current is 1.5mA. 0b11 = Normal mode. LDOx is forced into its normal operating mode. When FPSSRC_Lx[1:0] ≠ 0b11 0b00 = Output disabled. LDOx is off. 0b01 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled when the flexible power sequencer is enabled. When LDOx is enabled, it operates in normal mode when the global low-power mode signal is low, and it operates in low-power mode when the global low-power mode signal is logic high. 0b10 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in low-power mode when the flexible power sequencer is enabled. 0b11 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in normal-power mode when the flexible power sequencer is enabled.
PWR_MD_L3	1:0	When FPSSRC_Lx[1:0] = 0b11 0b00 = Output disabled. LDOx is off. 0b01 = Group low-power mode. LDOx operates in normal mode when the global low-power mode signal is low. When the global low-power mode signal is high, LDOx operates in low-power mode. 0b10 = Low-Power Mode. LDOx is forced into low-power mode. The maximum load current is 5mA and the quiescent supply current is 1.5mA. 0b11 = Normal mode. LDOx is forced into its normal operating mode. When FPSSRC_Lx[1:0] ≠ 0b11 0b00 = Output disabled. LDOx is off. 0b01 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled when the flexible power sequencer is enabled. When LDOx is enabled, it operates in normal mode when the global low-power mode signal is low, and it operates in low-power mode when the global low-power mode signal is logic high. 0b10 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in low-power mode when the flexible power sequencer is enabled. 0b11 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in normal-power mode when the flexible power sequencer is enabled.

LDO_PWR_MD4_7 (0x99)

BIT	7	6	5	4	3	2	1	0
Field	PWR_MD_L4[1:0]		PWR_MD_L5[1:0]		PWR_MD_L6[1:0]		PWR_MD_L7[1:0]	
Reset	OTP		OTP		OTP		OTP	
Access Type	Write, Read		Write, Read		Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION
PWR_MD_L4	7:6	When FPSSRC_Lx[1:0] = 0b11 0b00 = Output disabled. LDOx is off. 0b01 = Group low-power mode. LDOx operates in normal mode when the global low-power mode signal is low. When the global low-power mode signal is high, LDOx operates in low-power mode. 0b10 = Low-power mode. LDOx is forced into low-power mode. The maximum load current is 5mA and the quiescent supply current is 1.5mA. 0b11 = Normal mode. LDOx is forced into its normal operating mode. When FPSSRC_Lx[1:0] ≠ 0b11 0b00 = Output disabled. LDOx is off. 0b01 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled when the flexible power sequencer is enabled. When LDOx is enabled, it operates in normal mode when the global low-power mode signal is low, and it operates in low-power mode when the global low-power mode signal is logic high. 0b10 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in low-power mode when the flexible power sequencer is enabled. 0b11 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in normal-power mode when the flexible power sequencer is enabled.
PWR_MD_L5	5:4	When FPSSRC_Lx[1:0] = 0b11 0b00 = Output disabled. LDOx is off. 0b01 = Group low-power mode. LDOx operates in normal mode when the global low-power mode signal is low. When the global low-power mode signal is high, LDOx operates in low-power mode. 0b10 = Low-power mode. LDOx is forced into low-power mode. The maximum load current is 5mA and the quiescent supply current is 1.5mA. 0b11 = Normal mode. LDOx is forced into its normal operating mode. When FPSSRC_Lx[1:0] ≠ 0b11 0b00 = Output disabled. LDOx is off. 0b01 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled when the flexible power sequencer is enabled. When LDOx is enabled, it operates in normal mode when the global low-power mode signal is low, and it operates in low-power mode when the global low-power mode signal is logic high. 0b10 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in low-power mode when the flexible power sequencer is enabled. 0b11 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in normal-power mode when the flexible power sequencer is enabled.

BITFIELD	BITS	DESCRIPTION
PWR_MD_L6	3:2	When FPSSRC_Lx[1:0] = 0b11 0b00 = Output disabled. LDOx is off. 0b01 = Group low-power mode. LDOx operates in normal mode when the global low-power mode signal is low. When the global low-power mode signal is high, LDOx operates in low-power mode. 0b10 = Low-power mode. LDOx is forced into low-power mode. The maximum load current is 5mA and the quiescent supply current is 1.5mA. 0b11 = Normal mode. LDOx is forced into its normal operating mode. When FPSSRC_Lx[1:0] ≠ 0b11 0b00 = Output disabled. LDOx is off. 0b01 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled when the flexible power sequencer is enabled. When LDOx is enabled, it operates in normal mode when the global low-power mode signal is low, and it operates in low-power mode when the global low-power mode signal is logic high. 0b10 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in low-power mode when the flexible power sequencer is enabled. 0b11 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in normal-power mode when the flexible power sequencer is enabled.
PWR_MD_L7	1:0	When FPSSRC_Lx[1:0] = 0b11 0b00 = Output disabled. LDOx is off. 0b01 = Group low-power mode. LDOx operates in normal mode when the global low-power mode signal is low. When the global low-power mode signal is high, LDOx operates in low-power mode. 0b10 = Low-power mode. LDOx is forced into low-power mode. The maximum load current is 5mA and the quiescent supply current is 1.5mA. 0b11 = Normal mode. LDOx is forced into its normal operating mode. When FPSSRC_Lx[1:0] ≠ 0b11 0b00 = Output disabled. LDOx is off. 0b01 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled when the flexible power sequencer is enabled. When LDOx is enabled, it operates in normal mode when the global low-power mode signal is low, and it operates in low-power mode when the global low-power mode signal is logic high. 0b10 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in low-power mode when the flexible power sequencer is enabled. 0b11 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in normal-power mode when the flexible power sequencer is enabled.

LDO_PWR_MD8 (0x9A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	PWR_MD_L8[1:0]	
Reset	0b0	0b0	0b0	0b0	0b0	0b0	OTP	
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.

BITFIELD	BITS	DESCRIPTION
RSVD	5	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	4	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don't care.
PWR_MD_L8	1:0	When FPSSRC_Lx[1:0] = 0b11 0b00 = Output disabled. LDOx is off. 0b01 = Group low-power mode. LDOx operates in normal mode when the global low-power mode signal is low. When the global low-power mode signal is high, LDOx operates in low-power mode. 0b10 = Low-power Mode. LDOx is forced into low-power mode. The maximum load current is 5mA and the quiescent supply current is 1.5mA. 0b11 = Normal mode. LDOx is forced into its normal operating mode. When FPSSRC_Lx[1:0] ≠ 0b11 0b00 = Output disabled. LDOx is off. 0b01 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled when the flexible power sequencer is enabled. When LDOx is enabled, it operates in normal mode when the global low-power mode signal is low, and it operates in low-power mode when the global low-power mode signal is logic high. 0b10 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in low-power mode when the flexible power sequencer is enabled. 0b11 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in normal-power mode when the flexible power sequencer is enabled.

LDO0FPS (0x9B)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_L0[1:0]		LDO0UPSLT[2:0]			LDO0DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_L0	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence: • The LDO enables are controlled by PWR_MD_Lx.
LDO0UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

BITFIELD	BITS	DESCRIPTION
LDO0DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

LDO1FPS (0x9C)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_L1[1:0]		LDO1UPSLT[2:0]			LDO1DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_L1	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence: • The LDO enables are controlled by PWR_MD_Lx.
LDO1UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7
LDO1DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

LDO2FPS (0x9D)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_L2[1:0]		LDO2UPSLT[2:0]			LDO2DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_L2	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence: • The LDO enables are controlled by PWR_MD_Lx.

BITFIELD	BITS	DESCRIPTION
LDO2UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7
LDO2DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

LDO3FPS (0x9E)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_L3[1:0]		LDO3UPSLT[2:0]			LDO3DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_L3	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence: • The LDO enables are controlled by PWR_MD_Lx.
LDO3UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7
LDO3DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

LDO4FPS (0x9F)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_L4[1:0]		LDO4UPSLT[2:0]			LDO4DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_L4	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence: • The LDO enables are controlled by PWR_MD_Lx.
LDO4UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7
LDO4DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

LDO5FPS (0xA0)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_L5[1:0]		LDO5UPSLT[2:0]			LDO5DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_L5	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence: • The LDO enables are controlled by PWR_MD_Lx.
LDO5UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

BITFIELD	BITS	DESCRIPTION
LDO5DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

LDO6FPS (0xA1)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_L6[1:0]		LDO6UPSLT[2:0]			LDO6DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_L6	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence: • The LDO enables are controlled by PWR_MD_Lx.
LDO6UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7
LDO6DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

LDO7FPS (0xA2)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_L7[1:0]		LDO7UPSLT[2:0]			LDO7DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_L7	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence: • The LDO enables are controlled by PWR_MD_Lx.

BITFIELD	BITS	DESCRIPTION
LDO7UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7
LDO7DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

LDO8FPS (0xA3)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_L8[1:0]		LDO8UPSLT[2:0]			LDO8DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_L8	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence: • The LDO enables are controlled by PWR_MD_Lx.
LDO8UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7
LDO8DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

SD0FPS (0xA4)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_SD0[1:0]		SD0UPSLT[2:0]			SD0DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_SD0	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence.
SD0UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7
SD0DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

SD1FPS (0xA5)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_SD1[1:0]		SD1UPSLT[2:0]			SD1DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_SD1	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence.
SD1UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

BITFIELD	BITS	DESCRIPTION
SD1DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

SD2FPS (0xA6)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_SD2[1:0]		SD2UPSLT[2:0]			SD2DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_SD2	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence.
SD2UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7
SD2DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

SD3FPS (0xA7)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_SD3[1:0]		SD3UPSLT[2:0]			SD3DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_SD3	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence.

BITFIELD	BITS	DESCRIPTION
SD3UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7
SD3DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

GPIO0FPS (0xA8)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_GPIO0[1:0]		GPIO0UPSLT[2:0]			GPIO0DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_GPIO0	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence.
GPIO0UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7
GPIO0DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

GPIO1FPS (0xA9)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_GPIO1[1:0]		GPIO1UPSLT[2:0]			GPIO1DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_GPIO1	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence.
GPIO1UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7
GPIO1DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

GPIO2FPS (0xAA)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_GPIO2[1:0]		GPIO2UPSLT[2:0]			GPIO2DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_GPIO2	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence.
GPIO2UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7
GPIO2DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

GPIO7FPS (0xAB)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_GPIO7[1:0]		GPIO7UPSLT[2:0]			GPIO7DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_GPIO7	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence.
GPIO7UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7
GPIO7DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

RSTIOFPS (0xAC)

BIT	7	6	5	4	3	2	1	0
Field	FPSSRC_RSTIO[1:0]		RST7UPSLT[2:0]			RST7DNSLT[2:0]		
Reset	OTP		OTP			OTP		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION
FPSSRC_RSTIO	7:6	0b00 = FPS0 0b01 = FPS1 0b10 = FPS1 0b11 = Not configured as part of a flexible power sequence.
RST7UPSLT	5:3	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

BITFIELD	BITS	DESCRIPTION
RST7DNSLT	2:0	3'b000 = Slot 0 3'b001 = Slot 1 3'b010 = Slot 2 3'b011 = Slot 3 3'b100 = Slot 4 3'b101 = Slot 5 3'b110 = Slot 6 3'b111 = Slot 7

SD0_CNFG1 (0x40)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	SD0VOUT[6:0]						
Reset	0b0	OTP						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care
SD0VOUT	6:0	This 7-bit configuration is a linear transfer function that starts at 0.26V, ends at 1.52V, with 10mV increments. VSD1 = 0.26V + ((SD0VOUT[6:0] - 1) x 10mV) **Note:** The 0x00 setting is reserved.

SD1_CNFG1 (0x41)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	SD1VOUT[6:0]						
Reset	0b0	OTP						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care
SD1VOUT	6:0	This 7-bit configuration is a linear transfer function that starts at 0.26V, ends at 1.52V, with 10mV increments. VSD1 = 0.26V + ((SD1VOUT[6:0] - 1) x 10mV) **Note:** The 0x00 setting is reserved.

SD2_CNFG1 (0x42)

BIT	7	6	5	4	3	2	1	0
Field	SD2VOUT[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SD2VOUT	7:0	This 8-bit configuration is a linear transfer function that starts at 0.6V, ends at 2.194V, with 6.25mV increments. VSD2 = 0.6V + (SD2VOUT[7:0] x 6.25mV)

SD3_CNFG1 (0x43)

BIT	7	6	5	4	3	2	1	0
Field	SD3VOUT[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SD3VOUT	7:0	This 8-bit configuration is a linear transfer function that starts at 0.6V, ends at 3.7875V, with 12.5mV increments. VSD3 = 0.6V + (SD3VOUT[7:0] x 12.5mV)

SD0_CNFG2 (0x44)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	SD0_SSRAMP	RSVD	RSVD	SD0FSREN	SD0ADDIS	SD0FPWMEN
Reset	0b0	0b0	OTP	0b0	0b0	0b1	OTP	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
SD0_SSRAMP	5	0 = 2.5mV/μs Ramp rate 1 = 10mV/μs Ramp rate This bit was changed from function to OTP only to avoid the BUCKOV issue when the ramp rate if changed on the fly, from 10mV to 2.5mV. Customer does not change this setting on the fly, and to avoid a false trigger this bit is converted to OTP only.
RSVD	4	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
SD0FSREN	2	0 = Active Discharge Disabled SD0 is allowed to operate in skip mode during the time the output voltage decreases (only if SD0FPWMEN = 0). In skip mode, SD0 cannot sink current from the output capacitor and the output voltage falling slew rate is a function of the external load. If the external load is heavy, then the output voltage falling slew rate becomes the fixed output voltage ramp rate. If the external load is light, then the output voltage falling slew rate becomes a function of the output capacitance and the external load. Note that the internal feedback string always imposes a 2μA load on the output. 1 = Active-discharge enabled. SD0 operates in forced PWM mode during the time the output voltage decreases. With forced PWM mode enabled, SD0 can sink current from the output capacitor to ensure that the output voltage falls at the rate fixed for output voltage ramp. To ensure a smooth output voltage decrease, the PWM mode remains engaged for 50μs after the output voltage decreases to its target voltage.

BITFIELD	BITS	DESCRIPTION
SD0ADDIS	1	0 = The active discharge function is enabled. When SD0 converter is disabled, an internal 100Ω discharge resistor is connected to the output to discharge the energy stored in the output capacitor. When SD0 converter is enabled, the discharge resistor is disconnected from the output. 1 = The active discharge function is disabled. When SD1 converter is disabled, the internal 100Ω discharge resistor is not connected to the output, and the discharge rate is dependent on the output capacitance and the load present.
SD0FPWMEN	0	0 = SD0 converter automatically skips pulses under light load conditions and transfers to fixed frequency operation as the load current increases. 1 = SD0 converter operates with fixed frequency under all load conditions.

SD0_CNFG3 (0x45)

BIT	7	6	5	4	3	2	1	0
Field	SD0_BO_THR[1:0]		SD0_BO_HYS[1:0]		RSVD	SD0_BO_PR[1:0]		SD0_OV_THR
Reset	OTP		OTP		0x0	0b11		OTP
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION
SD0_BO_THR	7:6	This 2-bit configuration is a linear transfer function, expressed as a % of output voltage setting (SD0VOUT[6:0]), that starts at 75%, and ends at 90% in 5% increments. **Note:** With 24µF of effective output capacitance and the 1.0V target output voltage, corner simulations show an undershoot of 180mV (6.5%) for a 10mA to 3mA step in 4.8µs. For prototype margin testing, it is recommended to use the tighter 90% threshold to screen for potential issues. However, for production devices, it is recommended to use the 85% setting. 2'b00 = 75% 2'b01 = 80% 2'b10 = 85% 2'b11 = 90%
SD0_BO_HYS	5:4	This 2-bit configuration is a linear transfer function, expressed as a % of output voltage setting (SD0VOUT[6:0]), that starts at 5%, and ends at 20% in 5% increments. 2'b00 = 5% 2'b01 = 10% 2'b10 = 15% 2'b11 = 20%
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don't care.
SD0_BO_PR	2:1	This 2-bit configuration provides four settings for response time (and Iq). 2'b00 = Fast 2'b01 = Medium-fast 2'b10 = Medium-slow 2'b11 = Slow

BITFIELD	BITS	DESCRIPTION
SD0_OV_THR	0	This 1-bit configuration provides two options for SD0 output over-voltage comparator rising threshold, expressed as a % of the output voltage setting (SD0VOUT[6:0]). 0 = 108.3% 1 = 116.6% **Note:** With 24µF of effective output capacitance and the 1.0V target output voltage, corner simulations show an overshoot of 70mV (2.5%) for a 3A to 10mA step in 4.8µs. For prototype margin testing, it is recommended to use the tighter 108.3% threshold to screen for potential issues. However, for production devices, it is recommended to use the 116.6% setting.

SD1_CNFG2 (0x46)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	SD1_SSRAMP	RSVD	RSVD	SD0FSREN	SD0ADDIS	SD0FPWMEN
Reset	0b0	0b0	OTP	0b0	0b0	0b1	OTP	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don't care.	
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don't care.	
SD1_SSRAMP	5	This bit was changed from function to OTP only to avoid the BUCKOV issue when the ramp rate if changed on the fly from 10mV to 2.5mV. Customer does not change this setting on the fly, and to avoid any false trigger, this bit is converted to OTP only.	0x0: 2.5mV/µs 0x1: 10mV/µs Ramp rate
RSVD	4	Reserved. Unutilized bit. Write to 0. Reads are don't care.	
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don't care.	

BITFIELD	BITS	DESCRIPTION	DECODE
SD0FSREN	2	0 = Active discharge disabled. SD0 is allowed to operate in skip mode during the time the output voltage decreases (only if SD1FPWMEN = 0). In skip mode, SD1 cannot sink current from the output capacitor and the output voltage falling slew rate is a function of the external load. If the external load is heavy, then the output voltage falling slew rate becomes the fixed output voltage ramp rate. If the external load is light, then the output voltage falling slew rate becomes a function of the output capacitance and the external load. Note that the internal feedback string always imposes a 2μA load on the output. 1 = Active discharge enabled. SD1 operates in forced PWM mode during the time the output voltage decreases. With forced PWM mode enabled, SD1 sinks current from the output capacitor to ensure that the output voltage falls at the rate fixed for output voltage ramp. To ensure a smooth output voltage decrease, the PWM mode remains engaged for 50μs after the output voltage decreases to its target voltage.	
SD0ADDIS	1	0 = The active discharge function is enabled. When the SD1 converter is disabled, an internal 100Ω discharge resistor is connected to the output to discharge the energy stored in the output capacitor. When the SD1 converter is enabled, the discharge resistor is disconnected from the output. 1 = The active discharge function is disabled. When the SD1 converter is disabled, the internal 100Ω discharge resistor is not connected to the output, and the discharge rate is dependent on the output capacitance and the load present.	
SD0FPWMEN	0	0 = SD0 converter automatically skips pulses under light load conditions and transfers to fixed frequency operation as the load current increases. 1 = SD0 converter operates with fixed frequency under all load conditions.	

SD1_CNFG3 (0x47)

BIT	7	6	5	4	3	2	1	0
Field	SD1_BO_THR[1:0]		SD1_BO_HYS[1:0]		RSVD	SD1_BO_PR[1:0]		SD1_OV_THR
Reset	OTP		OTP		0b0	0b11		OTP
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION
SD1_BO_THR	7:6	This 2-bit configuration is a linear transfer function, expressed as a % of output voltage setting (SD1VOUT[6:0]), that starts at 75%, ends at 90% in 5% increments. **Note:** With 24µF of effective output capacitance and the 1.0V target output voltage, corner simulations show an undershoot of 180mV (6.5%) for a 10mA to 3mA step in 4.8µs. For prototype margin testings it is recommended to use the tighter 90% threshold to screen for potential issues. Howevers for production devices, it is recommended to use the 85% setting. 2'b00 = 75% 2'b01 = 80% 2'b10 = 85% 2'b11 = 90%
SD1_BO_HYS	5:4	This 2-bit configuration is a linear transfer function, expressed as a % of output voltage setting (SD1VOUT[6:0]), that starts at 5%, ends at 20% in 5% increments. 2'b00 = 5% 2'b01 = 10% 2'b10 = 15% 2'b11 = 20%
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don't care.
SD1_BO_PR	2:1	This 2-bit configuration provides four settings for response time (and Iq). 2'b00 = Fast 2'b01 = Medium-fast 2'b10 = Medium-slow 2'b11 = Slow
SD1_OV_THR	0	This 1-bit configuration provides two options for SD1 output over-voltage comparator rising threshold, expressed as a % of the output voltage setting (SD1VOUT[6:0]). 0 = 108.3% 1 = 116.6% **Note:** With 24µF of effective output capacitance and the 1.0V target output voltage, corner simulations show an overshoot of 70mV (2.5%) for a 3A to 10mA step in 4.8µs. For prototype margin testings it is recommended to use the tighter 108.3% threshold to screen for potential issues. Howevers for production devices, it is recommended to use the 116.6% setting.

SD2_CNFG2 (0x48)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	SD2ADDIS	SD2FPWM EN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	OTP	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	5	Reserved. Unutilized bit. Write to 0. Reads are don't care.

BITFIELD	BITS	DESCRIPTION
RSVD	4	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don't care.
SD2ADDIS	1	0 = The active discharge function is enabled. When the SD2 converter is disabled, an internal 100Ω discharge resistor is connected to the output to discharge the energy stored in the output capacitor. When the SD2 converter is enabled, the discharge resistor is disconnected from the output. 1 = The active discharge function is disabled. When the SD2 converter is disabled, the internal 100Ω discharge resistor is not connected to the output, and the discharge rate is dependent on the output capacitance and the load present.
SD2FPWMEN	0	0 = SD2 converter automatically skips pulses under light load conditions and transfers to fixed frequency operation as the load current increases. 1 = SD2 converter operates with fixed frequency under all load conditions.

SD2_CNFG3 (0x49)

BIT	7	6	5	4	3	2	1	0
Field	SD2_BO_THR[1:0]		SD2_BO_HYS[1:0]		RSVD	SD2_BO_PR[1:0]		SD2_OV_THR
Reset	OTP		OTP		0b0	OTP		OTP
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION
SD2_BO_THR	7:6	This 2-bit configuration is a linear transfer function, expressed as a % of output voltage setting (SD1VOUT[6:0]), that starts at 75%, ends at 90% in 5% increments. **Note:** With 24μF of effective output capacitance and the 1.0V target output voltage, corner simulations show an undershoot of 180mV (6.5%) for a 10mA to 3mA step in 4.8μs. For prototype margin testing, it is recommended to use the tighter 90% threshold to screen for potential issues. However, for production devices, it is recommended to use the 85% setting. 2'b00 = 75% 2'b01 = 80% 2'b10 = 85% 2'b11 = 90%
SD2_BO_HYS	5:4	This 2-bit configuration is a linear transfer function, expressed as a % of output voltage setting (SD2VOUT[6:0]), that starts at 5%, ends at 20% in 5% increments. 2'b00 = 5% 2'b01 = 10% 2'b10 = 15% 2'b11 = 20%
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don't care.
SD2_BO_PR	2:1	This 2-bit configuration provides four settings for response time (and Iq). 2'b00 = Fast 2'b01 = Medium-fast 2'b10 = Medium-slow 2'b11 = Slow

BITFIELD	BITS	DESCRIPTION
SD2_OV_THR	0	This 1-bit configuration provides two options for SD2 output over-voltage comparator rising threshold, expressed as a % of the output voltage setting (SD2VOUT[7:0]). 0 = 108.3% 1 = 116.6% **Note:** With 13µF of effective output capacitance and the 1.2V target output voltage, corner simulations show an overshoot of 133mV (11%) for a 2A to 10mA step in 3.2µs. For prototype margin testing, it is recommended to use the tighter 108.3% threshold to screen for potential issues. However, for production devices, it is recommended to use the 116.6% setting.

SD3_CNFG2 (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	SD3ADDIS	SD3FPWM EN
Reset	0b0	0b0	0b0	0b0	0b0	0b0	OTP	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RSVD	7	Blank. There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	6	Blank. There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	5	Blank. There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	4	Blank. There is no physical bit at this location. Write to 0. Reads are don't care.
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
SD3ADDIS	1	0 = The active discharge function is enabled. When the SD3 converter is disabled, an internal 100Ω discharge resistor is connected to the output to discharge the energy stored in the output capacitor. When the SD3 converter is enabled, the discharge resistor is disconnected from the output. 1 = The active discharge function is disabled. When the SD3 converter is disabled, the internal 100Ω discharge resistor is not connected to the output, and the discharge rate is dependent on the output capacitance and the load present.
SD3FPWMEN	0	0 = SD3 converter automatically skips pulses under light load conditions and transfers to fixed frequency operation as the load current increases. 1 = SD3 converter operates with fixed frequency under all load conditions.

SD3_CNFG3 (0x4B)

BIT	7	6	5	4	3	2	1	0
Field	SD3_BO_THR[1:0]		SD3_BO_HYS[1:0]		RSVD	SD3_BO_PR[1:0]		SD3_OV_T HR
Reset	OTP		OTP		0b0	0b11		OTP
Access Type	Write, Read		Write, Read		Write, Read	Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION
SD3_BO_THR	7:6	This 2-bit configuration is a linear transfer function, expressed as a % of output voltage setting (SD1VOUT[6:0]), that starts at 75%, ends at 90% in 5% increments. **Note:** With 24µF of effective output capacitance and the 1.0V target output voltage, corner simulations show an undershoot of 180mV (6.5%) for a 10mA to 3mA step in 4.8µs. For prototype margin testing, it is recommended to use the tighter 90% threshold to screen for potential issues. However, for production devices, it is recommended to use the 85% setting. 2'b00 = 75% 2'b01 = 80% 2'b10 = 85% 2'b11 = 90%
SD3_BO_HYS	5:4	This 2-bit configuration is a linear transfer function, expressed as a % of output voltage setting (SD3VOUT[6:0]), that starts at 5%, ends at 20% in 5% increments. 2'b00 = 5% 2'b01 = 10% 2'b10 = 15% 2'b11 = 20%
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don't care.
SD3_BO_PR	2:1	This 2-bit configuration provides four settings for response time (and Iq). 2'b00 = Fast 2'b01 = Medium-fast 2'b10 = Medium-slow 2'b11 = Slow
SD3_OV_THR	0	This 1-bit configuration provides two options for SD3 output over-voltage comparator rising threshold, expressed as a % of the output voltage setting (SD2VOUT[7:0]). 0 = 108.3% 1 = 116.6% **Note:** With 13µF of effective output capacitance and the 1.2V target output voltage, corner simulations show an overshoot of 133mV (11%) for a 2A to 10mA step in 3.2µs. For prototype margin testing, it is recommended to use the tighter 108.3% threshold to screen for potential issues. However, for production devices, it is recommended to use the 116.6% setting.

LDO_CNFG1_L0 (0x50)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	VOUT_LDO_L0[5:0]					
Reset	0b0	0b0	OTP					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don't care.
VOUT_LDO_L0	5:0	This 6-bit configuration is a linear transfer function that starts at 0.8V and ends at 2.375V, with 25mV increments. VLDO = 0.8V + (VOUT_LDO[5:0] x 25mV).

LDO_CNFG2_L0 (0x51)

BIT	7	6	5	4	3	2	1	0
Field	OVCLMP_EN_L0	ALPM_EN_L0	RSVD	RSVD	POK_L0	RSVD	ADE_L0	SS_L0
Reset	OTP	OTP	0b0	0b0	0b0	0b0	OTP	OTP
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
OVCLMP_EN_L0	7	0 = Overvoltage clamp disabled. 1 = Overvoltage clamp enabled (default).
ALPM_EN_L0	6	0 = Auto low-power mode is disabled (default). 1 = Auto low-power mode is enabled.
RSVD	5	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	4	Reserved. Unutilized bit. Write to 0. Reads are don't care.
POK_L0	3	0 = The voltage is less than the POK threshold. 1 = The voltage is above the POK threshold.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don't care.
ADE_L0	1	0 = The active discharge function is disabled. When the regulator is disabled, the internal active-discharge resistor is not connected to its output and the output voltage decays at a rate that is determined by the output capacitance and the external load. When the regulator is enabled, the internal active-discharge resistor is not connected to its output. 1 = The active discharge function is enabled. When the regulator is disabled, an internal active-discharge resistor is connected to its output which discharges the energy stored in the output capacitance. When this regulator is enabled, the internal active-discharge resistor is disconnected from its output.
SS_L0	0	(Applies to both start-up and output voltage setting changes) 0 = Fast start-up and dynamic voltage change = 100mV/μs. 1 = Slow start-up and dynamic voltage change = 5mV/μs.

LDO_CNFG1_L1 (0x52)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	VOUT_LDO_L1[5:0]					
Reset	0b0	0b0	OTP					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don't care.
VOUT_LDO_L1	5:0	This 6-bit configuration is a linear transfer function that starts at 0.8V and ends at 2.375V, with 25mV increments. VLDO = 0.8V + (VOUT_LDO[5:0] x 25mV).

LDO_CNFG2_L1 (0x53)

BIT	7	6	5	4	3	2	1	0
Field	OVCLMP_EN_L1	ALPM_EN_L1	RSVD	RSVD	POK_L1	RSVD	ADE_L1	SS_L1
Reset	OTP	OTP	0b0	0b0	0b0	0b0	OTP	OTP
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
OVCLMP_EN_L1	7	0 = Overvoltage clamp disabled. 1 = Overvoltage clamp enabled (default).
ALPM_EN_L1	6	0 = Auto low-power mode is disabled (default). 1 = Auto low-power mode is enabled.
RSVD	5	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	4	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
POK_L1	3	0 = The voltage is less than the POK threshold. 1 = The voltage is above the POK threshold.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
ADE_L1	1	0 = The active discharge function is disabled. When the regulator is disabled, the internal active-discharge resistor is not connected to its output and the output voltage decays at a rate that is determined by the output capacitance and the external load. When the regulator is enabled, the internal active-discharge resistor is not connected to its output. 1 = The active discharge function is enabled. When the regulator is disabled, an internal active-discharge resistor is connected to its output which discharges the energy stored in the output capacitance. When this regulator is enabled, the internal active-discharge resistor is disconnected from its output.
SS_L1	0	(Applies to both start-up and output voltage setting changes) 0 = Fast start-up and dynamic voltage change = 100mV/μs. 1 = Slow start-up and dynamic voltage change = 5mV/μs.

LDO_CNFG1_L2 (0x54)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	VOUT_LDO_L2[5:0]					
Reset	0b0	0b0	OTP					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
VOUT_LDO_L2	5:0	This 6-bit configuration is a linear transfer function that starts at 0.8V and ends at 3.95V, with 50mV increments. VLDO = 0.8V + (VOUT_LDO[5:0] x 50mV).

LDO_CNFG2_L2 (0x55)

BIT	7	6	5	4	3	2	1	0
Field	OVCLMP_EN_L2	ALPM_EN_L2	COMP_L2[1:0]		POK_L2	RSVD	ADE_L2	SS_L2
Reset	OTP	OTP	OTP		0b0	0b0	OTP	OTP
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
OVCLMP_EN_L2	7	0 = Overvoltage clamp disabled. 1 = Overvoltage clamp enabled (default).
ALPM_EN_L2	6	0 = Auto low-power mode is disabled (default). 1 = Auto low-power mode is enabled.
COMP_L2	5:4	0b00 = Fast transconductance setting for internal amplifier. Use this setting when the LDO output capacitor loop has a series R-L-C output impedance of 50mW, 5nH, and ≥ COUT_x. This output impedance corresponds to an output capacitor that is placed directly at the output pins of the LDO (i.e., not remote). Load transient performance with this setting is 55mV typical between OUTxx and GND (default).
POK_L2	3	0 = The voltage is less than the POK threshold. 1 = The voltage is above the POK threshold.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
ADE_L2	1	0 = The active discharge function is disabled. When the regulator is disabled, the internal active-discharge resistor is not connected to its output and the output voltage decays at a rate that is determined by the output capacitance and the external load. When the regulator is enabled, the internal active-discharge resistor is not connected to its output. 1 = The active discharge function is enabled. When the regulator is disabled, an internal active-discharge resistor is connected to its output which discharges the energy stored in the output capacitance. When this regulator is enabled, the internal active-discharge resistor is disconnected from its output.
SS_L2	0	(Applies to both start-up and output voltage setting changes) 0 = Fast start-up and dynamic voltage change = 100mV/µs. 1 = Slow start-up and dynamic voltage change = 5mV/µs.

LDO_CNFG1_L3 (0x56)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	VOUT_LDO_L3[5:0]					
Reset	0b0	0b0	OTP					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
VOUT_LDO_L3	5:0	This 6-bit configuration is a linear transfer function that starts at 0.8V and ends at 3.95V, with 50mV increments. VLDO = 0.8V + (VOUT_LDO[5:0] x 50mV).

LDO_CNFG2_L3 (0x57)

BIT	7	6	5	4	3	2	1	0
Field	OVCLMP_EN_L3	ALPM_EN_L3	COMP_L3[1:0]		POK_L3	RSVD	ADE_L3	SS_L3
Reset	OTP	OTP	OTP		0b0	0b0	OTP	OTP
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
OVCLMP_EN_L3	7	0 = Overvoltage clamp disabled. 1 = Overvoltage clamp enabled (default).
ALPM_EN_L3	6	0 = Auto low-power mode is disabled (default). 1 = Auto low-power mode is enabled.
COMP_L3	5:4	0b00 = Fast transconductance setting for internal amplifier. Use this setting when the LDOs output capacitor loop has a series R-L-C output impedance of 50mW, 5nH, and ≥ COUT_x. This output impedance corresponds to an output capacitor that is placed directly at the output pins of the LDO (i.e., not remote). Load transient performance with this setting is 55mV typical between OUTxx and GND (default).
POK_L3	3	0 = The voltage is less than the POK threshold. 1 = The voltage is above the POK threshold.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don't care.
ADE_L3	1	0 = The active discharge function is disabled. When the regulator is disabled, the internal active-discharge resistor is not connected to its output and the output voltage decays at a rate that is determined by the output capacitance and the external load. When the regulator is enabled, the internal active-discharge resistor is not connected to its output. 1 = The active discharge function is enabled. When the regulator is disabled, an internal active-discharge resistor is connected to its output which discharges the energy stored in the output capacitance. When this regulator is enabled, the internal active-discharge resistor is disconnected from its output.
SS_L3	0	(Applies to both start-up and output voltage setting changes) 0 = Fast start-up and dynamic voltage change = 100mV/μs. 1 = Slow start-up and dynamic voltage change = 5mV/μs.

LDO_CNFG1_L4 (0x58)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	VOUT_LDO_L4[5:0]					
Reset	0b0	0b0	OTP					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don't care.
VOUT_LDO_L4	5:0	This 6-bit configuration is a linear transfer function that starts at 0.4V and ends at 1.275V, with 12.5mV increments.

LDO_CNFG2_L4 (0x59)

BIT	7	6	5	4	3	2	1	0
Field	OVCLMP_EN_L4	ALPM_EN_L4	COMP_L4[1:0]		POK_L4	RSVD	ADE_L4	SS_L4
Reset	OTP	OTP	OTP		0b0	0b0	OTP	OTP
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
OVCLMP_EN_L4	7	0 = Overvoltage clamp disabled. 1 = Overvoltage clamp enabled (default).
ALPM_EN_L4	6	0 = Auto low-power mode is disabled (default). 1 = Auto low-power mode is enabled.
COMP_L4	5:4	0b00 = Fast transconductance setting for internal amplifier. Use this setting when the LDOs output capacitor loop has a series R-L-C output impedance of 50mW, 5nH, and ≥ COUT_4. This output impedance corresponds to an output capacitor that is placed directly at the output pins of the LDO (i.e., not remote). Load transient performance with this setting is 55mV typical between OUTxx and GND (default),
POK_L4	3	0 = The voltage is less than the POK threshold. 1 = The voltage is above the POK threshold.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don't care.
ADE_L4	1	0 = The active discharge function is disabled. When the regulator is disabled, the internal active-discharge resistor is not connected to its output and the output voltage decays at a rate that is determined by the output capacitance and the external load. When the regulator is enabled, the internal active-discharge resistor is not connected to its output. 1 = The active discharge function is enabled. When the regulator is disabled, an internal active-discharge resistor is connected to its output which discharges the energy stored in the output capacitance. When this regulator is enabled, the internal active-discharge resistor is disconnected from its output.
SS_L4	0	(Applies to both start-up and output voltage setting changes) 0 = Fast start-up and dynamic voltage change = 100mV/μs. 1 = Slow start-up and dynamic voltage change = 5mV/μs.

LDO_CNFG1_L5 (0x5A)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	VOUT_LDO_L5[5:0]					
Reset	0b0	0b0	OTP					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don't care.
VOUT_LDO_L5	5:0	This 6-bit configuration is a linear transfer function that starts at 0.8V and ends at 3.95V, with 50mV increments. VLDO = 0.8V + (VOUT_LDO[5:0] x 50mV).

LDO_CNFG2_L5 (0x5B)

BIT	7	6	5	4	3	2	1	0
Field	OVCLMP_EN_L5	ALPM_EN_L5	COMP_L5[1:0]		POK_L5	RSVD	ADE_L5	SS_L5
Reset	OTP	OTP	OTP		0b0	0b0	OTP	OTP
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
OVCLMP_EN_L5	7	0 = Overvoltage clamp disabled. 1 = Overvoltage clamp enabled (default).
ALPM_EN_L5	6	0 = Auto low-power mode is disabled (default). 1 = Auto low-power mode is enabled.
COMP_L5	5:4	0b00 = Fast transconductance setting for internal amplifier. Use this setting when the LDOs output capacitor loop has a series R-L-C output impedance of 50mW, 5nH, and ≥ COUT_x. This output impedance corresponds to an output capacitor that is placed directly at the output pins of the LDO (i.e., not remote). Load transient performance with this setting is 55mV typical between OUTxx and GND (default).
POK_L5	3	0 = The voltage is less than the POK threshold. 1 = The voltage is above the POK threshold.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don't care.
ADE_L5	1	0 = The active discharge function is disabled. When the regulator is disabled, the internal active-discharge resistor is not connected to its output and the output voltage decays at a rate that is determined by the output capacitance and the external load. When the regulator is enabled, the internal active-discharge resistor is not connected to its output. 1 = The active discharge function is enabled. When the regulator is disabled, an internal active-discharge resistor is connected to its output which discharges the energy stored in the output capacitance. When this regulator is enabled, the internal active-discharge resistor is disconnected from its output.
SS_L5	0	(Applies to both start-up and output voltage setting changes) 0 = Fast start-up and dynamic voltage change = 100mV/μs. 1 = Slow start-up and dynamic voltage change = 5mV/μs.

LDO_CNFG1_L6 (0x5C)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	VOUT_LDO_L6[5:0]					
Reset	0b0	0b0	OTP					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don't care.
VOUT_LDO_L6	5:0	This 6-bit configuration is a linear transfer function that starts at 0.8V and ends at 3.95V, with 50mV increments. VLDO = 0.8V + (VOUT_LDO[5:0] x 50mV).

LDO_CNFG2_L6 (0x5D)

BIT	7	6	5	4	3	2	1	0
Field	OVCLMP_EN_L6	ALPM_EN_L6	COMP_L6[1:0]		POK_L6	RSVD	ADE_L6	SS_L6
Reset	OTP	OTP	OTP		0b0	0b0	OTP	OTP
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
OVCLMP_EN_L6	7	0 = Overvoltage clamp disabled. 1 = Overvoltage clamp enabled (default).
ALPM_EN_L6	6	0 = Auto low-power mode is disabled (default). 1 = Auto low-power mode is enabled.
COMP_L6	5:4	0b00 = Fast transconductance setting for internal amplifier. Use this setting when the LDOs output capacitor loop has a series R-L-C output impedance of 50mW, 5nH, and ≥ COUT_x. This output impedance corresponds to an output capacitor that is placed directly at the output pins of the LDO (i.e., not remote). Load transient performance with this setting is 55mV typical between OUTxx and GND (default).
POK_L6	3	0 = The voltage is less than the POK threshold. 1 = The voltage is above the POK threshold.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don't care.
ADE_L6	1	0 = The active discharge function is disabled. When the regulator is disabled, the internal active-discharge resistor is not connected to its output and the output voltage decays at a rate that is determined by the output capacitance and the external load. When the regulator is enabled, the internal active-discharge resistor is not connected to its output. 1 = The active discharge function is enabled. When the regulator is disabled, an internal active-discharge resistor is connected to its output which discharges the energy stored in the output capacitance. When this regulator is enabled, the internal active-discharge resistor is disconnected from its output.
SS_L6	0	(Applies to both start-up and output voltage setting changes) 0 = Fast startup and dynamic voltage change = 100mV/μs. 1 = Slow startup and dynamic voltage change = 5mV/μs.

LDO_CNFG1_L7 (0x5E)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	VOUT_LDO_L7[5:0]					
Reset	0b0	0b0	OTP					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don't care.
VOUT_LDO_L7	5:0	This 6-bit configuration is a linear transfer function that starts at 0.8V and ends at 3.95V, with 50mV increments. VLDO = 0.8V + (VOUT_LDO[5:0] x 50mV).

LDO_CNFG2_L7 (0x5F)

BIT	7	6	5	4	3	2	1	0
Field	OVCLMP_EN_L7	ALPM_EN_L7	COMP_L7[1:0]		POK_L7	RSVD	ADE_L7	SS_L7
Reset	OTP	OTP	OTP		0b0	0b0	OTP	OTP
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
OVCLMP_EN_L7	7	0 = Overvoltage clamp disabled. 1 = Overvoltage clamp enabled (default).
ALPM_EN_L7	6	0 = Auto low-power mode is disabled (default). 1 = Auto low-power mode is enabled.
COMP_L7	5:4	0b00 = Fast transconductance setting for internal amplifier. Use this setting when the LDOs output capacitor loop has a series R-L-C output impedance of 50mW, 5nH, and ≥ COUT_x. This output impedance corresponds to an output capacitor that is placed directly at the output pins of the LDO (i.e., not remote). Load transient performance with this setting is 55mV typical between OUTxx and GND (default).
POK_L7	3	0 = The voltage is less than the POK threshold. 1 = The voltage is above the POK threshold.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
ADE_L7	1	0 = The active discharge function is disabled. When the regulator is disabled, the internal active-discharge resistor is not connected to its output and the output voltage decays at a rate that is determined by the output capacitance and the external load. When the regulator is enabled, the internal active-discharge resistor is not connected to its output. 1 = The active discharge function is enabled. When the regulator is disabled, an internal active-discharge resistor is connected to its output which discharges the energy stored in the output capacitance. When this regulator is enabled, the internal active-discharge resistor is disconnected from its output.
SS_L7	0	(Applies to both start-up and output voltage setting changes) 0 = Fast startup and dynamic voltage change = 100mV/μs. 1 = Slow startup and dynamic voltage change = 5mV/μs.

LDO_CNFG1_L8 (0x60)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	VOUT_LDO_L8[5:0]					
Reset	0b0	0b0	OTP					
Access Type	Write, Read	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
VOUT_LDO_L8	5:0	This 6-bit configuration is a linear transfer function that starts at 0.8V and ends at 3.95V, with 50mV increments. VLDO = 0.8V +(VOUT_LDO[5:0] x 50mV).

LDO_CNFG2_L8 (0x61)

BIT	7	6	5	4	3	2	1	0
Field	OVCLMP_EN_L8	ALPM_EN_L8	RSVD[1:0]		POK_L8	RSVD	ADE_L8	SS_L8
Reset	OTP	OTP	0b00		0b0	0b0	OTP	OTP
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
OVCLMP_EN_L8	7	0 = Overvoltage clamp disabled. 1 = Overvoltage clamp enabled (default).
ALPM_EN_L8	6	0 = Auto low-power mode is disabled (default). 1 = Auto low-power mode is enabled.
RSVD	5:4	Reserved. Unutilized bit. Write to 0. Reads are don't care.
POK_L8	3	0 = The voltage is less than the POK threshold. 1 = The voltage is above the POK threshold.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don't care.
ADE_L8	1	0 = The active discharge function is disabled. When the regulator is disabled, the internal active-discharge resistor is not connected to its output and the output voltage decays at a rate that is determined by the output capacitance and the external load. When the regulator is enabled, the internal active-discharge resistor is not connected to its output. 1 = The active discharge function is enabled. When the regulator is disabled, an internal active-discharge resistor is connected to its output which discharges the energy stored in the output capacitance. When this regulator is enabled, the internal active-discharge resistor is disconnected from its output.
SS_L8	0	(Applies to both start-up and output voltage setting changes) 0 = Fast startup and dynamic voltage change = 100mV/μs. 1 = Slow startup and dynamic voltage change = 5mV/μs.

LDO_CNFG3 (0x62)

BIT	7	6	5	4	3	2	1	0
Field	RSVD[6:0]							L_B_EN
Reset	0b0000000							0b0
Access Type	Write, Read							Write, Read

BITFIELD	BITS	DESCRIPTION
RSVD	7:1	Reserved. Unutilized bit. Write to 0. Reads are don't care.
L_B_EN	0	0 = Bias is disabled if all LDOs are disabled (default). 1 = Bias is enabled.

CNFG_GPIO0 (0x70)

BIT	7	6	5	4	3	2	1	0
Field	DBNC0[1:0]		REFE_IRQ[1:0]		DO0	DI0	DIR0	PPDRV0
Reset	0b0		0b0		0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
DBNC0	7:6	When set for GPO (DIRx = 0): DBNCx are don't care when GPO. When set for GPI (DIRx = 1): Debounce configuration. GPIx has the following debounce times for both rising and falling edges. 0b00 = No debounce 0b01 = 8ms 0b10 = 16ms 0b11 = 32ms
REFE_IRQ	5:4	When set for GPO (DIRx = 0): REFE_IRQx are don't care when GPO. When set for GPI (DIRx = 1): Rising edge and falling edge interrupt configuration. GPIx has the interrupt behavior which is programmed with REFE_IRQx. 0b00 = Mask interrupt 0b01 = Falling edge interrupt 0b10 = Rising edge interrupt 0b11 = Falling and rising edge interrupt
DO0	3	When set for GPO (DIRx = 0): GPO output drive level is programmed with DOx. 0 = Logic low 1 = Logic high (DRVx = 1) and open-drain (DRVx = 0) When set for GPI (DIRx = 1): 0 = Clear DOx to 0 and set PUEx to 1 to enable the internal pull-up. 1 = Set DOx to 1 and set PDEx to 1 to enable the internal pull-down. See the *GPIO Programming Matrix* section for more information.
DI0	2	When set for GPO (DIRx = 0): DIx is a don't care when GPO. When set for GPI (DIRx = 1): Input Drive Level. GPIOx input logic level is specified by DIx. 0 = Input logic-low 1 = Input logic-high When DIRx = 1, this bit is read only, writes to this bit are ignored.
DIR0	1	When AMEx = 0: GPIOx direction. 0 = General purpose output (GPO) 1 = General purpose input (GPI) When AMEx = 1: When GPIO1/2/3/4 is set as an alternate mode output, write DIR1/2/3/4 (respectively) to 0 but note that the output is internally set to be active-high. When GPIO0/5/6 is set as an alternate mode input, DIR0/5/6 (respectively) determines if the signal is active high or active low. 0 = Active-low 1 = Active-high
PPDRV0	0	When set for GPO (DIRx = 0): Push-pull output drive. GPIO output configuration is determined by PPDRVx. 0 = Open-drain 1 = Push-pull When set for GPI (DIRx = 1): PPDRVx is a don't care when GPI.

CNFG_GPIO1 (0x71)

BIT	7	6	5	4	3	2	1	0
Field	DBNC1[1:0]		REFE_IRQ[1:0]		DO1	DI1	DIR1	PPDRV1
Reset	0b0		0b0		0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
DBNC1	7:6	When set for GPO (DIRx = 0): DBNCx are don't care when GPO. When set for GPI (DIRx = 1): Debounce configuration. GPIx has the following debounce times for both rising and falling edges. 0b00 = No debounce 0b01 = 8ms 0b10 = 16ms 0b11 = 32ms
REFE_IRQ	5:4	When set for GPO (DIRx = 0): REFE_IRQx are don't care when GPO. When set for GPI (DIRx = 1): Rising edge and falling edge interrupt configuration. GPIx has the interrupt behavior which is programmed with REFE_IRQx. 0b00 = Mask interrupt 0b01 = Falling edge interrupt 0b10 = Rising edge interrupt 0b11 = Falling and rising edge interrupt
DO1	3	When set for GPO (DIRx = 0): GPO output drive level is programmed with DOx. 0 = Logic low 1 = Logic high (DRVx = 1) and open-drain (DRVx = 0) When set for GPI (DIRx = 1): 0 = Clear DOx to 0 and set PUEx to 1 to enable the internal pull-up. 1 = Set DOx to 1 and set PDEx to 1 to enable the internal pull-down. See the *GPIO Programming Matrix* section for more information.
DI1	2	When set for GPO (DIRx = 0): DIx is a don't care when GPO. When set for GPI (DIRx = 1): Input Drive Level. GPIOx input logic level is specified by DIx. 0 = Input logic-low 1 = Input logic-high When DIRx = 1, this bit is read only, writes to this bit are ignored.

BITFIELD	BITS	DESCRIPTION
DIR1	1	When AMEx = 0: GPIOx direction. 0 = General purpose output (GPO) 1 = General purpose input (GPI) When AMEx = 1: When GPIO1/2/3/4 is set as an alternate mode output, write DIR1/2/3/4 (respectively) to 0 but note that the output is internally set to be active-high. When GPIO0/5/6 is set as an alternate mode input, DIR0/5/6 (respectively) determines if the signal is active high or active low. 0 = Active-low 1 = Active-high
PPDRV1	0	When set for GPO (DIRx = 0): Push-pull output drive. GPIO output configuration is determined by PPDRVx. 0 = Open-drain 1 = Push-pull When set for GPI (DIRx = 1): PPDRVx is a don't care when GPI.

CNFG_GPIO2 (0x72)

BIT	7	6	5	4	3	2	1	0
Field	DBNC2[1:0]		REFE_IRQ[1:0]		DO2	DI2	DIR2	PPDRV2
Reset	0b0		0b0		0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
DBNC2	7:6	When set for GPO (DIRx = 0): DBNCx are don't care when GPO. When set for GPI (DIRx = 1): Debounce configuration. GPIx has the following debounce times for both rising and falling edges. 0b00 = No debounce 0b01 = 8ms 0b10 = 16ms 0b11 = 32ms
REFE_IRQ	5:4	When set for GPO (DIRx = 0): REFE_IRQx are don't care when GPO. When set for GPI (DIRx = 1): Rising edge and falling edge interrupt configuration. GPIx has the interrupt behavior which is programmed with REFE_IRQx. 0b00 = Mask interrupt 0b01 = Falling edge interrupt 0b10 = Rising edge interrupt 0b11 = Falling and rising edge interrupt

BITFIELD	BITS	DESCRIPTION
DO2	3	When set for GPO (DIRx = 0): GPO output drive level is programmed with DOx. 0 = Logic low 1 = Logic high (DRVx = 1) and open-drain (DRVx = 0) When set for GPI (DIRx = 1): 0 = Clear DOx to 0 and set PUEx to 1 to enable the internal pull-up. 1 = Set DOx to 1 and set PDEx to 1 to enable the internal pull-down. See the *GPIO Programming Matrix* section for more information.
DI2	2	When set for GPO (DIRx = 0): DIx is a don't care when GPO. When set for GPI (DIRx = 1): Input Drive Level. GPIOx input logic level is specified by DIx. 0 = Input logic-low 1 = Input logic-high When DIRx = 1, this bit is read only, writes to this bit are ignored.
DIR2	1	When AMEx = 0: GPIOx direction. 0 = General purpose output (GPO) 1 = General purpose input (GPI) When AMEx = 1: When GPIO1/2/3/4 is set as an alternate mode output, write DIR1/2/3/4 (respectively) to 0 but note that the output is internally set to be active-high. When GPIO0/5/6 is set as an alternate mode input, DIR0/5/6 (respectively) determines if the signal is active high or active low. 0 = Active-low 1 = Active-high
PPDRV2	0	When set for GPO (DIRx = 0): Push-pull output drive. GPIO output configuration is determined by PPDRVx. 0 = Open-drain 1 = Push-pull When set for GPI (DIRx = 1): PPDRVx is a don't care when GPI.

CNFG_GPIO3 (0x73)

BIT	7	6	5	4	3	2	1	0
Field	DBNC3[1:0]		REFE_IRQ[1:0]		DO3	DI3	DIR3	PPDRV3
Reset	0b0		0b0		0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
DBNC3	7:6	When set for GPO (DIRx = 0): DBNCx are don't care when GPO. When set for GPI (DIRx = 1): Debounce configuration. GPIx has the following debounce times for both rising and falling edges. 0b00 = No debounce 0b01 = 8ms 0b10 = 16ms 0b11 = 32ms

BITFIELD	BITS	DESCRIPTION
REFE_IRQ	5:4	When set for GPO (DIRx = 0): REFE_IRQx are don't care when GPO. When set for GPI (DIRx = 1): Rising edge and falling edge interrupt configuration. GPIx has the interrupt behavior which is programmed with REFE_IRQx. 0b00 = Mask interrupt 0b01 = Falling edge interrupt 0b10 = Rising edge interrupt 0b11 = Falling and rising edge interrupt
DO3	3	When set for GPO (DIRx = 0): GPO output drive level is programmed with DOx. 0 = Logic low 1 = Logic high (DRVx = 1) and open-drain (DRVx = 0) When set for GPI (DIRx = 1): 0 = Clear DOx to 0 and set PUEx to 1 to enable the internal pull-up. 1 = Set DOx to 1 and set PDEx to 1 to enable the internal pull-down. See the *GPIO Programming Matrix* section for more information.
DI3	2	When set for GPO (DIRx = 0): DIx is a don't care when GPO. When set for GPI (DIRx = 1): Input Drive Level. GPIOx input logic level is specified by DIx. 0 = Input logic-low 1 = Input logic-high When DIRx = 1, this bit is read only, writes to this bit are ignored.
DIR3	1	When AMEx = 0: GPIOx direction. 0 = General purpose output (GPO) 1 = General purpose input (GPI) When AMEx = 1: When GPIO1/2/3/4 is set as an alternate mode output, write DIR1/2/3/4 (respectively) to 0 but note that the output is internally set to be active-high. When GPIO0/5/6 is set as an alternate mode input, DIR0/5/6 (respectively) determines if the signal is active high or active low. 0 = Active-low 1 = Active-high
PPDRV3	0	When set for GPO (DIRx = 0): Push-pull output drive. GPIO output configuration is determined by PPDRVx. 0 = Open-drain 1 = Push-pull When set for GPI (DIRx = 1): PPDRVx is a don't care when GPI.

CNFG_GPIO4 (0x74)

BIT	7	6	5	4	3	2	1	0
Field	DBNC4[1:0]		REFE_IRQ[1:0]		DO4	DI4	DIR4	PPDRV4
Reset	0b0		0b0		0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
DBNC4	7:6	When set for GPO (DIRx = 0): DBNCx are don't care when GPO. When set for GPI (DIRx = 1): Debounce configuration. GPIx has the following debounce times for both rising and falling edges. 0b00 = No debounce 0b01 = 8ms 0b10 = 16ms 0b11 = 32ms
REFE_IRQ	5:4	When set for GPO (DIRx = 0): REFE_IRQx are don't care when GPO. When set for GPI (DIRx = 1): Rising edge and falling edge interrupt configuration. GPIx has the interrupt behavior which is programmed with REFE_IRQx. 0b00 = Mask interrupt 0b01 = Falling edge interrupt 0b10 = Rising edge interrupt 0b11 = Falling and rising edge interrupt
DO4	3	When set for GPO (DIRx = 0): GPO output drive level is programmed with DOx. 0 = Logic low 1 = Logic high (DRVx = 1) and open-drain (DRVx = 0) When set for GPI (DIRx = 1): 0 = Clear DOx to 0 and set PUEx to 1 to enable the internal pull-up. 1 = Set DOx to 1 and set PDEx to 1 to enable the internal pull-down. See the *GPIO Programming Matrix* section for more information.
DI4	2	When set for GPO (DIRx = 0): DIx is a don't care when GPO. When set for GPI (DIRx = 1): Input Drive Level. GPIOx input logic level is specified by DIx. 0 = Input logic-low 1 = Input logic-high When DIRx = 1, this bit is read only, writes to this bit are ignored.
DIR4	1	When AMEx = 0: GPIOx direction. 0 = General purpose output (GPO) 1 = General purpose input (GPI) When AMEx = 1: When GPIO1/2/3/4 is set as an alternate mode output, write DIR1/2/3/4 (respectively) to 0 but note that the output is internally set to be active-high. When GPIO0/5/6 is set as an alternate mode input, DIR0/5/6 (respectively) determines if the signal is active high or active low. 0 = Active-low 1 = Active-high
PPDRV4	0	When set for GPO (DIRx = 0): Push-pull output drive. GPIO output configuration is determined by PPDRVx. 0 = Open-drain 1 = Push-pull When set for GPI (DIRx = 1): PPDRVx is a don't care when GPI.

CNFG_GPIO5 (0x75)

BIT	7	6	5	4	3	2	1	0
Field	DBNC5[1:0]		REFE_IRQ[1:0]		DO5	DI5	DIR5	PPDRV5
Reset	0b0		0b0		0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
DBNC5	7:6	When set for GPO (DIRx = 0): DBNCx are don't care when GPO. When set for GPI (DIRx = 1): Debounce configuration. GPIx has the following debounce times for both rising and falling edges. 0b00 = No debounce 0b01 = 8ms 0b10 = 16ms 0b11 = 32ms
REFE_IRQ	5:4	When set for GPO (DIRx = 0): REFE_IRQx are don't care when GPO. When set for GPI (DIRx = 1): Rising edge and falling edge interrupt configuration. GPIx has the interrupt behavior which is programmed with REFE_IRQx. 0b00 = Mask interrupt 0b01 = Falling edge interrupt 0b10 = Rising edge interrupt 0b11 = Falling and rising edge interrupt
DO5	3	When set for GPO (DIRx = 0): GPO output drive level is programmed with DOx. 0 = Logic low 1 = Logic high (DRVx = 1) and open-drain (DRVx = 0) When set for GPI (DIRx = 1): 0 = Clear DOx to 0 and set PUEx to 1 to enable the internal pull-up. 1 = Set DOx to 1 and set PDEx to 1 to enable the internal pull-down. See the *GPIO Programming Matrix* section for more information.
DI5	2	When set for GPO (DIRx = 0): DIx is a don't care when GPO. When set for GPI (DIRx = 1): Input Drive Level. GPIOx input logic level is specified by DIx. 0 = Input logic-low 1 = Input logic-high When DIRx = 1, this bit is read only, writes to this bit are ignored.

BITFIELD	BITS	DESCRIPTION
DIR5	1	When AMEx = 0: GPIOx direction. 0 = General purpose output (GPO) 1 = General purpose input (GPI) When AMEx = 1: When GPIO1/2/3/4 is set as an alternate mode output, write DIR1/2/3/4 (respectively) to 0 but note that the output is internally set to be active-high. When GPIO0/5/6 is set as an alternate mode input, DIR0/5/6 (respectively) determines if the signal is active high or active low. 0 = Active-low 1 = Active-high
PPDRV5	0	When set for GPO (DIRx = 0): Push-pull output drive. GPIO output configuration is determined by PPDRVx. 0 = Open-drain 1 = Push-pull When set for GPI (DIRx = 1): PPDRVx is a don't care when GPI.

CNFG_GPIO6 (0x76)

BIT	7	6	5	4	3	2	1	0
Field	DBNC6[1:0]		REFE_IRQ[1:0]		DO6	DI6	DIR6	PPDRV6
Reset	0b0		0b0		0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
DBNC6	7:6	When set for GPO (DIRx = 0): DBNCx are don't care when GPO. When set for GPI (DIRx = 1): Debounce configuration. GPIx has the following debounce times for both rising and falling edges. 0b00 = No debounce 0b01 = 8ms 0b10 = 16ms 0b11 = 32ms
REFE_IRQ	5:4	When set for GPO (DIRx = 0): REFE_IRQx are don't care when GPO. When set for GPI (DIRx = 1): Rising edge and falling edge interrupt configuration. GPIx has the interrupt behavior which is programmed with REFE_IRQx. 0b00 = Mask interrupt 0b01 = Falling edge interrupt 0b10 = Rising edge interrupt 0b11 = Falling and rising edge interrupt

BITFIELD	BITS	DESCRIPTION
DO6	3	When set for GPO (DIRx = 0): GPO output drive level is programmed with DOx. 0 = Logic low 1 = Logic high (DRVx = 1) and open-drain (DRVx = 0) When set for GPI (DIRx = 1): 0 = Clear DOx to 0 and set PUEx to 1 to enable the internal pull-up. 1 = Set DOx to 1 and set PDEx to 1 to enable the internal pull-down. See the *GPIO Programming Matrix* section for more information.
DI6	2	When set for GPO (DIRx = 0): DIx is a don't care when GPO. When set for GPI (DIRx = 1): Input Drive Level. GPIOx input logic level is specified by DIx. 0 = Input logic-low 1 = Input logic-high When DIRx = 1, this bit is read only, writes to this bit are ignored.
DIR6	1	When AMEx = 0: GPIOx direction. 0 = General purpose output (GPO) 1 = General purpose input (GPI) When AMEx = 1: When GPIO1/2/3/4 is set as an alternate mode output, write DIR1/2/3/4 (respectively) to 0 but note that the output is internally set to be active-high. When GPIO0/5/6 is set as an alternate mode input, DIR0/5/6 (respectively) determines if the signal is active high or active low. 0 = Active-low 1 = Active-high
PPDRV6	0	When set for GPO (DIRx = 0): Push-pull output drive. GPIO output configuration is determined by PPDRVx. 0 = Open-drain 1 = Push-pull When set for GPI (DIRx = 1): PPDRVx is a don't care when GPI.

CNFG_GPIO7 (0x77)

BIT	7	6	5	4	3	2	1	0
Field	DBNC7[1:0]		REFE_IRQ[1:0]		DO7	DI7	DIR7	PPDRV7
Reset	0b0		0b0		0b0	0b0	0b0	0b0
Access Type	Write, Read		Write, Read		Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
DBNC7	7:6	When set for GPO (DIRx = 0): DBNCx are don't care when GPO. When set for GPI (DIRx = 1): Debounce configuration. GPIx has the following debounce times for both rising and falling edges. 0b00 = No debounce 0b01 = 8ms 0b10 = 16ms 0b11 = 32ms

BITFIELD	BITS	DESCRIPTION
REFE_IRQ	5:4	When set for GPO (DIRx = 0): REFE_IRQx are don’t care when GPO. When set for GPI (DIRx = 1): Rising edge and falling edge interrupt configuration. GPIx has the interrupt behavior which is programmed with REFE_IRQx. 0b00 = Mask interrupt 0b01 = Falling edge interrupt 0b10 = Rising edge interrupt 0b11 = Falling and rising edge interrupt
DO7	3	When set for GPO (DIRx = 0): GPO output drive level is programmed with DOx. 0 = Logic low 1 = Logic high (DRVx = 1) and open-drain (DRVx = 0) When set for GPI (DIRx = 1): 0 = Clear DOx to 0 and set PUEx to 1 to enable the internal pull-up. 1 = Set DOx to 1 and set PDEx to 1 to enable the internal pull-down. See the *GPIO Programming Matrix* section for more information.
DI7	2	When set for GPO (DIRx = 0): DIx is a don’t care when GPO. When set for GPI (DIRx = 1): Input Drive Level. GPIOx input logic level is specified by DIx. 0 = Input logic-low 1 = Input logic-high When DIRx = 1, this bit is read only, writes to this bit are ignored.
DIR7	1	When AMEx = 0: GPIOx direction. 0 = General purpose output (GPO) 1 = General purpose input (GPI) When AMEx = 1: When GPIO1/2/3/4 is set as an alternate mode output, write DIR1/2/3/4 (respectively) to 0 but note that the output is internally set to be active-high. When GPIO0/5/6 is set as an alternate mode input, DIR0/5/6 (respectively) determines if the signal is active high or active low. 0 = Active-low 1 = Active-high
PPDRV7	0	When set for GPO (DIRx = 0): Push-pull output drive. GPIO output configuration is determined by PPDRVx. 0 = Open-drain 1 = Push-pull When set for GPI (DIRx = 1): PPDRVx is a don’t care when GPI.

PUE_GPIO (0x78)

BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PUE7	PUE6	PUE5	PUE4	PUE3	PUE2	PUE1	PUE0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
PUE7	7	GPIOx Pullup Enable 0 = Pullup disabled 1 = Pullup enabled See the *GPIO Programming Matrix* section for more information. It is recommended that users disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.
PUE6	6	GPIOx Pullup Enable 0 = Pullup disabled 1 = Pullup enabled See the *GPIO Programming Matrix* section for more information. It is recommended that users disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.
PUE5	5	GPIOx Pullup Enable 0 = Pullup disabled 1 = Pullup enabled See the *GPIO Programming Matrix* section for more information. It is recommended that users disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.
PUE4	4	GPIOx Pullup Enable 0 = Pullup disabled 1 = Pullup enabled See the *GPIO Programming Matrix* section for more information. It is recommended that users disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.
PUE3	3	GPIOx Pullup Enable 0 = Pullup disabled 1 = Pullup enabled See the *GPIO Programming Matrix* section for more information. It is recommended that users disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.
PUE2	2	GPIOx Pullup Enable 0 = Pullup disabled 1 = Pullup enabled See the *GPIO Programming Matrix* section for more information. It is recommended that users disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.
PUE1	1	GPIOx Pullup Enable 0 = Pullup disabled 1 = Pullup enabled See the *GPIO Programming Matrix* section for more information. It is recommended that users disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.

BITFIELD	BITS	DESCRIPTION
PUE0	0	GPOIx Pullup Enable 0 = Pullup disabled 1 = Pullup enabled See the *GPIO Programming Matrix* section for more information. It is recommended that users disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.

PDE_GPIO (0x79)

BIT	7	6	5	4	3	2	1	0
Field	PDE7	PDE6	PDE5	PDE4	PDE3	PDE2	PDE1	PDE0
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
PDE7	7	GPOIx Pulldown Enable 0 = Pulldown disabled 1 = Pulldown enabled See the *GPIO Programming Matrix* section for more information. It is recommended that users disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.
PDE6	6	GPOIx Pulldown Enable 0 = Pulldown disabled 1 = Pulldown enabled See the *GPIO Programming Matrix* section for more information. It is recommended that users disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.
PDE5	5	GPOIx Pulldown Enable 0 = Pulldown disabled 1 = Pulldown enabled See the *GPIO Programming Matrix* section for more information. It is recommended that users disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.
PDE4	4	GPOIx Pulldown Enable 0 = Pulldown disabled 1 = Pulldown enabled See the *GPIO Programming Matrix* section for more information. It is recommended that users disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.

BITFIELD	BITS	DESCRIPTION
PDE3	3	GPIOx Pulldown Enable 0 = Pulldown disabled 1 = Pulldown enabled See the *GPIO Programming Matrix* section for more information. It is recommended that users disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.
PDE2	2	GPIOx Pulldown Enable 0 = Pulldown disabled 1 = Pulldown enabled See the *GPIO Programming Matrix* section for more information. It is recommended that users disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.
PDE1	1	GPIOx Pulldown Enable 0 = Pulldown disabled 1 = Pulldown enabled See the *GPIO Programming Matrix* section for more information. It is recommended that users disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.
PDE0	0	GPIOx Pulldown Enable 0 = Pulldown disabled 1 = Pulldown enabled See the GPIO Programming Matrix section for more information. It is recommended that users disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.

AME_GPIO (0x7A)

BIT	7	6	5	4	3	2	1	0
Field	AME7	AME6	AME5	AME4	AME3	AME2	AME1	AME0
Reset	OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
AME7	7	Alternate Mode Enable for GPIO7. 0 = Standard GPI or GPO as programmed by DIR1. 1 = Flexible power sequencer active-high Output.
AME6	6	Alternate Mode Enable for GPIO6. 0 = Standard GPI or GPO as programmed by DIR4. 1 = 32kHz output (32k_OUT1)
AME5	5	Alternate Mode Enable for GPIO5. 0 = Standard GPI or GPO as programmed by DIR4. 1 = 32kHz output (32k_OUT1)
AME4	4	Alternate Mode Enable for GPIO4. 0 = Standard GPI or GPO as programmed by DIR4. 1 = 32kHz output (32k_OUT1)

BITFIELD	BITS	DESCRIPTION
AME3	3	Alternate Mode Enable for GPIO3. 0 = Standard GPI or GPO as programmed by DIR4. 1 = ACOK input
AME2	2	Alternate Mode Enable for GPIO2. 0 = Standard GPI or GPO as programmed by DIR1. 1 = Flexible power sequencer active-high output.
AME1	1	Alternate Mode Enable for GPIO1. 0 = Standard GPI or GPO as programmed by DIR1. 1 = Flexible power sequencer active-high output.
AME0	0	Alternate Mode Enable for GPIO0. 0 = Standard GPI or GPO as programmed by DIR1. 1 = Flexible power sequencer active-high output.

CID0 (0xB0)

BIT	7	6	5	4	3	2	1	0
Field	SR[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SR	7:0	SR[23:16] + SR[15:8] + SR[7:0] form a 24-bit serial number.

CID1 (0xB1)

BIT	7	6	5	4	3	2	1	0
Field	SR[15:8]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SR	7:0	SR[23:16] + SR[15:8] + SR[7:0] form a 24-bit serial number.

CID2 (0xB2)

BIT	7	6	5	4	3	2	1	0
Field	SR[23:16]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
SR	7:0	SR[23:16] + SR[15:8] + SR[7:0] form a 24-bit serial number.

CID3 (0xB3)

BIT	7	6	5	4	3	2	1	0
Field	DIDM[3:0]				DIDO[3:0]			
Reset	Metal Version				OTP			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
DIDM	7:4	4'b0000 = Initial metal mask (device version 1) 4'b0001 = First metal revision (device version 2) 4'b0010 and above are reserved for future revisions.
DIDO	3:0	0x0 = Preproduction device 0x1 = Production device 0x2 = Experimental device 0x3 and above are reserved for future uses.

CID4 (0xB4)

BIT	7	6	5	4	3	2	1	0
Field	DRV[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
DRV	7:0	These bits track the OTP configuration for each part.

CNFG_BBC (0x80)

BIT	7	6	5	4	3	2	1	0
Field	BBCRS[1:0]		BBCLOWIEN	BBCVS[1:0]		BBCCS[1:0]		BBCEN
Reset	0b01		0b0	0b00		0b00		0b0
Access Type	Write, Read		Write, Read	Write, Read		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION
BBCRS	7:6	0x00 = 0.1kΩ 0x01 = 1kΩ 0x02 = 3kΩ 0x03 = 6kΩ
BBCLOWIEN	5	0 = Enable 1 = Disable
BBCVS	4:3	0x00 = 2.5V 0x01 = 3.0V 0x02 = 3.3V 0x03 = 3.5V

BITFIELD	BITS	DESCRIPTION
BBCCS	2:1	BBCLOWIEN = 0 0x00 = 50µA 0x01 = 50µA 0x02 = 50µA 0x03 = 100µA BBCLOWIEN = 1 0x00 = 200µA 0x01 = 600µA 0x10 = 800µA 0x11 = 400µA
BBCEN	0	0 = Backup battery charger off 1 = Backup battery charger on

I2C_CTRL1 (0xC0)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	PAIR	RSVD	RSVD	WD_EN	HS_EXT
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	5	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
PAIR	4	0 = Pair address mode is disabled and sequential mode is used for multiple register write protocol. 1 = Pair address mode is enabled for multiple register write protocol.
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
WD_EN	1	0 = Watchdog function is disabled (I^2C Rev 4.0 compliant) 1 = Watchdog function is enabled (SMBus compatible)
HS_EXT	0	0 = HS-mode extension is disabled (I^2C Rev 4.0 compliant) 1 = HS-mode extension is enabled. HS-mode is enabled without HS-mode entrace code and keeps HS-mode during and after STOP condition.

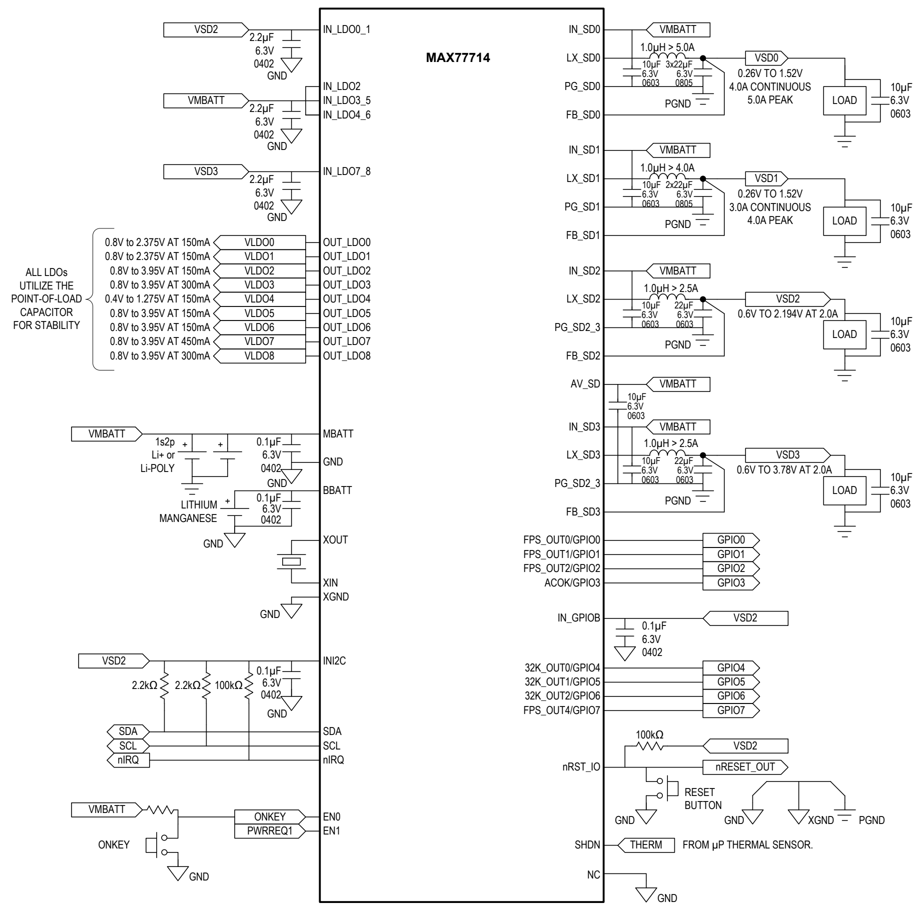
I2C_CTRL2 (0xC1)

BIT	7	6	5	4	3	2	1	0
Field	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	I2CWP
Reset	0b0	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION
RSVD	7	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	6	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	5	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	4	Reserved. Unutilized bit. Write to 0. Reads are don’t care.
RSVD	3	Reserved. Unutilized bit. Write to 0. Reads are don’t care.

BITFIELD	BITS	DESCRIPTION
RSVD	2	Reserved. Unutilized bit. Write to 0. Reads are don't care.
RSVD	1	Reserved. Unutilized bit. Write to 0. Reads are don't care.
I2CWP	0	0 = Disable write protect for all registers in the PMIC. Writes to any register through the I^2C write protocol results in the data value being written to the register. 1 = Enable write protect for all registers in the PMIC. Writes to any register through the I^2C write protocol does NOT result in the data value being written to the register. The STOP condition at the end of an I^2C transaction resets this bit back to its default value.

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP. RANGE	PIN-PACKAGE
MAX77714EWC+T	-40°C to +85°C	70-Bump, 0.4mm Pitch, WLP, 4.1mm x 3.25mm x 0.7mm; CID4 = 0x01
MAX77714FEWC+T	-40°C to +85°C	70-Bump, 0.4mm Pitch, WLP, 4.1mm x 3.25mm x 0.7mm; CID4 = 0x06
MAX77714FEWC+	-40°C to +85°C	70-Bump, 0.4mm Pitch, WLP, 4.1mm x 3.25mm x 0.7mm; CID4 = 0x06
MAX77714GEWC+	-40°C to +85°C	70-Bump, 0.4mm Pitch, WLP, 4.1mm x 3.25mm x 0.7mm; CID4 = 0x08
MAX77714GEWC+T	-40°C to +85°C	70-Bump, 0.4mm Pitch, WLP, 4.1mm x 3.25mm x 0.7mm; CID4 = 0x08

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/18	Initial release	—
1	7/19	Updated *Simplified Block Diagram* and TOC36, added MAX77714F to the *Ordering Information* table, and indicated which bits are OTP programmable in the *Register Map* tables	2, 39, 81–83, 97, 100–104, 106–119, 121, 123–150, 163–166, 170
2	2/22	Updated Or*dering Information* table	166