

CT431

XtremeSense® TMR Ultra-Low Noise, <1% Total Error Current Sensor

Features

- Integrated Contact Current Sensing for Low to Medium Current Ranges:
 - o 0 A to +20 A
 - -20 A to +20 A
 - 0 A to +30 A
 - \circ $\,$ -30 A to +30 A
 - \circ 0 A to +50 A
 - \circ $\,$ -50 A to +50 A
- Integrated Current Carrying Conductor (CCC)
- Linear Analog Output Voltage
- Total Error Output $\leq \pm 1.0\%$ FS, -40°C to +125°C
- 1 MHz Bandwidth
- Response Time: ~0.30 µs
- Low Noise: 9 mARMs to 15 mARMs @ fBW = 100 kHz
- Reference Voltage Output for AC/DC Current Measurements
- VOUT VREF < 1.0% FS, -40°C to +125°C
- Immunity to Common Mode Fields: < 5.0 mA/mT
- Supply Voltage: 3.0 V to 3.6 V
- Over-Current Detection (OCD™)
 Out of Range Currents
- 16-Lead SOIC-Wide Package

Applications

- Solar/Power Inverters
- UPS, SMPS and Telecom Power Supplies
- Battery Management Systems
- Motor Control
- White Goods
- Power Utility Meters
- Over-Current Fault Protection

Product Description

The CT431 is a high bandwidth and ultra-low noise integrated contact current sensor that uses Crocus Technology's patented XtremeSense® TMR technology to enable high accuracy current measurements for many consumer, enterprise, and industrial applications. It supports six (6) current ranges where the integrated current carrying conductor (CCC) will handle up to 50 A of current and generates a current measurement as a linear analog output voltage. It achieves a total output error of less than $\pm 1.0\%$ full-scale (FS) over voltage and the full temperature range.

It has about a 0.30 μ s output response time while the current consumption is about 6.0 mA and is immune to common mode fields. The CT431 has an integrated overcurrent detection (OCD) circuitry to identify out of range currents (OCD) with the result outputted to the fault-bar (FLT) pin. The FLT is an open drain, active LOW digital signal that is activated by the CT431 to alert the microcontroller that a fault condition has occurred.

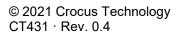
The CT431 is offered in an industry standard 16-lead SOIC-Wide package that is "green" and RoHS compliant.

Part Ordering Information

Part Number	Operating Temperature Range	Current Range	Package	Packing Method				
CT431-ESWF20DR	-40°C to +85°C	0 A to +20 A						
CT431-HSWF20DR	-40°C to +125°C	0 A 10 +20 A						
CT431-ESWF20MR	-40°C to +85°C	-20 A to +20 A						
CT431-HSWF20MR	-40°C to +125°C	-20 A 10 +20 A	4					
CT431-ESWF30DR	-40°C to +85°C	0 A to 120 A						
CT431-HSWF30DR	-40°C to +125°C	0 A to +30 A	16-lead SOIC-Wide					
CT431-ESWF30MR	-40°C to +85°C	20 A to 120 A	10.20 x 10.31 x 2.54 mm	Tape & Reel				
CT431-HSWF30MR	-40°C to +125°C	-30 A to +30 A						
CT431-ESWF50DR	-40°C to +85°C							
CT431-HSWF50DR	-40°C to +125°C	0 A to +50 A						
CT431-ESWF50MR	-40°C to +85°C							
CT431-HSWF50MR	-40°C to +125°C	-50 A to +50 A						

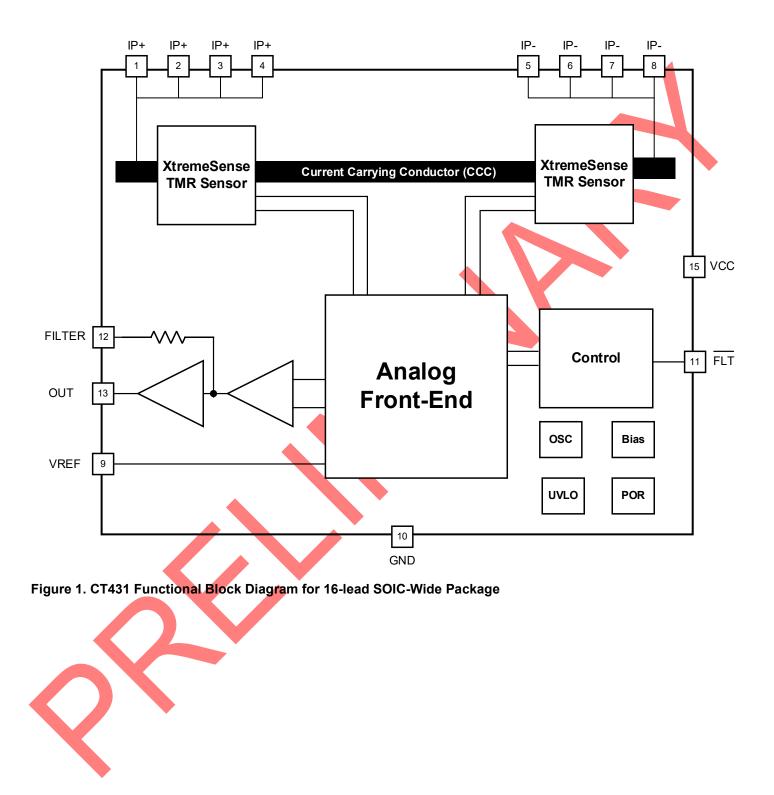
Evaluation Board Ordering Information

Part Number	Current Range	Operating Temperature Range
CTD431-20DC	0 A to +20 A	
CTD431-20AC	-20 A to +20 A	
CTD431-30DC	0 A to +30 A	-40°C to +85°C
CTD431-30AC	-30 A to +30 A	-40 C 10 +05 C
CTD431-50DC	0 A to +50 A	
CTD431-50AC	-50 A to +50 A	

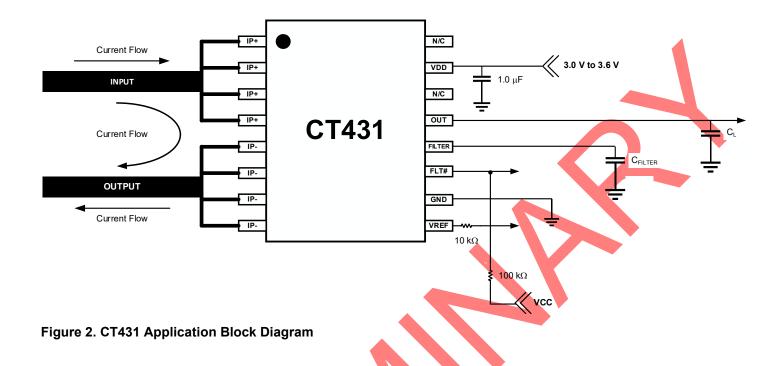


Block Diagram

CT431



Application Diagram



Component	Description	Vendor & Part Number	Parameter	Min.	Тур.	Max.	Unit
C _{BYP}	1.0 μF, X5R or Better	Murata GRM155C81A105KA12	С		1.0		μF
Cfilter	Various, X5R or Better	Murata			Table 2		pF
R _{FLT#}	100 kΩ Pull-up Resistor	Various	R1		100		kΩ
RVREF	10 k Ω Resistor	Various	R2		10		kΩ

CT431 Pin Configuration

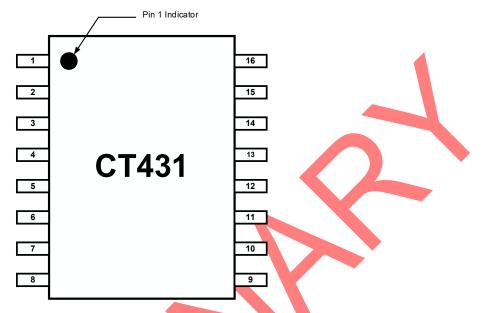


Figure 3. CT431 Pin-out Diagram for 16-lead SOIC-Wide Package (Top-Down View)

Pin Definition

Pin #	Pin Name	Pin Description
1		
2	IP+	Input primary conductor (positive).
3	1F-t	input primary conductor (positive).
4		
5		
6	JP-	Output primer conductor (pagetive)
7	IP-	Output primary conductor (negative).
8		
9	VREF	Reference voltage output. If not used, then do not connect.
10	GND	Ground.
		Active LOW output fault signal (open drain output) to indicate that the following parameters are outside of normal operational bounds:
11	FLT	Over-Current Detection
		UVLO
		If not used, then do not connect.
12	FILTER	Filter pin to improve noise performance by connecting an external capacitor to set the cut-off frequency.
13	OUT	Analog output voltage that represents the measured current.
14	N/C	No connect.
15	VCC	Supply voltage.
16	N/C	No connect

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the CT431 and may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
Vcc	Supply Voltage		-0.3	6.0	V
V _{I/O}	Analog Input/Output Pins	s Maximum Voltage	-0.3	Vcc + 0.3*	V
I _{CCC(MAX)}	Current Carrying Conduc	ctor, $T_A = +25^{\circ}C$		60	А
VSURGE	Dielectric Surge Strength Test Voltage	IEC 61000-4-5: Tested \pm 5 Pulses at 2/60 seconds, 1.2 μ s (rise) and 50 μ s (width)	10		kV
Isurge	Surge Strength Test Current	Tested ± 5 Pulses at 3/60 seconds, 8.0 μ s (rise) and 20 μ s (width)	10		kA
ESD	Electrostatic Discharge	Human Body Model (HBM) per JESD22-A114	±2.0		kV
ESD	Protection Level	Charged Device Model (CDM) per JESD22-C101	±0.5		ΚV
TJ	Junction Temperature		-40	+150	°C
Tstg	Storage Temperature		-65	+155	°C
TL	Lead Soldering Tempera	ture, 10 Seconds		+260	°C

*The lower of V_{CC} + 0.3 V or 6.0 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual operation of the CT431. Recommended operating conditions are specified to ensure optimal performance to the specifications. Crocus Technology does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter		Min.	Тур.	Max.	Unit
Vcc	Supply Voltage Range		3.0	3.3	3.6	V
Vout	OUT Voltage Range		0		Vcc	V
Іоит	OUT Current				±1.0	mA
т.	T Or and in a Marking t	Industrial	-40	+25	+85	°C
TA	Operating Ambient Temperature Extended Industria		-40	+25	+125	C

Thermal Properties

Junction-to-ambient thermal resistance is a function of application and board layout and is determined in accordance to JEDEC standard JESD51 for a four (4) layer 2s2p FR-4 printed circuit board (PCB) with 2 oz. of copper (Cu). Special attention must be paid not to exceed junction temperature $T_{J(MAX)}$ at a given ambient temperature T_A .

Symbol	Parameter	Min.	Тур.	Max.	Unit
θja_soicw	Junction-to-Ambient Thermal Resistance, SOICW-16		119	144	°C/W
θJC_SOICW	Junction-to-Case Thermal Resistance, SOICW-16		86	112	°C/W

Isolation Ratings

Symbol	Parameter	Conditions	Rating	Unit
V _{ISO} Rated Isolation Voltage		Agency Tested per IEC 62368* for 60 seconds. Production Tested at V_{ISO} for 1 second per IEC 62368.	5.0	kV _{RMS}
		Agency Tested per UL1577 for 60 seconds. Production Tested at $V_{\rm ISO}$ for 1 second per UL1577.	5.0	kV _{RMS}
Vwork_iso	Working Voltage for Basic Isolation	Tested per per IEC 62368*	1820 1287	Vpk Vrms
Vwork_ri	Working Voltage for Reinforced Isolation	Tested per IEC 62368*	915 647	Vpk Vrms
d _{CR}	Creepage Distance	Minimum Distance Along Package Body from IP Pins to I/O Pins	9.21	mm
dc∟	Clearance Distance	Minimum Distance Through Air from IP Pins to I/O Pins	8.79	mm
diso	Distance Through Isolation	Minimum Internal Distance Through Isolation	40	μm
CTI	Comparative Tracking Index	Material Group II	400 to 599	V

*IEC 62368 is the succeeding standard to IEC 60950-1 (Edition 2) for isolation testing specifications and as such it will be compliant to the latter standard.

Electrical Specifications

General Parameters

Unless otherwise specified: $V_{CC} = 3.0$ V to 3.6 V, $T_A = -40^{\circ}$ C to $+125^{\circ}$ C, $C_{BYP} = 1.0$ µF. Typical values are $V_{CC} = 3.3$ V and $T_A = +25^{\circ}$ C.

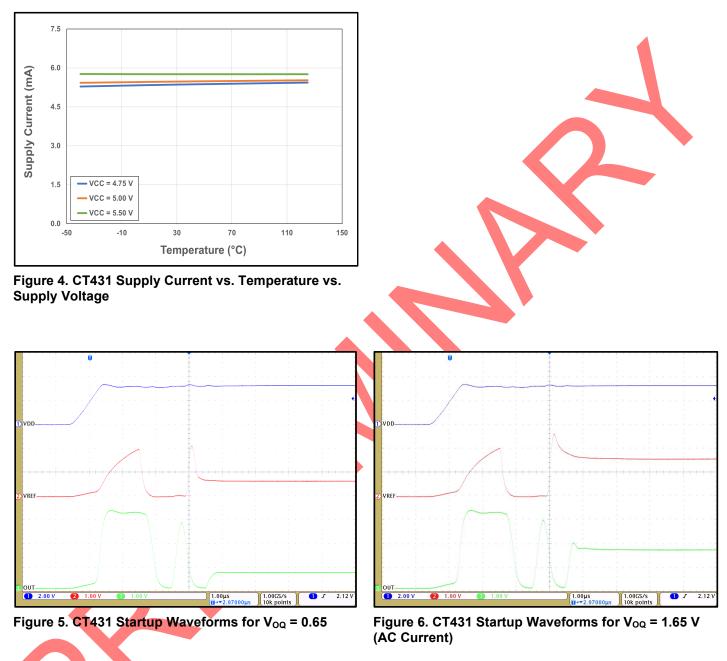
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Power Sup	plies					
Icc	Supply Current	f _{BW} = 1 MHz No load, I _P = 0 A		6.0	9.0	mA
I _{OUT}	OUT Maximum Drive Capability	OUT covers 10% to 90% of V_{CC} span.	-1.0		+1.0	mA
CL_OUT	OUT Capacitive Load ⁽¹⁾				100	pF
RL_OUT	OUT Resistive Load (1)			100		kΩ
IVREF	VREF Maximum Drive Capability		-50		+50	μA
CL_VREF	VREF Capacitive Load ⁽¹⁾				10	pF
RL_VREF	VREF Resistive Load (1)			100		kΩ
	Internal Filter Resistance (1)			15		kΩ
RIP	Primary Conductor Resistance ⁽¹⁾			0.5		mΩ
PSRR	Power Supply Rejection Ratio ⁽¹⁾			TBD		dB
SPSRR	Sensitivity Power Supply Rejection Ratio ⁽¹⁾			TBD		dB

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Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
OPSRR	Offset Power Supply Rejection Ratio ⁽¹⁾			TBD		dB
Analog Ou	tput (OUT)					
V _{OUT}	OUT Voltage Linear Range	$V_{SIG_AC} = \pm 1.00 V$ $V_{SIG_DC} = \pm 2.00 V$	0.65		2.65	V
Vout_sat	Output High Saturation Voltage	V _{OUT} , T _A = +25°C,	V _{CC} - 0.30	V _{cc} - 0.25		V
CMFR	Common Mode Field Rejection ⁽¹⁾			5		mA/mT
TCS	Temperature Coefficient of Sensitivity	Absolute Value T _A = -40°C to +125°C		10	40	ppm/°C
тсо	Temperature Coefficient of Offset ⁽¹⁾	Absolute Value T _A = -40°C to +125°C		0.16		% FS
Reference	Voltage (VREF)					
VREF	Reference Voltage	DC Current (Unipolar)		0.65 1.65		v
Fault Outp	ut (FLT)					
VFLT#_OL	FLT Voltage LOW	IFLT#_OUT ≤ 20 mA	0		0.5	V
I _{LEAK_FLT#}	High Impedance Output Leakage Current	V _{FLT#_OH} = V _{CC}		5		μA
RPU	FLT Pull-up Resistor			100		kΩ
Timings						
ton	Power-On Time ⁽¹⁾	$V_{CC} \ge 2.50 V$		100	200	μs
t _{RISE}	Rise Time ⁽¹⁾	$I_P = I_{RANGE(MAX)},$		0.20		μs
tresponse	Response Time ⁽¹⁾	T _A = +25°C,		0.30		μs
t _{DELAY}	Propagation Delay	C∟ = 220 pF		0.20		μs
Protection						
Vuvlo	Under-Voltage Lockout	Rising Vcc		2.50		V
VOVLO		Falling V _{cc}		2.45		V
VUV_HYS	UVLO Hysteresis			50		mV
locd_u	Over-Current Detection (OCD)	Rising I _P		1.1 × I _{RANGE(MAX)}		A
	for DC Current (Unipolar)	Falling I _P		0.9 × Irange(max)		
	Over-Current Detection (OCD)	Rising I _P		±1.1 × Irange(max)		
IOCD_B	for AC Current (Bipolar)	Falling I _P		±0.9 × I _{RANGE(MAX)}		A
locd_hys	Over-Current Detection Hysteresis			0.2 × Irange(max)		Α

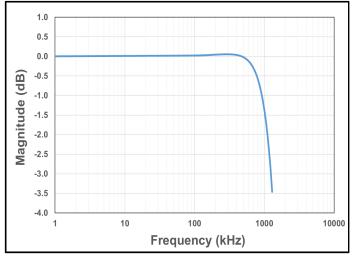
(1) Guaranteed by design and/or characterization; not tested in production.

Electrical Characteristics



Electrical Characteristics (continued)

 V_{CC} = 3.3 V and T_A = +25°C and C_{BYP} = 1.0 μ F (unless otherwise specified)





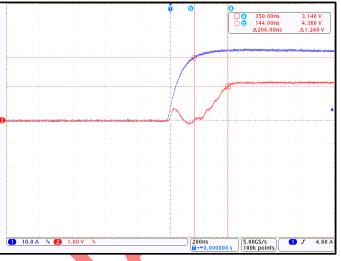
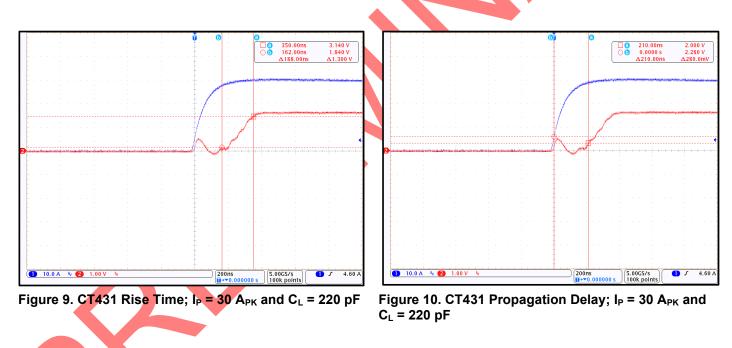


Figure 8. CT431 Response Time; $I_P = 30 A_{PK}$ and $C_L = 220 pF$



Electrical Characteristics (continued)

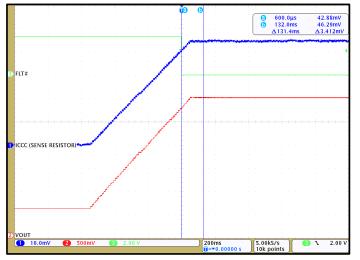


Figure 11. CT431 OCD enabled at 110% of +50 A_{DC} and FLT# is LOW

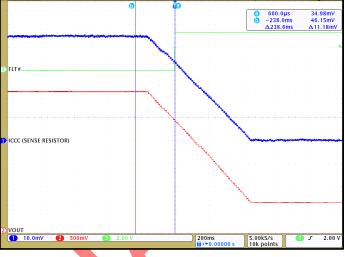


Figure 12. CT431 OCD disabled at 90% of +50 A_{DC} and FLT# is HIGH

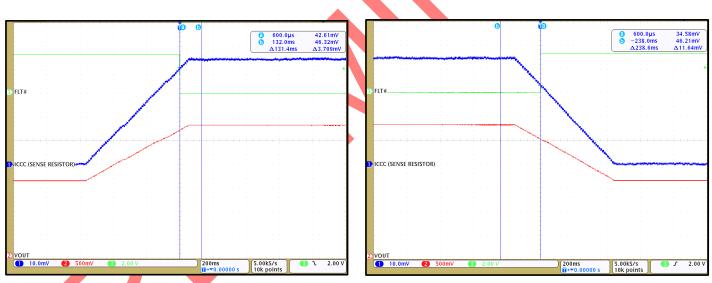
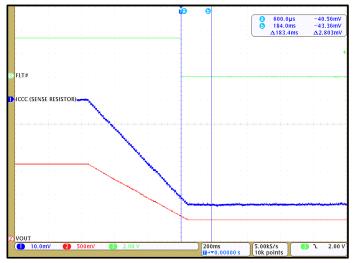


Figure 13. CT431 OCD enabled at +110% of +50 A_{PK} and FLT# is LOW

Figure 14. CT431 OCD disabled at +90% of +50 A_{PK} and FLT# is HIGH

Electrical Characteristics (continued)



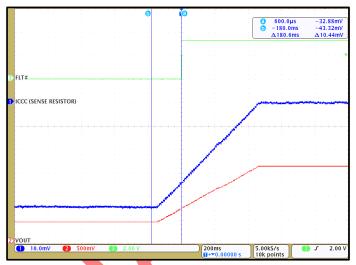


Figure 15. CT431 OCD enabled at -110% of -50 A_{PK} and FLT# is LOW

Figure 16. CT431 OCD disabled at -90% of -50 A_{PK} and FLT# is HIGH

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CT431-xSWF20DR: 0 A to +20 A

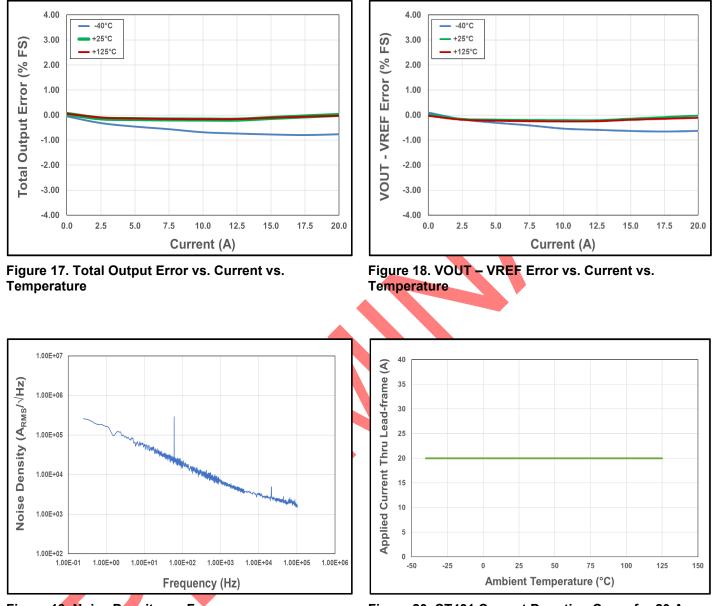
Unless otherwise specified: V_{CC} = 3.0 V to 3.6 V, T_A = -40°C to +125°C, C_{BYP} = 1.0 μ F. Typical values are V_{CC} = 3.3 V and T_A = +25°C.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit		
IRANGE	Current Range		0		+20	А		
Voq	Voltage Output Quiescent	T _A = +25°C, I _P = 0 A	0.645	0.650	0.655	V		
Vout - V _{REF}	OUT – VREF Offset Voltage	V _{CC} = 3.3 V T _A = -40°C to +125°C		5.0		mV		
S	Sensitivity	$I_{RANGE(MIN)} < I_P < I_{RANGE(MAX)}$		100		mV/A		
Eout	Total Output Error	$I_P = I_{P(MAX)}$		±0.7	±1.0	% FS		
ELIN	Non-Linearity Error	I _P = 0 A to +20 A		±0.3	±0.5	% FS		
EOUT-VREF	VOUT – VREF Error	$I_P = I_{P(MAX),} V_{CC} = 3.3 V$ $T_A = -40^{\circ}C \text{ to } +125^{\circ}C$			±1.0	% FS		
f _{BW}	Bandwidth ⁽¹⁾	Small Signal = -3 dB		1.0		MHz		
e _N	Noise ⁽¹⁾	T _A = +25°C, f _{BW} = 100 kHz		9.0		mA _{RMS}		
Lifetime D	Lifetime Drift							
ETOT_DRIFT	Total Output Error Lifetime Drift ⁽¹⁾	$I_P = I_{P(MAX)}$		±1.0		% FS		

(1) Guaranteed by design and characterization; not tested in production.

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Electrical Characteristics for CT431-xSWF20DR







CT431-xSWF20MR: -20 A to +20 A

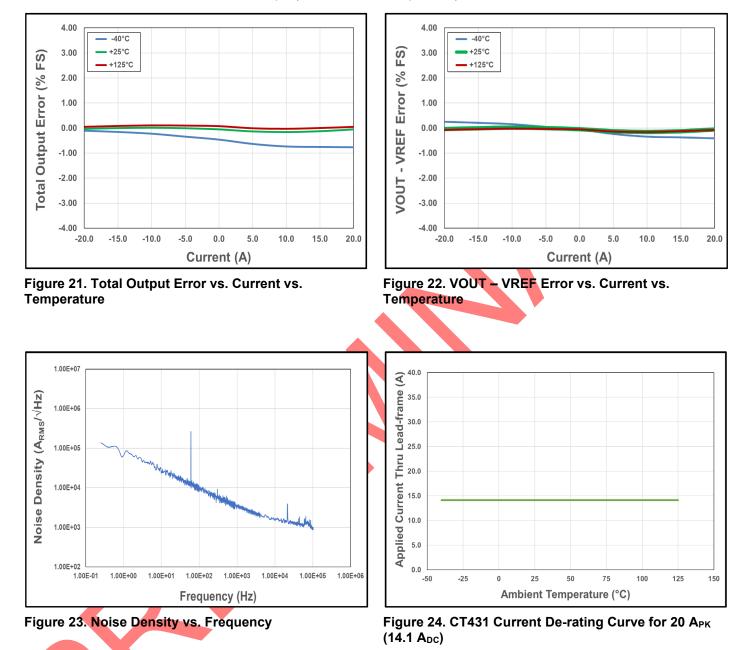
Unless otherwise specified: V_{CC} = 3.0 V to 3.6 V, T_A = -40°C to +125°C, C_{BYP} = 1.0 μ F. Typical values are V_{CC} = 3.3 V and T_A = +25°C.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
IRANGE	Current Range		-20		+20	А
Voq	Voltage Output Quiescent	T _A = +25°C, I _P = 0 A	1.645	1.650	1.655	V
V _{OUT} - V _{REF}	OUT – VREF Offset Voltage	V _{CC} = 3.3 V T _A = -40°C to +125°C		5.0		mV
S	Sensitivity	$I_{RANGE(MIN)} < I_P < I_{RANGE(MAX)}$		50		mV/A
Eout	Total Output Error	$I_{P} = I_{P(MAX)}$		±0.5	±1.0	% FS
ELIN	Non-Linearity Error	I _P = -20 A to +20 A		±0.3	±0.5	% FS
EOUT-VREF	VOUT – VREF Error	$I_P = I_{P(MAX),} V_{CC} = 3.3 V$ $T_A = -40^{\circ}C \text{ to } +125^{\circ}C$			±1.0	% FS
f _{BW}	Bandwidth ⁽¹⁾	Small Signal = -3 dB		1.0		MHz
e _N	Noise ⁽¹⁾	T _A = +25°C, f _{BW} = 100 kHz		10.0		mA _{RMS}
Lifetime D	rift					
ETOT_DRIFT	Total Output Error Lifetime Drift ⁽¹⁾	IP = IP(MAX)		±1.0		% FS

(1) Guaranteed by design and characterization; not tested in production.

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Electrical Characteristics for CT431-xSWF20MR



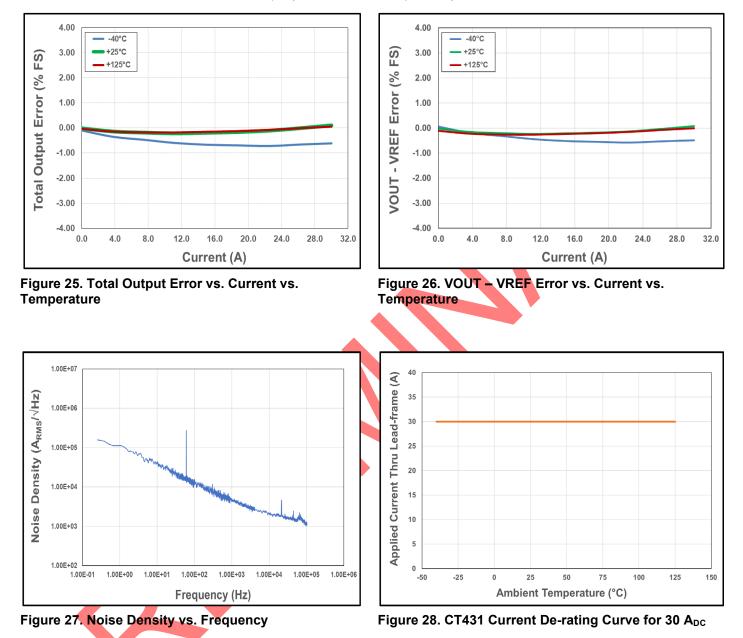
CT431-xSWF30DR: 0 A to +30 A

Unless otherwise specified: V_{CC} = 3.0 V to 3.6 V, T_A = -40°C to +125°C, C_{BYP} = 1.0 μ F. Typical values are V_{CC} = 3.3 V and T_A = +25°C.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
IRANGE	Current Range		0		+30	А
Voq	Voltage Output Quiescent	T _A = +25°C, I _P = 0 A	0.645	0.650	0.655	V
Vout - V _{REF}	OUT – VREF Offset Voltage	V _{CC} = 3.3 V T _A = -40°C to +125°C		5.0		mV
S	Sensitivity	$I_{RANGE(MIN)} < I_P < I_{RANGE(MAX)}$		66.7		mV/A
Еоит	Total Output Error	$I_P = I_{P(MAX)}$		±0.7	±1.0	% FS
ELIN	Non-Linearity Error	I _P = 0 A to +30 A		±0.3	±0.5	% FS
EOUT-VREF	VOUT – VREF Error	$I_P = I_{P(MAX),} V_{CC} = 3.3 V$ $T_A = -40^{\circ}C \text{ to } +125^{\circ}C$			±1.0	% FS
f _{BW}	Bandwidth ⁽¹⁾	Small Signal = -3 dB C _{FILTER} = 5 pF		1.0		MHz
e _N	Noise ⁽¹⁾	T _A = +25°C, f _{BW} = 100 kHz		10.0		mA _{RMS}
Lifetime D	rift					
ETOT_DRIFT	Total Output Error Lifetime Drift ⁽¹⁾	$I_P = I_{P(MAX)}$		±1.0		% FS

(1) Guaranteed by design and characterization; not tested in production.

Electrical Characteristics for CT431-xSWF30DR



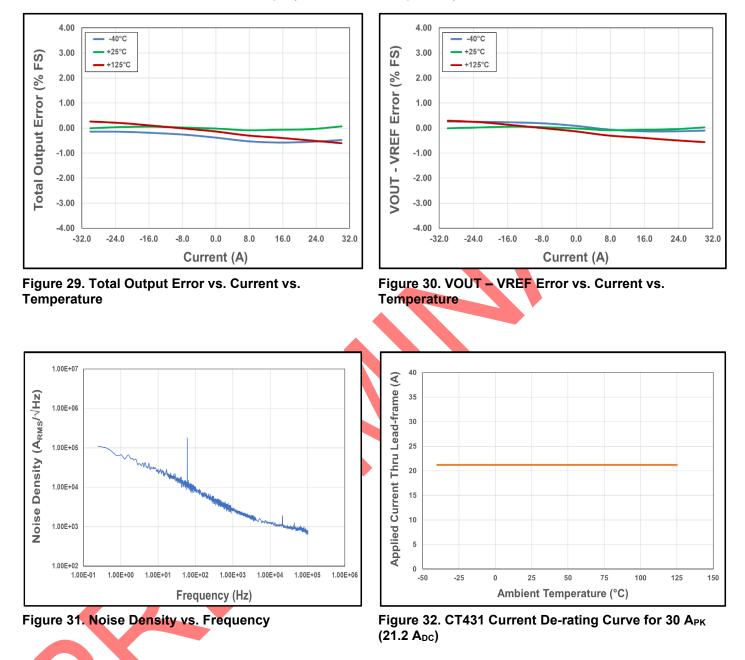
CT431-xSWF30MR: -30 A to +30 A

Unless otherwise specified: V_{CC} = 3.0 V to 3.6 V, T_A = -40°C to +125°C, C_{BYP} = 1.0 μ F. Typical values are V_{CC} = 3.3 V and T_A = +25°C.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
RANGE	Current Range		-30		+30	А
Voq	Voltage Output Quiescent	T _A = +25°C, I _P = 0 A	1.645	1.650	1.655	V
Vout - Vref	OUT – VREF Offset Voltage	V _{CC} = 3.3 V T _A = -40°C to +125°C		5.0		mV
S	Sensitivity	$I_{RANGE(MIN)} < I_P < I_{RANGE(MAX)}$		33.3		mV/A
Eout	Total Output Error	$I_P = I_{P(MAX)}$		±0.5	±1.0	% FS
ELIN	Non-Linearity Error	I _P = -30 A to +30 A		±0.3	±0.5	% FS
EOUT-VREF	VOUT – VREF Error	$I_P = I_{P(MAX),} V_{CC} = 3.3 V$ $T_A = -40^{\circ}C \text{ to } +125^{\circ}C$			±1.0	% FS
f _{BW}	Bandwidth ⁽¹⁾	Small Signal = -3 dB C _{FILTER} = 5 pF		1.0		MHz
e _N	Noise ⁽¹⁾	T _A = +25°C, f _{BW} = 100 kHz		11.5		mA _{RMS}
Lifetime D	rift					
ETOT_DRIFT	Total Output Error Lifetime Drift ⁽¹⁾	$I_P = I_{P(MAX)}$		±1.0		% FS

(1) Guaranteed by design and characterization; not tested in production.

Electrical Characteristics for CT431-xSWF30MR



CT431-xSWF50DR: 0 A to +50 A

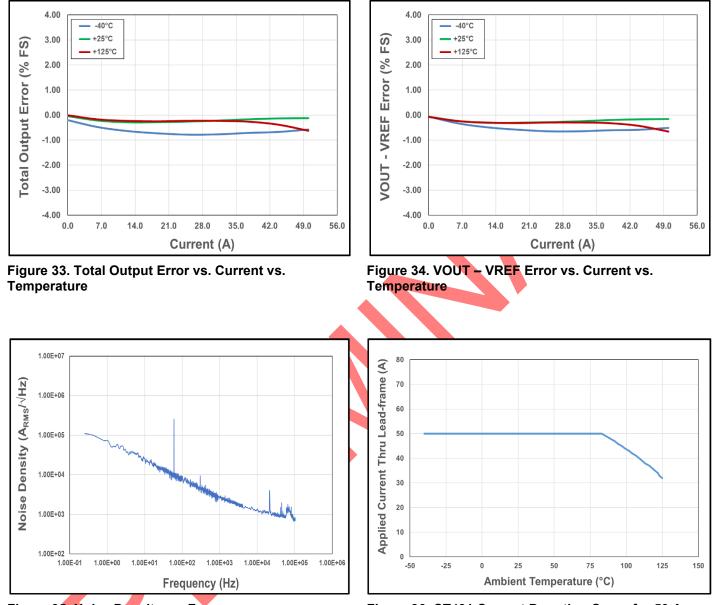
Unless otherwise specified: V_{CC} = 3.0 V to 3.6 V, T_A = -40°C to +125°C, C_{BYP} = 1.0 μ F. Typical values are V_{CC} = 3.3 V and T_A = +25°C.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
RANGE	Current Range		0		+50	А
Voq	Voltage Output Quiescent	T _A = +25°C, I _P = 0 A	0.645	0.650	0.655	V
Vout - Vref	OUT – VREF Offset Voltage	V _{CC} = 3.3 V T _A = -40°C to +125°C		5.0		mV
S	Sensitivity	$I_{RANGE(MIN)} < I_P < I_{RANGE(MAX)}$		40		mV/A
Еоит	Total Output Error	$I_{P} = I_{P(MAX)}$		±1.0	±1.5	% FS
ELIN	Non-Linearity Error	I _P = 0 A to +50 A		±0.3	±0.5	% FS
EOUT-VREF	VOUT – VREF Error	$I_P = I_{P(MAX),} V_{CC} = 3.3 V$ $T_A = -40^{\circ}C \text{ to } +125^{\circ}C$			±1.0	% FS
f _{BW}	Bandwidth ⁽¹⁾	Small Signal = -3 dB		1.0		MHz
e _N	Noise ⁽¹⁾	T _A = +25°C, f _{BW} = 100 kHz		10.0		mA _{RMS}
Lifetime D	rift					
ETOT_DRIFT	Total Output Error Lifetime Drift ⁽¹⁾	$I_P = I_{P(MAX)}$		±1.0		% FS

(1) Guaranteed by design and characterization; not tested in production.

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Electrical Characteristics for CT431-xSWF50DR







CT431-xSWF50MR: -50 A to +50 A

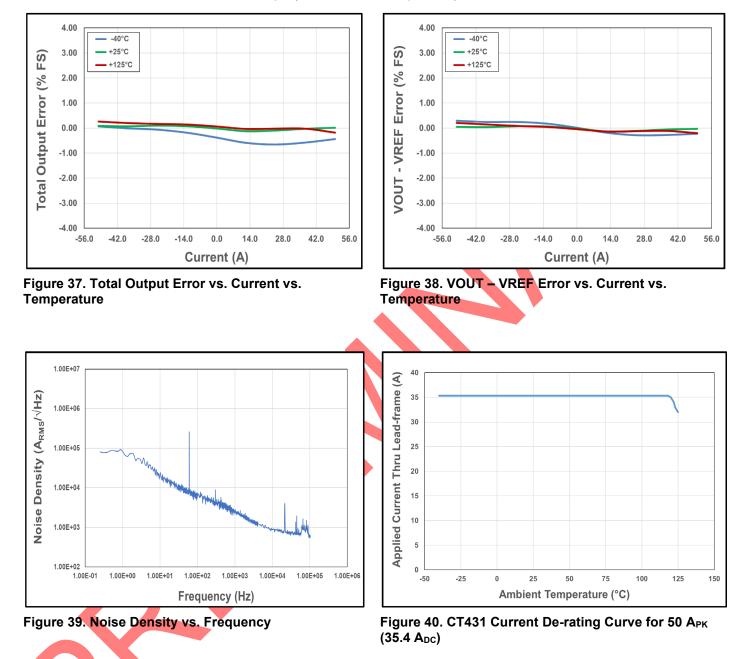
Unless otherwise specified: V_{CC} = 3.0 V to 3.6 V, T_A = -40°C to +125°C, C_{BYP} = 1.0 µF. Typical values are V_{CC} = 3.3 V and T_A = +25°C.

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
	Current Range		-50		+50	А
Voq	Voltage Output Quiescent	T _A = +25°C, I _P = 0 A	1.645	1.650	1.655	V
Vout - Vref	OUT – VREF Offset Voltage	V _{CC} = 3.3 V T _A = -40°C to +125°C		5.0		mV
S	Sensitivity	$ _{RANGE(MIN)} < _{P} < _{RANGE(MAX)}$		20		mV/A
Еоит	Total Output Error	$I_P = I_{P(MAX)}$		±0.5	±1.0	% FS
ELIN	Non-Linearity Error	I _P = -50 A to +50 A		±0.3	±0.5	% FS
EOUT-VREF	VOUT – VREF Error	$I_P = I_{P(MAX),} V_{CC} = 3.3 V$ $T_A = -40^{\circ}C \text{ to } +125^{\circ}C$			±1.0	% FS
f _{BW}	Bandwidth ⁽¹⁾	Small Signal = -3 dB		1.0		MHz
e _N	Noise ⁽¹⁾	T _A = +25°C, f _{BW} = 100 kHz		14.0		mA RMS
Lifetime Drift						
ETOT_DRIFT	Total Output Error Lifetime Drift ⁽¹⁾	$I_P = I_{P(MAX)}$		±1.0		% FS

(1) Guaranteed by design and characterization; not tested in production.

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Electrical Characteristics for CT431-xSWF50MR



Circuit Description

Overview

The CT431 is a very high accuracy contact current sensor with an integrated current carrying conductor (CCC) that handles up to 50 A. It has very high sensitivity and a wide dynamic range with excellent accuracy (very low total output error) across temperature. This current sensor supports six (6) current ranges:

- 0 A to +20A
- -20 A to +20 A
- 0 A to +30 A
- -30 A to +30 A
- 0 A to +50 A
- -50 A to +50 A

When current is flowing through the CCC, the XtemeSense TMR sensors inside the chip senses the field which in turn generates differential voltage signals that then goes through the Analog Front-End (AFE) to output a current measurement with less than $\pm 1.0\%$ full-scale (FS) total output error (E_{OUT}).

The chip is designed to enable a very fast response time of 0.30 μ s for the current measurement from the OUT pin as the bandwidth for the CT431 is 1.0 MHz. Even with a high bandwidth, the chip consumes a minimal amount of power.

Linear Output Current Measurement

The CT431 provides a continuous linear analog output voltage which represents the current measurement. The output voltage range of OUT is from 0.65 V to 2.65 V with a V_{OQ} of 0.65 V and 1.65 V for unidirectional and bidirectional currents, respectively. Figure 41 illustrates the output voltage range of the OUT pin as a function of the measured current.

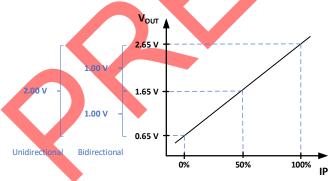


Figure 41. Linear Output Voltage Range (OUT) vs. Measured Current (IP)

Filter Function (FILTER)

The CT431 has a pin for the FILTER function which will enable it to improve the noise performance by changing the cut-off frequency. The bandwidth of the CT431 is 1.0 MHz however by adding a capacitor to the FILTER pin which will be in series with an internal resistance of approximately 15 k Ω will set the cut-off frequency to reduce the noise.

Table 2 shows the capacitor values required to achieve four (4) cut-off frequencies.

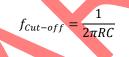


Table 2. R-C Filter Options for FILTER Pin

Cut-off Frequency	C _{FILTER} (pF)	Capacitor Part Number
100 kHz	47	GRM0225C1C470JA02
250 kHz	20	GRM0225C1C200JA02
500 kHz	10	GRM0225C1C100JA03
1.0 MHz	5 or lower	GRM0225C1C5R0CA03

Voltage Reference Function (VREF)

The CT431 has a reference voltage (VREF) pin that may be used as an output voltage reference for AC or DC current measurements. The VREF pin should be connected to a buffer circuit.

If the VREF is not used, then it should be left unconnected.

Sensitivity

The Sensitivity (S) is a change in CT431's output in response to a change in 1 A of current flowing through the CCC. It is defined by the product of the magnetic circuit sensitivity (G/A, where 1.0 G = 0.1 mT) and the chip's linear amplifier gain (mV/G). Therefore, the result of this gives a sensitivity unit of mV/A. The CT431 is factory calibrated to optimize the sensitivity for the full scale of the device's dynamic range.

Total Output Error

The Total Output Error is the difference between the current measured by CT431 and the actual current, relative to the actual current. It is equivalent to the ratio between the difference of the ideal and actual voltage to the ideal sensitivity multiplied by the current flowing through the primary conductor (CCC). The following

equation defines the Total Output Error (E_{OUT}) for the CT431:

$$E_{OUT} = \frac{V_{IOUT_IDEAL}(I_P) - V_{IOUT}(I_P)}{S_{IDEAL}(I_P) \times I_P}$$

The E_{OUT} incorporates all sources of error and is a function of the sensed current (I_P) from CT431. At high current levels, the E_{OUT} will be dominated by the sensitivity error whereas at low current, the dominant characteristic is the offset voltage. Figure 42 shows the behavior of E_{OUT} versus I_P. When I_P goes to 0 from both directions, the curves exhibit asymptotic behavior i.e. E_{OUT} approaches infinity.

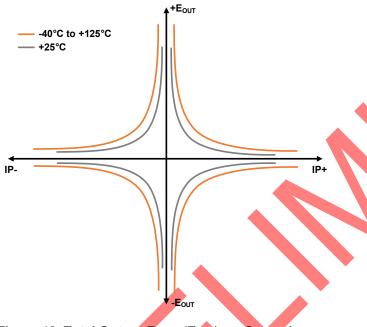


Figure 42. Total Output Error (Eout) vs. Sensed Current (IP)

The CT431 achieves a total output error (E_{OUT}) that is less than ±1.0% of Full-Scale (FS) over supply voltage and temperature. It is designed with innovative and proprietary TMR sensors and circuit blocks to provide very accurate current measurements regardless of the operating conditions.

Power-On Time (ton)

The Power-On Time (t_{ON}) of 100 µs is the amount of time required by CT431 to start up, fully power the chip and becoming fully operational from the moment the supply voltage is applied to it. This time includes the ramp up time and the settling time (within 10% of steady-state voltage) after the power supply has reached the minimum V_{cc}.

Response Time (tresponse)

The Response Time ($t_{RESPONSE}$) of 0.30 µs for the CT431 is the time interval between the following terms:

- 1. When the primary current signal reaches 90% of its final value,
- 2. When the chip reaches 90% of its output corresponding to the applied current.

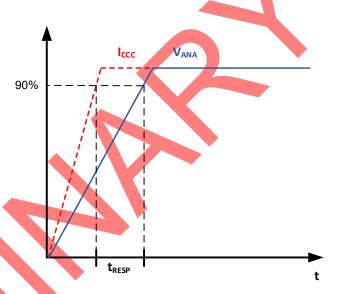


Figure 43. CT431 Response Time Curve

Rise Time (trise)

The CT431's rise time, t_{RISE} , is the time interval of when it reaches 10% and 90% of the full-scale output voltage. The t_{RISE} of the CT431 is 0.20 µs.

Propagation Delay (tDELAY)

The Propagation Delay (t_{DELAY}) is the time difference between these two events:

- 1. When the primary current reaches 20% of its final value
- 2. When the chip reaches 20% of its output corresponding to the applied current.

The CT431 has a propagation delay of 0.20 $\mu s.$

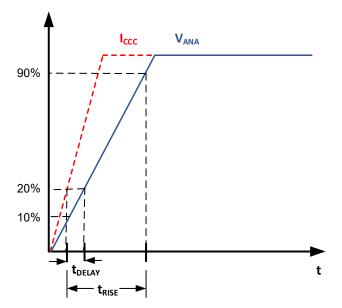


Figure 44. CT431 Propagation Delay and Rise Time Curve

Over-Current Detection (OCD)

The Over-Current Detection (OCD) circuitry detects measured current values that are 110% above the maximum current range value of the CT431 for the unipolar (DC current) variant. For the bipolar (AC current) variant of the CT431 it is greater than \pm 110% of the maximum current range. This will generate a fault signal via the Fault# Interrupt (FLT) pin (LOW) to the host system's microcontroller. Once the measured current falls to 90% of the maximum current range for the DC current variant or \pm 90% for the AC current version then the fault will be cleared, and the FLT pin will go HIGH.

Under-Voltage Lockout (UVLO)

The Under-Voltage Lock-out protection circuitry of the CT431 is activated when the supply voltage (V_{CC}) falls below 2.45 V. The CT431 remains in a low quiescent state until V_{CC} rises above the UVLO threshold (2.50 V). In this condition where the V_{CC} is less than 2.45 V and UVLO is triggered, the output from the CT431 is not valid and the FLT pin will go LOW. Once the V_{CC} rises above 2.50 V then the UVLO is cleared, and the FLT pin will be HIGH.

Fault# Interrupt (FLT)

The CT431 generates an active LOW digital fault signal via the FLT pin to interrupt the microcontroller to indicate a fault event has been triggered. It is an open drain output and requires a pull-up resistor with a value of 100 k Ω tied to V_{cc}. A fault signal will interrupt the host system for these events:

- OCD
- UVLO

The FLT signal will be asserted LOW whenever one of the above fault events occur. In the case of an UVLO event, the FLT pin will stay LOW until the fault is cleared and then go HIGH.

If the FLT is not used, then it should be left unconnected.

Immunity to Common Mode Fields

The CT431 is housed in custom plastic packages that utilize a "U-shaped" lead-frame to reduce the common mode fields generated as current flows through the CCC. With the "U-shaped" lead-frame, the stray fields cancel one another thus reducing electro-magnetic interference (EMI).

Also, good PCB layout of the CT431 will optimize performance and reduce EMI. Please see the Applications Information section in this data sheet for recommendations on PCB layout.

Creepage and Clearance

Two important terms as it relates to isolation provided by the package are: creepage and clearance. Creepage is defined as the shortest distance across the surface of the package from one side the leads to the other side of the leads. The definition for clearance is the shortest distance between the leads of opposite side through the air. Figure 45 illustrates the creepage and clearance for the SOICW-16 package of the CT431.



Figure 45. The Creepage and Clearance for the CT431's SOICW-16 package

Applications Information

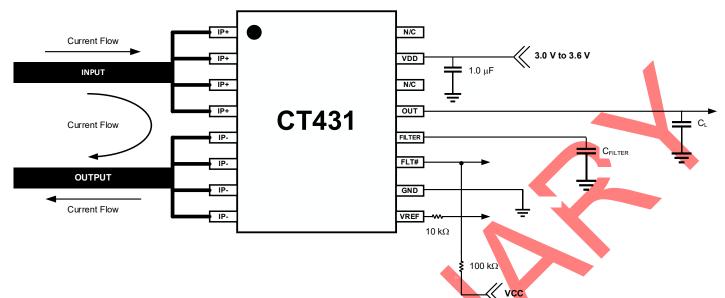


Figure 46. CT431 Application Block Diagram

Application

The CT431 is an integrated contact current sensor that can be used in many applications from measuring current in power supplies to motor control to over-current fault protection. It is a plug-and-play solution in that no calibration is required and it outputs to a microcontroller a simple linear analog output voltage which corresponds to a current measurement value. A second output called FLT# alerts the host system to any fault event that may occur in the CT431. Figure 46 is an application diagram of how CT431 would be implemented in a system. The third output is the VREF which provides the output reference voltage of the CT431.

It is designed to support an operating voltage range of 4.75 V to 5.50 V, but it is ideal to use a 3.3 V power supply where the output tolerance is less than $\pm 5\%$.

Bypass Capacitor

A single 1.0 μ F capacitor is needed for the VCC pin to reduce the noise from the power supply and other circuits. This capacitor should be placed as close as possible to the CT431 to minimize inductance and resistance between the two devices.

Filter Capacitor

A capacitor may be added to the FILTER pin of the CT431 if there is a requirement to improve the noise

performance. The capacitor will be connected to an internal resistor of 15 k Ω inside the chip to form a R-C filter. This R-C filter produces a cut-off frequency that will reduce the noise over this lower bandwidth.

FLT and VREF Resistors

For the CT431, the FLT# pin is an open drain output. It requires a pull-up resistor value of 100 k Ω to be connected from the pin to V_{CC}.

In designs where the VREF pin is used, a 10 k Ω resistor must be connected as close to the pin as possible in series with a load.

If the FLT# and/or VREF pins are not needed in the application, then these pins should not be connected and be left floating.

Recommended PCB Layout

Since the CT431 can measure up to 50 A of current, special care must be taken in the printed circuit board (PCB) layout of the CT431 and the surrounding circuitry. It is recommended that the CCC pins be connected to as much copper area as possible. It is also recommended that 2 oz. or heavier copper be used for PCB traces when the CT431 is used to measure 50 A of current. Additional layers of the PCB should also be used to carry current and be connected using the arrangement of vias.

CT431

Figure 47 shows the recommended the PCB layout for the 20 A and 30 A variants of CT431 while Figure 48 illustrates the 50 A variant. Please note that the traces connected to the IP+ and IP- pins of CT431 are very wide with multiple vias such that it can handle the high current.

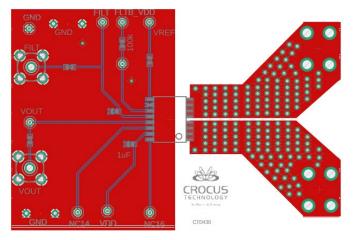


Figure 47. Recommended PCB Layout for the 20 A and 30 A variants of the CT431.

The PCB layout for the 50 A versions of the CT430 shows even wider traces in the below figure.

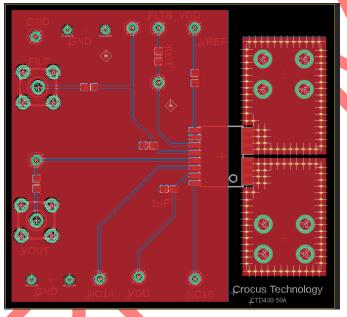
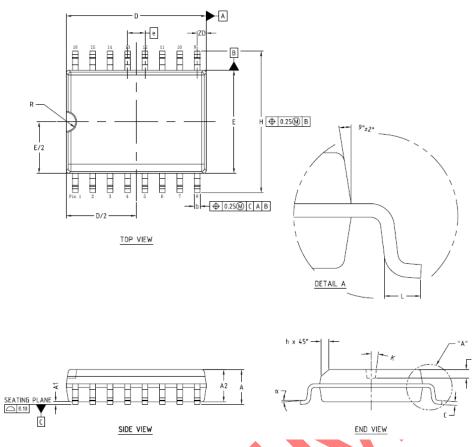


Figure 48. Recommended PCB Layout for the 50 A variant of the CT431.

SOICW-16 Package Drawing and Dimensions





1. ALL DIMENSIONS IN MM.

- 2. PACKAGE SURFACE FINISHING: 2.1. TOP : MATTE (CHARMILLES #18~30) 2.2. BOTTOM : MATTE (CHARMILLES #12~27)
- 3. LEAD COPLANARITY SHOULD BE OT 0.10M MAX. 4. ALL DIMENSIONS EXCLUDING MOLD FLASHES AND END FLASH FROM THE PACKAGE BODY SHALL NOT EXCEED 0.25MM PER SIDE (D)

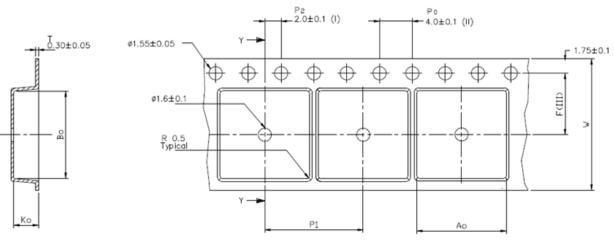
Figure 49. SOICW-16 Package Drawing

Table 3. CT431 SOICW-16 Package Dimensions

Symbol	Dime	Dimensions in Millimeters (mm)						
Symbol	Min.	Тур.	Max.					
А	2.44	2.54	2.64					
A1	0.10	0.20	0.30					
A2	2.24	2.34	2.44					
b	0.36	0.41	0.46					
С	0.24	0.25	0.26					
D	10.11	10.21	10.31					
E	7.40	7.50	7.60					
е		1.27 BSC						
Н	10.11	10.31	10.51					
h	0.31	0.51	0.71					
J	0.53	0.63	0.73					
K		7° BSC						
	0.51	0.76	1.01					
R	0.63	0.76	0.89					
ZD		0.66 REF						
α	0 °	-	8°					

Crocus Technology provides package drawings as a service to customers considering or planning to use Crocus products in their designs. Drawings may change without notice. Please note the revision and date of the data sheet and contact a Crocus Technology representative to verify or obtain the most recent version. The package specifications do not expand the terms of Crocus Technology's worldwide terms and conditions, specifically the warranty therein, which covers Crocus Technology's products.

SOICW-16 Tape & Pocket Drawing and Dimensions



SECTION Y-Y

ç

Ao	10.90 +/- 0.1
Bo	10.70 +/- 0.1
Ko	3.00 +/- 0.1
F	7.50 +/- 0.1
P 1	12.00 +/- 0.1
W	16.00 +/- 0.3

Figure 50. SOICW-16 Package Drawing

- Measured from centreline of sprocket hole (I)
- to centreline of pocket. Cumulative tolerance of 10 sprocket holes is \pm 0.20 . (II)
- (III)
- Measured from centreline of sprocket hole to centreline of pocket. Other material available.
- (IV)
- Typical SR of form tape Max 10⁹ OHM/SQ (V)
- ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.

CT431 Tape Pocket Orientation

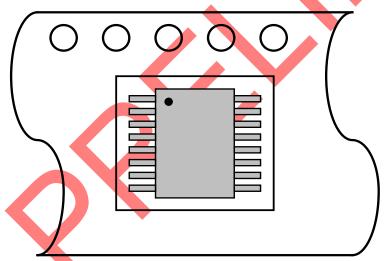


Figure 51. SOICW-16 Orientation in Tape Pocket

Package Information

Table 4. CT431 Package Information

Part Number	Package Type	# of Leads	Package Quantity	Lead Finish	Eco Plan ⁽¹⁾	MSL Rating ⁽²⁾	Operating Temperature ⁽³⁾	Device Marking
CT431-ESWF20DR	SOIC-W	16	1,000	Sn	Green & RoHS	3	-40°C to +85°C	CT431 ESWF20DR
CT431-HSWF20DR	SOIC-W	16	1,000	Sn	Green & RoHS	3	-40°C to +125°C	CT431 HSWF20DR
CT431-ESWF20MR	SOIC-W	16	1,000	Sn	Green & RoHS	3	-40°C to +85°C	CT431 ESWF20MR
CT431-HSWF20MR	SOIC-W	16	1,000	Sn	Green & RoHS	3	-40°C to +125°C	CT431 HSWF20MR
CT431-ESWF30DR	SOIC-W	16	1,000	Sn	Green & RoHS	3	-40°C to +85°C	CT431 ESWF30DR
CT431-HSWF30DR	SOIC-W	16	1,000	Sn	Green & RoHS	3	-40°C to +125°C	CT431 HSWF30DR
CT431-ESWF30MR	SOIC-W	16	1,000	Sn	Green & RoHS	3	-40°C to +85°C	CT431 ESWF30MR
CT431-HSWF30MR	SOIC-W	16	1,000	Sn	Green & RoHS	3	-40°C to +125°C	CT431 HSWF30MR
CT431-ESWF50DR	SOIC-W	16	1,000	Sn	Green & RoHS	3	-40°C to +85°C	CT431 ESWF50DR
CT431-HSWF50DR	SOIC-W	16	1,000	Sn	Green & RoHS	3	-40°C to +125°C	CT431 HSWF50DR
CT431-ESWF50MR	SOIC-W	16	1,000	Sn	Green & RoHS	3	-40°C to +85°C	CT431 ESWF50MR
CT431-HSWF50MR	SOIC-W	16	1,000	Sn	Green & RoHS	3	-40°C to +125°C	CT431 HSWF50MR

(1) RoHS is defined as semiconductor products that are compliant to the current EU RoHS requirements. It also will meet the requirement that RoHS substances do not exceed 0.1% by weight in homogeneous materials. Green is defined as the content of Chlorine (CI), Bromine (Br) and Antimony Trioxide based flame retardants satisfy JS709B low halogen requirements of ≤ 1,000 ppm.

(2) MSL Rating = Moisture Sensitivity Level Rating as defined by JEDEC standard classifications.

(3) Package will withstand ambient temperature range of -40°C to +125°C and storage temperature range of -65°C to +150°C.



CT431

Device Marking

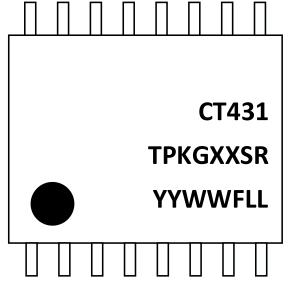


Figure 52. CT431 Device Marking for 16-lead Package

Code	Definition
•	Pin 1 Indicator
CT431	Crocus Part Number
Т	Temperature
PKG	Package Type
XX	Maximum Current Rating
SR	Current Range
YY	Calendar Year
WW	Work Week
F	Factory Code
LL	Lot Code
	CT431 T PKG XX SR YY WW F

Table 5. CT431 Device Marking Definition for 16-leadSOIC-W Package



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Objective	Proposed New Product Idea or In Development	Data sheet contains design target specifications and are subject to change without notice at any time.
Preliminary	First Production	Data sheet contains preliminary specifications obtained by measurements of early samples. Follow-on data will be published at a later date as more test data is acquired. Crocus reserves the right to make changes to the data sheet at any time.
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Obsolete	Not in Production	Data sheet for a product that is no longer in production at Crocus. It is for reference only.

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