

PROGRAMMABLE TIMING CONTROL HUB FOR INTEL BASED SYSTEMS

ICS9LRS3187B

Recommended Application:

CK505 version 1.1 clock, with fully integrated voltage regulators and series resistors

Output Features:

- 2 - CPU differential low power push-pull pairs
- 1 - SRC differential low power push-pull pair
- 1 - SATA differential low power push-pull pair
- 1 - DOT differential low power push-pull pair
- 1 - REF, able to drive 3 loads, 14.318MHz
- 1 - 27MHz_SS/non_SS single-ended output pair

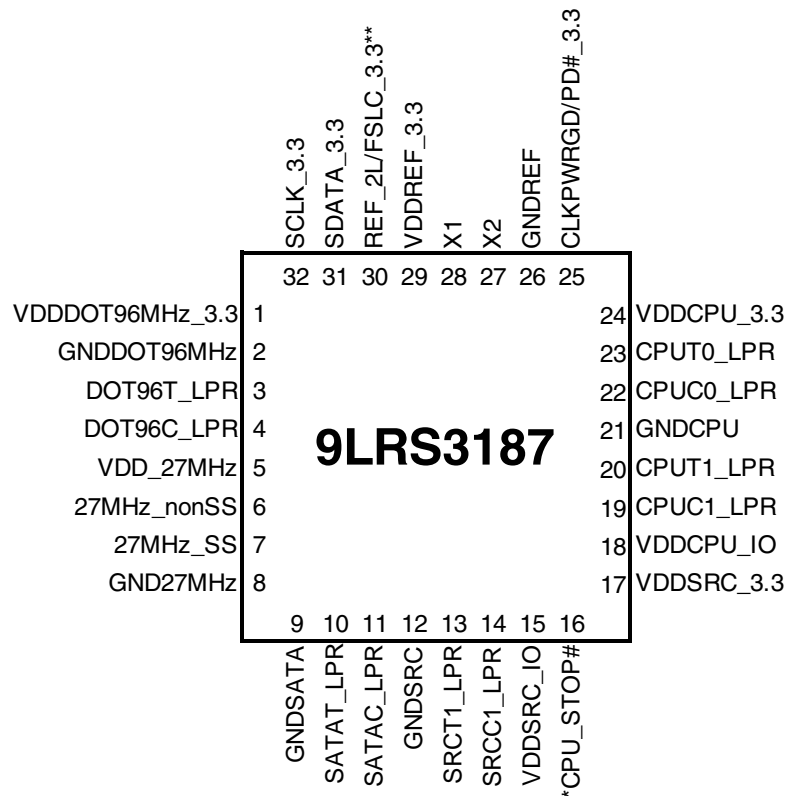
Features/Benefits:

- Supports spread spectrum modulation, 0 to -0.5% down spread for CPU and SRC clocks
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning
- Available in commercial (0 to +70°C) and industrial (-40 to +85°C) temperature ranges
- Meets PCIe Gen2 specifications

Key Specifications:

- CPU outputs cycle-cycle jitter <85ps
- SRC outputs cycle-cycle jitter <125ps
- +/- 100ppm frequency accuracy on all clocks

Pin Configuration



** Internal Pull-Down Resistor

* Internal Pull-Up Resistor

32-pin MLF

Pin Description

Pin#	Pin Name	Type	Pin Description
1	VDDDOT96MHz_3.3	PWR	Power pin for the 96MHz output 3.3V.
2	GNDDOT96MHz	PWR	Ground pin for the 96MHz output
3	DOT96T_LPR	OUT	True DOT96 output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
4	DOT96C_LPR	OUT	Complement DOT96 output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
5	VDD_27MHz	PWR	Power pin for the 27MHz output 3.3V.
6	27MHz_nonSS	OUT	3.3V Single-ended 27MHz non-spread clock.
7	27MHz_SS	OUT	3.3V Single-ended 27MHz spread clock.
8	GND27MHz	OUT	Ground pin for the 27MHz outputs.
9	GNDSATA	PWR	Ground pin for the SATA outputs.
10	SATAT_LPR	OUT	True clock of differential 0.8V push-pull SATA/SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
11	SATAC_LPR	OUT	Complementary clock of differential 0.8V push-pull SATA/SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
12	GNDSRC	PWR	Ground pin for the SRC outputs
13	SRCT1_LPR	OUT	True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
14	SRCC1_LPR	OUT	Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
15	VDDSRC_IO	PWR	1.05V to 3.3V from external power supply
16	*CPU_STOP#	IN	Stops all CPU clocks, except those set to be free running clocks
17	VDDSRC_3.3	PWR	Supply for SRC clocks, 3.3V nominal
18	VDDCPU_IO	PWR	1.05V to 3.3V from external power supply
19	CPUC1_LPR	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
20	CPUT1_LPR	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
21	GNDCPU	PWR	Ground pin for the CPU outputs.
22	CPUC0_LPR	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
23	CPUT0_LPR	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
24	VDDCPU_3.3	PWR	Supply for CPU clocks, 3.3V nominal
25	CLKPWRGD/PD#_3.3	IN	Notifies CK505 to sample latched inputs, or PWRDWN# mode
26	GNDREF	PWR	Ground pin for the REF outputs.
27	X2	OUT	Crystal output, Nominally 14.318MHz
28	X1	IN	Crystal input, Nominally 14.318MHz
29	VDDREF_3.3	PWR	Power pin for the XTAL and REF clocks, nominal 3.3V
30	REF_2/FSLC_3.3**	I/O	14.318 MHz reference clock, which can drive 2 loads / 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for V_{il_FS} and V_{ih_FS} values.
31	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant
32	SCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.

General Description

The **ICS9LRS3187B** is a CK505 clock synthesizer. The **ICS9LRS3187B** provides a single-chip solution for Intel based systems. The **ICS9LRS3187B** is driven with a 14.318MHz crystal.

Functional Block Diagram

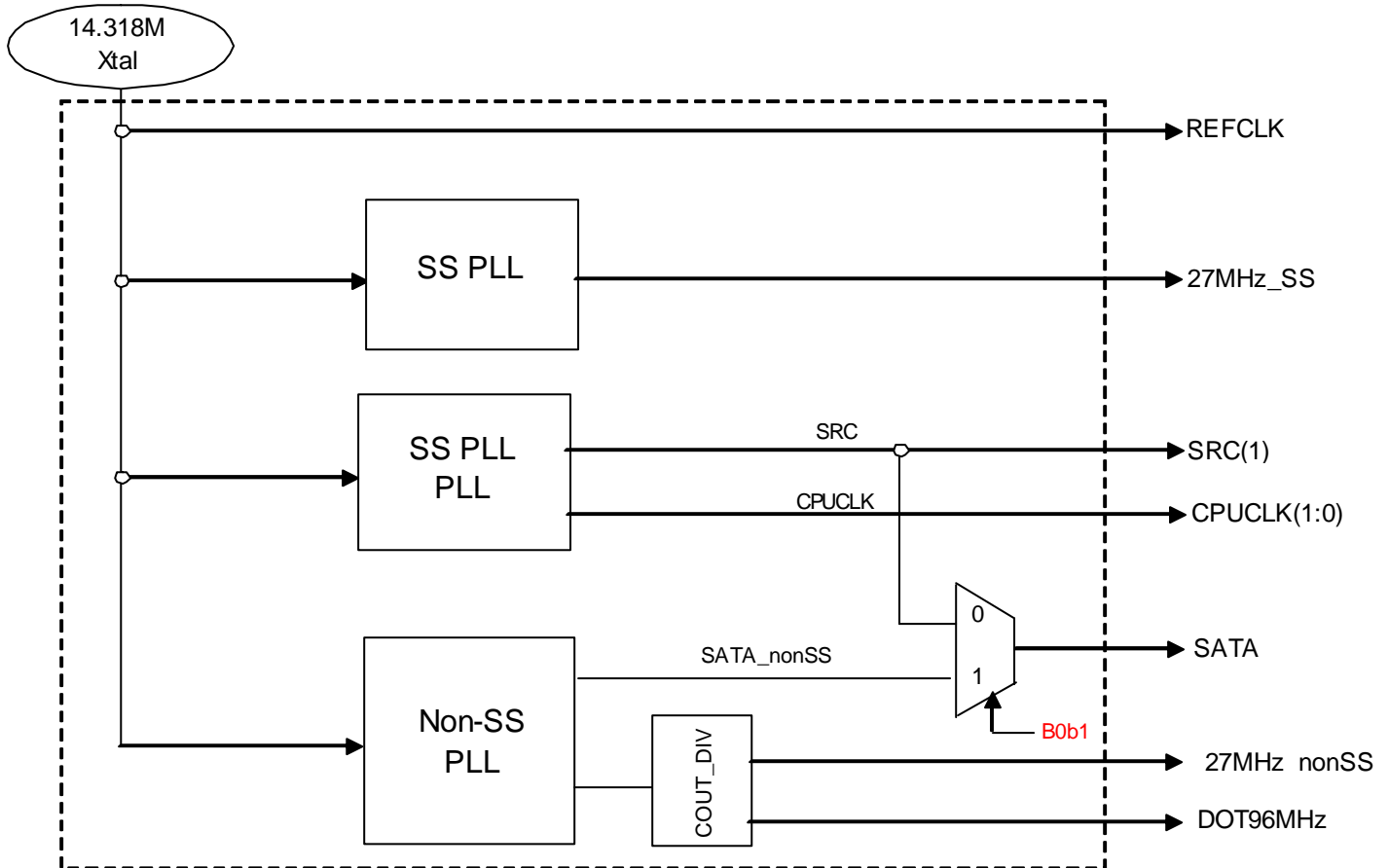


Table: Power Distribution

Ground	VDD_IO	VDD 3.3V	Output
2		1	DOT96
8		5	27M
9	15	17	SATA
12	15	17	SRC
21	18	24	CPU
26		29	REF

Table 1: CPU Frequency Select Table

FS _L C B0b7	CPU MHz	SRC MHz	REF MHz	DOT MHz
0 (Default)	133.33	100.00	14.318	96.00
1	100.00			

1. FS_LC is a low-threshold input. Please see V_{IL,FS} and V_{IH,FS} specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.

Table 2: pin 6, 7 Configuration

B1b3	B1b2	B1b1	Pin 6	Pin 7	Spread	Comment
			MHz	MHz	%	
0	0	0	27MHz_nonSS	27MHz_SS	-1.75%	
0	0	1	27MHz_nonSS	27MHz_SS	+0.5%	
0	1	0	27MHz_nonSS	27MHz_SS	-0.5%	Default
0	1	1	27MHz_nonSS	27MHz_SS	-1%	
1	0	0	27MHz_nonSS	27MHz_SS	-1.5%	
1	0	1	27MHz_nonSS	27MHz_SS	-2%	
1	1	0	27MHz_nonSS	27MHz_SS	-0.75%	
1	1	1	27MHz_nonSS	27MHz_SS	-1.25%	

Table 3: IO_Vout select table

B9b2	B9b1	B9b0	IO_Vout
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V
1	1	0	0.9V
1	1	1	1.0V

CPU Power Management Table

PD#	CPU_STOP#	SMBus Reg. OE	CPU1	CPU1#	CPU0	CPU0#
1	1	Enable	Running	Running	Running	Running
0	X	Enable	Low/20K	Low	Low/20K	Low
1	0	Enable	High	Low	High	Low
1	X	Disable	Low/20K	Low	Low/20K	Low
M1			Running	Running	Low/20K	Low

SRC and DOT96MHz Power Management Table

PD#	CPU_STOP#	SMBus Reg. OE	SRC	SRC#	DOT	DOT#
0	X	Enable	Low/20K	Low	Low/20K	Low
1	X	Enable	Running	Running	Running	Running
1	X	Disable	Low/20K	Low	Low/20K	Low
M1			Low/20K	Low	Low/20K	Low

Singled-ended Power Management Table

PD#	CPU_STOP#	SMBus Reg. OE	27M	REF
1	X	Enable	Running	Running
0	X	Enable	Low	Hi-Z
1	X	Disable	Low	Low
M1			Low	Hi-Z

General SMBus serial interface information for the ICS9LRS3187B

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the data byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D2_{(H)}$
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D3_{(H)}$
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends **Byte N + X - 1**
- IDT clock sends **Byte 0 through byte X (if $X_{(H)}$ was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation		
Controller (Host)		IDT (Slave/Receiver)
T	starT bit	
Slave Address $D2_{(H)}$		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N	X Byte	
◊		ACK
◊		◊
◊		◊
◊		◊
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation		
Controller (Host)		IDT (Slave/Receiver)
T	starT bit	
Slave Address $D2_{(H)}$		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
RT	Repeat starT	
Slave Address $D3_{(H)}$		
RD	ReaD	
		ACK
		Data Byte Count = X
ACK		
		Beginning Byte N
ACK		
◊		◊
◊		◊
◊		◊
		Byte N + X - 1
N	Not acknowledge	
P	stoP bit	

Byte 0 FS Readback and PLL Selection Register

Bit	Pin	Name	Description	Type	0	1	Default
7	-	FSLC	CPU Freq. Sel. Bit	R			Latch
6	-	Reserved	Reserved	RW	-	-	0
5	-	Reserved	Reserved	RW	-	-	1
4	-	iAMT_EN	Set via SMBus	RW (Sticky "1")	Legacy Mode	iAMT Enabled	0
3		Reserved	Reserved	RW			0
2	-	Reserved	Reserved	RW			0
1	-	SATA_SEL	Select source for SATA clock	RW	SATA (SRC2 100MHz_SS) = SRC_Main	SATA (100MHz non_SS) = SATA PLL	0
0	-	PD_Restore	1 = on Power Down de-assert return to last known state 0 = clear all SMBus configurations as if cold power-on and go to latches open state This bit is ignored and treated at '1' if device is in iAMT mode.	RW	Configuration Not Saved	Configuration Saved	1

Byte 1 DOT96 Select and PLL3 Quick Config Register,

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW	-	-	1
6		SRC_PLL_SSC_SEL	Select 0.5% down or center SSC	RW	Down spread	Center spread	0
5		Reserved	Reserved	RW	-	-	1
4		Reserved	Reserved	RW			0
3		27SS PLL CF2	27SS PLL Quick Config Bit 2	RW	See Table 2: pin 6/7 Configuration		0
2		27SS PLL CF1	27SS PLL Quick Config Bit 1	RW		1	
1		27SS PLL CF0	27SS PLL Quick Config Bit 0	RW		0	
0		Reserved	Reserved	RW	-	-	1

Byte 2 Output Enable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		REF_3L_OE	Output enable for REF0, if disabled output is tri-stated	RW	Output Disabled	Output Enabled	1
6		Reserved	Reserved	RW	-	-	1
5		Reserved	Reserved	RW	-	-	1
4		Reserved	Reserved	RW	-	-	1
3		Reserved	Reserved	RW	-	-	1
2		Reserved	Reserved	RW	-	-	1
1		Reserved	Reserved	RW	-	-	1
0		Reserved	Reserved	RW	-	-	1

Byte 3 Output Enable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW	-	-	1
6		Reserved	Reserved	RW	-	-	1
5		Reserved	Reserved	RW	-	-	1
4		Reserved	Reserved	RW	-	-	1
3		Reserved	Reserved	RW	-	-	1
2		Reserved	Reserved	RW	-	-	1
1		Reserved	Reserved	RW	-	-	1
0		Reserved	Reserved	RW	-	-	1

Byte 4 Output Enable and Spread Spectrum Disable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW	-	-	1
6		SATA_OE	Output enable for SATA	RW	Output Disabled	Output Enabled	1
5		SRC1_OE	Output enable for SRC1	RW	Output Disabled	Output Enabled	1
4		DOT96_OE	Output enable for DOT96	RW	Output Disabled	Output Enabled	1
3		CPU1_OE	Output enable for CPU1	RW	Output Disabled	Output Enabled	1
2		CPU0_OE	Output enable for CPU0	RW	Output Disabled	Output Enabled	1
1		27SS_ON	Enable 27SS's spread modulation	RW	Spread Disabled	Spread Enabled	1
0		SRC_SSC_ON	Enable SRC's spread modulation	RW	Spread Disabled	Spread Enabled	1

Byte 5 Reserved Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW	-	-	1
6		Reserved	Reserved	RW	-	-	1
5		Reserved	Reserved	RW	-	-	1
4		Reserved	Reserved	RW	-	-	1
3		Reserved	Reserved	RW	-	-	1
2		Reserved	Reserved	RW	-	-	1
1		Reserved	Reserved	RW	-	-	1
0		Reserved	Reserved	RW	-	-	1

Byte 6 Slew Rate Control Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW	-	-	0
6		Reserved	Reserved	RW	-	-	0
5		REF Slew	Slew Rate Control	RW	2 V/ns	1 V/ns	0
4		Reserved	Reserved	RW	-	-	0
3		27MHz Slew	Slew Rate Control	RW	2 V/ns	1 V/ns	0
2		Reserved	Reserved	RW	-	-	0
1		Reserved	Reserved	RW	-	-	0
0		Reserved	Reserved	RW	-	-	0

Byte 7 Vendor ID/ Revision ID

Bit	Pin	Name	Description	Type	0	1	Default
7		Rev Code Bit 3	Revision ID	R	Vendor specific		X
6		Rev Code Bit 2		R			X
5		Rev Code Bit 1		R			X
4		Rev Code Bit 0		R			X
3		Vendor ID bit 3	Vendor ID ICS is 0001, binary	R			0
2		Vendor ID bit 2		R			0
1		Vendor ID bit 1		R			0
0		Vendor ID bit 0		R	1		

Byte 8 Device ID and Output Enable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Device_ID3	Table of Device identifier codes, used for differentiating between CK505 package options, etc.	R	See Device ID Table		1
6		Device_ID2		R			0
5		Device_ID1		R			0
4		Device_ID0		R			0
3		Reserved	Reserved	RW	-	-	0
2		Reserved	Reserved	RW	-	-	0
1		27MHz_nonSS_OE	Output enable for 27MHz_nonSS	RW	Disabled	Enabled	1
0		27MHz_SS_OE	Output enable for 27MHz_SS	RW	Disabled	Enabled	1

Byte 9 Output Control Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW	-	-	0
6		Reserved	Reserved	R	-	-	0
5		Reserved	Reserved	RW	-	-	1
4		Reserved	Reserved	RW	-	-	0
3		Reserved	Reserved	RW	-	-	0
2		IO_VOUT2	IO Output Voltage Select (Most Significant Bit)	RW	See Table 3: V_IO Selection (Default is 0.8V)		1
1		IO_VOUT1	IO Output Voltage Select	RW			0
0		IO_VOUT0	IO Output Voltage Select (Least Significant Bit)	RW			1

Byte 10 Output Control Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW	-	-	0
6		Reserved	Reserved	RW	-	-	0
5		Reserved	Reserved	RW	-	-	0
4		Reserved	Reserved	RW	-	-	0
3		Reserved	Reserved	RW	-	-	0
2		Reserved	Reserved	RW	-	-	0
1		CPU 1 Stop Enable	Enables control of CPU1 with CPU_STOP#	RW	Free Running	Stoppable	1
0		CPU 0 Stop Enable	Enables control of CPU 0 with CPU_STOP#	RW	Free Running	Stoppable	1

Byte 11 Reserved Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW			0
6		Reserved	Reserved	RW			0
5		Reserved	Reserved	RW			0
4		Reserved	Reserved	RW			0
3		Reserved	Reserved	RW	-	-	0
2		CPU1_AMT_EN	M1 mode clk enable	RW	Disable	Enable	1
1		PCI-E_GEN2	Determines if PCI-E Gen2 compliant	R	non-Gen2	PCI-E Gen2 Compliant	1
0		Reserved	Reserved	RW	-	-	1

Byte 12 Byte Count Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved		RW			0
6		Reserved		RW			0
5		BC5	Read Back byte count register, max bytes = 32	RW			0
4		BC4		RW			0
3		BC3		RW			1
2		BC2		RW			1
1		BC1		RW			0
0		BC0		RW			1

Absolute Maximum Ratings - DC Parameters, Commercial Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Maximum Supply Voltage	VDDxxx	Supply Voltage			4.6	V	1
Maximum Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply			3.8	V	1
Maximum Input Voltage	V _{IH}	3.3V Inputs			4.6	V	1,2
Minimum Input Voltage	V _{IL}	Any Input	GND - 0.5			V	1
Storage Temperature	T _s	-	-65		150	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1,3

Notes: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

¹ Operation under these conditions is neither implied, nor guaranteed.

² Maximum V_{IH} is not to exceed VDD

³ Human Body Model

Electrical Characteristics - Input/Supply/Common Output DC Parameters, Commercial Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Ambient Operating Temp	T _{ambient}	-	0		70	°C	
Supply Voltage	VDDxxx	Supply Voltage	3.135		3.465	V	
Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply	0.9975		3.465	V	5
Input High Voltage	V _{IHSE}	Single-ended 3.3V inputs	2		V _{DD} + 0.3	V	3
Input Low Voltage	V _{ILSE}	Single-ended 3.3V inputs	V _{SS} - 0.3		0.8	V	3
Low Threshold Input- FSC = '1' Voltage	V _{IH_FSC}	3.3 V +/-5%	0.7		3.3	V	4
Low Threshold Input-Low Voltage	V _{IL_FSC}	3.3 V +/-5%	V _{SS} - 0.3		0.35	V	
Input Leakage Current	I _{IN}	V _{IN} = V _{DD} , V _{IN} = GND	-5		5	uA	2
Input Leakage Current	I _{INRES}	Inputs with pull up or pull down resistors V _{IN} = V _{DD} , V _{IN} = GND	-200		200	uA	
Output High Voltage	V _{OHSE}	Single-ended outputs, I _{OH} = -1mA	2.4			V	1
Output Low Voltage	V _{OLSE}	Single-ended outputs, I _{OL} = 1 mA			0.4	V	1
Operating Supply Current	I _{DDOP3.3}	Full Active, C _L = Full load; I _{DD} 3.3V		85	110	mA	
	I _{DDOPIO}	Full Active, C _L = Full load; I _{DD} IO		18	25	mA	5
iAMT Mode Current	I _{DDIAMT3.3}	M1 mode, 3.3V Rail		48	60	mA	
	I _{DDIAMTIO}	M1 Mode, IO Rail		6	10	mA	5
Powerdown Current	I _{DDPD3.3}	Power down mode, 3.3V Rail		6	5	mA	
	I _{DDPDIO}	Power down mode, IO Rail		0	0.1	mA	5
Input Frequency	F _i	V _{DD} = 3.3 V		14.3182	15	MHz	
Pin Inductance	L _{pin}				7	nH	
Input Capacitance	C _{IN}	Logic Inputs	1.5		5	pF	
	C _{OUT}	Output pin capacitance			6	pF	
	C _{INX}	X1 & X2 pins			6	pF	
Clk Stabilization	T _{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock		1.0	1.8	ms	
T _{fall_SE}	T _{FALL}	Fall/rise time of all 3.3V control inputs from 20-80%			10	ns	1
T _{rise_SE}	T _{RISE}				10	ns	1
SMBus Voltage	V _{DD}		2.7		5.5	V	
Low-level Output Voltage	V _{OLSMB}	@ I _{PULLUP}			0.4	V	
Current sinking at V _{OLSMB} = 0.4 V	I _{PULLUP}	SMB Data Pin	4	5		mA	
SCLK/SDATA Clock/Data Rise Time	T _{RI2C}	(Max V _{IL} - 0.15) to (Min V _{IH} + 0.15)			1000	ns	
SCLK/SDATA Clock/Data Fall Time	T _{FI2C}	(Min V _{IH} + 0.15) to (Max V _{IL} - 0.15)			300	ns	
Maximum SMBus Operating Frequency	F _{SMBUS}				100	kHz	
Spread Spectrum Modulation Frequency	f _{SSMOD}	Triangular Modulation	30	32.54	33	kHz	

Notes: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

¹ Signal is required to be monotonic in this region.

² Input leakage current does not include inputs with pull-up or pull-down resistors

³ 3.3V referenced inputs are: SCLK, SDATA, and CKPWRGD

⁴ Frequency Select pins which have tri-level input

⁵ If present, not all parts have this feature.

AC Electrical Characteristics - Low Power Differential Outputs, Commercial Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Rising Edge Slew Rate	tSLR	Averaging on	2.5	3.7	4	V/ns	2, 3
Falling Edge Slew Rate	tFLR	Averaging on	2.5	3.7	4	V/ns	2, 3
Slew Rate Variation	tSLVAR	Averaging on		3.6	20	%	1, 6
Differential Voltage Swing	VSWING	Averaging off	300			mV	2
Crossing Point Voltage	VXABS	Averaging off	300	446	550	mV	1,4,5
Crossing Point Variation	VXABSVAR	Averaging off		70	140	mV	1,4,9
Maximum Output Voltage	VHIGH	Averaging off			1150	mV	1,7
Minimum Output Voltage	VLOW	Averaging off	-300			mV	1,8
Duty Cycle	DCYC	Averaging on	45	49.8	55	%	2
CPU Skew	CPUSKEW	Averaging on		35	100	ps	
SRC Skew	t _{SKEW} SRC	Averaging on, SRC to SATA skew when Byte0, bit 1 = 0		259	350	ps	

NOTES: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production). C_L = 2pF, R_s = 0 ohms.

¹Measurement taken for single ended waveform on a component test board (not in system)

²Measurement taken from differential waveform on a component test board. (not in system)

³Slew rate emastured through V_{swing} voltage range centered about differential zero

⁴V_{cross} is defined at the voltage where Clock = Clock#, measured on a component test board (not in system)

⁵Only applies to the differential rising edge (Clock rising, Clock# falling)

⁶Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage

⁷The max voltage including overshoot.

⁸The min voltage including undershoot.

⁹The total variation of all V_{cross} measurements in any particular system. Note this is a subset of V_{cross} min/mas (V_{Cross} absolute) allowed. The intent is to limit V_{cross} induced modulation by setting C_{cross_delta} to be smaller than V_{Cross} absolute

Clock Jitter Specs - Low Power Differential Outputs, Commercial Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
CPU Jitter - Cycle to Cycle	CPUJC2C	Differential Measurement		50	85	ps	1
SRC/SATA Jitter - Cycle to Cycle	SRCJC2C	Differential Measurement		50	125	ps	1,2
DOT Jitter - Cycle to Cycle	DOTJC2C	Differential Measurement		50	250	ps	1
SRC Phase Jitter	t _{jphase} PLL	PCIe Gen 1		35	86	ps (p-p)	1,2,3
	t _{jphase} Lo	PCIe Gen 2 10kHz < f < 1.5MHz		1.8	3	ps (RMS)	1,2,3
	t _{jphase} High	PCIe Gen 2 1.5MHz < f < Nyquist (50MHz)		2.3	3.1	ps (RMS)	1,2,3

NOTES: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production). C_L = 2pF, R_s = 0 ohms.

¹Jitter specs are specified as measured on a clock characterization board. System designers need to take special care not to use these numbers, as the in-system performance will be somewhat degraded. The receiver EMTS (chispet or CPU) will have the receiver jitter specs as measured in a real system.

²Phase jitter requirement: The designated Gen2 outputs will meet the reference clock jitter requirements from the PCI Express Gen2 Base Spec. The test is performed on a component test board under quiet conditions with all outputs on.

³See <http://www.pcisig.com> for complete specs

Electrical Characteristics - REF-14.318MHz, Commercial Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	2, 4
Clock period	Tperiod	14.318MHz output nominal	69.82033	69.84129	69.86224	ns	2, 3
Absolute min/max period	Tab	14.318MHz output nominal	69.83400		70.84800	ns	2
CLK High Time	THIGH		29.97543		38.46654	V	
CLK Low time	TLOW		29.57543		38.26654	V	
Output High Current	IOH	VOH @MIN = 1.0 V, VOH@MAX = 3.135 V	-33		-33	mA	
Output Low Current	IOL	VOL @MIN = 1.95 V, VOL @MAX = 0.4 V	30		38	mA	
Rising/Falling Edge Slew Rate	t _{SLEW}	Measured between 0.8 to 2.0 V	1	1.7	4	V/ns	1
Duty Cycle	dt1	V _T = 1.5 V	45	53	55	%	2
Jitter, Cycle to cycle	t _{jyc-cyc}	V _T = 1.5 V		115	1000	ps	2

NOTES: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

¹Edge rate in system is measured from 0.8V to 2.0V.

²Duty cycle, Period and Jitter are measured with respect to 1.5V

³The average period over any 1us period of time

⁴Using frequency counter with the measurement interval equal or greater that 0.15s, target frequency is 14.318180 MHz

Electrical Characteristics - 27MHz_Spread / 27MHz_NonSpread, Commercial Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-50		50	ppm	1,2
			-15		15		1,2,3
Clock period	T _{period}	27.000MHz output nominal	37.0365		37.0376		
Output High Current	I _{OH}	VOH @MIN = 1.0 V, VOH@MAX = 3.135 V	-29		-23	mA	1
Output Low Current	I _{OL}	VOL @MIN = 1.95 V, VOL @MAX = 0.4 V	29		27	mA	1
Rising/Falling Edge Slew Rate	t _{slewr/f}	Rising/Falling edge rate	1	2	4	V/ns	1
Duty Cycle	d _{t1}	V _T = 1.5 V	45	50.4	55	%	1
Jitter, 27MHz_NonSpread Output	t _{jt}	Long Term (10us)		485	800	ps	
		V _T = 1.5 V	-100		100	ps	
		V _T = 1.5 V		57	120	ps	
Jitter, 27MHz_Spread Output	t _{jyc-cyc}	V _T = 1.5 V SS% <= 1.5% pk to pk		82	200	ps	4
		V _T = 1.5 V, SS% > 1.5% pk to pk		134	200	ps	4

NOTES: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

¹Edge rate in system is measured from 0.8V to 2.0V at default slew rate control setting.

²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF out is at 14.31818MHz

³At nominal temperature and voltage.

⁴Long term and peak to peak jitter do not apply to the 27MHz spreading output. The spread modulation directly impacts these values.

Absolute Maximum Ratings - DC Parameters, Industrial Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Maximum Supply Voltage	VDD _{xxx}	Supply Voltage			4.6	V	1
Maximum Supply Voltage	VDD _{xxx IO}	Low-Voltage Differential I/O Supply			3.8	V	1
Maximum Input Voltage	V _{IH}	3.3V Tolerant Inputs			4.6	V	1,2
Minimum Input Voltage	V _{IL}	Any Input	GND - 0.5			V	1
Storage Temperature	T _s	-	-65		150	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1,3

Notes: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

¹ Operation under these conditions is neither implied, nor guaranteed.

² Maximum V_{IH} is not to exceed VDD

³ Human Body Model

Electrical Characteristics - Input/Supply/Common Output DC Parameters, Industrial Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Ambient Operating Temp	T _{ambind}	Industrial Range	-40		85	°C	
Supply Voltage, Core	VDD _{xxx}	Supply Voltage	3.135	3.3	3.465	V	
Supply Voltage, I/O	VDD _{xxx IO}	Low-Voltage Differential I/O Supply	0.9975	1.05	3.465	V	5
Input High Voltage	V _{IHSE}	Single-ended 3.3V inputs	2	2.4	V _{DD} + 0.3	V	3
Input Low Voltage	V _{ILSE}	Single-ended 3.3V inputs	V _{SS} - 0.3	0.4	0.8	V	3
Low Threshold Input - High Voltage	V _{IH_FSC}	3.3 V +/-5%, Voltage for which FSC = '1'	0.7		3.3	V	4
Low Threshold Input - Low Voltage	V _{IL_FSC}	3.3 V +/-5%	V _{SS} - 0.3		0.35	V	
Input Leakage Current	I _{IN}	V _{IN} = V _{DD} , V _{IN} = GND	-5		5	uA	2
Input Leakage Current	I _{INRES}	Inputs with pull up or pull down resistors V _{IN} = V _{DD} , V _{IN} = GND	-200		200	uA	
Output High Voltage	V _{OHSE}	Single-ended outputs, I _{OH} = -1mA	2.4			V	1
Output Low Voltage	V _{OLSE}	Single-ended outputs, I _{OL} = 1 mA			0.4	V	1
Operating Supply Current	I _{DDOP3.3}	Full Active, C _L = Full load; I _{DD} 3.3V		92	110	mA	
	I _{DDOPIO}	Full Active, C _L = Full load; I _{DD} IO		18	25	mA	5
iAMT Mode Current	I _{DDIAMT3.3}	M1 mode, 3.3V Rail		48	65	mA	
	I _{DDIAMTIO}	M1 Mode, IO Rail		6	15	mA	5
Powerdown Current	I _{DDPD3.3}	Power down mode, 3.3V Rail		3.2	8	mA	
	I _{DDPDIO}	Power down mode, IO Rail		0	0.05	mA	5
Input Frequency	F _i	V _{DD} = 3.3 V		14.318	15	MHz	
Pin Inductance	L _{pin}			5	7	nH	
Input Capacitance	C _{IN}	Logic Inputs	1.5	4	5	pF	
	C _{OUT}	Output pin capacitance		5	6	pF	
	C _{INX}	X1 & X2 pins		4	6	pF	
Clk Stabilization	T _{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock			1.8	ms	
T _{fall_SE}	T _{FALL}	Fall/rise time of all 3.3V control inputs from 20-80%			10	ns	1
T _{rise_SE}	T _{RISE}				10	ns	1
SMBus Voltage	V _{DD}		2.7	3.3	5.5	V	
Low-level Output Voltage	V _{OLSMB}	@ I _{PULLUP}			0.4	V	
Current sinking at V _{OLSMB} = 0.4 V	I _{PULLUP}	SMB Data Pin	4	5		mA	
SCLK/SDATA Clock/Data Rise Time	T _{RI2C}	(Max V _{IL} - 0.15) to (Min V _{IH} + 0.15)			1000	ns	
SCLK/SDATA Clock/Data Fall Time	T _{FI2C}	(Min V _{IH} + 0.15) to (Max V _{IL} - 0.15)			300	ns	
Maximum SMBus Operating Frequency	F _{SMBUS}				100	kHz	
Spread Spectrum Modulation Frequency	f _{SSMOD}	Triangular Modulation	30	32.54	33	kHz	

Notes: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

¹ Signal is required to be monotonic in this region.

² Input leakage current does not include inputs with pull-up or pull-down resistors

³ 3.3V referenced inputs are: SCLK, SDATA, and CKPWRGD

⁴ Frequency Select pins which have tri-level input

⁵ If present, not all parts have this feature.

AC Electrical Characteristics - Low Power Differential Outputs, Industrial Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Rising Edge Slew Rate	t_{SLR}	Averaging on	2.5	3.7	4.2	V/ns	2, 3
Falling Edge Slew Rate	t_{FLR}	Averaging on	2.5	3.7	4.2	V/ns	2, 3
Slew Rate Variation	t_{SLVAR}	Averaging on		12.2	20	%	1, 6
Differential Voltage Swing	V_{SWING}	Averaging off	300			mV	2
Crossing Point Voltage	V_{XABS}	Averaging off	300	447	550	mV	1,4,5
Crossing Point Variation	$V_{XABSVAR}$	Averaging off		19	140	mV	1,4,9
Maximum Output Voltage	V_{HIGH}	Averaging off		941	1150	mV	1,7
Minimum Output Voltage	V_{LOW}	Averaging off	-300	-43		mV	1,8
Duty Cycle	DCYC	Averaging on	45	49.8	55	%	2
CPU Skew	$t_{SKEWCPU}$	Averaging on		35	100	ps	
SRC Skew	$t_{SKEWSRC}$	Averaging on, SRC to SATA skew when Byte0, bit 1 = 0		288	350	ps	

NOTES: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production). $C_L = 2pF$, $R_s = 0$ ohms.

¹Measurement taken for single ended waveform on a component test board (not in system)

²Measurement taken from differential waveform on a component test board. (not in system)

³Slew rate measured through minimum V_{swing} voltage range centered about differential zero

⁴ V_{cross} is defined at the voltage where Clock = Clock#, measured on a component test board (not in system)

⁵Only applies to the differential rising edge (Clock rising, Clock# falling)

⁶Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage

⁷The max voltage including overshoot.

⁸The min voltage including undershoot.

⁹The total variation of all V_{cross} measurements in any particular system. Note this is a subset of V_{cross} min/max (V_{Cross} absolute) allowed. The intent is to limit V_{cross} induced modulation by setting C_{cross_delta} to be smaller than V_{Cross} absolute

Clock Jitter Specifications - Low Power Differential Outputs, Industrial Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
CPU Jitter - Cycle to Cycle	$CPUJ_{C2C}$	Differential Measurement		55	85	ps	1
SRC Jitter - Cycle to Cycle	$SRCJ_{C2C}$	Differential Measurement		55	125	ps	1
SATA Jitter - Cycle to Cycle	$SATAJ_{C2C}$	Differential Measurement		55	125	ps	1
DOT Jitter - Cycle to Cycle	$DOTJ_{C2C}$	Differential Measurement		55	250	ps	1
SRC Phase Jitter	$t_{jphasePLL}$	PCIe Gen 1		45	86	ps (p-p)	1,2,3
	$t_{jphaseLo}$	PCIe Gen 2 10kHz < f < 1.5MHz		2	3	ps (RMS)	1,2,3
	$t_{jphaseHigh}$	PCIe Gen 2 1.5MHz < f < Nyquist (50MHz)		2.6	3.1	ps (RMS)	1,2,3

NOTES: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production). $C_L = 2pF$, $R_s = 0$ ohms.

¹Jitter specs are specified as measured on a clock characterization board. System designers need to take special care not to use these numbers, as the in-system performance will be somewhat degraded. The receiver EMTS (chispet or CPU) will have the receiver jitter specs as measured in a real system.

²Phase jitter requirement: The designated Gen2 outputs will meet the reference clock jitter requirements from the PCI Express Gen2 Base Spec. The test is performed on a component test board under quiet conditions with all outputs on.

³See <http://www.pcisig.com> for complete specs

Electrical Characteristics - REF-14.318MHz, Industrial Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	2, 4
Clock period	Tperiod	14.318MHz output nominal	69.82033	69.84129	69.86224	ns	2, 3
Absolute min/max period	Tabs	14.318MHz output nominal	69.83400		70.84800	ns	2
CLK High Time	THIGH		29.97543		38.46654	V	
CLK Low time	TLOW		29.57543		38.26654	V	
Output High Current	IOH	VOH @MIN = 1.0 V, VOH@MAX = 3.135 V	-33		-33	mA	
Output Low Current	IOL	VOL @MIN = 1.95 V, VOL @MAX = 0.4 V	30		38	mA	
Rising/Falling Edge Slew Rate	tSLEW	Measured between 0.8 to 2.0 V	1	1.8	4	V/ns	1
Duty Cycle	dt1	VT = 1.5 V	45	52.8	55	%	2
Jitter, Cycle to cycle	tjyc-cyc	VT = 1.5 V		122	500	ps	2

NOTES: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

¹Edge rate in system is measured from 0.8V to 2.0V at default slew rate control setting.

²Duty cycle, Period and Jitter are measured with respect to 1.5V

³The average period over any 1us period of time

⁴Using frequency counter with the measurement interval equal or greater that 0.15s, target frequency is 14.318180 MHz

Electrical Characteristics - 27MHz_Spread / 27MHz_NonSpread, Industrial Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-50		50	ppm	1,2
			-15		15		1,2,3
Clock period	Tperiod	27.000M outputs, 27M SS with SS OFF	37.0365		37.0376		
Output High Current	IOH	VOH @MIN = 1.0 V, VOH@MAX = 3.135 V	-29		-23	mA	
Output Low Current	IOL	VOL @MIN = 1.95 V, VOL @MAX = 0.4 V	29		27	mA	
Rising/Falling Edge Slew Rate	tSLEW	Measured between 0.8 to 2.0 V	1	2	4	V/ns	1
Duty Cycle	dt1	VT = 1.5 V	45	50.4	55	%	
Jitter, 27MHz_NonSpread Output	tRj	Long Term (10us)		485	800	ps	
	tjpk-pk	VT = 1.5 V	-100		100	ps	
	tjvc-cvc	VT = 1.5 V		57	120	ps	
Jitter, 27MHz_Spread Output	tjyc-cyc	VT = 1.5 V SS% <= 1.5% pk to pk		108	200	ps	4
		VT = 1.5 V, SS% > 1.5% pk to pk		140	200	ps	4

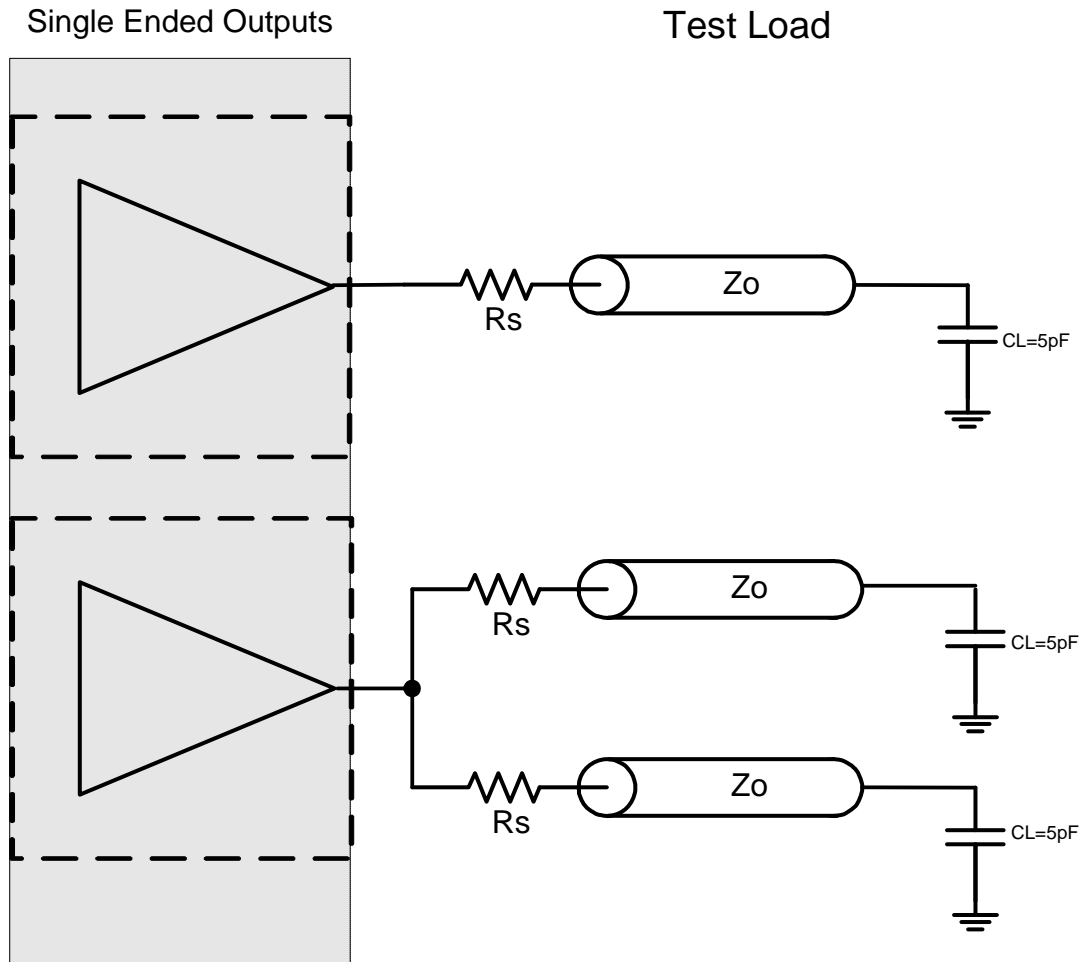
NOTES: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

¹Edge rate in system is measured from 0.8V to 2.0V at default slew rate control setting.

²All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF out is at 14.31818MHz

³At nominal temperature and voltage.

⁴Long term and peak to peak jitter do not apply to the 27MHz spreading output. The spread modulation directly impacts these values.



Suggested Suggested termination resistors for various driving conditions are as follows for transmission lines with $Z_o = 50$ ohms:

REF Output	Driving 1 load, $R_s = 39$ ohms
	Driving 2 loads, $R_s = 22$ ohms
27M SS and Non-SS outputs	Driving 1 load, $R_s = 39$ ohms
	Driving 2 loads, $R_s = 22$ ohms

Clock Periods Differential Outputs with Spread Spectrum Enabled

Measurement Window		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Symbol		- c-c jitter	-SSC	-ppm error	0ppm	+ ppm error	+SSC	+ c-c jitter		
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Absolute Period	Units	Notes
		Minimum	Minimum	Minimum	Nominal	Maximum	Maximum	Maximum		
Signal Name	SRC 100	9.87400	9.99900	9.99900	10.00000	10.00100	10.05130	10.17630	ns	1,2
	CPU 100	9.91400	9.99900	9.99900	10.00000	10.00100	10.05130	10.13630	ns	1,2
	CPU 133	7.41425	7.49925	7.49925	7.50000	7.50075	7.53845	7.62345	ns	1,2
	CPU 166	5.91440	5.99940	5.99940	6.00000	6.00060	6.03076	6.11576	ns	1,2
	CPU 200	4.91450	4.99950	4.99950	5.00000	5.00050	5.02563	5.11063	ns	1,2
	CPU 266	3.66463	3.74963	3.74963	3.75000	3.75038	3.76922	3.85422	ns	1,2
	CPU 333	2.91470	2.99970	2.99970	3.00000	3.00030	3.01538	3.10038	ns	1,2
	CPU 400	2.41475	2.49975	2.49975	2.50000	2.50025	2.51282	2.59782	ns	1,2

Clock Periods Differential Outputs with Spread Spectrum Disabled

Measurement Window		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
Symbol		- c-c jitter	-SSC	-ppm error	0ppm	+ ppm error	+SSC	+ c-c jitter		
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Absolute Period	Units	Notes
		Minimum	Minimum	Minimum	Nominal	Maximum	Maximum	Maximum		
Signal Name	SRC 100	9.87400		9.99900	10.00000	10.00100		10.17630	ns	1,2
	CPU 100	9.91400		9.99900	10.00000	10.00100		10.13630	ns	1,2
	CPU 133	7.41425		7.49925	7.50000	7.50075		7.62345	ns	1,2
	CPU 166	5.91440		5.99940	6.00000	6.00060		6.11576	ns	1,2
	CPU 200	4.91450		4.99950	5.00000	5.00050		5.11063	ns	1,2
	CPU 266	3.66463		3.74963	3.75000	3.75038		3.85422	ns	1,2
	CPU 333	2.91470		2.99970	3.00000	3.00030		3.10038	ns	1,2
	CPU 400	2.41475		2.49975	2.50000	2.50025		2.59782	ns	1,2
	DOT 96	10.16560		10.41560	10.41670	10.41770		10.66770	ns	1,2

Notes:

¹ Guaranteed by design and characterization, not 100% tested in production.

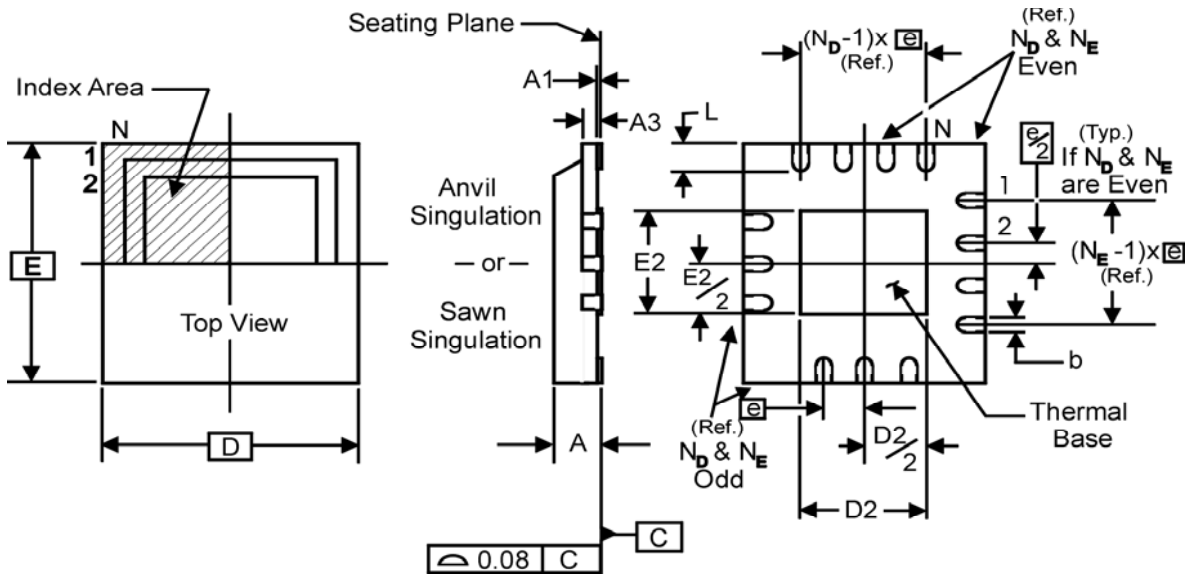
² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz

Test Clarification Table

Comments	HW		SW		OUTPUT
	FSLC/ TEST_SEL HW PIN	FSLB/ TEST_MODE HW PIN	TEST ENTRY BIT B9b3	REF/N or HI-Z B9b4	
	<2.0V	X	0	0	NORMAL
Power-up w/ TEST_SEL = 1 to enter test mode	>2.0V	0	X	0	HI-Z
Cycle power to disable test mode	>2.0V	0	X	1	REF/N
FSLC./TEST_SEL -->3-level latched input	>2.0V	1	X	0	REF/N
If power-up w/ V>2.0V then use TEST_SEL					
If power-up w/ V<2.0V then use FSLC	>2.0V	1	X	1	REF/N
FSLB/TEST_MODE -->low Vth input					
TEST_MODE is a real time input					
	<2.0V	X	1	0	HI-Z
If TEST_SEL HW pin is 0 during power-up, test mode can be invoked through B9b3.					
If test mode is invoked by B9b3, only B9b4 is used to select HI-Z or REF/N	<2.0V	X	1	1	REF/N
FSLB/TEST_Mode pin is not used.					
Cycle power to disable test mode, one shot control					

B9b3: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)

B9b4: 1= REF/N, Default = 0 (HI-Z)



THERMALLY ENHANCED, VERY THIN, FINE PITCH
 QUAD FLAT / NO LEAD PLASTIC PACKAGE

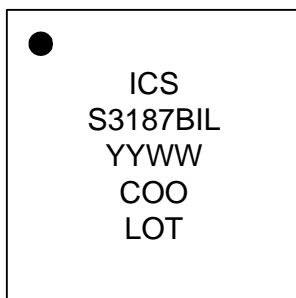
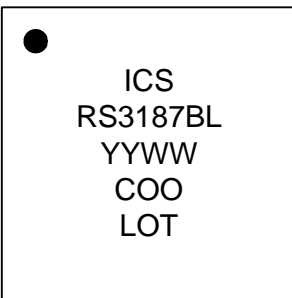
DIMENSIONS

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.20 Reference	
b	0.18	0.3
e	0.50 BASIC	

DIMENSIONS

SYMBOL	ICS 32L TOLERANCE
N	32
N_D	8
N_E	8
D x E BASIC	5.00 x 5.00
D2 MIN. / MAX.	3.0 / 3.3
E2 MIN. / MAX.	3.0 / 3.3
L MIN. / MAX.	0.30 / 0.50

Marking Diagrams



Ordering Information

Part / Order Number	Shipping Package	Package	Temperature
9LRS3187BKLF	Tubes	32-pin MLF	0 to +70° C
9LRS3187BKLF	Tape and Reel	32-pin MLF	0 to +70° C
9LRS3187BKILF	Tubes	32-pin MLF	-40 to +85° C
9LRS3187BKILF	Tape and Reel	32-pin MLF	-40 to +85° C

“LF” suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“B” is the device revision designator (will not correlate to the datasheet revision).

Revision History

A	04/13/10	RDW	Released to final	
B	04/15/10	RDW	Revised Commercial and Industrial Electrical Tables for Consistency	
C	06/02/10	LPL	Added Features bullet: Meets PCIe Gen2 Specifications	1
D	10/01/10	LPL	Updated pins 1/2 descriptions	2
E	04/29/11	RDW	Updated marking diagrams	19
F	11/04/11	DC	Updated CPU/SRC specs under Key Specifications	1

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.