KSZ8895MQX/RQX/FQX/ML

Integrated 5-Port 10/100 Managed Ethernet Switch with MII/RMII Interface

Revision 1.3

General Description

The KSZ8895MQX/RQX/FQX/ML is a highly-integrated, Layer 2 managed, five-port switch with numerous features designed to reduce system cost. Intended for cost-sensitive 10/100Mbps five-port switch systems with low power consumption, on-chip termination, and internal core power controllers, it supports high-performance memory bandwidth and shared memory-based switch fabric with non-blocking configuration. Its extensive feature set includes power management, programmable rate limit and priority ratio, tag/port-based VLAN, packets filtering, four-queue QoS prioritization, management interfaces, and MIB counters. The KSZ8895 family provides multiple CPU data interfaces to effectively address both current and emerging fast Ethernet applications when Port 5 is configured to separate MAC5 with SW5-MII/RMII and PHY5 with P5-MII/RMII interfaces.

The KSZ8895 family offers three configurations, providing the flexibility to meet different requirements:

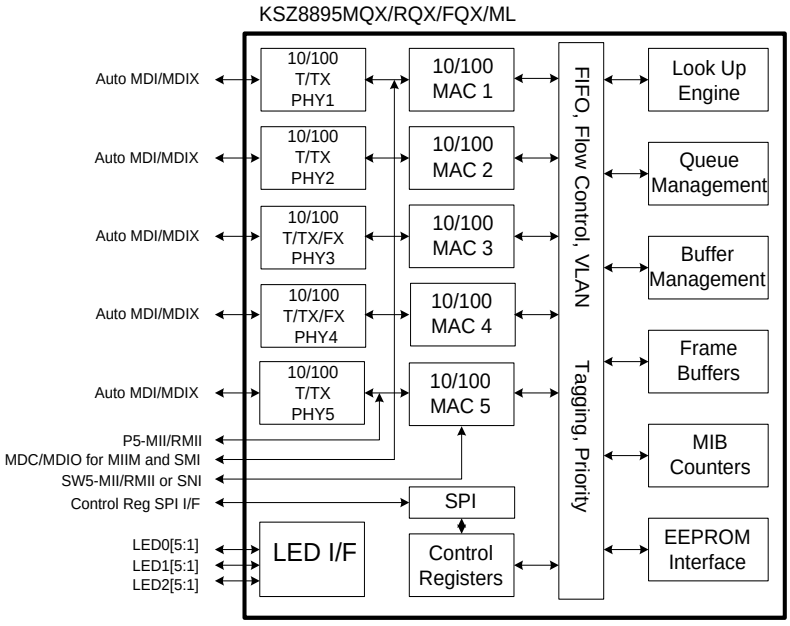
- KSZ8895MQX/ML: 5 10/100Base-T/TX transceivers, 1 SW5-MII and 1 P5-MII interface
- KSZ8895RQX: 5 10/100Base-T/TX transceivers, 1 SW5-RMII and 1 P5-RMII interface
- KSZ8895FQX: 4 10/100Base-T/TX transceivers on Ports 1, 2, 3 and 5 (port 3 can be set to the fiber mode). 1 100Base-FX transceivers on Port 4. 1 SW5-MII and 1 P5-MII interface

All registers of MACs and PHYs units can be managed by the SPI or the SMI interface. MIIM registers can be accessed through the MDC/MDIO interface. EEPROM can set all control registers for the unmanaged mode.

KSZ8895MQX/RQX/FQX are 128-pin PQFP package. KSZ8895ML is 128-pin LQFP package.

Datasheets and support documentation are available on Micrel's web site at: www.micrel.com.

Functional Diagram



Note:

SW5 indicates the MAC5 of the switch side, P5 indicates the PHY5 of the Port 5.

Features

Advanced Switch Features

- IEEE 802.1q VLAN support for up to 128 active VLAN groups (full-range 4096 of VLAN IDs).
- Static MAC table supports up to 32 entries.
- VLAN ID tag/untag options, per port basis
- IEEE 802.1p/q tag insertion or removal on a per port basis based on ingress port (egress).
- Programmable rate limiting at the ingress and egress on a per port basis.
- Jitter-free per packet based rate limiting support.
- Broadcast storm protection with percentage control (global and per port basis).
- IEEE 802.1d rapid spanning tree protocol RSTP support.
- Tail tag mode (1 byte added before FCS) support at Port 5 to inform the processor which ingress port receives the packet.
- 1.4Gbps high-performance memory bandwidth and shared memory-based switch fabric with fully non-blocking configuration.
- Dual MII with MAC5 and PHY5 on port 5, SW5-MII/RMII for MAC 5 and P5-MII/RMII for PHY 5.
- Enable/Disable option for huge frame size up to 2000 Bytes per frame.
- IGMP v1/v2 snooping (Ipv4) support for multicast packet filtering.
- IPv4/IPv6 QoS support.
- Support unknown unicast/multicast address and unknown VID packet filtering.
- Self-address filtering.

Comprehensive Configuration Register Access

- Serial management interface (MDC/MDIO) to all PHYs registers and SMI interface (MDC/MDIO) to all registers.
- High speed SPI (up to 25MHz) and I^2C master Interface to all internal registers.
- I/0 pins strapping and EEPROM to program selective registers in unmanaged switch mode.
- Control registers configurable on the fly (port-priority, 802.1p/d/q, AN and so on).

QoS/CoS Packet Prioritization Support

- Per port, 802.1p and DiffServ-based.
- 1/2/4-queue QoS prioritization selection.
- Programmable weighted fair queuing for ratio control.
- Re-mapping of 802.1p priority field per port basis.

Integrated Five-Port 10/100 Ethernet Switch

- New generation switch with five MACs and five PHYs with fully compliant with IEEE 802.3u standard.
- PHYs designed with patented enhanced mixed-signal technology.
- Non-blocking switch fabric assures fast packet delivery by utilizing a 1K MAC address lookup table and a store-and-forward architecture.
- On-chip 64Kbyte memory for frame buffering (not shared with 1K unicast address table).
- Full duplex IEEE 802.3x flow control (PAUSE) with force mode option.
- Half-duplex back pressure flow control.
- HP Auto MDI/MDI-X and IEEE Auto crossover support.
- SW-MII interface supports both MAC mode and PHY mode.
- 7-wire serial network interface (SNI) support for legacy MAC.
- Per port LED Indicators for link, activity, and 10/100 speed.
- Register port status support for link, activity, full/half duplex and 10/100 speed.
- Micrel LinkMD® cable diagnostic capabilities.
- On-chip terminations and internal biasing technology for cost down and lowest power consumption.

Switch Monitoring Features

- Port mirroring/monitoring/sniffing: ingress and/or egress traffic to any port or MII.
- MIB counters for fully compliant statistics gathering 34 MIB counters per port.
- Loop-back support for MAC, PHY and remote diagnostic of failure.
- Interrupt for the link change on any ports.

Features (Continued)

Low Power Dissipation

- Full-chip hardware power-down.
- Full-chip software power-down and per port software power down.
- Energy-detect mode support < 100mW full chip-power consumption when all ports have no activity.
- Very low full chip power consumption (<0.5W) in standalone 5-port, without extra power consumption on transformers.
- Dynamic clock tree shutdown feature.
- Voltages: Single 3.3V supply with 3.3V VDDIO and Internal 1.2V LDO controller enabled, or external 1.2V LDO solution.
  - Analog VDDAT 3.3V only.
  - VDDIO support 3.3V, 2.5V and 1.8V.
  - Low 1.2V core power .
- 0.11µm CMOS technology.
- Commercial temperature range: 0°C to +70°C.
- Industrial Temperature Range: -40°C to +85°C.
- 128-pin PQFP and 128-pin LQFP, lead-free package.

Applications

- Typical
- VOIP phone
- Set-top/game box
- Automotive
- Industrial control
- IPTV POF
- SOHO residential gateway
- Broadband gateway/firewall/VPN
- Integrated DSL/cable modem
- Wireless LAN access point + gateway
- Standalone 10/100 5-port switch

Ordering Information

Part Number	Temperature Range	Package	Description
KSZ8895MQXCA	0°C to 70°C	128-Pin PQFP	MII, Pb-Free, Commercial temperature
KSZ8895MQXIA	-40°C to +85°C	128-Pin PQFP	MII, Pb-Free, Industrial temperature
KSZ8895RQXCA	0°C to 70°C	128-Pin PQFP	RMII, Pb-Free, Commercial temperature
KSZ8895RQXIA	-40°C to +85°C	128-Pin PQFP	RMII, Pb-Free, Industrial temperature
KSZ8895FQXCA	0°C to 70°C	128-Pin PQFP	MII, support fiber, Pb-Free, Commercial part
KSZ8895FQXIA	-40°C to +85°C	128-Pin PQFP	MII, support fiber, Pb-Free, Industrial part
KSZ8895ML	0°C to 70°C	128-Pin LQFP	MII, Pb-Free, Commercial temperature
KSZ8895MLI	-40°C to +85°C	128-Pin LQFP	MII, Pb-Free, Industrial temperature
KSZ8895MQX-EVAL	Evaluation Board for KSZ8895MQX		
KSZ8895RQX-EVAL	Evaluation Board for KSZ8895RQX		
KSZ8895FQX-EVAL	Evaluation Board for KSZ8895FQX		
KSZ8895ML-EVAL	Evaluation Board for KSZ8895ML		

Revision History

Revision	Description	Date
1.0	Initial document created	O2/21/14
1.1	Update description for Register 1 bits [7:4], update the descriptions in the section of the internal 1.2V LDO controller. Update the Pin 125/Pin126 descriptions. Add evaluation boards in ordering information.	04/28/14
1.2	Update registers 131-134 bits [4:0] descriptions. Update Figure 16 and Figure 18. Add 100Base-FX data in Electrical Characteristics Table. Update Figure 3. Update pin description for Pin 107 and Pin 108. Added silver wire bonding part numbers to Ordering Information. Updated Ordering Information to include Ordering Part Number and Device Marking. Add a note for the register 14 bits [4:3].	12/9/14
1.3	Add register 137 (0x89) for 0.11µm and 0.13µm silicon identification. Update 1.2V core power high to 1.32V (1.2V+10%) in Operating Ratings section. Updated the Ordering Information Table to include only standard parts numbers. Updated description for Figure 35.	10/26/15

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System Level Applications

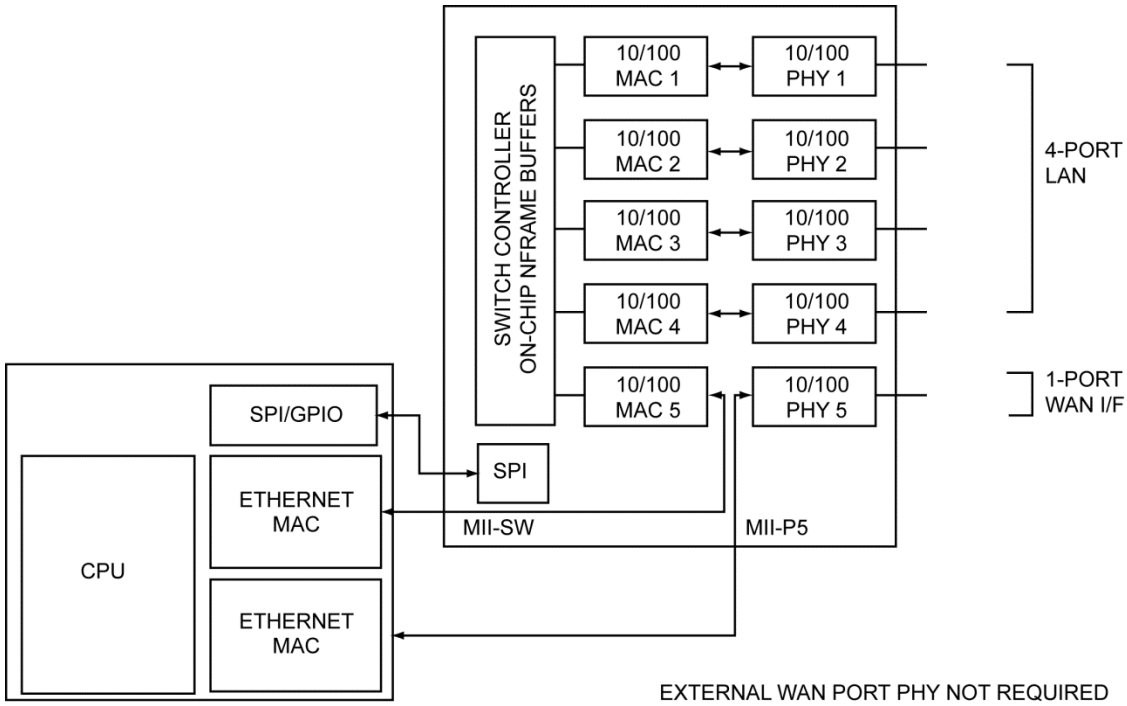


Figure 1. Broadband Gateway

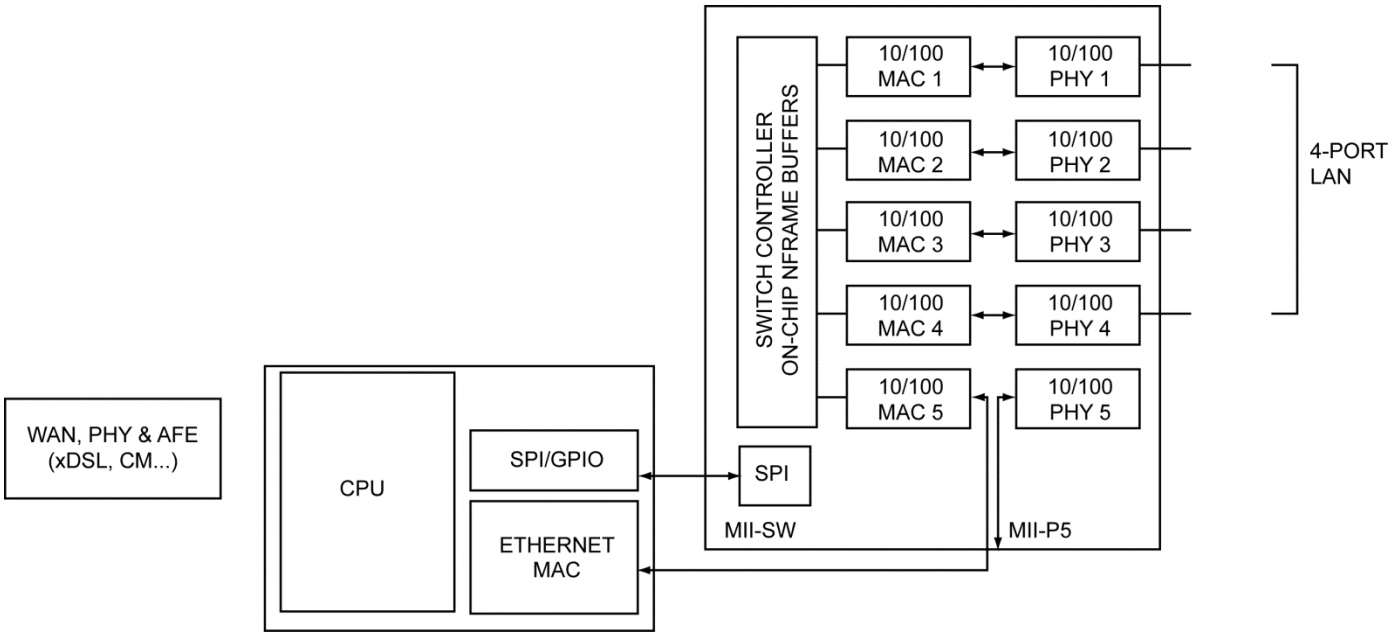


Figure 2. Integrated Broadband Router

System Level Applications (Continued)

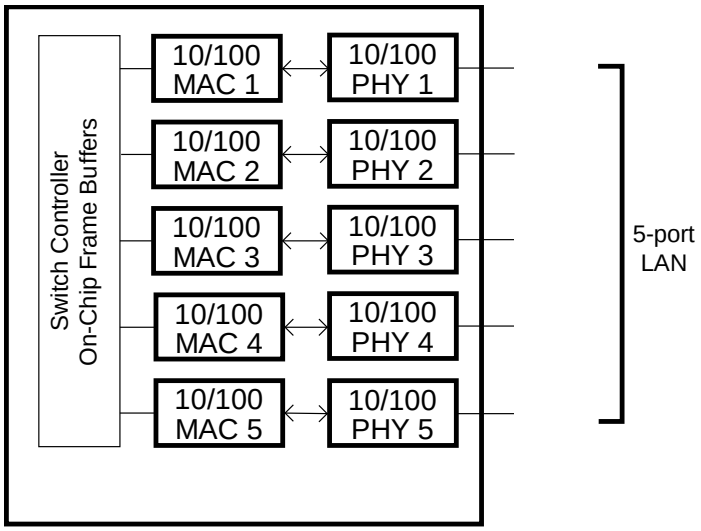


Figure 3. Standalone Switch

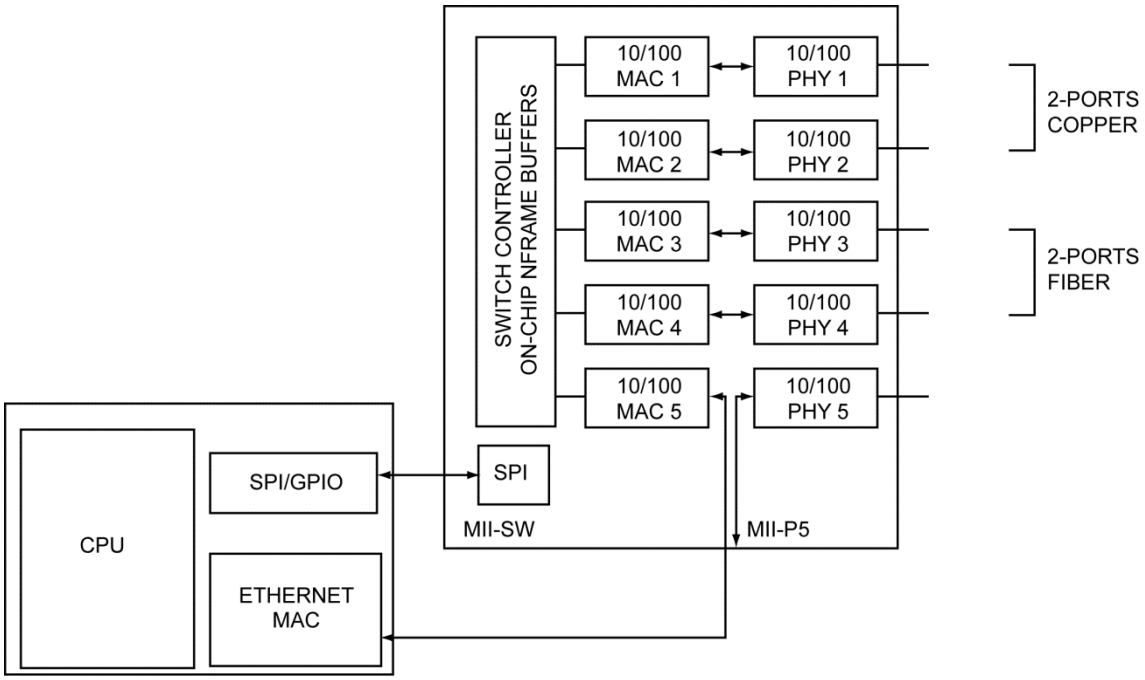
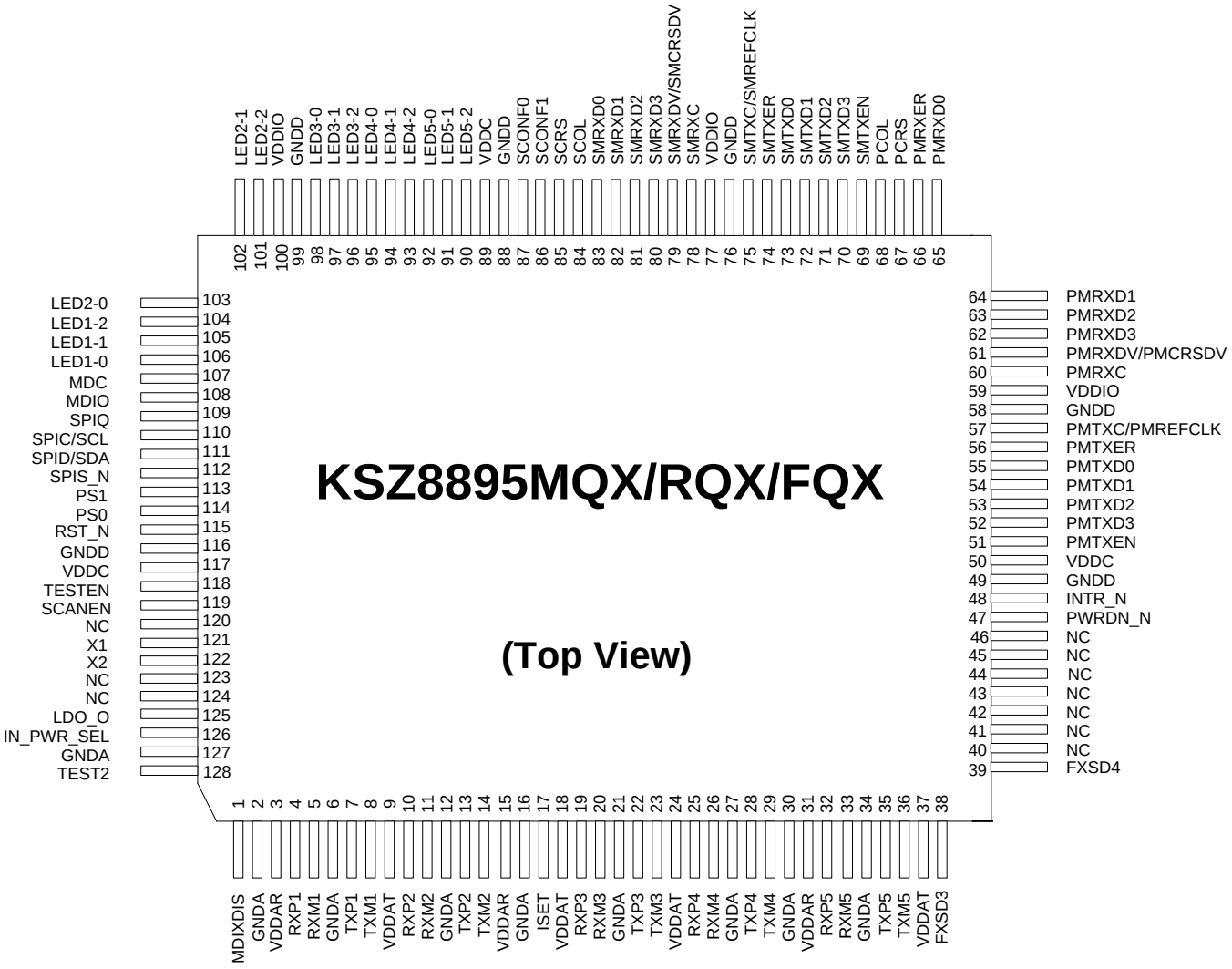


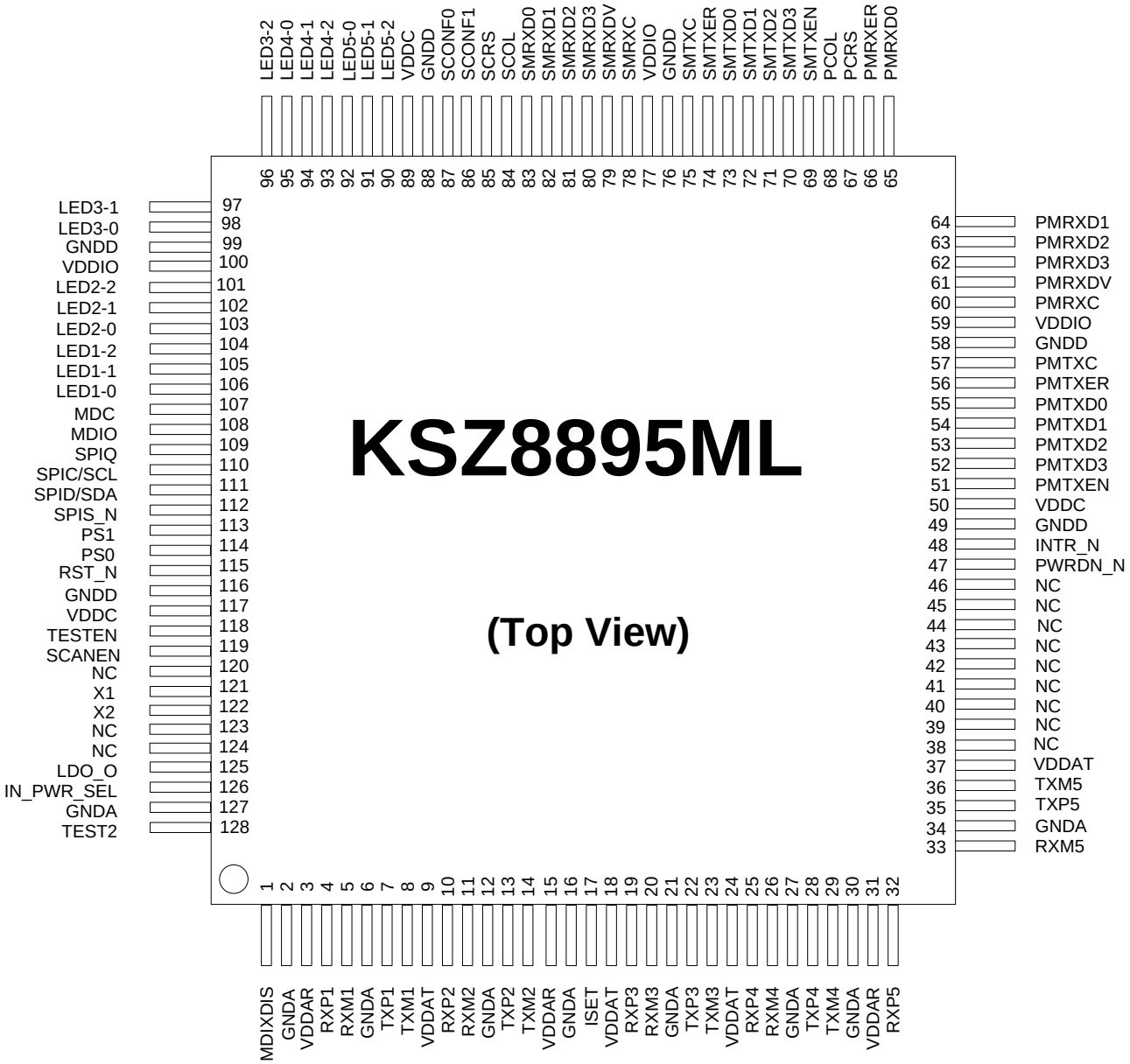
Figure 4. Using KSZ8895FQX for Dual Media Converter

Pin Configurations



128-Pin PQFP

Pin Configurations (Continued)



128-Pin LQFP Pin Configuration

Pin Description

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
1	MDI-XDIS	IPD	1 – 5	Disable auto MDI/MDI-X. PD (default) = normal operation. PU = disable auto MDI/MDI-X on all ports.
2	GNDA	GND		Analog ground.
3	VDDAR	P		1.2V analog V_{DD}.
4	RXP1	I	1	Physical receive signal + (differential).
5	RXM1	I	1	Physical receive signal - (differential).
6	GNDA	GND		Analog ground.
7	TXP1	O	1	Physical transmit signal + (differential).
8	TXM1	O	1	Physical transmit signal - (differential).
9	VDDAT	P		3.3V analog V_{DD}.
10	RXP2	I	2	Physical receive signal + (differential).
11	RXM2	I	2	Physical receive signal - (differential).
12	GNDA	GND		Analog ground.
13	TXP2	O	2	Physical transmit signal + (differential).
14	TXM2	O	2	Physical transmit signal - (differential).
15	VDDAR	P		1.2V analog V_{DD}.
16	GNDA	GND		Analog ground.
17	ISET			Set physical transmit output current. Pull-down with a 12.4kΩ1% resistor.
18	VDDAT	P		3.3V analog V_{DD}.
19	RXP3	I	3	Physical receive signal + (differential).
20	RXM3	I	3	Physical receive signal - (differential).
21	GNDA	GND		Analog ground.
22	TXP3	O	3	Physical transmit signal + (differential).
23	TXM3	O	3	Physical transmit signal – (differential).

Notes:

1. P = Power supply.
   I = Input.
   O = Output.
   I/O = Bidirectional.
   GND = Ground.
   IPU = Input w/internal pull-up.
   IPD = Input w/internal pull-down.
   IPD/O = Input w/internal pull-down during reset, output pin otherwise.
   OTRI = Output tristated.
2. NC = Do not connect to PCB.
   PU = Strap pin pull-up.
   PD = Strap pull-down.

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
24	VDDAT	P		3.3V analog V_{DD}.
25	RXP4	I	4	Physical receive signal + (differential).
26	RXM4	I	4	Physical receive signal - (differential).
27	GNDA	GND		Analog ground.
28	TXP4	O	4	Physical transmit signal + (differential).
29	TXM4	O	4	Physical transmit signal - (differential).
30	GNDA	GND		Analog ground.
31	VDDAR	P		1.2V analog V_{DD}.
32	RXP5	I	5	Physical receive signal + (differential).
33	RXM5	I	5	Physical receive signal - (differential).
34	GNDA	GND		Analog ground.
35	TXP5	O	5	Physical transmit signal + (differential).
36	TXM5	O	5	Physical transmit signal - (differential).
37	VDDAT	P		3.3V analog V_{DD}.
38	NC/FXSD3	IPD	3	FQX: This pin can be floating when port 3 is used as copper port (default). Port 3 can be set to fiber mode by Register 239 bit [7], this pin is used for fiber signal detect pin on Port 3 in Fiber mode. MQX/RQX/ML: no connection.
39	FXSD4	IPD	4	FQX: Fiber signal detect pin for Port 4. MQX/RQX/ML: no connection.
40	NC	NC		No connection. Leave NC pin floating.
41	NC	NC		No connection. Leave NC pin floating.
42	NC	NC		No connection. Leave NC pin floating.
43	NC	NC		No connection. Leave NC pin floating.
44	NC	NC		No connection. Leave NC pin floating.
45	NC	NC		No connection. Leave NC pin floating.
46	NC	NC		No connection. Leave NC pin floating.
47	PWRDN_N	IPU		Full-chip power down. Active low.
48	INTR_N	OPU		Interrupt. This pin is Open-Drain output pin.
49	GNDD	GND		Digital ground.
50	VDDC	P		1.2V digital core V_{DD}.
51	PMTXEN	IPD	5	PHY [5] MII/RMII transmit enable.
52	PMTXD3	IPD	5	MQX/FQX/ML: PHY [5] MII transmit bit 3. RQX: no connection for RMII.
53	PMTXD2	IPD	5	MQX/FQX/ML: PHY [5] MII transmit bit 2. RQX: no connection for RMII.
54	PMTXD1	IPD	5	PHY [5] MII/RMII transmit bit 1.
55	PMTXD0	IPD	5	PHY [5] MII/RMII transmit bit 0.

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
56	PMTXER	IPD	5	MQX/FQX/ML: PHY [5] MII transmit error. RQX: no connection for RMII.
57	PMTXC/PMREFCLK	I/O	5	MQX/FQX/ML: Output PHY [5] MII transmit clock RQX: Input PHY [5] RMII reference clock, 50MHz ±50ppm, the 50MHz clock comes from PMRXC Pin 60.
58	GNDD	GND		Digital ground.
59	VDDIO	P		3.3V, 2.5V or 1.8V digital V_{DD} for digital I/O circuitry.
60	PMRXC	I/O	5	MQX/FQX/ML: Output PHY [5] MII receive clock. RQX: Output PHY [5] RMII reference clock, this clock is used when opposite doesn't provide RMII 50MHz clock or the system doesn't provide an external 50MHz clock for the P5-RMII interface.
61	PMRXDV/PMCRSDV	IPD/O	5	MQX/FQX/ML: PMRXDV is for PHY [5] MII receive data valid. RQX: PMCRSDV is for PHY [5] RMII Carrier Sense/Receive Data Valid Output.
62	PMRXD3	IPD/O	5	MQX/FQX/ML: PHY [5] MII receive bit 3. RQX: no connection for RMII. Strap option: PD (default) = enable flow control. PU = disable flow control.
63	PMRXD2	IPD/O	5	MQX/FQX/ML: PHY [5] MII receive bit 2. RQX: no connection for RMII. Strap option: PD (default) = disable back pressure. PU = enable back pressure.
64	PMRXD1	IPD/O	5	PHY [5] MII/RMII receive bit 1. Strap option: PD (default) = drop excessive collision packets. PU = does not drop excessive collision packets.
65	PMRXD0	IPD/O	5	PHY [5] MII/RMII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode. PU = enable for performance enhancement.
66	PMRXER	IPD/O	5	MQX/FQX/ML:PHY [5] MII receive error RQX: no connection for RMII Strap option: PD (default) = packet size 1518/1522 bytes. PU = 1536 bytes.

Pin Descriptions (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
67	PCRS	IPD/O	5	MQX/FQX/ML: PHY [5] MII carrier sense. RQX: no connection for RMII. Strap option for port 4 only. PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto negotiation is disabled or fails. Refer to Register 76.
68	PCOL	IPD/O	5	MQX/FQX/ML: PHY [5] MII collision detect. RQX: no connection. Strap option for port 4 only. PD (default) = no force flow control, normal operation. PU = force flow control. Refer to Register 66.
69	SMTXEN	IPD		Port 5 Switch MII/RMII transmit enable.
70	SMTXD3	IPD		MQX/FQX/ML: Port 5 Switch MII transmit bit 3. RQX: no connection for RMII.
71	SMTXD2	IPD		MQX/FQX/ML: Port 5 Switch MII transmit bit 2. RQX: no connection for RMII.
72	SMTXD1	IPD		Port 5 Switch MII/RMII transmit bit 1.
73	SMTXD0	IPD		Port 5 Switch MII/RMII transmit bit 0.
74	SMTXER	IPD		MQX/FQX/ML: Port 5 Switch MII transmit error. RQX: no connection for RMII.
75	SMTXC/SMREFCLK	I/O		MQX/FQX/ML: Port 5 Switch MII transmit clock, Input: SW5-MII MAC mode, Output: SW5-MII PHY modes. RQX: Input SW5-RMII 50MHz +/-50ppm reference clock. The 50MHz clock comes from SMRXC Pin 78 when the device is the clock mode which the device's clock comes from 25MHz crystal/oscillator from Pins X1/X2. Or the 50MHz clock comes from external 50MHz clock source when the device is the normal mode which the device's clock source comes from SMTXC pin not from X1/X2 pins.
76	GNDD	GND		Digital ground.
77	VDDIO	P		3.3V, 2.5V or 1.8V digital V_{DD} for digital I/O circuitry.
78	SMRXC	I/O		MQX/FQX/ML: Port 5 Switch MII receive clock, Input: SW5-MII MAC mode, Output: SW5-MII PHY mode. RQX: Output SW5-RMII 50MHz clock, this clock is used when opposite doesn't provide RMII reference clock or the system doesn't provide an external 50MHz clock for the RMII interface.
79	SMRXDV/SMCRSDV	IPD/O		MQX/FQX/ML: SMRXDV is for Switch MAC5 MII receive data valid. RQX: SMCRSDV is for MAC5 RMII Carrier Sense/Receive Data Valid Output.
80	SMRXD3	IPD/O		MQX/FQX/ML: Port 5 Switch MII receive bit 3. RQX: no connection for RMII Strap option: PD (default) = Disable Switch SW5-MII full-duplex flow control PU = Enable Switch SW5-MII full-duplex flow control.

Pin Description (Continued)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Port</th><th>Pin Function(2)</th></tr>
<tr><td>81</td><td>SMRXD2</td><td>IPD/O</td><td></td><td>MQX/FQX/ML: Port 5 Switch MII receive bit 2.
RQX: no connection for RMII
Strap option:
PD (default) = Switch SW5-MII in full-duplex mode;
PU = Switch SW5-MII in half-duplex mode.</td></tr>
<tr><td>82</td><td>SMRXD1</td><td>IPD/O</td><td></td><td>Port 5 Switch MII/RMII receive bit 1.
Strap option:
PD (default) = Port 5 Switch SW5-MII in 100Mbps mode.
PU = Switch SW5-MII in 10Mbps mode.</td></tr>
<tr><td>83</td><td>SMRXD0</td><td>IPD/O</td><td></td><td>Port 5 Switch MII/RMII receive bit 0.
Strap option:
LED mode
PD (default) = mode 0; PU = mode 1. See “Register 11.”
Mode 0, link at:
100/Full LEDx[2,1,0] = 0, 0, 0
100/Half LEDx[2,1,0] = 0, 1, 0
10/Full LEDx[2,1,0] = 0, 0, 1
10/Half LEDx[2,1,0] = 0, 1, 1
Mode 1, link at:
100/Full LEDx[2,1,0] = 0, 1, 0
100/Half LEDx[2,1,0] = 0, 1, 1
10/Full LEDx[2,1,0] = 1, 0, 0
10/Half LEDx[2,1,0] = 1, 0, 1

<table><tr><th></th><th>Mode 0</th><th>Mode 1</th></tr><tr><td>LEDX_2</td><td>Lnk/Act</td><td>100Lnk/Act</td></tr><tr><td>LEDX_1</td><td>Fulld/Col</td><td>10Lnk/Act</td></tr><tr><td>LEDX_0</td><td>Speed</td><td>Full duplex</td></tr></table></td></tr>
<tr><td>84</td><td>SCOL</td><td>IPD/O</td><td></td><td>MQX/FQX/ML: Port switch MII collision detect,
Input: SW5-MII MAC modes, Output: SW5-MII PHY modes
RQX: no connection for RMII</td></tr>
<tr><td>85</td><td>SCRS</td><td>IPD/O</td><td></td><td>MQX/FQX/ML: Port switch MII collision detect,
Input: SW5-MII MAC modes, Output: SW5-MII PHY modes
RQX: no connection for RMII</td></tr>
</table>

Pin Description (Continued)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>Type(1)</th><th>Port</th><th>Pin Function(2)</th></tr>
<tr><td>86</td><td>SCONF1</td><td>IPD</td><td></td><td>Pins 91, 86, and 87 are dual MII/RMII configuration pins for the Port 5 MAC5 MII/RMII and PHY [5] MII/RMII. SW5-MII supports both MAC mode and PHY modes. P5-MII supports PHY mode only. See pins configuration below:
<table>
<tr><th>Pin# (91, 86, 87)</th><th>Port 5 Switch MAC5 SW5-MII/RMII</th><th>Port5 PHY5 P5- MII/RMII</th></tr>
<tr><td>000</td><td>Disable, Otri</td><td>Disable, Otri</td></tr>
<tr><td>001</td><td>PHY Mode MII, or RMII</td><td>Disable, Otri</td></tr>
<tr><td>010</td><td>MAC Mode MII, or RMII</td><td>Disable, Otri</td></tr>
<tr><td>011</td><td>PHY Mode SNI</td><td>Disable, Otri</td></tr>
<tr><td>100</td><td>Disable (default)</td><td>Disable (default)</td></tr>
<tr><td>101</td><td>PHY Mode MII or RMII</td><td>P5-MII/RMII</td></tr>
<tr><td>110</td><td>MAC Mode MII or RMII</td><td>P5-MII/RMII</td></tr>
<tr><td>111</td><td>PHY Mode SNI</td><td>P5- MII/RMII</td></tr>
</table></td></tr>
<tr><td>87</td><td>SCONF0</td><td>IPD</td><td></td><td>Dual MII/RMII configuration pin. See Pin 86 descriptions.</td></tr>
<tr><td>88</td><td>GNDD</td><td>GND</td><td></td><td>Digital ground.</td></tr>
<tr><td>89</td><td>VDDC</td><td>P</td><td></td><td>1.2V digital core V_{DD}.</td></tr>
<tr><td>90</td><td>LED5-2</td><td>IPU/O</td><td>5</td><td>LED indicator 2.
Strap option:
Aging setup. See “Aging” section.
PU (default) = aging enable
PD = aging disable.</td></tr>
<tr><td>91</td><td>LED5-1</td><td>IPU/O</td><td>5</td><td>LED indicator 1.
Strap option:
PU (default): enable PHY [5] MII I/F.
PD: tri-state all PHY [5] MII output. See “Pin 86 SCONF1.”</td></tr>
<tr><td>92</td><td>LED5-0</td><td>IPU/O</td><td>5</td><td>LED indicator 0.
Strap option for port 4 only.
PU (default) = Enable auto-negotiation.
PD = Disable auto-negotiation. Strap to Register76 bit [7].</td></tr>
<tr><td>93</td><td>LED4-2</td><td>IPU/O</td><td>4</td><td>LED indicator 2.</td></tr>
<tr><td>94</td><td>LED4-1</td><td>IPU/O</td><td>4</td><td>LED indicator 1.</td></tr>
</table>

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
95	LED4-0	IPU/O	4	LED indicator 0. Strap option: PU (default) = Normal mode. PD = Energy Detection mode (EDPD mode) Strap to Register 14 bits [4:3]
96	LED3-2	IPU/O	3	LED indicator 2.
97	LED3-1	IPU/O	3	LED indicator 1.
98	LED3-0	IPU/O	3	LED indicator 0. Strap option: PU (default) = Select I/O drive strength (8mA); PD = Select I/O drive strength (12mA). Strap to Register132 bit [7-6].
99	GNDD	GND		Digital ground.
100	VDDIO	P		3.3V, 2.5V or 1.8V digital V_{DD} for digital I/O circuitry.
101	LED2-2	IPU/O	2	LED indicator 2. Strap option for RQX only: PU (default) = Select the device as clock mode in SW5- RMII, 25MHz crystal/oscillator to X1/X2 pins of the device and pins of SMRXC and PMRXC output 50MHz clock. PD = Select the device as normal mode in SW5-RMII. Switch MAC5 used only. The input clock from X1/X2 pins is not used, the device's clock source comes from SMTXC/SMREFCLK pin which the 50MHz reference clock comes from external 50MHz clock source, PMRXC can output 50MHz clock for P5-RMII interface in the normal mode.
102	LED2-1	IPU/O	2	LED indicator 1. Strap option: for Port 3 only. PU (default) = Enable auto-negotiation. PD = Disable auto-negotiation. Strap to Register60 bit [7].
103	LED2-0	IPU/O	2	LED indicator 0.
104	LED1-2	IPU/O	1	LED indicator 2.
105	LED1-1	IPU/O	1	LED indicator 1. Strap option: for port 3 only. PU (default) = no force flow control, normal operation. PD = force flow control. Strap to Register60 bit [4].
106	LED1-0	IPU/O	1	LED indicator 0. Strap option for port 3 only. PU (default) = force half-duplex if auto-negotiation is disabled or fails. PD = force full-duplex if auto negotiation is disabled or fails. Strap to Register60 bit [5].

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
107	MDC	IPU	All	PHYs MII management (MIIM registers) data clock. Or SMI interface clock
108	MDIO	IPU/O	All	PHYs MII management (MIIM registers) data I/O. Or SMI interface data I/O Note: Need an external pull-up when driven.
109	SPIQ	IPU/O	All	SPI serial data output in SPI slave mode. Note: Need an external pull-up when driven.
110	SPIC/SCL	IPU/O	All	(1) Input clock up to 25MHz in SPI slave mode, (2) Output clock at 61kHz in I^2C master mode. See “Pin 113.” Note: Need an external pull-up when driven.
111	SSPID/SDA	IPU/O	All	(1) Serial data input in SPI slave mode; (2) serial data input/output in I^2C master mode. See “Pin 113.” Note: Need an external pull-up when driven.
112	SPIS_N	IPU	All	Active low. (1) SPI data transfer start in SPI slave mode. When SPIS_N is high, the KSZ8895MQX/RQX/FQX/ML is deselected and SPIQ is held in high impedance state, a high-to-low transition to initiate the SPI data transfer. (2) not used in I^2C master mode.
113	PS1	IPD		Serial bus configuration pin. For this case, if the EEPROM is not present, the KSZ8895MQX/RQX/FQX/ML will start itself with the PS[1.0] = 00 default register values. **Pin Configuration** / **Serial Bus Configuration** PS[1.0] = 00 / I^2C Master Mode for EEPROM PS[1.0] = 01 / SMI Interface Mode PS[1.0] = 10 / SPI Slave Mode for CPU Interface PS[1.0] = 11 / Factory Test Mode (BIST)
114	PS0	IPD		Serial bus configuration pin. See “Pin 113.”
115	RST_N	IPU		Reset the KSZ8895MQX/RQX/FQX/ML device. Active low.
116	GNDD	GND		Digital ground.
117	VDDC	P		1.2V digital core V_{DD}.
118	TESTEN	IPD		NC for normal operation. Factory test pin.
119	SCANEN	IPD		NC for normal operation. Factory test pin.
120	NC	NC		No connection. Leave NC pin floating.
121	X1	I		25MHz crystal clock connection/or 3.3V Oscillator input. Crystal/Oscillator should be ±50ppm tolerance.
122	X2	O		25MHz crystal clock connection.
123	NC	NC		No connection. Leave NC pin floating.
124	NC	NC		No connection. Leave NC pin floating.

Pin Description (Continued)

Pin Number	Pin Name	Type[1]	Port	Pin Function[2]
125	LDO_O	P		LDO_O pin connect to gate pin of MOSFET if using the internal 1.2V LDO controller. LDO_O pin will be floating if using an external 1.2V LDO. Note: When Pin126 voltage is greater than the internal 1.2V LDO controller enable threshold (1V), the internal 1.2V LDO controller is enabled and creates a 1.2V output when using an external MOSFET. When Pin126 is pull-down, the internal 1.2V LDO controller is disabled and Pin 125 tri-stated.
126	IN_PWR_SEL	I		Pull-up or a resistor divider: Enable internal 1.2V LDO controller. Pull-down: Disable internal 1.2V LDO controller by a pull-down resistor. Note: A 4k pull-up and a 2k pull-down resistors divider network is recommended if using the internal 1.2V LDO controller and an external MOSFET for 1.2V power. A 100Ω (approximately) resistor between the source and drain pins on the MOSFET is highly recommended as well. You can also use an external 1.2V LDO for 1.2V power supply.
127	GNDA	GND		Analog ground.
128	TEST2	NC		NC for normal operation. Factory test pin.

Pins for Strap-in Options

The KSZ8895MQX/RQX/FQX/ML can function as a managed switch or an unmanaged switch. If no EEPROM or micro-controller exists, then the KSZ8895MQX/RQX/FQX/ML will operate from its default setting. The strap-in option pins can be configured by external pull-up/down resistors and take effect after power down reset or warm reset. The functions are described in the table below.

Pin Number	Pin Name	PU/PD[3]	Description[4]
1	MDI-XDIS	IPD	Disable auto MDI/MDI-X. Strap option: PD = (default) = normal operation. PU = disable auto MDI/MDI-X on all ports.
62	PMRXD3	IPD/O	PHY [5] MII receive bit 3. Strap option: PD (default) = enable flow control; PU = disable flow control.
63	PMRXD2	IPD/O	PHY [5] MII receive bit 2. Strap option: PD (default) = disable back pressure; PU = enable back pressure.
64	PMRXD1	IPD/O	PHY [5] MII receive bit 1. Strap option: PD (default) = drop excessive collision packets; PU = does not drop excessive collision packets.
65	PMRXD0	IPD/O	PHY [5] MII receive bit 0. Strap option: PD (default) = disable aggressive back-off algorithm in half-duplex mode; PU = enable for performance enhancement.
66	PMRXER	IPD/O	PHY [5] MII receive error. Strap option: PD (default) = 1522/1518 bytes; PU = packet size up to 1536 bytes.
67	PCRS	IPD/O	PHY [5] MII carrier sense Strap option for Port 4 only. PD (default) = force half-duplex if auto-negotiation is disabled or fails. PU = force full-duplex if auto-negotiation is disabled or fails. Refer to Register 76.
68	PCOL	IPD/O	PHY [5] MII collision detect Strap option for Port 4 only. PD (default) = no force flow control. PU = force flow control. Refer to Register 66.

Notes:

3. NC = No connect.
   IPD = Input w/internal pull-down.
   IPD/O = Input w/internal pull-down during reset, output pin otherwise.
   IPU/O = Input w/internal pull-up during reset, output pin otherwise.
4. NC = Do not connect to PCB.
   PD = Strap pin pull-down.
   PU = Strap pin pull-up.

Pins for Strap-in Options (Continued)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>PU/PD[3]</th><th>Description[4]</th></tr>
<tr><td>80</td><td>SMRXD3</td><td>IPD/O</td><td>Switch MII receive bit 3.
Strap option:
PD (default) = disable switch SW5-MII full-duplex flow control;
PU = enable switch SW5-MII full-duplex flow control.</td></tr>
<tr><td>81</td><td>SMRXD2</td><td>IPD/O</td><td>Switch MII receive bit 2.
Strap option:
PD (default) = switch SW5-MII in full-duplex mode;
PU = switch SW5-MII in half-duplex mode.</td></tr>
<tr><td>82</td><td>SMRXD1</td><td>IPD/O</td><td>Switch MII receive bit 1.
Strap option:
PD (default) = switch SW5-MII in 100Mbps mode.
PU = switch MII in 10Mbps mode.</td></tr>
<tr><td>83</td><td>SMRXD0</td><td>IPD/O</td><td>Switch MII receive bit 0.
Strap option: LED mode PD (default) = mode 0; PU = mode 1. See “Register 11.”
<table>
<tr><th></th><th>Mode 0</th><th>Mode 1</th></tr>
<tr><td>LEDX_2</td><td>Lnk/Act</td><td>100Lnk/Act</td></tr>
<tr><td>LEDX_1</td><td>Fulld/Col</td><td>10Lnk/Act</td></tr>
<tr><td>LEDX_0</td><td>Speed</td><td>Fulld</td></tr>
</table></td></tr>
<tr><td>86</td><td>SCONF1</td><td>IPD</td><td>Pin 91,86,87 are dual MII/RMII configuration pins for the Port 5 MAC 5 MII/RMII and PHY [5] MII/RMII. SW5-MII supports both MAC mode and PHY modes. P5-MII supports PHY mode only. See pins configuration below.
<table>
<tr><th>Pins [91, 86, 87]</th><th>Port 5 Switch MAC5 SW5- MII/RMII</th><th>Port5 PHY5 P5- MII/RMII</th></tr>
<tr><td>000</td><td>Disable, Otri</td><td>Disable, Otri</td></tr>
<tr><td>001</td><td>PHY Mode MII, or RMII</td><td>Disable, Otri</td></tr>
<tr><td>010</td><td>MAC Mode MII, or RMII</td><td>Disable, Otri</td></tr>
<tr><td>011</td><td>PHY Mode SNI</td><td>Disable, Otri</td></tr>
<tr><td>100</td><td>Disable (default)</td><td>Disable (default)</td></tr>
<tr><td>101</td><td>PHY Mode MII or RMII</td><td>P5-MII/RMII</td></tr>
<tr><td>110</td><td>MAC Mode MII or RMII</td><td>P5-MII/RMII</td></tr>
<tr><td>111</td><td>PHY Mode SNI</td><td>P5- MII/RMII</td></tr>
</table></td></tr>
<tr><td>87</td><td>SCONF0</td><td>IPD</td><td>Dual MII/RMII configuration pin. See Pin 86 description.</td></tr>
<tr><td>90</td><td>LED5-2</td><td>IPU/O</td><td>LED5 indicator 2.
Strap option: Aging setup. See “Aging” section
PU (default) = aging enable;
PD = aging disable.</td></tr>
</table>

Pins for Strap-in Options (Continued)

Pin Number	Pin Name	PU/PD[3]	Description[4]
91	LED5-1	IPU/O	LED5 indicator 1. Strap option: PU (default): enable PHY [5] MII I/F. PD: tri-state all PHY [5] MII output. See “Pin 86 SCONF1.”
92	LED5-0	IPU/O	LED5 indicator 0. Strap option for Port 4 only. PU (default) = Enable auto-negotiation. PD = Disable auto-negotiation. Strap to Register76 bit [7].
95	LED4-0	IPU/O	LED indicator 0. Strap option: PU (default) = Normal mode. PD = Energy Detection mode (EDPD mode). Strap to Register 14 bits [4:3].
98	LED3-0	IPU/O	LED3 indicator 0. Strap option: PU (default) = Select I/O current drive strength (8mA); PD = Select I/O current drive strength (12mA). Strap to Register132 bit [7:6].
101	LED2-2	IPU/O	LED2 indicator 2. Strap option for KSZ8895RQX only: PU (default) = Select the device as clock mode in RQX SW5- RMII, 25MHz crystal to X1/X2 pins of the device and REFCLK output 50MHz clock. PD = Select the device as normal mode in SW5-RMII. Switch MAC5 used only. The input clock is useless from X1/X2 pin, the device’s clock comes from SMTXC/SMREFCLK pin, 50MHz reference clock from external 50MHz clock source.
102	LED2-1	IPU/O	LED2 indicator 1. Strap option for Port 3 only. PU (default) = Enable auto-negotiation. PD = Disable auto-negotiation. Strap to Register60 bit [7].
105	LED1-1	IPU/O	LED1 indicator 1. Strap option for Port 3 only. PU (default) = no force flow control, normal operation. PD = force flow control. Strap to Register50 bit [4].
106	LED1-0	IPU/O	LED1 indicator 0. Strap option for Port 3 only. PU (default) = force half-duplex if auto-negotiation is disabled or fails. PD = force full-duplex if auto negotiation is disabled or fails. Strap to Register60 bit [5].

Pins for Strap-in Options (Continued)

<table>
<tr><th>Pin Number</th><th>Pin Name</th><th>PU/PD[3]</th><th>Description[4]</th></tr>
<tr><td>113</td><td>PS1</td><td>IPD</td><td>Serial bus configuration pin. For this case, if the EEPROM is not present, the KSZ8895MQX/RQX/FQX/ML will start itself with the PS[1:0] = 00 default register values .
<table>
<tr><th>Pin Configuration</th><th>Serial Bus Configuration</th></tr>
<tr><td>PS[1:0] = 00</td><td>I^2C Master Mode for EEPROM</td></tr>
<tr><td>PS[1:0] = 01</td><td>SMI Interface Mode</td></tr>
<tr><td>PS[1:0] = 10</td><td>SPI Slave Mode for CPU Interface</td></tr>
<tr><td>PS[1:0] = 11</td><td>Factory Test Mode (BIST)</td></tr>
</table></td></tr>
<tr><td>114</td><td>PS0</td><td>IPD</td><td>Serial bus configuration pin. See “Pin 113.”</td></tr>
<tr><td>128</td><td>TEST2</td><td>NC</td><td>NC for normal operation. Factory test pin.</td></tr>
</table>

Introduction

The KSZ8895MQX/RQX/FQX/ML contains five 10/100 physical layer transceivers and five media access control (MAC) units with an integrated Layer 2 managed switch. The device runs in three modes. The first mode is as a five-port integrated switch. The second is as a five-port switch with the fifth port decoupled from the physical port. In this mode, access to the fifth MAC is provided through a media independent interface (MII/RMII). This is useful for implementing an integrated broadband router. The third mode uses the dual MII/RMII feature to recover the use of the fifth PHY. This allows the additional broadband gateway configuration, where the fifth PHY may be accessed through the P5-MII/RMII port.

The KSZ8895MQX/RQX/FQX/ML has the flexibility to reside in a managed or unmanaged design. In a managed design, a host processor has complete control of the KSZ8895MQX/RQX/FQX/ML via the SPI bus, or the MDC/MDIO interface. An unmanaged design is achieved through I/O strapping or EEPROM programming at system reset time.

On the media side, the KSZ8895MQX/RQX/FQX/ML supports IEEE 802.3 10BASE-T, 100BASE-TX on all copper ports with Auto MDI/MDIX. The KSZ8895FQX supports 100BASE-FX on port 4, and port 3 is configurable either copper as default or fiber. The KSZ8895MQX/RQX/FQX/ML can be used as a fully managed five-port switch or hooked up to a microprocessor by its SW-MII/RMII interfaces for any application solutions.

Physical signal transmission and reception are enhanced through the use of patented analog circuitry and DSP technology that make the design more efficient and allows for reduced power consumption and strong electrical noise immunity.

Major enhancements from the KS8995MQ/RQ/FMQ to the KSZ8895MQX/RQX/FQX include more saving power, there is no a limitation for the center taps of the transformer in KSZ8895MQX/RQX/FQX, KSZ8895MQ/RQ/FMQ request the center taps of RX an TX of the transformer not to be tied together for saving power, except using 0.11um process and add Micrel LinkMD feature in KSZ8895MQX/RQX/FQX switches. The KSZ8895MQX/RQX/FQX are complete compatible with KSZ8895MQ/RQ/FMQ.

Functional Overview: Physical Layer Transceiver

100BASE-TX Transmit

The 100BASE-TX transmit function performs parallel-to-serial conversion, 4B/5B coding, scrambling, NRZ-to-NRZI conversion, MLT3 encoding and transmission. The circuit starts with a parallel-to-serial conversion, which converts the MII data from the MAC into a 125MHz serial bit stream. The data and control stream is then converted into 4B/5B coding followed by a scrambler. The serialized data is further converted from NRZ-to-NRZI format, and then transmitted in MLT3 current output. The output current is set by an external 1% 12.4kΩ resistor for the 1:1 transformer ratio. It has a typical rise/fall time of 4ns and complies with the ANSI TP-PMD standard regarding amplitude balance, overshoot, and timing jitter. The wave-shaped 10BASE-T output is also incorporated into the 100BASE-TX transmitter.

100BASE-TX Receive

The 100BASE-TX receiver function performs adaptive equalization, DC restoration, MLT3-to-NRZI conversion, data and clock recovery, NRZI-to-NRZ conversion, descrambling, 4B/5B decoding, and serial-to-parallel conversion. The receiving side starts with the equalization filter to compensate for intersymbol interference (ISI) over the twisted pair cable. Since the amplitude loss and phase distortion is a function of the length of the cable, the equalizer has to adjust its characteristics to optimize the performance. In this design, the variable equalizer will make an initial estimation based on comparisons of incoming signal strength against some known cable characteristics, then tunes itself for optimization. This is an ongoing process and can self-adjust against environmental changes such as temperature variations.

The equalized signal then goes through a DC restoration and data conversion block. The DC restoration circuit is used to compensate for the effect of baseline wander and improve the dynamic range. The differential data conversion circuit converts the MLT3 format back to NRZI. The slicing threshold is also adaptive.

The clock recovery circuit extracts the 125MHz clock from the edges of the NRZI signal. This recovered clock is then used to convert the NRZI signal into the NRZ format. The signal is then sent through the de-scrambler followed by the 4B/5B decoder. Finally, the NRZ serial data is converted to the MII format and provided as the input data to the MAC.

PLL Clock Synthesizer

The KSZ8895MQX/RQX/FQX/ML generates 125MHz, 83MHz, 41MHz, 25MHz and 10MHz clocks for system timing. Internal clocks are generated from an external 25MHz crystal or oscillator.

Scrambler/Descrambler (100BASE-TX only)

The purpose of the scrambler is to spread the power spectrum of the signal in order to reduce EMI and baseline wander. The data is scrambled through the use of an 11-bit wide linear feedback shift register (LFSR). This can generate a 2047-bit non-repetitive sequence. The receiver will then descramble the incoming data stream with the same sequence at the transmitter.

100BASE-FX Operation

100BASE-FX operation is very similar to 100BASE-TX operation except that the scrambler/descrambler and MLT3 encoder/decoder are bypassed on transmission and reception. In this mode, the auto-negotiation feature is bypassed since there is no standard that supports fiber auto-negotiation.

100BASE-FX Signal Detection

The physical port runs in 100BASE-FX fiber mode for the Port 3 and Port 4 of the KSZ8895FQX. This signal is internally referenced to 1.2V. The fiber module interface should be set by a voltage divider such that FXSDx ‘H’ is above this 1.2V reference, indicating signal detect, and FXSDx ‘L’ is below the 1.2V reference to indicate no signal. There is no auto-negotiation for 100BASE-FX mode, the ports must be forced to either full or half-duplex for the fiber ports. Note that strap-in options support Port 3 and Port 4 to disable auto-negotiation, force 100Base-FX speed, force duplex mode, and force flow control for KSZ8895FQX with unmanaged mode.

100BASE-FX Far End Fault

Far end fault occurs when the signal detection is logically false from the receive fiber module. When this occurs, the transmission side signals the other end of the link by sending 84 1s followed by a zero in the idle period between frames. The far end fault may be disabled through register settings.

10BASE-T Transmit

The output 10BASE-T driver is incorporated into the 100BASE-T driver to allow transmission with the same magnetics. They are internally wave-shaped and pre-emphasized into outputs with a typical 2.3V amplitude. The harmonic contents are at least 27dB below the fundamental when driven by an all-ones Manchester-encoded signal.

10BASE-T Receive

On the receive side, input buffer and level detecting squelch circuits are employed. A differential input receiver circuit and a PLL perform the decoding function. The Manchester-encoded data stream is separated into clock signal and NRZ data. A squelch circuit rejects signals with levels less than 400mV or with short pulsewidths in order to prevent noises at the RXP or RXM input from falsely triggering the decoder. When the input exceeds the squelch limit, the PLL locks onto the incoming signal and the KSZ8895MQX/RQX/FQX/ML decodes a data frame. The receiver clock is maintained active during idle periods in between data reception.

MDI/MDI-X Auto Crossover

To eliminate the need for crossover cables between similar devices, the KSZ8895MQX/RQX/FQX/ML supports HP Auto MDI/MDI-X and IEEE 802.3u standard MDI/MDI-X auto crossover. HP Auto MDI/MDI-X is the default.

The auto-sense function detects remote transmit and receive pairs and correctly assigns transmit and receive pairs for the KSZ8895MQX/RQX/FQX/ML device. This feature is extremely useful when end users are unaware of cable types, and also, saves on an additional uplink configuration connection. The auto-crossover feature can be disabled through the port control registers, or MIIM PHY registers. The IEEE 802.3u standard MDI and MDI-X definitions are:

Table 1. MDI/MDI-X Pin Definitions

MDI		MDI-X	
RJ-45 Pins	**Signals**	**RJ-45 Pins**	**Signals**
1	TD+	1	RD+
2	TD-	2	RD-
3	RD+	3	TD+
6	RD-	6	TD-

Straight Cable

A straight cable connects an MDI device to an MDI-X device, or an MDI-X device to an MDI device. The following diagram depicts a typical straight cable connection between a NIC card (MDI) and a switch, or hub (MDI-X).

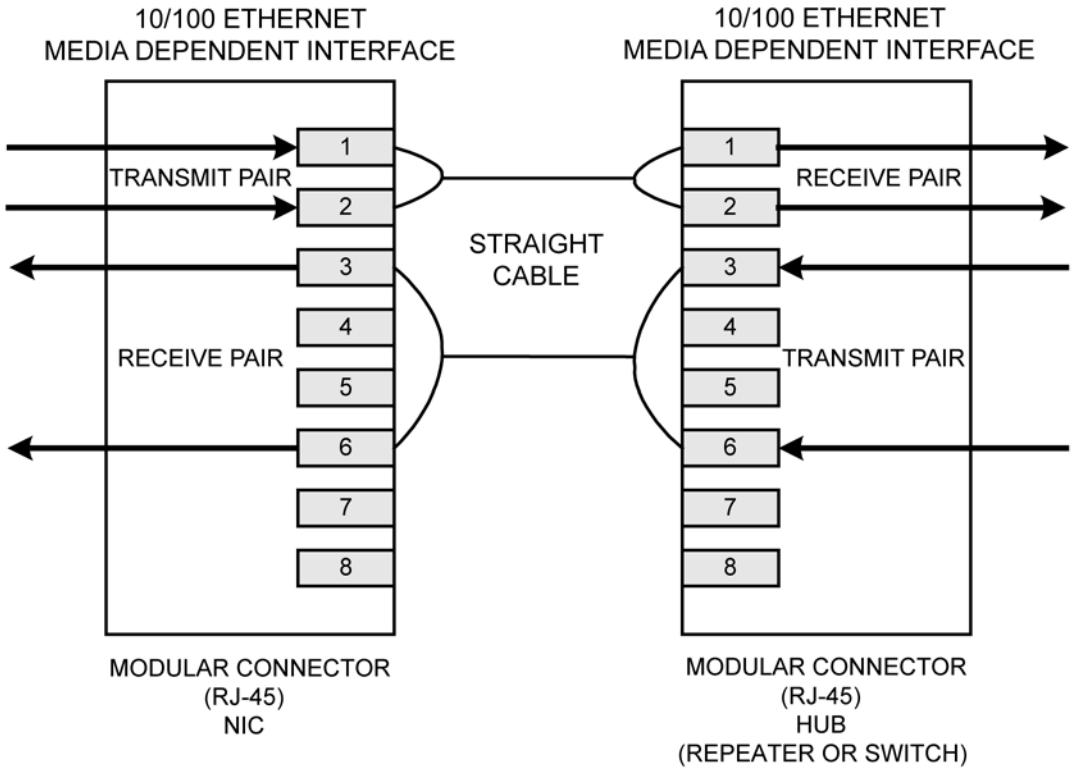


Figure 5. Typical Straight Cable Connection

Crossover Cable

A crossover cable connects an MDI device to another MDI device, or an MDI-X device to another MDI-X device. The following diagram shows a typical crossover cable connection between two switches or hubs (two MDI-X devices).

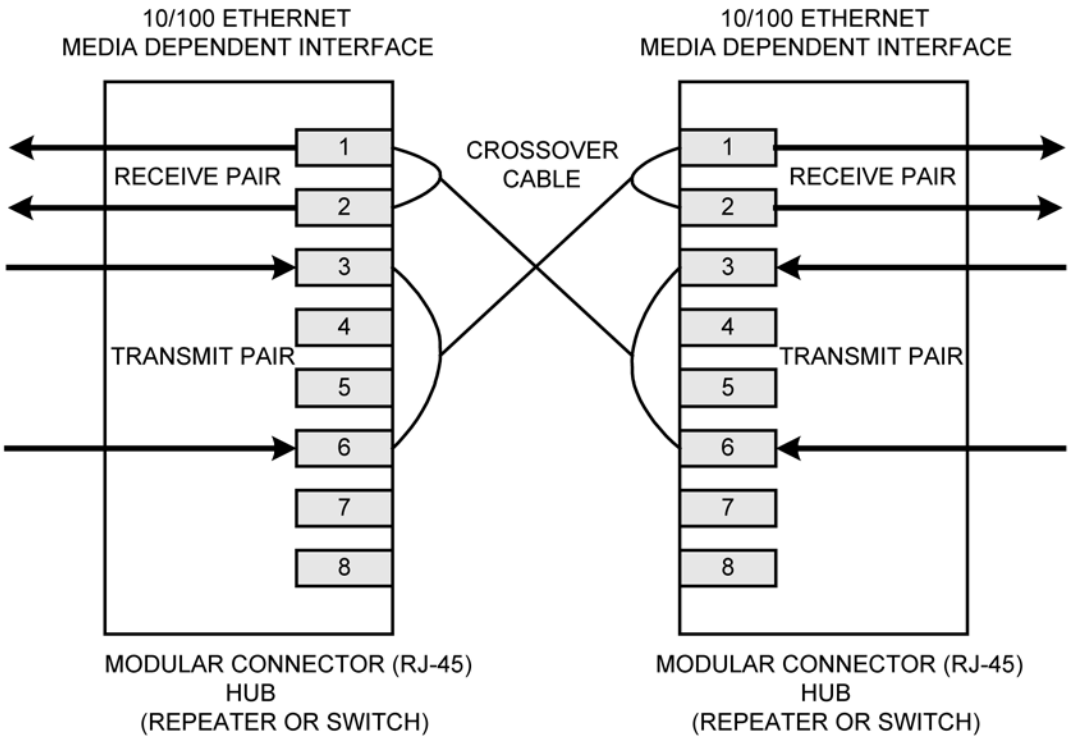


Figure 6. Typical Crossover Cable Connection

Auto-Negotiation

The KSZ8895MQX/RQX/FQX/ML conforms to the auto-negotiation protocol as described by the 802.3 committee. Auto-negotiation allows unshielded twisted pair (UTP) link partners to select the highest common mode of operation. Link partners advertise their capabilities to each other, and then compare their own capabilities with those they received from their link partners. The highest speed and duplex setting that is common to the two link partners is selected as the mode of operation. Auto-negotiation is supported for the copper ports only.

The following list shows the speed and duplex operation mode from highest to lowest.

- Highest: 100Base-TX, full-duplex
- High: 100Base-TX, half-duplex
- Low: 10Base-T, full-duplex
- Lowest: 10Base-T, half-duplex

If auto-negotiation is not supported or the KSZ8895MQX/RQX/FQX/ML link partner is forced to bypass auto-negotiation, the KSZ8895MQX/RQX/FQX/ML sets its operating mode by observing the signal at its receiver. This is known as parallel detection, and allows the KSZ8895MQX/RQX/FQX/ML to establish link by listening for a fixed signal protocol in the absence of auto-negotiation advertisement protocol. The auto-negotiation link up process is shown in the following flow chart.

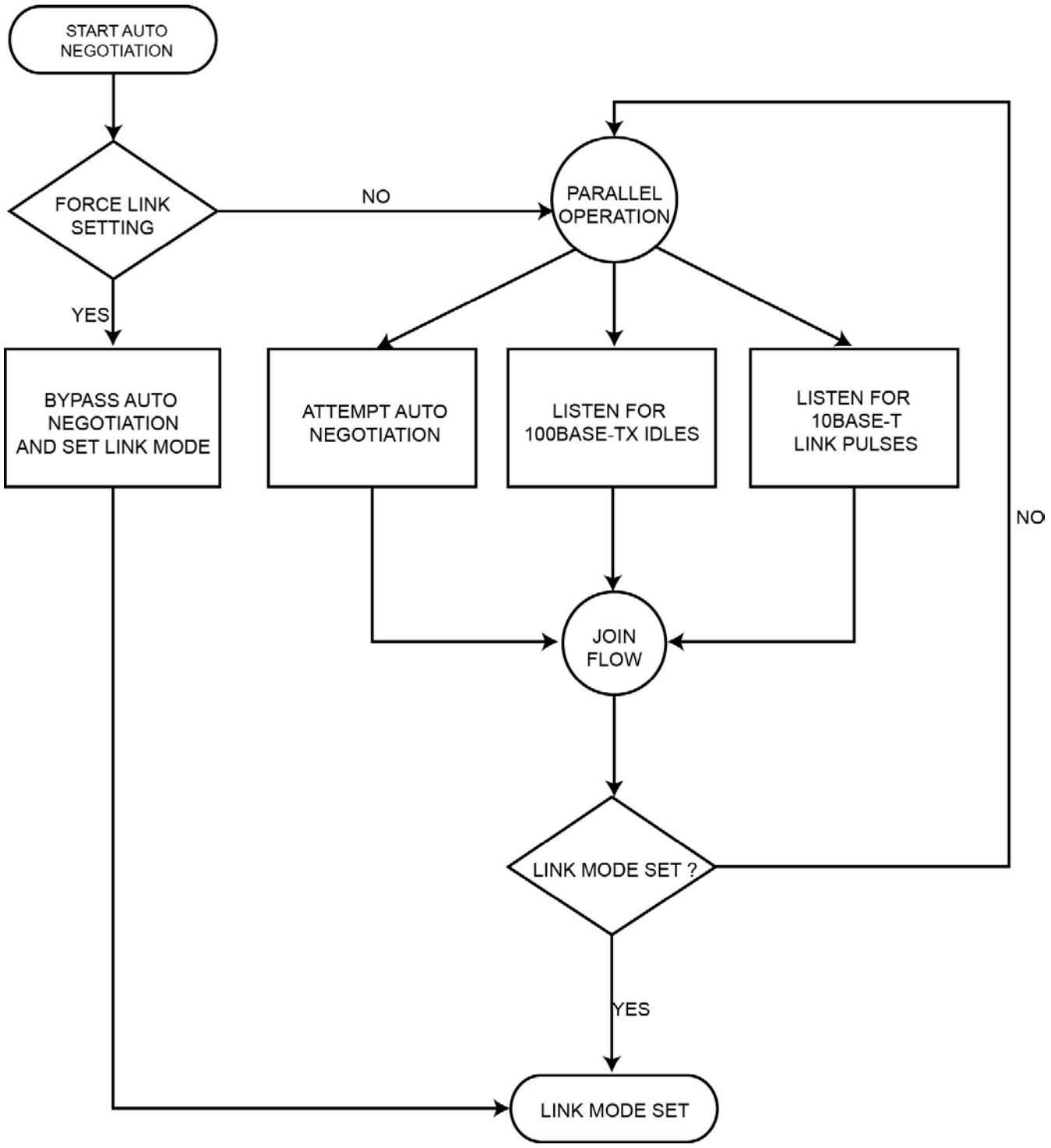


Figure 7. Auto-Negotiation

LinkMD® Cable Diagnostics

The LinkMD® feature utilizes time domain reflectometry (TDR) to analyze the cabling plant for common cabling problems such as open circuits, short circuits and impedance mismatches.

LinkMD® works by sending a pulse of known amplitude and duration down the MDI and MDI-X pairs and then analyzes the shape of the reflected signal. Timing the pulse duration gives an indication of the distance to the cabling fault with maximum distance of 200m and accuracy of ±2m. Internal circuitry displays the TDR information in a user-readable digital format.

Note:

Cable diagnostics are only valid for copper connections and do not support fiber optic operation.

Access

LinkMD® is initiated by accessing the PHY special control/status Registers {26, 42, 58, 74, 90} and the LinkMD result Registers {27, 43, 59, 75, 91} for ports 1, 2, 3, 4 and 5 respectively; and in conjunction with the Registers Port Control 12 and 13 for ports 1, 2, 3, 4 and 5 respectively to disable Auto-Negotiation and Auto MDI/MDIX.

Alternatively, the MIIM PHY Registers 0 and 1d can be used for LinkMD® access also.

Usage

The following is a sample procedure for using LinkMD® with Registers {26, 27, 28, 29} on port 1.

1. Disable Auto-Negotiation by writing a ‘1’ to Register 28 (0x1c), bit [7].
2. Disable auto MDI/MDI-X by writing a ‘1’ to Register 29 (0x1d), bit [2] to enable manual control over the differential pair used to transmit the LinkMD® pulse.
3. A software sequence set up to the internal registers for LinkMD only, see an example below.
4. Start cable diagnostic test by writing a ‘1’ to Register 26 (0x1a), bit [4]. This enable bit is self-clearing.
5. Wait (poll) for Register 26 (0x1a), bit [4] to return a ‘0’, and indicating cable diagnostic test is completed.
6. Read cable diagnostic test results in Register 26 (0x1a), bits [6:5]. The results are as follows:

   00 = normal condition (valid test)
   01 = open condition detected in cable (valid test)
   10 = short condition detected in cable (valid test)
   11 = cable diagnostic test failed (invalid test)

   The ‘11’ case, invalid test, occurs when the KSZ8895 is unable to shut down the link partner. In this instance, the test is not run, since it would be impossible for the KSZ8895 to determine if the detected signal is a reflection of the signal generated or a signal from another source.
7. Get distance to fault by concatenating Register 26 (0x1a), bit [0] and Register 27 (0x1b), bits [7:0]; and multiplying the result by a constant of 0.4. The distance to the cable fault can be determined by the following formula:

   D (distance to cable fault) = 0.4 x { (Register 26, bit [0]),(Register 27, bits [7:0]) }

   D (distance to cable fault) is expressed in meters.

   Concatenated value of Registers 26 bit [0] and 27 bit [7:0] should be converted to decimal before decrease 26 and multiplying by 0.4.

   The constant (0.4) may be calibrated for different cabling conditions, including cables with a velocity of propagation that varies significantly from the norm.

For port 2, 3, 4, 5 and for the MIIM PHY registers, LinkMD® usage is similar.

A LinkMD Example

The following is a sample procedure for using LinkMD® on port 1.

//Set Force 100/Full and Force MDIX mode

//W is WRITE the register. R is READ register

W 1c ff

W 1d 04

//Set Internal Registers Temporary Adjustment for LinkMD

W 47 b0

W 27 00

W 37 03 (03- port 1, 04-port2, 05-port3, 06-port4, 07-port5)

W 47 80 (bit7-port1, bit6-port2, bit5-port3, bit4-port4, bit3-port5)

W 27 00

W 37 00

//Enable LinkMD Testing with Fault Cable for port 1

W 1a 10

R 1a

R 1b

//Result analysis based on the values of the Register 0x1a and 0x1b for port 1:

//The Register 0x1a bits [6-5] are for the open or the short detection.

//The Register 0x1a bit [0] + the Register 0x1b bits [7-0] = Vct_Fault [8-0]

//The distance to fault is about 0.4 x {Vct_Fault [8-0] – 26}

Note:

After end the testing, set all registers above to their default value, the default values are ‘00’ for the Register (0x37) and the Register (0x47)

On-Chip Termination Resistors

The KSZ8895MQX/RQX/FQX/ML reduces the board cost and simplifies the board layout by using on-chip termination resistors for all ports and RX/TX differential pairs without the external termination resistors. The combination of the on-chip termination and internal biasing will save power consumption as compared to using external biasing and termination resistors, and the transformer will not consume power any more. The center tap of the transformer does not need to be tied to the analog power and does not tie the center taps together between RX and TX pairs for its application.

Internal 1.2V LDO Controller

The KSZ8895MQX/RQX/FQX/ML reduces board cost and simplifies board layout by integrating an internal 1.2V LDO controller to drive a low cost MOSFET to supply the 1.2V core power voltage for a single 3.3V power supply solution.

The internal 1.2V LDO controller can be disabled by Pin 126 IN_PWR_SEL pull-down in order to use an external 1.2V LDO.

Functional Overview: Power

The KSZ8895 device has two options for the power circuit in the design. one is a single 3.3V supply with 3.3V I/O power by using internal 1.2V LDO controller and one MOSFET for 1.2V analog and digital power. Another one is using external 1.2V LDO and provide 1.2V power for 1.2V analog and digital power. Table 2 illustrates the various voltage options and requirements of the device.

Table 2. Voltages and Power Pins

Power Signal Name	Device Pins	Requirement
VDDAT	9,18,24,37	3.3V analog power to the transceiver of the device.
VDDIO	59,77,100	Choice of 1.8V or 2.5V or 3.3V for the I/O circuits. These input power pins power the I/O circuitry of the device.
VDDAR	3, 15, 31	Filtered 1.2V analog voltage. This is where filtered 1.2V is fed back into the device to power the Analog block.
VDDC	50,89,117	Filtered 1.2V digital voltage. This pin feeds 1.2V to digital circuits within the Analog block.
GNDA	2,6,12,16,21,27,30,34,127	Analog Ground.
GNDD	49,58,76,88,99,116	Digital Ground.

Using Internal 1.2V LDO Controller

The preferred method of using the internal 1.2V LDO controller with an external MOSFET is illustrated in the figure below. The number of capacitors, ferrite beads (FB), values of capacitors, and exact placement of components will depend on the specific design. The 1.2V rail from the drain pin of the MOSFET to VDDAR Pin 3 is the 1.2V LDO feedback path. This connection should be as short as possible and there should be no series components on this feedback path. When the voltage of Pin 126 is just over 1V – along with the 3.3V power-up – the internal 1.2V LDO controller is enabled. The 1.2V LDO regulator (internal 1.2V LDO controller plus an external MOSFET) requests about 3.0V voltage at the 'S' pin of MOSFET when the internal 1.2V LDO controller is just enabled, the resistor divider will meet this requirement.

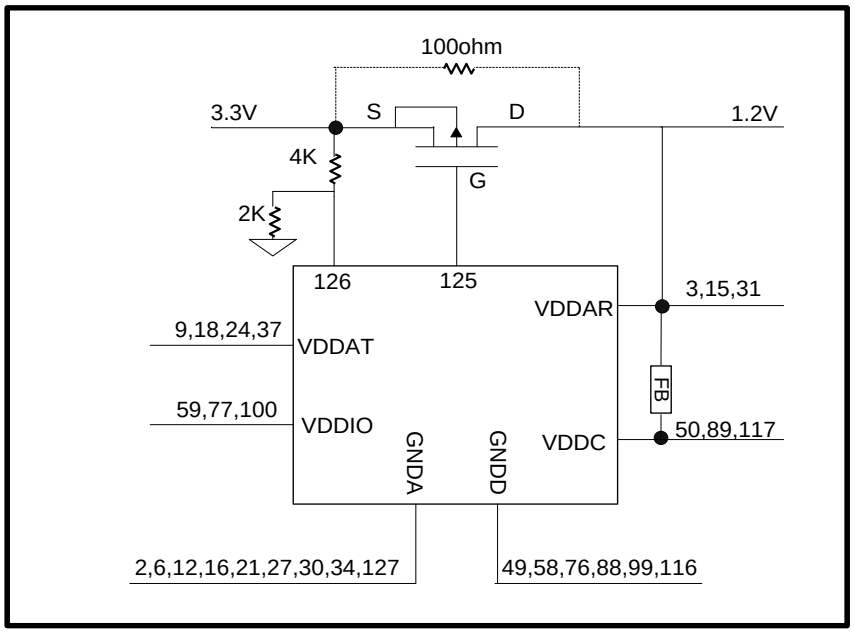


Figure 8. Recommended 1.2V Power Connection using Internal 1.2V LDO Controller

Using External 1.2V LDO Regulator

The KSZ8895MQX/RQX/FQX/ML can use an external 1.2V LDO regulator too. When use an external 1.2V LDO regulator solution, the Pin 126 should be pulled down by the pull-down resistor to disable the internal 1.2V LDO controller. There is no a power sequence request if all power rails voltage are ready after the power-up reset done.

Using the external 1.2V LDO regulator is illustrated in Figure 9. The number of capacitors, values of capacitors, and exact placement of components will depend on the specific design.

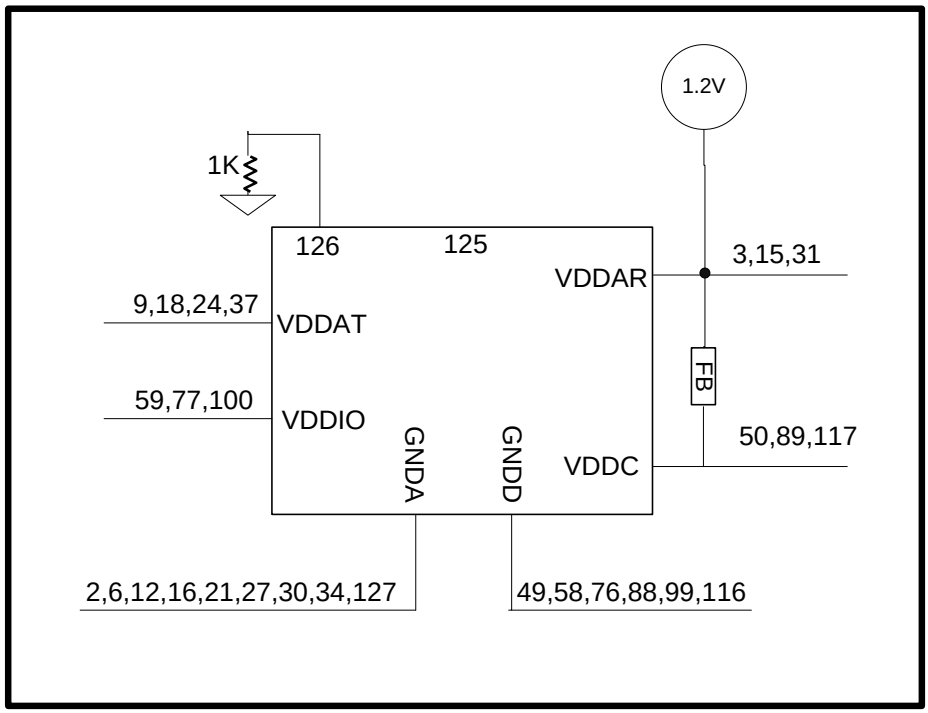


Figure 9. Recommended 1.2V Power Connection Using the External 1.2V Regulator

Functional Overview: Power Management

The KSZ8895MQX/RQX/FQX/ML supports a full chip hardware power down mode. When the PWRDN Pin 47 is internally activated low (pin PWRDN = 0), the entire chip is powered down. If this pin is de-asserted, the chip will be reset internally.

The KSZ8895MQX/RQX/FQX/ML can also use multiple power levels of 3.3V, 2.5V or 1.8V for VDDIO to support different I/O voltage.

The KSZ8895MQX/RQX/FQX/ML supports enhanced power management in a low power state, with energy detection to ensure low power dissipation during device idle periods. There are five operation modes under the power management function which are controlled by the Register 14 bit [4:3] and the Port Register Control 13 bit 3 as shown below:

Register 14 bits [4:3] = 00 Normal Operation Mode

Register 14 bits [4:3] = 01 Energy Detect Mode

Register 14 bits [4:3] = 10 Soft Power Down Mode

Register 14 bits [4:3] = 11 Power Saving Mode

The Port Register 29, 45, 61, 77, 93 Control 13 bit3 = 1 are for the Port Based Power-Down Mode.

Table 3 indicates all internal function blocks' status under four different power management operation modes.

Table 3. Internal Function Block Status

KSZ8895MQX/RQX/FQX/ML Function Blocks	Power Management Operation Modes			
	Normal Mode	Power Saving Mode	Energy Detect Mode	Soft Power-Down Mode
Internal PLL Clock	Enabled	Enabled	Disabled	Disabled
Tx/Rx PHY	Enabled	*Rx unused block disabled*	Energy detect at Rx	Disabled
MAC	Enabled	Enabled	Disabled	Disabled
Host Interface	Enabled	Enabled	Disabled	Disabled

Normal Operation Mode

This is the default setting bits [4:3] = 00 in Register 14 after chip power-up or hardware reset. When KSZ8895MQX/RQX/FQX/ML is in normal operation mode, all PLL clocks are running, PHY and MAC are on, and the host interface is ready for CPU READ or WRITE.

During normal operation mode, the host CPU can set the bits [4:3] in Register 14 to change the current normal operation mode to any one of the other three power management operation modes.

Energy Detect Mode

Energy detect mode provides a mechanism to save more power than in the normal operation mode when the KSZ8895MQX/RQX/FQX/ML port is not connected to an active link partner. In this mode, the device will save more power when the cables are unplugged. If the cable is not plugged in, the device can automatically enter a low power state—the energy detect mode. In this mode, the device will keep transmitting 120ns width pulses at 1 pulse/s rate. Once activity resumes due to plugging a cable in or attempting by the far end to establish link, the device can automatically power up to normal power state in energy detect mode.

Energy detect mode consists of two states, normal power state and low power state. While in low power state, the device reduces power consumption by disabling all circuitry except the energy detect circuitry of the receiver. The energy detect mode is entered by setting bits [4:3] = 01 in Register 14. When the KSZ8895MQX/RQX/FQX/ML is in this mode, it will monitor the cable energy. If there is no energy on the cable for a time longer than the pre-configured value at bit [7:0] Go-Sleep time in Register 15, the device will go into low power state. When KSZ8895MQX/RQX/FQX/ML is in low power state, it will keep monitoring the cable energy.

Once the energy is detected from the cable, the device will enter normal power state. When the device is at normal power state, it is able to transmit or receive packet from the cable.

Soft Power Down Mode

The soft power down mode is entered by setting bits [4:3] = 10 in Register 14. When KSZ8895MQX/RQX/FQX/ML is in this mode, all PLL clocks are disabled, also all of PHYs and the MACs are off. Any dummy host access will wake-up this device from current soft power down mode to normal operation mode and internal reset will be issued to make all internal registers go to the default values.

Power Saving Mode

The power saving mode is entered when auto-negotiation mode is enabled, the cable is disconnected, and by setting bits [4:3] = 11 in Register 14. When KSZ8895MQX/RQX/FQX/ML is in this mode, all PLL clocks are enabled, MAC is on, all internal register values will not change, and the host interface is ready for CPU read or write. In this mode, it mainly controls the PHY transceiver on or off, based on line status to achieve power saving. The PHY continues to transmit, only turning off the unused receiver block. Once activity resumes, due to plugging a cable or attempting by the far end to establish link, the KSZ8895MQX/RQX/FQX/ML can automatically enable the PHY to power up to normal power state from power saving mode.

During power saving mode, the host CPU can set bits [4:3] in Register 14 to change the current power saving mode to any one of the other three power management operation modes.

Port-Based Power-Down Mode

In addition, the KSZ8895MQX/RQX/FQX/ML features a per-port power-down mode. To save power, a PHY port that is not in use can be powered down via the Registers Port Control 13 bit 3, or MIIM PHY Registers 0 bit 11.

Functional Overview: Switch Core

Address Look-Up

The internal look-up table stores MAC addresses and their associated information. It contains a 1K unicast address table plus switching information. The KSZ8895MQX/RQX/FQX/ML is guaranteed to learn 1K addresses and distinguishes itself from a hash-based look-up table, which, depending on the operating environment and probabilities, may not guarantee the absolute number of addresses it can learn.

Learning

The internal look-up engine updates its table with a new entry if the following conditions are met:

- The received packet's source address (SA) does not exist in the look-up table.
- The received packet is good; the packet has no receiving errors and is of legal length.

The look-up engine inserts the qualified SA into the table, along with the port number and time stamp. If the table is full, the last entry of the table is deleted first to make room for the new entry.

Migration

The internal look-up engine also monitors whether a station is moved. If this occurs, it updates the table accordingly. Migration happens when the following conditions are met:

- The received packet's SA is in the table but the associated source port information is different.
- The received packet is good; the packet has no receiving errors and is of legal length.

The look-up engine will update the existing record in the table with the new source port information.

Aging

The look-up engine will update the time stamp information of a record whenever the corresponding SA appears. The time stamp is used in the aging process. If a record is not updated for a period of time, the look-up engine will remove the record from the table. The look-up engine constantly performs the aging process and will continuously remove aging records. The aging period is 300 +/- 75 seconds. This feature can be enabled or disabled through Register 3 or by external pull-up or pull-down resistors on LED[5][2]. See “Register 3” section.

Forwarding

The KSZ8895MQX/RQX/FQX/ML will forward packets using an algorithm that is depicted in the following flowcharts. Figure 6 shows stage one of the forwarding algorithm where the search engine looks up the VLAN ID, static table, and dynamic table for the destination address, and comes up with “port to forward 1” (PTF1). PTF1 is then further modified by the spanning tree, IGMP snooping, port mirroring, and port VLAN processes to come up with “port to forward 2” (PTF2), as shown in Figure 7. This is where the packet will be sent.

The KSZ8895MQX/RQX/FQX/ML will not forward the following packets:

- Error packets. These include framing errors, FCS errors, alignment errors, and illegal size packet errors.
- 802.3x pause frames. The KSZ8895MQX/RQX/FQX/ML will intercept these packets and perform the appropriate actions.
- “Local” packets. Based on destination address (DA) look-up. If the destination port from the look-up table matches the port where the packet was from, the packet is defined as “local.”

Switching Engine

The KSZ8895MQX/RQX/FQX/ML features a high-performance switching engine to move data to and from the MAC’s packet buffers. It operates in store and forward mode, while the efficient switching mechanism reduces overall latency. The KSZ8895MQX/RQX/FQX/ML has a 64kB internal frame buffer. This resource is shared between all five ports. There are a total of 512 buffers available. Each buffer is sized at 128B.

Media Access Controller (MAC) Operation

The KSZ8895MQX/RQX/FQX/ML strictly abides by IEEE 802.3 standards to maximize compatibility.

Inter-Packet Gap (IPG)

If a frame is successfully transmitted, the 96-bit time IPG is measured between the two consecutive MTXEN. If the current packet is experiencing collision, the 96-bit time IPG is measured from MCRS and the next MTXEN.

Backoff Algorithm

The KSZ8895MQX/RQX/FQX/ML implements the IEEE Standard 802.3 binary exponential backoff algorithm, and optional “aggressive mode” backoff. After 16 collisions, the packet will be optionally dropped, depending on the chip configuration in Register 3. See “Register 3.”

Late Collision

If a transmit packet experiences collisions after 512-bit times of the transmission, the packet will be dropped.

Illegal Frames

The KSZ8895MQX/RQX/FQX/ML discards frames less than 64 bytes and can be programmed to accept frames up to 1536 bytes in Register 4. For special applications, the KSZ8895MQX/RQX/FQX/ML can also be programmed to accept frames up to 1916 bytes in Register 4. Since the KSZ8895MQX/RQX/FQX/ML supports VLAN tags, the maximum sizing is adjusted when these tags are present.

Flow Control

The KSZ8895MQX/RQX/FQX/ML supports standard 802.3x flow control frames on both transmit and receive sides.
On the receive side, if the KSZ8895MQX/RQX/FQX/ML receives a pause control frame, the KSZ8895MQX/RQX/FQX/ML will not transmit the next normal frame until the timer, specified in the pause control frame, expires. If another pause frame is received before the current timer expires, the timer will be updated with the new value in the second pause frame. During this period (being flow controlled), only flow control packets from the KSZ8895MQX/RQX/FQX/ML will be transmitted.

On the transmit side, the KSZ8895MQX/RQX/FQX/ML has intelligent and efficient ways to determine when to invoke flow control. The flow control is based on availability of the system resources, including available buffers, available transmit queues and available receive queues.

The KSZ8895MQX/RQX/FQX/ML flow controls a port that has just received a packet if the destination port resource is busy. The KSZ8895MQX/RQX/FQX/ML issues a flow control frame (XOFF), containing the maximum pause time defined in IEEE standard 802.3x. Once the resource is freed up, the KSZ8895MQX/RQX/FQX/ML sends out the other flow control frame (XON) with zero pause time to turn off the flow control (turn on transmission to the port). A hysteresis feature is also provided to prevent over-activation and deactivation of the flow control mechanism.

The KSZ8895MQX/RQX/FQX/ML flow controls all ports if the receive queue becomes full.

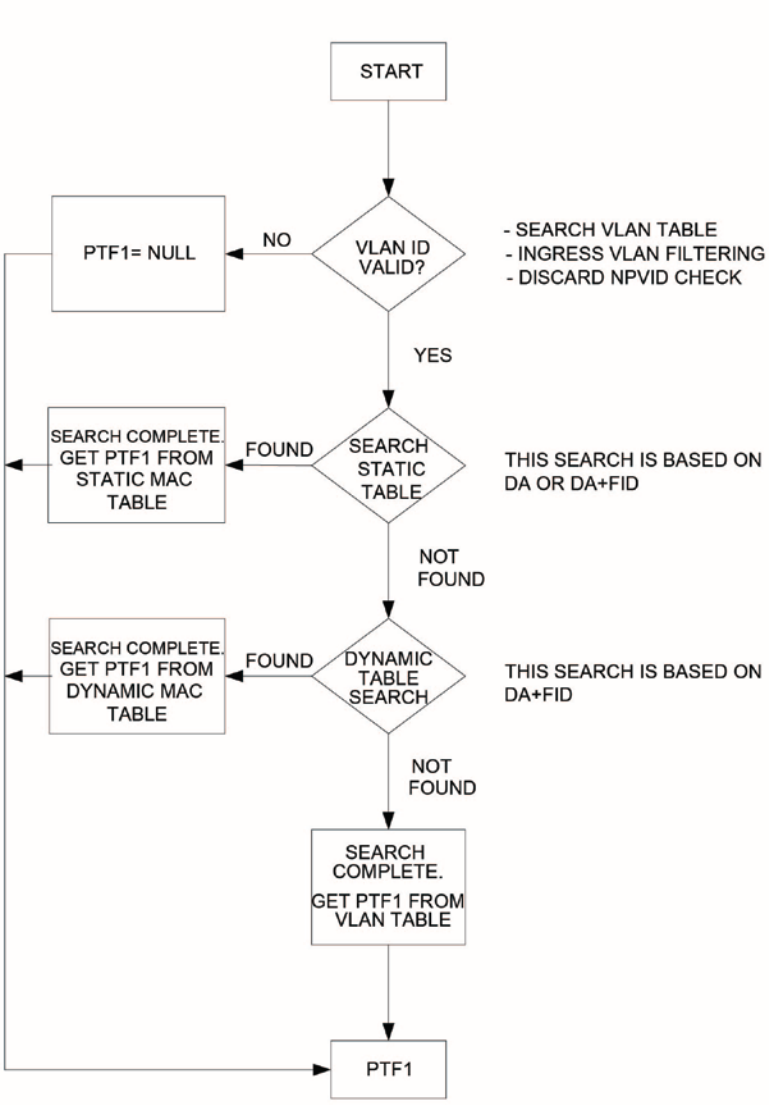


Figure 10. Destination Address Lookup Flow Chart, Stage 1

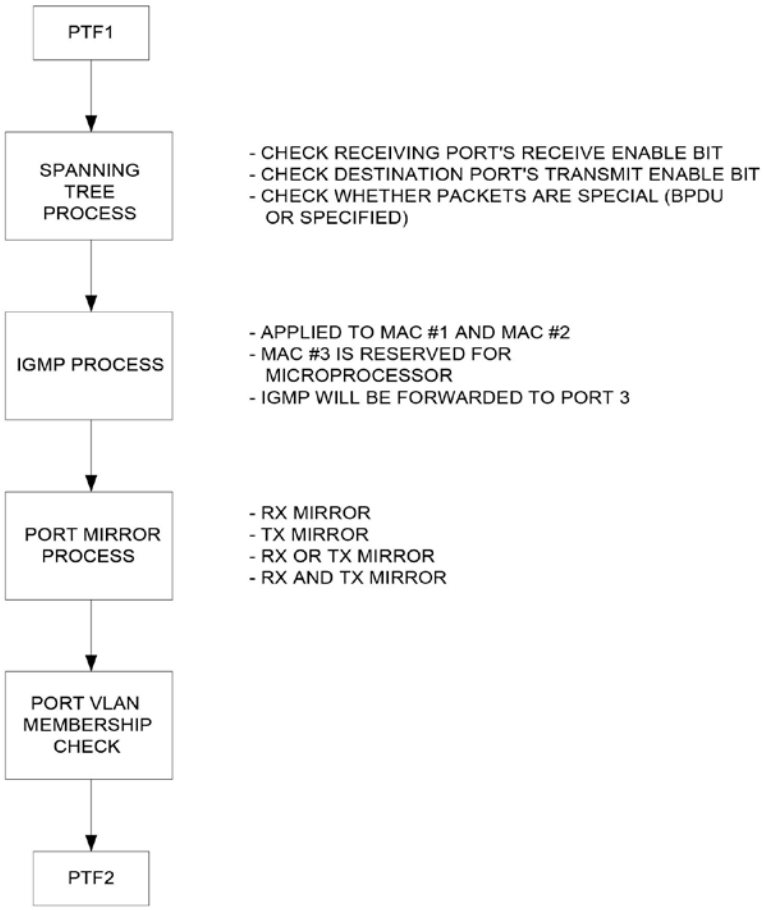


Figure 11. Destination Address Resolution Flow Chart, Stage 2

The KSZ8895MQX/RQX/FQX/ML will not forward the following packets:

1. Error packets

These include framing errors, Frame Check Sequence (FCS) errors, alignment errors, and illegal size packet errors.

2. IEEE802.3x PAUSE frames

KSZ8895MQX/RQX/FQX/ML intercepts these packets and performs full duplex flow control accordingly.

3. "Local" packets

Based on destination address (DA) lookup, if the destination port from the lookup table matches the port from which the packet originated, the packet is defined as "local."

Half-Duplex Back Pressure

The KSZ8895MQX/RQX/FQX/ML also provides a half-duplex back pressure option (note: this is not in IEEE 802.3 standards). The activation and deactivation conditions are the same as the ones given for full-duplex mode. If back pressure is required, the KSZ8895MQX/RQX/FQX/ML sends preambles to defer the other station's transmission (carrier sense deference). To avoid jabber and excessive deference as defined in IEEE 802.3 standards, after a certain period of time, the KSZ8895MQX/RQX/FQX/ML discontinues carrier sense but raises it quickly after it drops packets to inhibit other transmissions. This short silent time (no carrier sense) is to prevent other stations from sending out packets and keeps other stations in a carrier sense-deferred state. If the port has packets to send during a back pressure situation, the carrier sense-type back pressure is interrupted and those packets are transmitted instead. If there are no more packets to send, carrier sense-type back pressure becomes active again until switch resources are free. If a collision occurs, the binary exponential backoff algorithm is skipped and carrier sense is generated immediately, reducing the chance of further colliding and maintaining carrier sense to prevent reception of packets. To ensure no packet loss in 10BASE-T or 100BASE-TX half-duplex modes, the user must enable the following:

- Aggressive backoff (Register 3, bit 0)
- No excessive collision drop (Register 4, bit 3)
- Back pressure (Register 4, bit 5)

These bits are not set as the default because this is not the IEEE standard.

Broadcast Storm Protection

The KSZ8895MQX/RQX/FQX/ML has an intelligent option to protect the switch system from receiving too many broadcast packets. Broadcast packets are normally forwarded to all ports except the source port and thus use too many switch resources (bandwidth and available space in transmit queues). The KSZ8895MQX/RQX/FQX/ML has the option to include “multicast packets” for storm control. The broadcast storm rate parameters are programmed globally and can be enabled or disabled on a per port basis. The rate is based on a 50ms (0.05s) interval for 100BT and a 500ms (0.5s) interval for 10BT. At the beginning of each interval, the counter is cleared to zero and the rate limit mechanism starts to count the number of bytes during the interval. The rate definition is described in Registers 6 and 7. The default setting for Registers 6 and 7 is 0x4A (74 decimal). This is equal to a rate of 1%, calculated as follows:

148,80 frames/sec X 50ms (0.05s)/interval X 1% = 74 frames/interval (approx.) = 0x4A

MII Interface Operation

The media-independent interface (MII) is specified by the IEEE 802.3 committee and provides a common interface between physical layer and MAC layer devices. The KSZ8895MQX/RQX/FQX/ML provides two such interfaces. The P5-MII interface is used to connect to the fifth PHY, where as the SW-MII interface is used to connect to the fifth MAC. Each of these MII interfaces contains two distinct groups of signals, one for transmission and the other for receiving.

Port 5 PHY 5 P5-MII/RMII Interface

The media independent interface (MII) is specified by the IEEE 802.3 committee and provides a common interface between the physical layer and MAC layer devices. The Reduced Media Independent Interface (RMII) specifies a low pin count MII. The KSZ8895MQX/RQX/FQX/ML provides two such interfaces for MAC5 and PHY5. The Port 5 PHY5 P5-MII/RMII interface is used to connect to the fifth PHY, where as the SW-MII/RMII interface is used to connect to the fifth MAC. The KSZ8895MQX/FQX/ML support P5-MII, the KSZ8895RQX supports P5-RMII. Each of these MII/RMII interfaces contains two distinct groups of signals, one for transmission and the other for receiving. Table 4 describes the signals used in the PHY [5] P5-MII/RMII interface. The P5-MII interface operates in PHY mode only.

Table 4. Port 5 PHY P5-MII/RMII Signals

MII Signal	Description	KSZ8895MQX/FQX/ML P5-MII	KSZ8895MQX/FQX/ML MII Signal Type	KSZ8895RQX P5-RMII	KSZ8895RQX RMII Signal Type
MTXEN	Transmit enable	PMTXEN	I	PMTXEN	I
MTXER	Transmit error	PMTXER	I		
MTXD3	Transmit data bit 3	PMTXD[3]	I		
MTXD2	Transmit data bit 2	PMTXD[2]	I		
MTXD1	Transmit data bit 1	PMTXD[1]	I	PMTXD[1]	I
MTXD0	Transmit data bit 0	PMTXD[0]	I	PMTXD[0]	I
MTXC	Transmit clock	PMTXC	O	PMREFCLK/PMTXC	I
MCOL	Collision detection	PCOL	O		
MCRS	Carrier sense	PCRS	O		
MRXDV	Receive data valid	PMRXDV	O	PMRXDV	O
MRXER	Receive error	PMRXER	O	PMRXER	O
MRXD3	Receive data bit 3	PMRXD[3]	O		
MRXD2	Receive data bit 2	PMRXD[2]	O		
MRXD1	Receive data bit 1	PMRXD[1]	O	PMRXD[1]	O
MRXD0	Receive data bit 0	PMRXD[0]	O	PMRXD[0]	O
MRXC	Receive clock	PMRXC	O	PMRXC	O

Port 5 MAC 5 SW5-MII Interface for the KSZ8895MQX/FQX/ML

Table 5 shows two connection manners:

- The first is an external MAC connects to SW5-MII PHY mode.
- The second is an external PHY connects to SW5-MII MAC mode.

Please see the pin [91, 86, 87] descriptions for configuration details for the MAC mode and PHY mode. SW5-MII works with 25MHz clock for 100Base-TX, SW5-MII works with 2.5MHz clock for 10Base-T.

Table 5. Switch MAC5 MII Signals

KSZ8895MQX/FQX/ML PHY Mode Connection				KSZ8895MQX/FQX/ML MAC Mode Connection		
External MAC	**KSZ8895MQX/FQX/ML SW5-MII Signals**	**Type**	**Description**	**External PHY**	**KSZ8895MQX/FQX/ML SW5-MII Signals**	**Type**
MTXEN	SMTXEN	Input	Transmit enable	MTXEN	SMRXDV	Output
MTXER	SMTXER	Input	Transmit error	MTXER	Not used	Not used
MTXD3	SMTXD[3]	Input	Transmit data bit 3	MTXD3	SMRXD[3]	Output
MTXD2	SMTXD[2]	Input	Transmit data bit 2	MTXD2	SMRXD[2]	Output
MTXD1	SMTXD[1]	Input	Transmit data bit 1	MTXD1	SMRXD[1]	Output
MTXD0	SMTXD[0]	Input	Transmit data bit 0	MTXD0	SMRXD[0]	Output
MTXC	SMTXC	Output	Transmit clock	MTXC	SMRXC	Input
MCOL	SCOL	Output	Collision detection	MCOL	SCOL	Input
MCRS	SCRS	Output	Carrier sense	MCRS	SCRS	Input
MRXDV	SMRXDV	Output	Receive data valid	MRXDV	SMTXEN	Input
MRXER	Not used	Output	Receive error	MRXER	SMTXER	Input
MRXD3	SMRXD[3]	Output	Receive data bit 3	MRXD3	SMTXD[3]	Input
MRXD2	SMRXD[2]	Output	Receive data bit 2	MRXD2	SMTXD[2]	Input
MRXD1	SMRXD[1]	Output	Receive data bit 1	MRXD1	SMTXD[1]	Input
MRXD0	SMRXD[0]	Output	Receive data bit 0	MRXD0	SMTXD[0]	Input
MRXC	SMRXC	Output	Receive clock	MRXC	SMTXC	Input

The switch MII interface operates in either MAC mode or PHY mode for KSZ8895MQX/FQX/ML. These interfaces are nibble-wide data interfaces, so they run at one-quarter the network bit rate (not encoded). Additional signals on the transmit side indicate when data is valid or when an error occurs during transmission. Likewise, the receive side has indicators that convey when the data is valid and without physical layer errors. For half-duplex operation, there is a signal that indicates a collision has occurred during transmission.

Note that the signal MRXER is not provided on the MII-SW interface for PHY mode operation and the signal MTXER is not provided on the SW-MII interface for MAC mode operation. Normally MRXER would indicate a receive error coming from the physical layer device. MTXER would indicate a transmit error from the MAC device. These signals are not appropriate for this configuration. For PHY mode operation with an external MAC, if the device interfacing with the KSZ8895MQX/FQX/ML has an MRXER pin, it should be tied low. For MAC mode operation with an external PHY, if the device interfacing with the KSZ8895MQX/FQX/ML has an MTXER pin, it should be tied low.

Port 5 MAC 5 Switch SW5-RMII Interface for the KSZ8895RQX

The Reduced Media Independent Interface (RMII) specifies a low pin count Media Independent Interface (MII). The KSZ8895RQX supports RMII interface at Port 5 switch side and provides a common interface at MAC5 layer in the device, and has the following key characteristics:

- Supports 10Mbps and 100Mbps data rates.
- Uses a single 50MHz clock reference (provided internally or externally): in internal mode, the chip provides a reference clock from the SMRXC pin to the SMTXC pin and provides the clock to the opposite clock input pin for RMII interface. In external mode, the chip receives 50MHz reference clock from an external oscillator or opposite RMII interface.
- Provides independent 2-bit wide (bi-bit) transmit and receive data paths.

KSZ8895RQX supports MAC5 RMII interfaces at the switch side:

- For the detail of SW5-RMII (Port 5 MAC5 RMII) signals connection see the table below:
- The KSZ8895RQX can provide a 50MHz reference clock for both MAC to MAC and MAC to PHY RMII interfaces when SW5-RMII is used in the clock mode of the device (default with strap pin LED2_2 internal pull-up for the clock mode).
- The KSZ8895RQX can also receive a 50MHz reference clock from an external 50MHz clock source or opposite RMII to SW5-RMII SMTXC pin when the device is set to normal mode (the strap pin LED2_2 is pulled down).

When the device is strapped to normal mode by pin LED2_2 pull-down, the reference clock comes from SMTXC which will be used as the device's clock source. The external 25MHz crystal clock from pins X1/X2 will be ignored.

Note: In normal mode, the 50MHz clock from SMTXC will be used as the clock source for whole device. The PHY5 PMTXC/PMREFCLK pin can't be used as the clock source for whole device. The pin of PMTXC/PMREFCLK can receive the 50MHz clock from PMRXC when the device is strapped to normal mode and an external 50MHz reference clock comes in from pin SMTXC. In normal mode, the 50MHz clock on pin SMRXC can be disabled by register, and the PMRXC 50MHz clock can be used when P5-RMII interface is used.

There is a Register 12 bit 6 to monitor the status of the device for the clock mode or normal mode.

When using an external 50MHz clock source as RMII reference clock, the KSZ8895RQX should be set to normal mode by pulling down its LED2_2 strap-in pin first before power up reset or warm reset. The normal mode of the KSZ8895RQX device will start to work when it gets the 50MHz reference clock from pin SMTXC/SMREFCLK from an external 50MHz clock source. For the RMII connection examples, please refer to the application note included in the design kit.

Table 6. Port 5 MAC5 SW5-RMII Connection

SW5-RMII MAC to MAC Connection ('PHY mode')				SW5-RMII MAC to PHY Connection ('MAC mode')		
External MAC	**KSZ8895RQX SW5-RMII**	**KSZ8895RQX SW Signal Type**	**Description**	**External PHY**	**KSZ8895RQX SW5-RMII**	**KSZ8895RQX SW Signal Type**
REF_CLK	xSMRXC	Output (clock mode with 50MHz) (Normal mode without connection)	Reference Clock	--------	SMTXC/SM REFCLK	Input (clock comes from SMRXC in clock mode or external clock in normal mode)
CRS_DV	SMRXDV /SMCRSDV	Output	Carier sense/Receive data valid	CRS_DV	SMTXEN	Input
RXD1	SMRXD[1]	Output	Receive data bit 1	RXD1	SMTXD[1]	Input
RXD0	SMRXD[0]	Output	Receive data bit 0	RXD0	SMTXD[0]	Input
TX_EN	SMTXEN	Input	Transmit data enable	TX_EN	SMRXDV /SMCRSDV	Output
TXD1	SMTXD[1]	Input	Transmit data bit 1	TXD1	SMRXD[1]	Output
TXD0	SMTXD[0]	Input	Transmit data bit 0	TXD0	SMRXD[0]	Output
(not used)	(not used)		Receive error	(not used)	(not used)	
---	SMTXC/SM REFCLK	Input (clock comes from SMRXC in clock mode or external clock in normal mode)	Reference Clock	REF_CLK	SMRXC	Output (clock mode with 50MHz) (Normal mode without connection)

Note:

5. MAC/PHY mode in RMII is difference with MAC/PHY mode in MII, there is no strap pin and register configuration request in RMII, just follow the signals connection in the table.

SNI Interface Operation

The serial network interface (SNI) is compatible with some controllers used for network layer protocol processing. This interface can be directly connected to these types of devices. The signals are divided into two groups, one for transmission and the other for reception. The signals involved are described in Table 7.

Table 7. SNI Signals

SNI Signal	Description	KSZ8895MQX/RQX/FQX/ML Signal
TXEN	Transmit Enable	SMTXEN
TXD	Serial Transmit Data	SMTXD[0]
TXC	Transmit Clock	SMTXC
COL	Collision Detection	SCOL
CRS	Carrier Sense	SMRXDV
RXD	Serial Receive Data	SMRXD[0]
RXC	Receive Clock	SMRXC

This interface is a bit-wide data interface, so it runs at the network bit rate (not encoded). An additional signal on the transmit side indicates when data is valid. Likewise, the receive side has an indicator that shows when the data is valid.

For half-duplex operation there is a signal that indicates a collision has occurred during transmission.

Advanced Functionality

QoS Priority Support

The KSZ8895MQX/RQX/FQX/ML provides Quality of Service (QoS) for applications such as VoIP and video conferencing. The KSZ8895MQX/RQX/FQX/ML offers one, two, or four priority queues per port by setting the Registers port control 9 bit 1 and the Registers port control 0 bit 0, the 1/2/4 queues split as follows:

- [Registers port control 9 bit 1, control 0 bit 0] = 00 single output queue as default.
- [Registers port control 9 bit 1, control 0 bit 0] = 01 egress port can be split into two priority transmit queues.
- [Registers port control 9 bit 1, control 0 bit 0] = 10 egress port can be split into four priority transmit queues.

The four priority transmit queue is a new feature in the KSZ8895MQX/RQX/FQX/ML. The queue 3 is the highest priority queue and queue 0 is the lowest priority queue. The port Registers xxx control 9 bit 1 and the Registers port control 0 bit 0 are used to enable split transmit queues for ports 1, 2, 3, 4 and 5, respectively. If a port's transmit queue is not split, high priority and low priority packets have equal priority in the transmit queue.

There is an additional option to either always deliver high priority packets first or to use programmable weighted fair queuing for the four priority queue scale by the Registers Port Control 10, 11, 12 and 13 (default value are 8, 4, 2, 1 by their bit [6:0].

Register 130 bit [7:6] Prio_2Q[1:0] is used when the 2 Queue configuration is selected, these bits are used to map the 2-bit result of IEEE 802.1p from the Registers 128, 129 or TOS/DiffServ mapping from Registers 144-159 (for 4 Queues) into two-queue mode with priority high or low.

Please see the descriptions of the Register 130 bits [7:6] for detail.

Port-Based Priority

With port-based priority, each ingress port is individually classified as a priority 0-3 receiving port. All packets received at the priority 3 receiving port are marked as high priority and are sent to the high-priority transmit queue if the corresponding transmit queue is split. The Port Registers Control 0 bits [4:3] is used to enable port-based priority for ports 1, 2, 3, 4 and 5, respectively.

802.1p-Based Priority

For 802.1p-based priority, the KSZ8895MQX/RQX/FQX/ML examines the ingress (incoming) packets to determine whether they are tagged. If tagged, the 3-bit priority field in the VLAN tag is retrieved and compared against the “priority mapping” value, as specified by the Registers 128 and 129, both Register 128/129 can map 3-bit priority field of 0-7 value to 2-bit result of 0-3 priority levels. The “priority mapping” value is programmable.

Figure 12 illustrates how the 802.1p priority field is embedded in the 802.1Q VLAN tag.

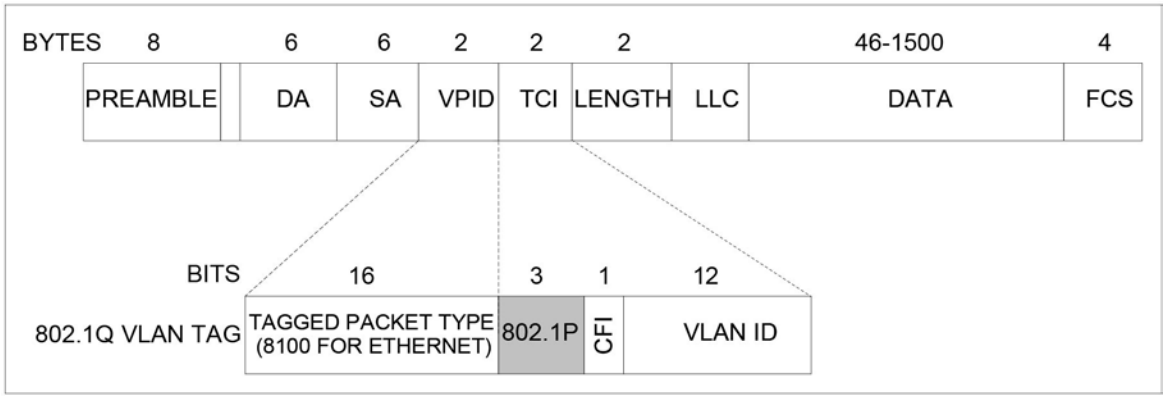


Figure 12. 802.1p Priority Field Format

802.1p-based priority is enabled by bit [5] of the Registers Port Control 0 for ports 1, 2, 3, 4 and 5, respectively.

The KSZ8895MQX/RQX/FQX/ML provides the option to insert or remove the priority tagged frame's header at each individual egress port. This header, consisting of the two-byte VLAN Protocol ID (VPID) and the two-byte Tag Control Information field (TCI), is also referred to as the IEEE 802.1Q VLAN tag.

Tag Insertion is enabled by bit [2] of the Registers Port Control 0 and the Register Port Control 8 to select which source port (ingress port) PVID can be inserted on the egress port for ports 1, 2, 3, 4 and 5, respectively. At the egress port, untagged packets are tagged with the ingress port's default tag. The default tags are programmed in the Registers Port Control 3 and control 4 for ports 1, 2, 3, 4 and 5, respectively. The KSZ8895MQX/RQX/FQX/ML will not add tags to already tagged packets.

Tag Removal is enabled by bit [1] of the Registers Port Control 0 for ports 1, 2, 3, 4 and 5, respectively. At the egress port, tagged packets will have their 802.1Q VLAN tags removed. The KSZ8895MQX/RQX/FQX/ML will not modify untagged packets.

The CRC is recalculated for both tag insertion and tag removal.

802.1p Priority Field Re-Mapping is a QoS feature that allows the KSZ8895MQX/RQX/FQX/ML to set the "User Priority Ceiling" at any ingress port by the Register Port Control 2 bit 7. If the ingress packet's priority field has a higher priority value than the default tag's priority field of the ingress port, the packet's priority field is replaced with the default tag's priority field.

DiffServ-Based Priority

DiffServ-based priority uses the ToS Registers (Registers 144 to 159) in the Advanced Control Registers section. The ToS priority control registers implement a fully decoded, 128-bit Differentiated Services Code Point (DSCP) register to determine packet priority from the 6-bit ToS field in the IP header. When the most significant six bits of the ToS field are fully decoded, 64 code points for DSCP result. These are compared with the corresponding bits in the DSCP register to determine priority.

Spanning Tree Support

Port 5 is the designated port for spanning tree support.

The other ports (Port 1 – Port 4) can be configured in one of the five spanning tree states via "transmit enable," "receive enable," and "learning disable" register settings in Registers 18, 34, 50, and 66 for Ports 1, 2, 3, and 4, respectively. The following description shows the port setting and software actions taken for each of the five spanning tree states.

Disable state: the port should not forward or receive any packets. Learning is disabled.

Port setting: "transmit enable = 0, receive enable = 0, learning disable = 1."

Software action: the processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the static table with "overriding bit" set) and the processor should discard those packets. Note: the processor is connected to Port 5 via MII interface. Address learning is disabled on the port in this state.

Blocking state: only packets to the processor are forwarded. Learning is disabled.

Port setting: "transmit enable = 0, receive enable = 0, learning disable = 1"

Software action: the processor should not send any packets to the port(s) in this state. The processor should program the "Static MAC table" with the entries that it needs to receive (e.g., BPDU packets). The "overriding" bit should also be set so that the switch will forward those specific packets to the processor. Address learning is disabled on the port in this state.

Listening state: only packets to and from the processor are forwarded. Learning is disabled.

Port setting: "transmit enable = 0, receive enable = 0, learning disable = 1.

"Software action: The processor should program the static MAC table with the entries that it needs to receive (e.g. BPDU packets). The "overriding" bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state, see the "Tail Tagging Mode" sub-section for details. Address learning is disabled on the port in this state.

Learning state: only packets to and from the processor are forwarded. Learning is enabled.

Port setting: “transmit enable = 0, receive enable = 0, learning disable = 0.”

Software action: The processor should program the static MAC table with the entries that it needs to receive (e.g., BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state, see “Tail Tagging Mode” section for details. Address learning is enabled on the port in this state.

Forwarding state: packets are forwarded and received normally. Learning is enabled.

Port setting: “transmit enable = 1, receive enable = 1, learning disable = 0.”

Software action: The processor should program the static MAC table with the entries that it needs to receive (e.g., BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state, see “Tail Tagging Mode” section for details. Address learning is enabled on the port in this state.

Rapid Spanning Tree Support

There are three operational states of Discarding, Learning, and Forwarding assigned to each port for RSTP:

Discarding ports do not participate in the active topology and do not learn MAC addresses.

Discarding state: the state includes three states of the disable, blocking and listening of STP.

Port setting: "transmit enable = 0, receive enable = 0, learning disable = 1."

Software action: the processor should not send any packets to the port. The switch may still send specific packets to the processor (packets that match some entries in the static table with “overriding bit” set) and the processor should discard those packets. When disabling the port’s learning capability (learning disable = ’1’), set the Register 1 bit 5 and bit 4 will flush rapidly with the port related entries in the dynamic MAC table and static MAC table.

Note:

The processor is connected to Port 5 via MII interface. Address learning is disabled on the port in this state.

Ports in Learning states learn MAC addresses, but do not forward user traffic.

Learning state: only packets to and from the processor are forwarded. Learning is enabled.

Port setting: “transmit enable = 0, receive enable = 0, learning disable = 0.”

Software action: The processor should program the static MAC table with the entries that it needs to receive (e.g., BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state, see “Tail Tagging Mode” section for details. Address learning is enabled on the port in this state.

Ports in Forwarding states fully participate in both data forwarding and MAC learning.

Forwarding state: packets are forwarded and received normally. Learning is enabled.

Port setting: “transmit enable = 1, receive enable = 1, learning disable = 0.”

Software action: The processor should program the static MAC table with the entries that it needs to receive (e.g., BPDU packets). The “overriding” bit should be set so that the switch will forward those specific packets to the processor. The processor may send packets to the port(s) in this state, see “Tail Tagging Mode” section for details. Address learning is enabled on the port in this state.

RSTP uses only one type of BPDU called RSTP BPDUs. They are similar to STP Configuration BPDUs with the exception of a type field set to “version 2” for RSTP and “version 0” for STP, and a flag field carrying additional information.

Tail Tagging Mode

The Tail Tag is only seen and used by the Port 5 interface, which should be connected to a processor by SW5-MII/RMII interface. The one byte tail tagging is used to indicate the source/destination port in Port 5. Only bit [3-0] are used for the destination in the tail tagging byte. Other bits are not used. The Tail Tag feature is enabled by setting Register 12 bit 1.

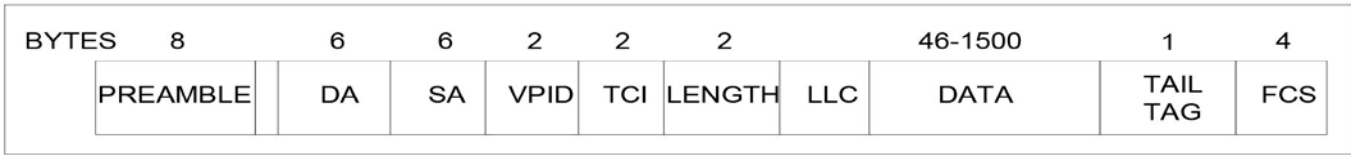


Figure 13. Tail Tag Frame Format

Table 8. Tail Tag Rules

Ingress to Port 5 (Host --> KSZ8895MQX/RQX/FQX/ML)	
Bit [3:0]	Destination
0,0,0,0	Reserved
0,0,0,1	Port 1 (direct forward to Port1)
0,0,1,0	Port 2 (direct forward to Port2)
0,1,0,0	Port 3 (direct forward to Port3)
1,0,0,0	Port 4 (direct forward to Port4)
1,1,1,1	Port 1, 2,3 and 4 (direct forward to Port 1,2,3,4,)
Bit[7:4]	
0,0,0,0	Queue 0 is used at destination port
0,0,0,1	Queue 1 is used at destination port
0,0,1,0	Queue 2 is used at destination port
0,0,1,1	Queue 3 is used at destination port
x, 1,x,x	Anyhow send packets to specified port in bit [3:0]
1, x,x,x	Bit[6:0] will be ignored as normal (Address look-up)
Egress from Port 5 (KSZ8895MQX/RQX/FQX/ML --> Host)	
Bit [1:0]	Source
0,0	Port 1 (packets from Port 1)
0,1	Port 2 (packets from Port 2)
1,0	Port 3 (packets from Port 3)
1,1	Port 4 (packets from Port 4)

IGMP Support

There are two parts involved to support the Internet Group Management Protocol (IGMP) in Layer 2. The first part is IGMP snooping, the second part is this IGMP packet to be sent back to the subscribed port. Describe them as follows.

IGMP Snooping

The KSZ8895MQX/RQX/FQX/ML traps IGMP packets and forwards them only to the processor (Port 5 SW5-MII/RMII). The IGMP packets are identified as IP packets (either Ethernet IP packets, or IEEE 802.3 SNAP IP packets) with IP version = 0x4 and protocol version number = 0x2. Set Register 5 bit [6] to '1' to enable IGMP snooping.

IGMP Send Back to the Subscribed Port

Once the host responds the received IGMP packet, the host should know the original IGMP ingress port and send back the IGMP packet to this port only; otherwise this IGMP packet will be broadcasted to all port to downgrade the performance.

Enable the tail tag mode, the host will know the IGMP packet received port from tail tag bits [1:0] and can send back the response IGMP packet to this subscribed port by setting the bits [3:0] in the tail tag. Enable "Tail tag mode" by setting Register 12 bit 1.

Port Mirroring Support

The KSZ8895MQX/RQX/FQX/ML supports "port mirror" comprehensively as:

"Receive Only" Mirror on a Port

All the packets received on the port will be mirrored on the sniffer port. For example, Port 1 is programmed to be "rx sniff," and Port 5 is programmed to be the "sniffer port." A packet, received on Port 1, is destined to Port 4 after the internal look-up. The KSZ8895MQX/RQX/FQX/ML will forward the packet to both Port 4 and Port 5. KSZ8895MQX/RQX/FQX/ML can optionally forward even "bad" received packets to Port 5.

"Transmit Only" Mirror on a Port

All the packets transmitted on the port will be mirrored on the sniffer port. For example, Port 1 is programmed to be "tx sniff," and Port 5 is programmed to be the "sniffer port." A packet, received on any of the ports, is destined to Port 1 after the internal look-up. The KSZ8895MQX/RQX/FQX/ML will forward the packet to both Ports 1 and 5.

"Receive and Transmit" Mirror on Two Ports

All the packets received on port A AND transmitted on port B will be mirrored on the sniffer port. To turn on the "AND" feature, set Register 5 bit 0 to 1. For example, Port 1 is programmed to be "rx sniff," Port 2 is programmed to be "transmit sniff," and Port 5 is programmed to be the "sniffer port." A packet, received on Port 1, is destined to Port 4 after the internal look-up. The KSZ8895MQX/RQX/FQX/ML will forward the packet to Port 4 only, since it does not meet the "AND" condition. A packet, received on Port 1, is destined to Port 2 after the internal look-up. The KSZ8895MQX/RQX/FQX/ML will forward the packet to both Port 2 and Port 5.

Multiple ports can be selected to be "rx sniffed" or "tx sniffed." And any port can be selected to be the "sniffer port." All these per port features can be selected through Register 17.

VLAN Support

The KSZ8895MQX/RQX/FQX/ML supports 128 active VLANs and 4096 possible VIDs specified in IEEE 802.1q. KSZ8895MQX/RQX/FQX/ML provides a 128-entry VLAN table, which correspond to 4096 possible VIDs and converts to FID (7 bits) for address look-up max 128 active VLANs. If a non-tagged or null-VID-tagged packet is received, then the ingress port VID is used for look-up when 802.1q is enabled by the global Register 5 control 3 bit 7. In the VLAN mode, the look-up process starts from VLAN table look-up to determine whether the VID is valid. If the VID is not valid, the packet will then be dropped and its address will not be learned. If the VID is valid, FID is retrieved for further look-up by the static MAC table or dynamic MAC table. FID+DA is used to determine the destination port. Table 9 describes the different actions in different situations of DA and FID+DA in the static MAC table and dynamic MAC table after the VLAN table finish a look-up action. FID+SA is used for learning purposes. Table 10 also describes learning in the dynamic MAC table when the VLAN table has done a look-up in the static MAC table without a valid entry.

Table 9. FID+DA Look-Up in the VLAN Mode

DA found in Static MAC table	USE FID Flag?	FID Match?	DA+FID found in Dynamic MAC table	Action
No	Do Not care	Do Not care	No	Broadcast to the membership ports defined in the VLAN table bit [11:7].
No	Do Not care	Do Not care	Yes	Send to the destination port defined in the dynamic MAC table bit [58:56].
Yes	0	Do Not care	Do Not care	Send to the destination port(s) defined in the static MAC table bit [52:48].
Yes	1	No	No	Broadcast to the membership ports defined in the VLAN table bit [11:7].
Yes	1	No	Yes	Send to the destination port defined in the dynamic MAC table bit [58:56].
Yes	1	Yes	Do Not care	Send to the destination port(s) defined in the static MAC table bit [52:48].

Table 10. FID+SA Look-Up in the VLAN Mode

SA+FID found in Dynamic MAC table	Action
No	The SA+FID will be learned into the dynamic table.
Yes	Time stamp will be updated.

Advanced VLAN features are also supported in KSZ8895MQX/RQX/FQX/ML, such as “VLAN ingress filtering” and “discard non PVID” defined in bits [6:5] of the port Register Control 2. These features can be controlled on a port basis.

Rate Limiting Support

The KSZ8895MQX/RQX/FQX/ML provides a fine resolution hardware rate limiting. The rate step is 64Kbps when the rate limit is less than 1Mbps rate for 100BT or 10BT. The rate step is 1Mbps when the rate limit is more than 1Mbps rate for 100BT or 10BT (refer to Data Rate Selection Table which follow the end of the Port Register Queue 0-3 Ingress/Egress Limit Control section). The rate limit is independently on the “receive side” and on the “transmit side” on a per port basis. For 10BASE-T, a rate setting above 10 Mbps means the rate is not limited. On the receive side, the data receive rate for each priority at each port can be limited by setting up Ingress Rate Control Registers. On the transmit side, the data transmit rate for each priority queue at each port can be limited by setting up Egress Rate Control Registers. The size of each frame has options to include minimum IFG (Inter Frame Gap) or Preamble byte, in addition to the data field (from packet DA to FCS).

Ingress Rate Limit

For ingress rate limiting, KSZ8895MQX/RQX/FQX/ML provides options to selectively choose frames from all types, multicast, broadcast, and flooded unicast frames by bits [3-2] of the port rate limit control register. The KSZ8895MQX/RQX/FQX/ML counts the data rate from those selected type of frames. Packets are dropped at the ingress port when the data rate exceeds the specified rate limit or the flow control takes effect without packet dropped when the ingress rate limit flow control is enabled by the port rate limit control register bit 4. The ingress rate limiting supports the port-based, 802.1p and DiffServ-based priorities, the port-based priority is fixed priority 0-3 selection by bits [4-3] of the Register Port Control 0. The 802.1p and DiffServ-based priority can be mapped to priority 0-3 by default of the Register 128 and 129. In the ingress rate limit, set Register 135 global control 19 bit 3 to enable queue-based rate limit if using two-queue or four-queue mode. All related ingress ports and egress port should be split to two-queue or four-queue mode by the Registers Port Control 9 and control 0. The four-queue mode will use Q0-Q3 for priority 0-3 by bit [6-0] of the port Register ingress limit control 1-4. The two-queue mode will use Q0-Q1 for priority 0-1by bit [6-0] of the port Register ingress limit control 1-2. The priority levels in the packets of the 802.1p and DiffServ can be programmed to priority 0-3 by the Register 128 and 129 for a re-mapping.

Egress Rate Limit

For egress rate limiting, the Leaky Bucket algorithm is applied to each output priority queue for shaping output traffic. Interframe gap is stretched on a per frame base to generate smooth, non-burst egress traffic. The throughput of each output priority queue is limited by the egress rate specified by the data rate selection table followed the egress rate limit control registers.

If any egress queue receives more traffic than the specified egress rate throughput, packets may be accumulated in the output queue and packet memory. After the memory of the queue or the port is used up, packet dropping or flow control will be triggered. As a result of congestion, the actual egress rate may be dominated by flow control/dropping at the ingress end, and may be therefore slightly less than the specified egress rate. The egress rate limiting supports the port-based, 802.1p and DiffServ-based priorities, the port-based priority is fixed priority 0-3 selection by bits [4-3] of the Register Port Control 0. The 802.1p and DiffServ-based priority can be mapped to priority 0-3 by default of the Register 128 and 129. In the egress rate limit, set Register 135 global control 19 bit 3 for queue-based rate limit to be enabled if using two-queue or four-queue mode. All related ingress ports and egress port should be split to two-queue or four-queue mode by the Registers Port Control 9 and control 0. The four-queue mode will use Q0-Q3 for priority 0-3 by bit [6-0] of the port Register egress limit control 1-4. The two-queue mode will use Q0-Q1 for priority 0-1by bit [6-0] of the port Register egress limit control 1-2. The priority levels in the packets of the 802.1p and DiffServ can be programmed to priority 0-3 by the Register 128 and 129 for a re-mapping.

When the egress rate is limited, just use one queue per port for the egress port rate limit. The priority packets will be based upon the data rate selection table (see Tables 13 and 14). If the egress rate limit uses more than one queue per port for the egress port rate limit, then the highest priority packets will be based upon the data rate selection table for the rate limit exact number. Other lower priority packet rates will be limited based upon 8:4:2:1 (default) priority ratio, which is based on the highest priority rate. The transmit queue priority ratio is programmable.

To reduce congestion, it is good practice to make sure the egress bandwidth exceeds the ingress bandwidth.

Transmit Queue Ratio Programming

In transmit queues 0-3 of the egress port, the default priority ratio is 8:4:2:1. The priority ratio can be programmed by the Registers Port Control 10, 11, 12 and 13. When the transmit rate exceeds the ratio limit in the transmit queue, the transmit rate will be limited by the transmit queue 0-3 ratio of the Register Port Control 10, 11, 12 and 13. The highest priority queue will not be limited. Other lower priority queues will be limited based on the transmit queue ratio.

Filtering for Self-Address, Unknown Unicast/Multicast Address and Unknown VID Packet/IP Multicast

Enable Self-address filtering, the unknown unicast packet filtering and forwarding by the Register 131 Global Control 15. Enable Unknown multicast packet filtering and forwarding by the Register 132 Global Control 16.

Enable Unknown VID packet filtering and forwarding by the Register 133 Global Control 17.

Enable Unknown IP multicast packet filtering and forwarding by the Register 134 Global Control 18.

This function is very useful in preventing packets that could degrade the quality of the port in applications such as voice over Internet Protocol (VoIP) and the daisy chain connection.

Configuration Interface

I²C Master Serial Bus Configuration

If a 2-wire EEPROM exists, then the KSZ8895MQX/RQX/FQX/ML can perform more advanced features like broadcast storm protection and rate control. The EEPROM should have the entire valid configuration data from Register 0 to Register 255 defined in the "Memory Map," except the chipID = 0 in the Register1 and the status registers. After reset, the KSZ8895MQX/RQX/FQX/ML will start to read all 255 registers sequentially from the EEPROM. The configuration access time (t_{prgm}) is less than 30ms, as shown in Figure 14.

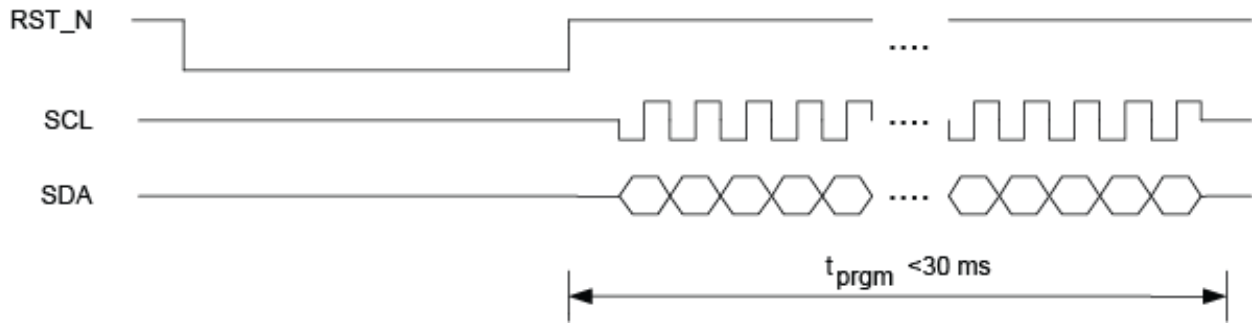


Figure 14. KSZ8895MQX/RQX/FQX/ML EEPROM Configuration Timing Diagram

To configure the KSZ8895MQX/RQX/FQX/ML with a pre-configured EEPROM use the following steps:

1. At the board level, connect Pin 110 on the KSZ8895MQX/RQX/FQX/ML to the SCL pin on the EEPROM. Connect Pin 111 on the KSZ8895MQX/RQX/FQX/ML to the SDA pin on the EEPROM.
2. A[2-0] address pins of EEPROM should be tied to ground for address A[2-0] = '000' to be identified by the KSZ8895MQX/RQX/FQX/ML.
3. Set the input signals PS[1:0] (pins 113 and 114, respectively) to "00." This puts the KSZ8895MQX/RQX/FQX/ML serial bus configuration into I2C master mode.
4. Be sure the board-level reset signal is connected to the KSZ8895MQX/RQX/FQX/ML reset signal on Pin115 (RST_N).
5. Program the contents of the EEPROM before placing it on the board with the desired configuration data. Note that the first byte in the EEPROM must be "95" for the loading to occur properly. If this value is not correct, all other data will be ignored.
6. Place EEPROM on the board and power up the board. Assert the active-low board level reset to RST_N on the KSZ8895MQX/RQX/FQX/ML. After the reset is de-asserted, the KSZ8895MQX/RQX/FQX/ML will begin reading configuration data from the EEPROM. The configuration access time (tprgm) is less than 30ms.

Note:

For proper operation, make sure that Pin47 (PWRDN_N) is not asserted during the reset operation.

SPI Slave Serial Bus Configuration

The KSZ8895MQX/RQX/FQX/ML can also act as a SPI slave device. Through the SPI, the entire feature set can be enabled, including “VLAN,” “IGMP snooping,” “MIB counters,” etc. The external master device can access any register from Register 0 to Register 255 randomly. The system should configure all the desired settings before enabling the switch in the KSZ8895MQX/RQX/FQX/ML. To enable the switch, write a "1" to Register 1 bit 0.

Two standard SPI commands are supported (00000011 for “READ DATA,” and 00000010 for “WRITE DATA”). To speed configuration time, the KSZ8895MQX/RQX/FQX/ML also supports multiple reads or writes. After a byte is written to or read from the KSZ8895MQX/RQX/FQX/ML, the internal address counter automatically increments if the SPI Slave Select Signal (SPIS_N) continues to be driven low. If SPIS_N is kept low after the first byte is read, the next byte at the next address will be shifted out on SPIQ. If SPIS_N is kept low after the first byte is written, bits on the Master Out Slave Input (SPID) line will be written to the next address. Asserting SPIS_N high terminates a read or write operation. This means that the SPIS_N signal must be asserted high and then low again before issuing another command and address. The address counter wraps back to zero once it reaches the highest address. Therefore the entire register set can be written to or read from by issuing a single command and address.

The default SPI clock speed is 12.5MHz. The KSZ8895MQX/RQX/FQX/ML is able to support a SPI bus up to 25MHz (set Register 12 bit [5:4] = 0x10). A high performance SPI master is recommended to prevent internal counter overflow.

To use the KSZ8895MQX/RQX/FQX/ML SPI:

1. At the board level, connect KSZ8895MQX/RQX/FQX/ML pins as follows:

Table 11. SPI Connections

KSZ8895MQX/RQX/FQX/ML Pin Number	KSZ8895MQX/RQX/FQX/ML Signal Name	Microprocessor Signal Description
112	SPIS_N	SPI Slave Select
110	SPIC	SPI Clock
111	SPID	Master Out Slave Input
109	SPIQ	Master In Slave Output

2. Set the input signals PS[1:0] (pins 113 and 114, respectively) to “10” to set the serial configuration to SPI slave mode.
3. Power up the board and assert a reset signal. After reset wait 100µs, the start switch bit in Register 1 will be set to ‘0’. Configure the desired settings in the KSZ8895MQX/RQX/FQX/ML before setting the start register to ‘1.'
4. Write configuration to registers using a typical SPI write data cycle as shown in Figure 15 or SPI multiple write as shown in Figure 17. Note that data input on SPID is registered on the rising edge of SPIC.
5. Registers can be read and configuration can be verified with a typical SPI read data cycle as shown in Figure 16 or a multiple read as shown in Figure 18. Note that read data is registered out of SPIQ on the falling edge of SPIC.
6. After configuration is written and verified, write a ‘1’ to Register 1 bit 0 to begin KSZ8895MQX/RQX/FQX/ML switch operation.

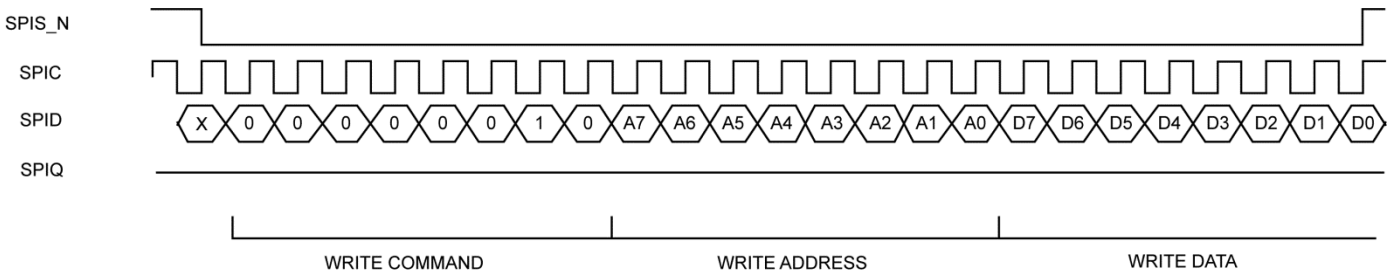


Figure 15. SPI Write Data Cycle

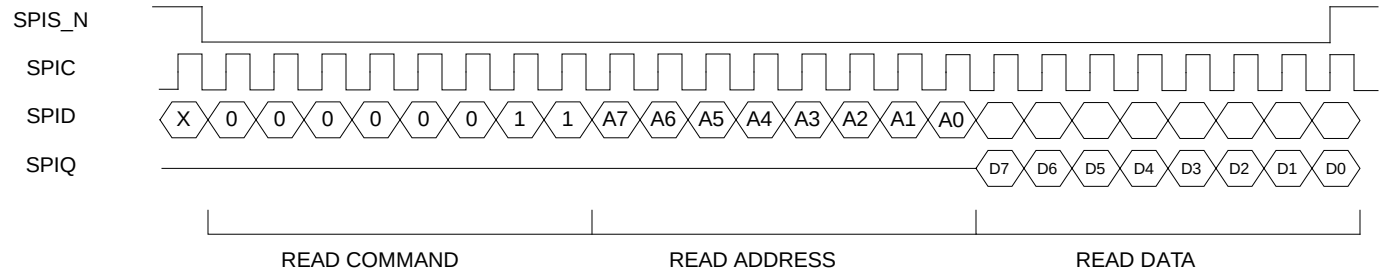


Figure 16. SPI Read Data Cycle

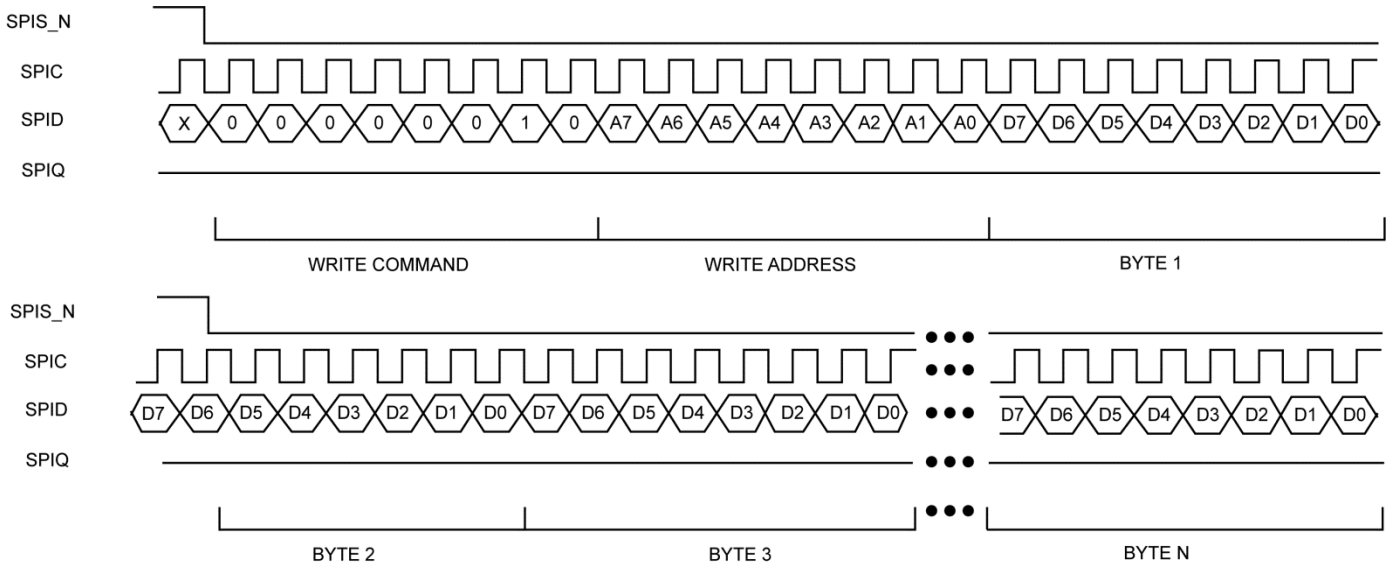


Figure 17. SPI Multiple Write

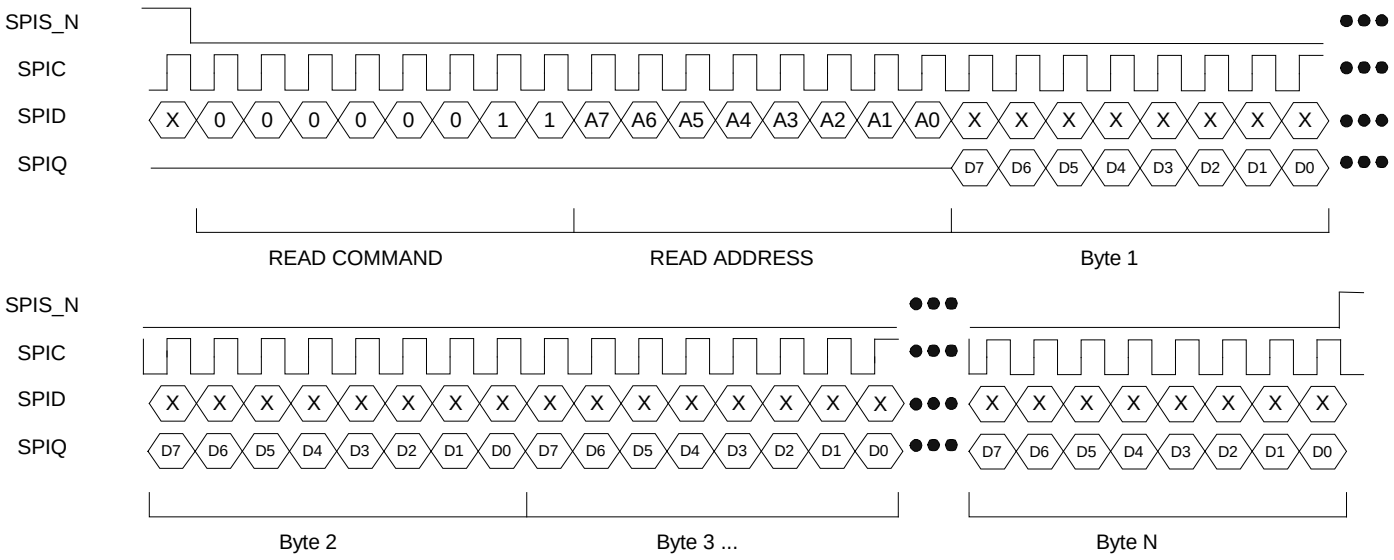


Figure 18. SPI Multiple Read

MII Management Interface (MIIM)

The KSZ8895MQX/RQX/FQX/ML supports the standard IEEE 802.3 MII Management Interface, also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the states of the KSZ8895MQX/RQX/FQX/ML. An external device with MDC/MDIO capability is used to read the PHY status or configure the PHY settings. Further details on the MIIM interface are found in Clause 22.2.4.5 of the IEEE 802.3u Specification.

The MIIM interface consists of the following:

- A physical connection that incorporates the data line (Pin108 MDIO) and the clock line (Pin107 MDC).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with the KSZ8895MQX/RQX/FQX/ML device.
- Access to a set of eight 16-bit registers, consisting of 8 standard MIIM Registers [0:5h], 1d and 1f MIIM registers per port.

The MIIM Interface can operate up to a maximum clock speed of 10MHz MDC clock.

Table 12 depicts the MII Management Interface frame format.

Table 12. MII Management Interface Frame Format

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits[4:0]	REG Address Bits[4:0]	TA	Data Bits[15:0]	Idle
Read	32 1's	01	10	AAAAA	RRRRR	Z0	DDDDDDDD_DDDDDDDD	Z
Write	32 1's	01	01	AAAAA	RRRRR	10	DDDDDDDD_DDDDDDDD	Z

The MIIM interface does not have access to all the configuration registers in the KSZ8895MQX/RQX/FQX/ML. It can only access the standard MIIM registers. See "MIIM Registers". The SPI interface and MDC/MDIO SMI mode, on the other hand, can be used to access all registers with the entire KSZ8895MQX/RQX/FQX/ML feature set.

Serial Management Interface (SMI)

The SMI is the KSZ8895MQX/RQX/FQX/ML non-standard MIIM interface that provides access to all KSZ8895MQX/RQX/FQX/ML configuration registers. This interface allows an external device with MDC/MDIO interface to completely monitor and control the states of the KSZ8895MQX/RQX/FQX/ML.

The SMI interface consists of the following:

- A physical connection that incorporates the data line (MDIO) and the clock line (MDC).
- A specific protocol that operates across the aforementioned physical connection that allows an external controller to communicate with the KSZ8895MQX/RQX/FQX/ML device.
- Access to all KSZ8895MQX/RQX/FQX/ML configuration registers. Register access includes the Global, Port and Advanced Control Registers 0-255 (0x00 – 0xFF), and indirect access to the standard MIIM Registers [0:5] and custom MIIM Registers [29, 31].

The SMI Interface can operate up to a maximum clock speed of 10MHz MDC clock.

Table 13 depicts the SMI frame format.

Table 13. Serial Management Interface (SMI) Frame Format

	Preamble	Start of Frame	Read/Write OP Code	PHY Address Bits[4:0]	REG Address Bits[4:0]	TA	Data Bits[15:0]	Idle
Read	32 1's	01	10	RR11R	RRRRR	Z0	0000_0000_DDDD_DDDD	Z
Write	32 1's	01	01	RR11R	RRRRR	10	xxxx_xxxx_DDDD_DDDD	Z

SMI register Read access is selected when OP Code is set to "10" and bits [2:1] of the PHY address is set to '11'. The 8-bit register address is the concatenation of {PHY address bits [4:3], PHY address bits [0], REG address bit [4:0]}. TA is turn-around bits. TA bits [1:0] are 'Z0' means the processor MDIO pin is changed to input Hi-Z from output mode and the followed '0' is the read response from device, as the switch configuration registers are 8-bit wide, only the lower 8 bits of data bits [15:0] are used

SMI register Write access is selected when OP Code is set to "01" and bits [2:1] of the PHY address is set to '11'. The 8-bit register address is the concatenation of {PHY address bits [4:3], PHY address bits [0], REG address bit [4:0]}. TA bits [1:0] are set to '10', as the switch configuration registers are 8-bit wide, only the lower 8 bits of data bits [15:0] are used.

To access the KSZ8895MQX/RQX/FQX/ML Registers 0-255 (0x00 - 0xFF), the following applies:

PHYAD [4, 3, 0] and REGAD [4:0] are concatenated to form the 8-bit address; that is, {PHYAD [4, 3, 0], REGAD [4:0]} = bits [7:0] of the 8-bit address.

Registers are 8 data bits wide. For read operation, data bits [15:8] are read back as zeroes. For write operation, data bits [15:8] are not defined, and hence can be set to either zeroes or ones.

SMI register access is the same as the MIIM register access, except for the register access requirements presented in this section.

Register Descriptions

Offset		
Decimal	**Hex**	**Description**
0-1	0x00-0x01	Chip ID Registers.
2-13	0x02-0x0D	Global Control Registers.
14-15	0x0E-0x0F	Power Down Management Control Registers.
16-20	0x10-0x14	Port 1 Control Registers.
21-23	0x15-0x17	Port 1 Reserved (Factory Test Registers).
24-31	0x18-0x1F	Port 1 Control/Status Registers.
32-36	0x20-0x24	Port 2 Control Registers.
37-39	0x25-0x27	Port 2 Reserved (Factory Test Registers).
40-47	0x28-0x2F	Port 2 Control/Status Registers.
48-52	0x30-0x34	Port 3 Control Registers.
53-55	0x35-0x37	Port 3 Reserved (Factory Test Registers).
56-63	0x38-0x3F	Port 3 Control/Status Registers.
64-68	0x40-0x44	Port 4 Control Registers.
69-71	0x45-0x47	Port 4 Reserved (Factory Test Registers).
72-79	0x48-0x4F	Port 4 Control/Status Registers.
80-84	0x50-0x54	Port 5 Control Registers.
85-87	0x55-0x57	Port 5 Reserved (Factory Test Registers).
88-95	0x58-0x5F	Port 5 Control/Status Registers.
96-103	0x60-0x67	Reserved (Factory Testing Registers).
104-109	0x68-0x6D	MAC Address Registers.
110-111	0x6E-0x6F	Indirect Access Control Registers.
112-120	0x70-0x78	Indirect Data Registers.
121-123	0x79-0x7B	Reserved (Factory Testing Registers).
124-125	0x7C-0x7D	Port Interrupt Registers.
126-127	0x7E-0x7F	Reserved (Factory Testing Registers).
128-135	0x80-0x87	Global Control Registers.
136	0x88	Switch Self Test Control Register.
137-143	0x89-0x8F	QM Global Control Registers.
144-145	0x90-0x91	TOS Priority Control Registers.
146-159	0x92-0x9F	TOS Priority Control Registers.
160-175	0xA0-0xAF	Reserved (Factory Testing Registers).
176-190	0xB0-0xBE	Port 1 Control Registers.
191	0xBF	Reserved (Factory Testing Register): Transmit Queue Remap Base Register.

Register Descriptions (Continued)

Offset		
Decimal	**Hex**	**Description**
192-206	0xC0-0xCE	Port 2 Control Registers.
207	0xCF	Reserved (Factory Testing Register).
208-222	0xD0-0xDE	Port 3 Control Registers.
223	0xDF	Reserved (Factory Testing Register).
224-238	0xE0-0xEE	Port 4 Control Registers.
239	0xEF	Reserved (Factory Testing Register).
240-254	0xF0-0xFE	Port 5 Control Registers.
255	0xFF	Reserved (Factory Testing Register).

Global Registers

Address	Name	Description	Mode	Default
Register 0 (0x00): Chip ID0				
7-0	Family ID	Chip family.	RO	0x95
Register 1 (0x01): Chip ID1 / Start Switch				
7-4	Chip ID	0100 = KSZ8895MQX/FQX/ML 0110 = KSZ8995RQX	RO	0x4 is for MQX, FQX, and ML 0x6 is for RQX
3-1	Revision ID	Revision ID	RO	0x0
0	Start Switch	1, Start the chip when external pins (PS1, PS0) = (1,0) **Note:** in (PS1,PS0) = (0,0) mode, the chip will start automatically, after trying to read the external EEPROM. If EEPROM does not exist, the chip will use default values for all internal registers. If EEPROM is present, the contents in the EEPROM will be checked. The switch will check: (1) Register 0 = 0x95. (2) Register 1 [7:4] = 0x0. If this check is OK, the contents in the EEPROM will override chip register default values =0, chip will not start when external pins (PS1, PS0) = (1,0) or (0,1). **Note:** (PS1, PS0) = (1,1) for Factory test only. 0, stop the switch function of the chip.	R/W	0

Global Registers (Continued)

Address	Name	Description	Mode	Default
Register 2 (0x02): Global Control 0				
7	New Back-off Enable	New Back-off algorithm designed for UNH 1 = Enable 0 = Disable	R/W	0
6	Reserved	Reserved.	RO	0
5	Flush dynamic MAC table	Flush the entire dynamic MAC table for RSTP 1 = Trigger the flush dynamic MAC table operation. This bit is self-clear 0 = normal operation **Note:** All the entries associated with a port that has its learning capability being turned off (Learning Disable) will be flushed. If you want to flush the entire Table, all ports learning capability must be turned off.	R/W (SC)	0
4	Flush static MAC table	Flush the matched entries in static MAC table for RSTP 1 = Trigger the flush static MAC table operation. This bit is self-clear 0 = normal operation **Note:** The matched entry is defined as the entry whose Forwarding Ports field contains a single port and MAC address with unicast. This port, in turn, has its learning capability being turned off (Learning Disable). Per port, multiple entries can be qualified as matched entries.	R/W (SC)	0
3	Enable PHY MII/RMII	1, enable PHY P5-MII/RMII interface (default). **Note:** if not enabled, the switch will be tri-state all outputs.	R/W	1 Pin LED[5][1] strap option. PD(0): isolate. PU(1): Enable. **Note:** LED[5][1] has internal pull-up (PU).
2	Reserved	N/A, do not change	RO	1
1	UNH Mode	1, the switch will drop packets with 0x8808 in T/L filed, or DA = 01-80-C2-00-00-01. 0, the switch will drop packets qualified as “flow control” packets.	R/W	0
0	Link Change Age	1, link change from “link” to “no link” will cause fast aging (<800µs) to age address table faster. After an age cycle is complete, the age logic will return to normal (300 +/- 75 seconds). **Note:** If any port is unplugged, all addresses will be automatically aged out.	R/W	0

Global Registers (Continued)

Address	Name	Description	Mode	Default
Register 3 (0x03): Global Control 1				
7	Pass All Frames	1, switch all packets including bad ones. Used solely for debugging purpose. Works in conjunction with sniffer mode.	R/W	0
6	2K Byte packet support	1 = enable support 2K Byte packet 0 = disable support 2K Byte packet	R/W	0
5	IEEE 802.3x Transmit Flow Control Disable	0, will enable transmit flow control based on AN result. 1, will not enable transmit flow control regardless of AN result.	R/W	0 Pin PMRXD3 strap option. PD(0): Enable Tx flow control (default). PU(1): Disable Tx/Rx flow control. **Note:** PMRXD3 has internal pull-down.
4	IEEE 802.3x Receive Flow Control Disable	0, will enable receive flow control based on AN result. 1, will not enable receive flow control regardless of AN result. **Note**: Bit 5 and bit 4 default values are controlled by the same pin, but they can be programmed independently.	R/W	0 Pin PMRXD3 strap option. PD (0): Enable Rx flow control (default). PU(1): Disable Tx/Rx flow control. **Note:** PMRXD3 has internal pull-down.
3	Frame Length Field Check	1, will check frame length field in the IEEE packets If the actual length does not match, the packet will be dropped (for L/T <1500).	R/W	0
2	Aging Enable	1, Enable age function in the chip. 0, Disable aging function.	R/W	1 Pin LED[5][2] strap option. PD(0): Aging disable. PU(1): Aging enable (default). **Note**: LED[5][2] has internal pull up.

Global Registers (Continued)

Address	Name	Description	Mode	Default
1	Fast age Enable	1 = Turn on fast age (800µs).	R/W	0
0	Aggressive Back Off Enable	1 = Enable more aggressive back-off algorithm in half duplex mode to enhance performance. This is not an IEEE standard.	R/W	0 Pin PMRXD0 strap option. PD(0): Disable aggressive back off (default). PU(1): Aggressive back off. **Note:** PMRXD0 has internal pull down.
Register 4 (0x04): Global Control 2				
7	Unicast Port-VLAN Mismatch Discard	This feature is used for port VLAN (described in Register 17, Register 33...). 1, all packets cannot cross VLAN boundary. 0, unicast packets (excluding unknown/ multicast/broadcast) can cross VLAN boundary.	R/W	1
6	Multicast Storm Protection Disable	1, “Broadcast Storm Protection” does not include multicast packets. Only DA = FFFFFFFFFFFF packets will be regulated. 0, “Broadcast Storm Protection” includes DA = FFFFFFFFFFFF and DA[40] = 1 packet.	R/W	1
5	Back Pressure Mode	1, carrier sense based backpressure is selected. 0, collision based backpressure is selected.	R/W	1
4	Flow Control and Back Pressure fair Mode	1, fair mode is selected. In this mode, if a flow control port and a non-flow control port talk to the same destination port, then packets from the non-flow control port may be dropped. This is to prevent the flow control port from being flow controlled for an extended period of time. 0, in this mode, if a flow control port and a non-flow control port talk to the same destination port, the flow control port will be flow controlled. This may not be “fair” to the flow control port.	R/W	1

Global Registers (Continued)

Address	Name	Description	Mode	Default
3	No Excessive Collision Drop	1, the switch will not drop packets when 16 or more collisions occur. 0, the switch will drop packets when 16 or more collisions occur.	R/W	0 Pin PMRXD1 strap option. PD(0): (default) Drop excessive collision packets. PU(1): Do Not drop excessive collision packets. **Note:** PMRXD1 has internal pull-down.
2	Huge Packet Support	1, will accept packet sizes up to 1916 bytes (inclusive). This bit setting will override setting from bit 1 of the same register. 0, the max packet size will be determined by bit 1 of this register.	R/W	0
1	Legal Maximum Packet Size Check Disable	1, will accept packet sizes up to 1536 bytes (inclusive). 0, 1522 bytes for tagged packets (not including packets with STPID from CPU to ports 1-4), 1518 bytes for untagged packets. Any packets larger than the specified value will be dropped.	R/W	0 Pin PMRXER strap option. PD(0): (default) 1518/1522 byte packets. PU(1): 1536 byte packets. **Note:** PMRXER has internal pull-down.
0	Reserved	N/A	RO	0
Register 5 (0x05): Global Control 3				
7	802.1q VLAN Enable	1, 802.1q VLAN mode is turned on. VLAN table needs to set up before the operation. 0, 802.1q VLAN is disabled.	R/W	0
6	IGMP Snoop Enable on Switch SW5-MII/RMII Interface	1, IGMP snoop enabled. All the IGMP packets will be forwarded to Switch MII/RMII port. 0, IGMP snoop disabled.	R/W	0
5	Enable Direct Mode on Switch SW5-MII/RMII Interface	1, direct mode on Port 5. This is a special mode for the Switch MII/RMII interface. Using preamble before MRXDV to direct switch to forward packets, bypassing internal look-up. 0, normal operation.	R/W	0

Global Registers (Continued)

Address	Name	Description	Mode	Default
4	Enable Pre-Tag on Switch SW5-MII/RMIII Interface	1, packets forwarded to Switch MII/RMII interface will be pre-tagged with the source port number (preamble before MRXDV). 0, normal operation.	R/W	0
3-2	Reserved	N/A	RO	00
1	Enable “Tag” Mask	1, the last 5 digits in the VID field are used as a mask to determine which port(s) the packet should be forwarded to. 0, no tag masks. **Note:** you need to turn off the 802.1q VLAN mode (reg0x5, bit 7 = 0) for this bit to work	R/W	0
0	Sniff Mode Select	1, will do Rx AND Tx sniff (both source port and destination port need to match). 0, will do Rx OR Tx sniff (Either source port or destination port needs to match). This is the mode used to implement Rx only sniff.	R/W	0
Register 6 (0x06): Global Control 4				
7	Switch SW5-MII/RMII Back Pressure Enable	1, enable half-duplex back pressure on switch MII/RMII interface. 0, disable back pressure on switch MII interface.	R/W	0
6	Switch SW5-MII/RMII Half-Duplex Mode	1, enable MII/RMII interface half-duplex mode. 0, enable MII/RMII interface full-duplex mode.	R/W	0 Pin SMRXD2 strap option. PD(0): (default) Full-duplex mode. PU(1): Half-duplex mode. **Note:** SMRXD2 has internal pull-down.
5	Switch SW5-MII/RMII Flow Control Enable	1, enable full-duplex flow control on switch MII/RMII interface. 0, disable full-duplex flow control on switch MII/RMII interface.	R/W	0 Pin SMRXD3 strap option. PD(0): (default) Disable flow control. PU(1): enable flow control. **Note:** SMRXD3 has internal pull-down.

Global Registers (Continued)

Address	Name	Description	Mode	Default
4	Switch SW5-MII/RMII Speed	1, the switch SW5-MII/RMII is in 10Mbps mode. 0, the switch SW5-MII/RMII is in 100Mbps mode.	R/W	0 Pin SMRXD1 strap option. PD(0): (default) Enable 100Mbps. PU(1): Enable 10Mbps. **Note:** SMRXD1 has internal pull-down.
3	Null VID Replacement	1, will replace null VID with port VID (12 bits). 0, no replacement for null VID.	R/W	0
2-0	Broadcast Storm Protection Rate Bit[10:8]	This along with the next register determines how many "64 byte blocks" of packet data allowed on an input port in a preset period. The period is 50ms for 100BT or 500ms for 10BT. The default is 1%.	R/W	000
Register 7 (0x07): Global Control 5				
7-0	Broadcast Storm Protection Rate Bit[7:0]	This along with the previous register determines how many "64-byte blocks" of packet data are allowed on an input port in a preset period. The period is 50ms for 100BT or 500ms for 10BT. The default is 1%.	R/W	0x4A[6]
Register 8 (0x08): Global Control 6				
7-0	Factory Testing	N/A, do not change	RO	0x00
Register 9 (0x09): Global Control 7				
7-0	Factory Testing	N/A, do not change	RO	0x4C

Note:

6. 148,800 frames/sec × 50ms/interval × 1% = 74 frames/interval (approx.) = 0x4A.

Global Registers (Continued)

Address	Name	Description	Mode	Default
Register 10 (0x0A): Global Control 8				
7-0	Factory Testing	N/A, do not change	RO	0x00
Register 11 (0x0B): Global Control 9				
7	Reversed	N/A, do not change	RO	0
6	Port 5 SW5- RMII reference clock edge select	RQX: Select the data sampling edge of Switch MAC5 SW5- RMII reference clock: 1 = data sampling on negative edge of refclk 0 = data sampling on positive edge of refclk (default) **Note**: MQX/FQX/ML is reserved with read only for this bit.	R/W	0
5	Reserved	N/A, do not change	RO	0
4	Reserved	N/A, do not change	RO	0
3	PHY Power Save	1 = disable PHY power save mode. 0 = enable PHY power save mode.	R/W	0
2	Reserved	N/A, do not change	RO	0
1	LED Mode	0 = led mode 0. 1 = led mode 1. Mode 0, link at 100/Full LEDx[2,1,0] = 0,0,0 100/Half LEDx[2,1,0] = 0,1,0 10/Full LEDx[2,1,0] = 0,0,1 10/Half LEDx[2,1,0] = 0,1,1 Mode 1, link at 100/Full LEDx[2,1,0] = 0,1,0 100/Half LEDx[2,1,0] = 0,1,1 10/Full LEDx[2,1,0] = 1,0,0 10/Half LEDx[2,1,0] = 1,0,1 (0 = LED on, 1 = LED off)	R/W	0 Pin SMRXD0 – strap option. Pull-down(0): Enabled led mode 0. Pull-up(1): Enabled led mode 1. **Note:** SMRXD0 has internal pull-down 0.
		Mode 0 / **Mode 1** LEDX_2: Lnk/Act / 100Lnk/Act LEDX_1: Fulld/Col / 10Lnk/Act LEDX_0: Speed / Fulld		
0	SPI/SMI read sampling clock edge select	Select the SPI/SMI clock edge for sampling SPI/SMI read data. 1 = trigger by rising edge of SPI/SMI clock (for high speed SPI about 25MHz and SMI about 10MHz) 0 = trigger by falling edge of SPI/SMI clock.	R/W	0

Global Registers (Continued)

Address	Name	Description	Mode	Default
Register 12 (0x0C): Global Control 10				
7	Reserved	Reserved	RO	0
6	Status of device with RMII interface at clock mode or normal mode, default is clock mode with 25MHz Crystal clock from pins X1/X2 (used for RMII of the KSZ8895RQX only)	1 = The device is in clock mode when use RMII interface, 25 MHz Crystal clock input as clock source for internal PLL. This internal PLL will provide the 50 MHz output on the pin SMRXC for RMII reference clock (Default). 0 = The device is in normal mode when use SW4-RMII interface and 50 MHz clock input from external clock through pin SM4TXC as device's clock source and internal PLL clock source from this pin not from the 25MHz crystal. **Note:** This bit is set by strap option only. Write to this bit has no effect on mode selection. **Note:** The normal mode is used in SW5-RMII interface reference clock from external.	RO	1 Pin LED[2][2] strap option. PD(0): Select SW5-RMII at normal mode to receive external 50MHz RMII reference clock PU(1): (default) Select SW5-RMII at clock mode, RMII output 50MHz **Note:** LED[2][2] has internal pull-up.
5 – 4	CPU interface clock select	Select the internal clock speed for SPI, MDI interface: 00 = 41.67MHz (SPI up to 6.25MHz, MDC up to 6MHz) 01 = 83.33MHz Default (SPI SCL up to 12.5MHz, MDC up to 12MHz) 10 = 125MHz (for high speed SPI about 25MHz) 11 = Reserved	R/W	01
3	Reserved	N/A, do not change	RO	0
2	Enable restore preamble	This bit is to enable PHY5, when in 10BT mode, to restore preamble before sending data on P5-MII interface. 1 = Enable PHY5 to restore preamble. 0 = Disable PHY5 to restore preamble.	R/W	1
1	Tail Tag Enable	Tail Tag feature is applied for Port 5 only. 1 = Insert 1 Byte of data right before FCS. 0 = Do not insert.	R/W	0
0	Pass Flow Control Packet	1 = Switch will not filter 802.1x "flow control" packets. 0 = Switch will filter 802.1x "flow control" packets.	R/W	0
Register 13 (0x0D): Global Control 11				
7 – 0	Factory Testing	N/A, do not change	RO	00000000
Register 14 (0x0E): Power-Down Management Control 1				
7	Reserved	N/A, do not change	RO	0
6	Reserved	N/A, do not change	RO	0

Global Registers (Continued)

Address	Name	Description	Mode	Default
5	PLL Power Down	Pll power down enable: 1 = Enable 0 = Disable	R/W	0
4 – 3	Power Management Mode	Power management mode : 00 = Normal mode (D0) 01 = Energy Detection mode (D2) 10 = soft Power Down mode (D3) 11 = Power Saving mode (D1) Note: For soft Power Down mode to take effect, have to write '10' only without read value back.	R/W	00 Pin LED[4][0] strap option. PD(0): Select Energy detection mode PU(1): (default) Normal mode **Note:** LED[4][0] has internal pull-up.
2-0	Reserved	N/A, do not change	RO	000
Register 15 (0x0F): Power-Down Management Control 2				
7 – 0	Go_sleep_time[7:0]	When the Energy Detect mode is on, this value is used to control the minimum period that the no energy event has to be detected consecutively before the device enters the low power state. The unit is 20ms. The default of go_sleep time is 1.6 seconds (80Dec x 20ms).	R/W	01010000

Port Registers

The following registers are used to enable features that are assigned on a per port basis. The register bit assignments are the same for all ports, but the address for each port is different, as indicated.

Register 16 (0x10): Port 1 Control 0

Register 32 (0x20): Port 2 Control 0

Register 48 (0x30): Port 3 Control 0

Register 64 (0x40): Port 4 Control 0

Register 80 (0x50): Port 5 Control 0

Address	Name	Description	Mode	Default
7	Broadcast Storm Protection Enable	1, enable broadcast storm protection for ingress packets on the port. 0, disable broadcast storm protection.	R/W	0
6	DiffServ Priority Classification Enable	1, enable DiffServ priority classification for ingress packets on port. 0, disable DiffServ function.	R/W	0
5	802.1p Priority Classification Enable	1, enable 802.1p priority classification for ingress packets on port. 0, disable 802.1p.	R/W	0
4 – 3	Port-Based Priority Classification Enable	= 00, ingress packets on port will be classified as priority 0 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. = 01, ingress packets on port will be classified as priority 1 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. = 10, ingress packets on port will be classified as priority 2 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. = 11, ingress packets on port will be classified as priority 3 queue if “Diffserv” or “802.1p” classification is not enabled or fails to classify. **Note:** “DiffServ”, “802.1p” and port priority can be enabled at the same time. The OR’ed result of 802.1p and DSCP overwrites the port priority.	R/W	00
2	Tag insertion	1, when packets are output on the port, the switch will add 802.1q tags to packets without 802.1q tags when received. The switch will not add tags to packets already tagged. The tag inserted is the ingress port’s “port VID.” 0, disable tag insertion.	R/W	0
1	Tag Removal	1, when packets are output on the port, the switch will remove 802.1q tags from packets with 802.1q tags when received. The switch will not modify packets received without tags. 0, disable tag removal.	R/W	0

Port Registers (Continued)

Address	Name	Description	Mode	Default
0	Two Queues Split Enable	This bit 0 in the Register16/32/48/64/80 should be in combination with Register177/193/209/225/241 bit 1 for Port 1-5 will select the split of ½/4 queues: For Port 1, [Register 177 bit 1, Register 16 bit 0] = [11], Reserved [10], the port output queue is split into four priority queues or if map 802.1p to priority 0-3 mode. [01], the port output queue is split into two priority queues or if map 802.1p to priority 0-3 mode. [00], single output queue on the port. There is no priority differentiation even though packets are classified into high or low priority.	R/W	0

Register 17 (0x11): Port 1 Control 1

Register 33 (0x21): Port 2 Control 1

Register 49 (0x31): Port 3 Control 1

Register 65 (0x41): Port 4 Control 1

Register 81 (0x51): Port 5 Control 1

Address	Name	Description	Mode	Default
7	Sniffer Port	1, port is designated as sniffer port and will transmit packets that are monitored. 0, port is a normal port.	R/W	0
6	Receive Sniff	1, all the packets received on the port will be marked as “monitored packets” and forwarded to the designated “sniffer port.” 0, no receive monitoring.	R/W	0
5	Transmit Sniff	1, all the packets transmitted on the port will be marked as “monitored packets” and forwarded to the designated “sniffer port.” 0, no transmit monitoring.	R/W	0
4-0	Port VLAN Membership	Define the port’s Port VLAN membership. Bit 4 stands for Port 5, bit 3 for Port 4...bit 0 for Port 1. The port can only communicate within the membership. A ‘1’ includes a port in the membership, a ‘0’ excludes a port from membership.	R/W	0x1f

Port Registers (Continued)

Register 18 (0x12): Port 1 Control 2

Register 34 (0x22): Port 2 Control 2

Register 50 (0x32): Port 3 Control 2

Register 66 (0x42): Port 4 Control 2

Register 82 (0x52): Port 5 Control 2

Address	Name	Description	Mode	Default
7	User Priority Ceiling	1, If packet 's "user priority field" is greater than the "user priority field" in the port default tag register, replace the packet's "user priority field" with the "user priority field" in the port default tag Register control 3. 0, no replace packet's priority filed with port default tag priority filed of the Register Port Control 3 bit [7:5].	R/W	0
6	Ingress VLAN Filtering.	1, the switch will discard packets whose VID port membership in VLAN table bit [11:7] does not include the ingress port. 0, no ingress VLAN filtering.	R/W	0
5	Discard Non-PVID packets	1, the switch will discard packets whose VID does not match ingress port default VID. 0, no packets will be discarded.	R/W	0
4	Force Flow Control	1, will always enable Rx and Tx flow control on the port, regardless of AN result. 0, the flow control is enabled based on AN result (Default)	R/W	0 Strap-in option LED1_1/PCOL For port 3/port 4 LED1_1 default Pull up (1): Not force flow control; PCOL default Pull-down (0): Not force flow control. LED1_1 Pull down (0): Force flow control; PCOL Pull-up (1): Force flow control. **Note:** LED1_1 has internal pull-up; PCOL have internal pull-down.
3	Back Pressure Enable	1, enable port half-duplex back pressure. 0, disable port half-duplex back pressure.	R/W	Pin PMRXD2 strap option. Pull-down (0): disable back pressure. Pull-up(1): enable back pressure. **Note:** PMRXD2 has internal pull-down.
2	Transmit Enable	1, enable packet transmission on the port. 0, disable packet transmission on the port.	R/W	1
1	Receive Enable	1, enable packet reception on the port. 0, disable packet reception on the port.	R/W	1

Note:

Bits 2-0 are used for spanning tree support. See "Spanning Tree Support" section.

Port Registers (Continued)

Address	Name	Description	Mode	Default
0	Learning Disable	1, disable switch address learning capability. 0, enable switch address learning.	R/W	0

Register 19 (0x13): Port 1 Control 3

Register 35 (0x23): Port 2 Control 3

Register 51 (0x33): Port 3 Control 3

Register 67 (0x43): Port 4 Control 3

Register 83 (0x53): Port 5 Control 3

Address	Name	Description	Mode	Default
7-0	Default Tag [15:8]	Port's default tag, containing: 7-5: user priority bits 4: CFI bit 3-0 : VID[11:8]	R/W	0

Register 20 (0x14): Port 1 Control 4

Register 36 (0x24): Port 2 Control 4

Register 52 (0x34): Port 3 Control 4

Register 68 (0x44): Port 4 Control 4

Register 84 (0x54): Port 5 Control 4

Address	Name	Description	Mode	Default
7-0	Default Tag [7:0]	Default port 1's tag, containing: 7-0: VID[7:0]	R/W	1

Note:

Registers 19 and 20 (and those corresponding to other ports) serve two purposes: (1) Associated with the ingress untagged packets, and used for egress tagging; (2) Default VID for the ingress untagged or null-VID-tagged packets, and used for address look up.

Port Registers (Continued)

Register 87 (0x57): RMII Management Control Register

Address	Name	Description	Mode	Default
7 - 4	Reserved	N/A, do not change	RO	0000
3	Port 5 SW5-RMII 50MHz clock output disable (used for KSZ8895RQX only)	Disable the output of port 5 SW5-RMII 50 MHz output clock on RXC pin when 50MHz clock is not being used by the device and the 50MHz clock from external oscillator or opposite device in RMII mode 1 = Disable clock output when RXC pin is not used in RMII mode 0 = Enable clock output in RMII mode **Note:** MQX/FQX/ML is reserved with read only for this bit.	R/W	0
2	P5-RMII 50MHz clock output disable (used for KSZ8895RQX only)	Disable the output of port 5 P5-RMII 50 MHz output clock on RXC pin when 50MHz clock is not being used by the device and the 50MHz clock from external oscillator or opposite device in RMII mode 1 = Disable clock output when RXC pin is not used in RMII mode 0 = Enable clock output in RMII mode **Note:** MQX/FQX/ML is reserved with read only for this bit.	R/W	0
1 - 0	Reserved	N/A, do not change	RO	00

Register 25 (0x19): Port 1 Status 0

Register 41 (0x29): Port 2 Status 0

Register 57 (0x39): Port 3 Status 0

Register 73 (0x49): Port 4 Status 0

Register 89 (0x59): Port 5 Status 0

Address	Name	Description	Mode	Default
7	Hp_mdix	1 = HP Auto MDI/MDI-X mode 0 = Micrel Auto MDI/MDI-X mode	R/W	1
6	Factory Testing	N/A, do not change	RO	0
5	Polrvs	1 = Polarity is reversed 0 = Polarity is not reversed	RO	0
4	Transmit Flow Control Enable	1 = Transmit flow control feature is active 0 = Transmit flow control feature is inactive	RO	0
3	Receive Flow Control Enable	1 = Receive flow control feature is active 0 = Receive flow control feature is inactive	RO	0
2	Operation Speed	1 = Link speed is 100Mbps 0 = Link speed is 10Mbps	RO	0
1	Operation Duplex	1 = Link duplex is full 0 = Link duplex is half	RO	0
0	Reserved	N/A, do not change	RO	0

Port Registers (Continued)

Register 26 (0x1A): Port 1 PHY Special Control/Status

Register 42 (0x2A): Port 2 PHY Special Control/Status

Register 58 (0x3A): Port 3 PHY Special Control/Status

Register 74 (0x4A): Port 4 PHY Special Control/Status

Register 90 (0x5A): Port 5 PHY Special Control/Status

Address	Name	Description	Mode	Default
7	Vct 10M Short	1 = less than 10 meter short detected	RO	0
6 - 5	Vct_result	00 = Normal condition 01 = Open condition detected in cable 10 = Short condition detected in cable 11 = Cable diagnostic test has failed	RO	00
4	Vct_enable	1 = Enable cable diagnostic test. After VCT test has completed, this bit will be self-cleared. 0 = Indicate cable diagnostic test (if enabled) has completed and the status information is valid for read.	R/W (SC)	0
3	Force_lnk	1 = Force link pass 0 = Normal Operation	R/W	0
2	Pwrsave	1 = Enable power saving 0 = Disable power saving	R/W	0
1	Remote Loopback	1 = Perform Remote loopback, loopback on port 1 as follows: Port 1 (reg. 26, bit 1 = '1') Start : RXP1/RXM1 (port 1) Loopback: PMD/PMA of port 1's PHY End: TXP1/TXM1 (port 1) Setting reg. 42, 58, 74, 90, bit 1 = '1' will perform remote loopback on port 2, 3, 4, 5. 0 = Normal Operation.	R/W	0
0	Vct_fault_count[8]	Bits[8] of VCT fault count Distance to the fault. It's approximately 0.4m*Vct_fault_count[8:0]	RO	0

Port Registers (Continued)

Register 27 (0x1B): Port 1 LinkMD result

Register 43 (0x2B): Port 2 LinkMD result

Register 59 (0x3B): Port 3 LinkMD result

Register 75 (0x4B): Port 4 LinkMD result

Register 91 (0x5B): Port 5 LinkMD result

Address	Name	Description	Mode	Default
7-0	Vct_fault_count[7:0]	Bits[7:0] of VCT fault count Distance to the fault. It's approximately 0.4m*Vct_fault_count[8:0]	RO	0

Register 28 (0x1C): Port 1 Control 5

Register 44 (0x2C): Port 2 Control 5

Register 60 (0x3C): Port 3 Control 5

Register 76 (0x4C): Port 4 Control 5

Register 92 (0x5C): Port 5 Control 5

Address	Name	Description	Mode	Default
7	Disable Auto-Negotiation	1, disable auto-negotiation, speed and duplex are decided by bit 6 and 5 of the same register. 0, auto-negotiation is on. **Note:** The register bit value is the INVERT of the strap value at the pin.	R/W	0 For Port 3/Port 4 only. INVERT of pins LED[2][1]/LED[5][0] strap option. PD(0): Disable Auto-Negotiation. PU(1): Enable Auto-Negotiation. **Note:** LED[2][1]/LED[5][0] have internal pull up.
6	Forced Speed	1, forced 100BT if AN is disabled (bit 7). 0, forced 10BT if AN is disabled (bit 7).	R/W	1

Port Registers (Continued)

Address	Name	Description	Mode	Default
5	Forced Duplex	1, forced full-duplex if (1) AN is disabled or (2) AN is enabled but failed. 0, forced half-duplex if (1) AN is disabled or (2) AN is enabled but failed (Default).	R/W	0 For Port 3/Port 4 only. Pins LED1_0/PCRS strap option: 1). Force half-duplex mode: LED1_0 pin Pull-up(1) (default) for Port 3 PCRS pin Pull-down (0) (default) for Port 4 2). Force full-Duplex mode: LED1_0 pin Pull-down(0) for Port 3 PCRS Pull-up (1) for Port 4. **Note:** LED1_0 has internal pull-up; PCRS have internal pull down.
4	Advertised Flow Control Capability	1, advertise flow control capability. 0, suppress flow control capability from transmission to link partner.	R/W	1
3	Advertised 100BT Full-Duplex Capability	1, advertise 100BT full-duplex capability. 0, suppress 100BT full-duplex capability from transmission to link partner.	R/W	1
2	Advertised 100BT Half-Duplex Capability	1, advertise 100BT half-duplex capability. 0, suppress 100BT half-duplex capability from transmission to link partner.	R/W	1
1	Advertised 10BT Full-Duplex Capability	1, advertise 10BT full-duplex capability. 0, suppress 10BT full-duplex capability from transmission to link partner.	R/W	1
0	Advertised 10BT Half-Duplex Capability	1, advertise 10BT half-duplex capability. 0, suppress 10BT half-duplex capability from transmission to link partner.	R/W	1

Port Registers (Continued)

Register 29 (0x1D): Port 1 Control 6

Register 45 (0x2D): Port 2 Control 6

Register 61 (0x3D): Port 3 Control 6

Register 77 (0x4D): Port 4 Control 6

Register 93 (0x5D): Port 5 Control 6

Address	Name	Description	Mode	Default
7	LED Off	1, turn off all port's LEDs (LEDx_2, LEDx_1, LEDx_0, where "x" is the port number). These pins will be driven high if this bit is set to one. 0, normal operation.	R/W	0
6	Txids	1, disable port's transmitter. 0, normal operation.	R/W	0
5	Restart AN	1, restart auto-negotiation. 0, normal operation.	R/W (SC)	0
4	FX reserved	N/A	RO	0
3	Power Down	1, power down. 0, normal operation.	R/W	0
2	Disable Auto MDI/MDI-X	1, disable auto MDI/MDI-X function. 0, enable auto MDI/MDI-X function.	R/W	0
1	Forced MDI	1, if auto MDI/MDI-X is disabled, force PHY into MDI mode (transmit on RX pair). 0, MDI-X mode (transmit on TX pair).	R/W	0
0	MAC Loopback	1 = Perform MAC loopback, loop back path as follows: E.g. set port 1 MAC Loopback (reg. 29, bit 0 = '1'), use port 2 as monitor port. The packets will transfer Start: Port 2 receiving (also can start to receive packets from port 3, 4, 5). Loop-back: Port 1's MAC. End: Port 2 transmitting (also can end at Port 3, 4, 5 respectively). Setting reg. 45, 61, 77, 93, bit 0 = '1' will perform MAC loopback on port 2, 3, 4, 5 respectively. 0 = Normal Operation.	R/W	0

Port Registers (Continued)

Register 30 (0x1E): Port 1 Status 1

Register 46 (0x2E): Port 2 Status 1

Register 62 (0x3E): Port 3 Status 1

Register 78 (0x4E): Port 4 Status 1

Register 94 (0x5E): Port 5 Status 1

Address	Name	Description	Mode	Default
7	MDIX Status	1, MDI. 0, MDI-X.	RO	0
6	AN Done	1, AN done. 0, AN not done.	RO	0
5	Link Good	1, link good. 0, link not good.	RO	0
4	Partner Flow Control Capability	1, link partner flow control capable. 0, link partner not flow control capable.	RO	0
3	Partner 100BT Full-Duplex Capability	1, link partner 100BT full-duplex capable. 0, link partner not 100BT full-duplex capable.	RO	0
2	Partner 100BT Half-Duplex Capability	1, link partner 100BT half-duplex capable. 0, link partner not 100BT half-duplex capable.	RO	0
1	Partner 10BT Full-Duplex Capability	1, link partner 10BT full-duplex capable. 0, link partner not 10BT full-duplex capable.	RO	0
0	Partner 10BT Half-Duplex Capability	1, link partner 10BT half-duplex capable. 0, link partner not 10BT half-duplex capable.	RO	0

Register 31 (0x1F): Port 1 Control 7 and Status 2

Register 47 (0x2F): Port 2 Control 7 and Status 2

Register 63 (0x3F): Port 3 Control 7 and Status 2

Register 79 (0x4F): Port 4 Control 7 and Status 2

Register 95 (0x5F): Port 5 Control 7 and Status 2

Address	Name	Description	Mode	Default
7	PHY Loopback	1 = Perform PHY loopback, loop back path as follows: E.g. set port 1 PHY Loopback (reg. 31, bit 7 = '1') Use the port 2 as monitor port. The packets will transfer. Start: Port 2 receiving (also can start from port 3, 4, 5). Loopback: PMD/PMA of Port 1's PHY End: Port 2 transmitting (also can end at Port 3, 4, 5 respectively). Setting reg. 47, 63, 79, 95, bit 7 = '1' will perform PHY loopback on port 2, 3, 4, 5 respectively. 0 = Normal Operation.	R/W	0

Port Registers (Continued)

Address	Name	Description	Mode	Default
6	Reserved		RO	0
5	PHY Isolate	1, Electrical isolation of PHY from MII/RMII and TX+/TX-. 0, normal operation.	R/W	0
4	Soft Reset	1, PHY soft reset. This bit is self-clear. 0, normal operation.	R/W (SC)	0
3	Force Link	1, force link in the PHY. 0, normal operation	R/W	0
2-0	Port Operation Mode Indication	Indicate the current state of port operation mode: [000] = Reserved [001] = still in auto-negotiation [010] = 10BASE-T half duplex [011] = 100BASE-TX half duplex [100] = Reserved [101] = 10BASE-T full duplex [110] = 100BASE-TX full duplex [111] = Reserved	RO	001

Note:

Port Control 12 and 13, 14 and Port Status 1,2 contents can be accessed by MIIM (MDC/MDIO) interface via the standard MIIM register definition.

Advanced Control Registers

Registers 104 to 109 define the switching engine's MAC address. This 48-bit address is used as the source address in MAC pause control frames.

Address	Name	Description	Mode	Default
Register 104 (0x68): MAC Address Register 0				
7-0	MACA[47:40]		R/W	0x00
Register 105 (0x69): MAC Address Register 1				
7-0	MACA[39:32]		R/W	0x10
Register 106 (0x6A): MAC Address Register 2				
7-0	MACA[31:24]		R/W	0xA1
Register 107 (0x6B): MAC Address Register 3				
7-0	MACA[23:16]		R/W	0xff
Register 108 (0x6C): MAC Address Register 4				
7-0	MACA[15:8]		R/W	0xff
Register 109 (0X6D): MAC Address Register 5				
7-0	MACA[7:0]		R/W	0xff

Note:

Use Registers 110 and 111 to read or write data to the static MAC address table, VLAN table, dynamic address table, or the MIB counters.

Advanced Control Registers (Continued)

Address	Name	Description	Mode	Default
Register 110 (0x6E): Indirect Access Control 0				
7-5	Reserved	Reserved.	R/W	000
4	Read High Write Low	1, read cycle. 0, write cycle.	R/W	0
3-2	Table Select	00 = static mac address table selected. 01 = VLAN table selected. 10 = dynamic address table selected. 11 = MIB counter selected.	R/W	0
1-0	Indirect Address High	Bit 9-8 of indirect address.	R/W	00
Register 111 (0x6F): Indirect Access Control 1				
7-0	Indirect Address Low	Bit 7-0 of indirect address.	R/W	00000000

Note:

Write to Register 111 will actually trigger a command. Read or write access will be decided by bit 4 of Register 110.

Address	Name	Description	Mode	Default
Register 112 (0x70): Indirect Data Register 8				
68-64	Indirect Data	Bit 68-64 of indirect data.	R/W	00000
Register 113 (0x71): Indirect Data Register 7				
63-56	Indirect Data	Bit 63-56 of indirect data.	R/W	00000000
Register 114 (0x72): Indirect Data Register 6				
55-48	Indirect Data	Bit 55-48 of indirect data.	R/W	00000000
Register 115 (0x73): Indirect Data Register 5				
47-40	Indirect Data	Bit 47-40 of indirect data.	R/W	00000000
Register 116 (0x74): Indirect Data Register 4				
39-32	Indirect Data	Bit 39-32 of indirect data.	R/W	00000000
Register 117 (0x75): Indirect Data Register 3				
31-24	Indirect Data	Bit of 31-24 of indirect data	R/W	00000000
Register 118 (0x76): Indirect Data Register 2				
23-16	Indirect Data	Bit 23-16 of indirect data.	R/W	00000000
Register 119 (0x77): Indirect Data Register 1				
15-8	Indirect Data	Bit 15-8 of indirect data.	R/W	00000000
Register 120 (0x78): Indirect Data Register 0				
7-0	Indirect Data	Bit 7-0 of indirect data.	R/W	00000000

Advanced Control Registers (Continued)

Address	Name	Description	Mode	Default
Register 124 (0x7C): Interrupt Status Register				
7 – 5	Reserved	Reserved.	RO	000
4	Port 5 Interrupt Status	1, Port 5 interrupt request 0, normal **Note:** This bit is set by Port 5 link change. Write a "1" to clear this bit	RO	0
3	Port 4 Interrupt Status	1, Port 4 interrupt request 0, normal **Note:** This bit is set by Port 4 link change. Write a "1" to clear this bit	RO	0
2	Port 3 Interrupt Status	1, Port 3 interrupt request 0, normal **Note:** This bit is set by Port 3 link change. Write a "1" to clear this bit	RO	0
1	Port 2 Interrupt Status	1, Port 2 interrupt request 0, normal **Note:** This bit is set by Port 2 link change. Write a "1" to clear this bit	RO	0
0	Port 1 Interrupt Status	1, Port 1 interrupt request 0, normal **Note:** This bit is set by Port 1 link change. Write a "1" to clear this bit	RO	0
Register 125 (0x7D): Interrupt Mask Register				
7 – 5	Reserved	Reserved.	RO	000
4	Port 5 Interrupt Mask	1, Enable Port 5 interrupt. 0, normal	R/W	0
3	Port 4 Interrupt Mask	1, Enable Port 4 interrupt. 0, normal	R/W	0
2	Port 3 Interrupt Mask	1, Enable Port 3 interrupt. 0, normal	R/W	0
1	Port 2 Interrupt Mask	1, Enable Port 2 interrupt. 0, normal	R/W	0
0	Port 1 Interrupt Mask	1, Enable Port 1 interrupt. 0, normal	R/W	0

Advanced Control Registers (Continued)

The Registers 128, 129 can be used to map from 802.1p priority field 0-7 to switch's four priority queues 0-3, 0x3 is highest priority queues as priority 3, 0x0 is lowest priority queues as priority 0.

Address	Name	Description	Mode	Default
Register 128 (0x80): Global Control 12				
7 – 6	Tag_0x3	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x3.	R/W	0x1
5 – 4	Tag_0x2	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x2.	R/W	0x1
3 – 2	Tag_0x1	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x1.	R/W	0x0
1 – 0	Tag_0x0	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x0.	R/W	0x0
Register 129 (0x81): Global Control 13				
7 – 6	Tag_0x7	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x7.	R/W	0x3
5 – 4	Tag_0x6	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x6.	R/W	0x3
3 – 2	Tag_0x5	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x5.	R/W	0x2
1 – 0	Tag_0x4	IEEE 802.1p mapping. The value in this field is used as the frame's priority when its IEEE 802.1p tag has a value of 0x4.	R/W	0x2
Register 130 (0x82): Global Control 14				
7 – 6	Pri_2Q[1:0] (Note that program Prio_2Q[1:0] = 01 is not supported and should be avoided)	When the 2 Queues configuration is selected, these Pri_2Q[1:0] bits are used to map the 2-bit result of IEEE 802.1p from Register 128/129 or TOS/DiffServ from Register 144- 159 mapping (for 4 Queues) into two queues low/high priorities. 2-bit result of IEEE 802.1p or TOS/DiffServ 00 (0) = map to Low priority queue 01 (1) = Prio_2Q[0] map to Low/High priority queue 10 (2) = Prio_2Q[1] map to Low/High priority queue 11 (3) = map to High priority queue Pri_2Q[1:0] = 00: Result 0,1,2 are low priority. 3 is high priority. 10: Result 0,1 are low priority. 2,3 are high priority (default). 11: Result 0 is low priority. 1,2,3 are high priority.	R/W	10

Advanced Control Registers (Continued)

Address	Name	Description	Mode	Default
5	Reserved	N/A, do not change	RO	0
4	Reserved	N/A, do not change	RO	0
3 – 2	Reserved	N/A, do not change	RO	01
1	Reserved	N/A, do not change	RO	0
0	Reserved	N/A, do not change	RO	0
Register 131 (0x83): Global Control 15				
7	Reserved	N/A	RO	1
6	Reserved	N/A	RO	0
5	Unknown unicast packet forward	1 = enable supporting unknown unicast packet forward 0 = disable	R/W	0
4 – 0	Unknown unicast packet forward port map	00000 = filter unknown unicast packet 00001 = forward unknown unicast packet to port 1, 00010 = forward unknown unicast packet to port 2, 00011 = forward unknown unicast packet to port 1, port 2 … 11111 = broadcast unknown unicast packet to all ports	R/W	00000
Register 132 (0x84): Global Control 16				
7 – 6	Chip I/O output drive strength select[1:0]	Output drive strength select[1:0] = 00 = 4mA drive strength 01 = 8mA drive strength (default) 10 = 10mA drive strength 11 = 14mA drive strength **Note:** Bit [1] value is the INVERT of the strap value at the pin. Bit[0] value is the SAME of the strap value at the pin	R/W	01 Pin LED [3][0] strap option. Pull-down (0): Select 10mA drive strength. Pull-up (1): Select 8mA drive strength. **Note:** LED [3][0] has internal pull-up.
5	Unknown multicast packet forward (not including IP multicast packet)	1 = enable supporting unknown multicast packet forward 0 = disable	R/W	0
4 – 0	Unknown multicast packet forward port map	00000 = filter unknown multicast packet 00001 = forward unknown multicast packet to port 1, 00010 = forward unknown multicast packet to port 2, 00011 = forward unknown multicast packet to port 1, port 2 … 11111 = broadcast unknown multicast packet to all ports	R/W	00000

Advanced Control Registers (Continued)

Address	Name	Description	Mode	Default
Register 133(0x85): Global Control 17				
7 – 6	Reserved		RO	00
5	Unknown VID packet forward	1 = enable supporting unknown VID packet forward 0 = disable	R/W	0
4 – 0	Unknown VID packet forward port map	00000 = filter unknown VID packet 00001 = forward unknown VID packet to port 1, 00010 = forward unknown VID packet to port 2, 00011 = forward unknown VID packet to port 1, port 2 … 11111 = broadcast unknown VID packet to all ports	R/W	00000
Register 134 (0x86): Global Control 18				
7	Reserved	N/A	RO	0
6	Self-Address Filter Enable	1 = Enable filtering of self-address unicast and multicast packet 0 = Do not filter self-address packet **Note:** The self-address filtering will filter packets on the egress port, self MAC address is assigned in the Register 104-109.	R/W	0
5	Unknown IP multicast packet forward	1 = enable supporting unknown IP multicast packet forward 0 = disable	R/W	0
4 – 0	Unknown IP multicast packet forward port map	00000 = filter unknown IP multicast packet 00001 = forward unknown IP multicast packet to port 1, 00010 = forward unknown IP multicast packet to port 2, 00011 = forward unknown IP multicast packet to port 1, port 2 … 11111 = broadcast unknown IP multicast packet to all ports	R/W	00000
Register 135 (0x87): Global Control 19				
7	Reserved	N/A, do not change	RO	0
6	Reserved	N/A, do not change	RO	0
5 – 4	Ingress Rate Limit Period	The unit period for calculating Ingress Rate Limit 00 = 16ms 01 = 64ms 1x = 256ms	R/W	01
3	Queue-based Egress Rate Limit Enabled	Enable Queue-based Egress Rate Limit 0 = port-base Egress Rate Limit (default) 1 = queue-based Egress Rate Limit	R/W	0

Advanced Control Registers (Continued)

Address	Name	Description	Mode	Default
2	Insertion Source Port PVID Tag Selection Enable	1 = enable source port PVID tag insertion or non-insertion option on the egress port for each source port PVID based on the ports Registers control 8. 0 = disable, all packets from any ingress port will be inserted PVID based on Register Port Control 0 bit [2].	R/W	0
1 – 0	Reserved	N/A, do not change	RO	00
Register 137 (0x89): Identification Register				
7 – 4	Revision ID	These bits are for the device identification 0000: Reserved 0001-0011: For MQ/FMQ 0.13um silicon devices. 0100 (0x4): For MQX/FQX Rev.A2 and ML Rev.B2 0101 (0x5): For MQX/FQX Rev.A3 and ML Rev.B3 0110 (0x6): For MQX/FQX Rev.A4 and ML Rev.B4 0111-1111: Reserved	RO	Depends on Revision #
3 – 0	Reserved	N/A, do not change	RO	00
Register 144 (0x90): TOS Priority Control Register 0 The Ipv4/Ipv6 TOS priority control registers implement a fully decoded 64 bit differentiated services code point (DSCP) register used to determine priority from the 6 bit TOS field in the IP header. The most significant 6 bits of the TOS field are fully decoded into 64 possibilities, and the singular code that results is mapped to the value in the corresponding bit in the DSCP register.				
7 – 6	DSCP[7:6]	**Ipv4 and Ipv6 mapping** The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x03	R/W	00
5 – 4	DSCP[5:4]	**Ipv4 and Ipv6 mapping** The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x02	R/W	00
3 – 2	DSCP[3:2]	**Ipv4 and Ipv6 mapping** The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x01	R/W	00
1 – 0	DSCP[1:0]	**Ipv4 and Ipv6 mapping** The value in this field is used as the frame's priority when bits [7:2] of the frame's IP TOS/DiffServ/Traffic Class value is 0x00	R/W	00
Register 145 (0x91): TOS Priority Control Register 1				
7 – 6	DSCP[15:14]	**Ipv4 and Ipv6 mapping** _ for value 0x07	R/W	00
5 – 4	DSCP[13:12]	**Ipv4 and Ipv6 mapping** _ for value 0x06	R/W	00
3 – 2	DSCP[11:10]	**Ipv4 and Ipv6 mapping** _ for value 0x05	R/W	00
1 – 0	DSCP[9:8]	**Ipv4 and Ipv6 mapping** _ for value 0x04	R/W	00

Advanced Control Registers (Continued)

Address	Name	Description	Mode	Default
Register 146 (0x92): TOS Priority Control Register 2				
7 – 6	DSCP[23:22]	**Ipv4 and Ipv6 mapping** _ for value 0x0B	R/W	00
5 – 4	DSCP[21:20]	**Ipv4 and Ipv6 mapping** _ for value 0x0A	R/W	00
3 – 2	DSCP[19:18]	**Ipv4 and Ipv6 mapping** _ for value 0x09	R/W	00
1 – 0	DSCP[17:16]	**Ipv4 and Ipv6 mapping** _ for value 0x08	R/W	00
Register 147 (0x93): TOS Priority Control Register 3				
7 – 6	DSCP[31:30]	**Ipv4 and Ipv6 mapping** _ for value 0x0F	R/W	00
5 – 4	DSCP[29:28]	**Ipv4 and Ipv6 mapping** _ for value 0x0E	R/W	00
3 – 2	DSCP[27:26]	**Ipv4 and Ipv6 mapping** _ for value 0x0D	R/W	00
1 – 0	DSCP[25:24]	**Ipv4 and Ipv6 mapping** _ for value 0x0C	R/W	00
Register 148 (0x94): TOS Priority Control Register 4				
7 – 6	DSCP[39:38]	**Ipv4 and Ipv6 mapping** _ for value 0x13	R/W	00
5 – 4	DSCP[37:36]	**Ipv4 and Ipv6 mapping** _ for value 0x12	R/W	00
3 – 2	DSCP[35:34]	**Ipv4 and Ipv6 mapping** _ for value 0x11	R/W	00
1 – 0	DSCP[33:32]	**Ipv4 and Ipv6 mapping** _ for value 0x10	R/W	00
Register 149 (0x95): TOS Priority Control Register 5				
7 – 6	DSCP[47:46]	**Ipv4 and Ipv6 mapping** _ for value 0x17	R/W	00
5 – 4	DSCP[45:44]	**Ipv4 and Ipv6 mapping** _ for value 0x16	R/W	00
3 – 2	DSCP[43:42]	**Ipv4 and Ipv6 mapping** _ for value 0x15	R/W	00
1 – 0	DSCP[41:40]	**Ipv4 and Ipv6 mapping** _ for value 0x14	R/W	00
Register 150 (0x96): TOS Priority Control Register 6				
7 – 6	DSCP[55:54]	**Ipv4 and Ipv6 mapping** _ for value 0x1B	R/W	00
5 – 4	DSCP[53:52]	**Ipv4 and Ipv6 mapping** _ for value 0x1A	R/W	00
3 – 2	DSCP[51:50]	**Ipv4 and Ipv6 mapping** _ for value 0x19	R/W	00
1 – 0	DSCP[49:48]	**Ipv4 and Ipv6 mapping** _ for value 0x18	R/W	00
Register 151 (0x97): TOS Priority Control Register 7				
7 – 6	DSCP[63:62]	**Ipv4 and Ipv6 mapping** _ for value 0x1F	R/W	00
5 – 4	DSCP[61:60]	**Ipv4 and Ipv6 mapping** _ for value 0x1E	R/W	00
3 – 2	DSCP[59:58]	**Ipv4 and Ipv6 mapping** _ for value 0x1D	R/W	00
1 – 0	DSCP[57:56]	**Ipv4 and Ipv6 mapping** _ for value 0x1C	R/W	00

Advanced Control Registers (Continued)

Address	Name	Description	Mode	Default
Register 152 (0x98): TOS Priority Control Register 8				
7 – 6	DSCP[71:70]	**Ipv4 and Ipv6 mapping** _ for value 0x23	R/W	00
5 – 4	DSCP[69:68]	**Ipv4 and Ipv6 mapping** _ for value 0x22	R/W	00
3 – 2	DSCP[67:66]	**Ipv4 and Ipv6 mapping** _ for value 0x21	R/W	00
1 – 0	DSCP[65:64]	**Ipv4 and Ipv6 mapping** _ for value 0x20	R/W	00
Register 153 (0x99): TOS Priority Control Register 9				
7 – 6	DSCP[79:78]	**Ipv4 and Ipv6 mapping** _ for value 0x27	R/W	00
5 – 4	DSCP[77:76]	**Ipv4 and Ipv6 mapping** _ for value 0x26	R/W	00
3 – 2	DSCP[75:74]	**Ipv4 and Ipv6 mapping** _ for value 0x25	R/W	00
1 – 0	DSCP[73:72]	**Ipv4 and Ipv6 mapping** _ for value 0x24	R/W	00
Register 154 (0x9A): TOS Priority Control Register 10				
7 – 6	DSCP[87:86]	**Ipv4 and Ipv6 mapping** _ for value 0x2B	R/W	00
5 – 4	DSCP[85:84]	**Ipv4 and Ipv6 mapping** _ for value 0x2A	R/W	00
3 – 2	DSCP[83:82]	**Ipv4 and Ipv6 mapping** _ for value 0x29	R/W	00
1 – 0	DSCP[81:80]	**Ipv4 and Ipv6 mapping** _ for value 0x28	R/W	00
Register 155 (0x9B): TOS Priority Control Register 11				
7 – 6	DSCP[95:94]	**Ipv4 and Ipv6 mapping** _ for value 0x2F	R/W	00
5 – 4	DSCP[93:92]	**Ipv4 and Ipv6 mapping** _ for value 0x2E	R/W	00
3 – 2	DSCP[91:90]	**Ipv4 and Ipv6 mapping** _ for value 0x2D	R/W	00
1 – 0	DSCP[89:88]	**Ipv4 and Ipv6 mapping** _ for value 0x2C	R/W	00
Register 156 (0x9C): TOS Priority Control Register 12				
7 – 6	DSCP[103:102]	**Ipv4 and Ipv6 mapping** _ for value 0x33	R/W	00
5 – 4	DSCP[101:100]	**Ipv4 and Ipv6 mapping** _ for value 0x32	R/W	00
3 – 2	DSCP[99:98]	**Ipv4 and Ipv6 mapping** _ for value 0x31	R/W	00
1 – 0	DSCP[97:96]	**Ipv4 and Ipv6 mapping** _ for value 0x30	R/W	00
Register 157 (0x9D): TOS Priority Control Register 13				
7 – 6	DSCP[111:110]	**Ipv4 and Ipv6 mapping** _ for value 0x37	R/W	00
5 – 4	DSCP[109:108]	**Ipv4 and Ipv6 mapping** _ for value 0x36	R/W	00
3 – 2	DSCP[107:106]	**Ipv4 and Ipv6 mapping** _ for value 0x35	R/W	00
1 – 0	DSCP[105:104]	**Ipv4 and Ipv6 mapping** _ for value 0x34	R/W	00
Register 158 (0x9E): TOS Priority Control Register 14				
7 – 6	DSCP[119:118]	**Ipv4 and Ipv6 mapping** _ for value 0x3B	R/W	00
5 – 4	DSCP[117:116]	**Ipv4 and Ipv6 mapping** _ for value 0x3A	R/W	00
3 – 2	DSCP[115:114]	**Ipv4 and Ipv6 mapping** _ for value 0x39	R/W	00
1 – 0	DSCP[113:112]	**Ipv4 and Ipv6 mapping** _ for value 0x38	R/W	00

Advanced Control Registers (Continued)

Address	Name	Description	Mode	Default
Register 159 (0x9F): TOS Priority Control Register 15				
7 – 6	DSCP[127:126]	**Ipv4 and Ipv6 mapping** _ for value 0x3F	R/W	00
5 – 4	DSCP[125:124]	**Ipv4 and Ipv6 mapping** _ for value 0x3E	R/W	00
3 – 2	DSCP[123:122]	**Ipv4 and Ipv6 mapping** _ for value 0x3D	R/W	00
1 – 0	DSCP[121:120]	**Ipv4 and Ipv6 mapping** _ for value 0x3C	R/W	00
Register 165 (0xA5): Reserved				
7 – 0	Reserved	N/A, do not change	RO	0x30
Register 176 (0xB0): Port 1 Control 8 ***Register 192 (0xC0): Port 2 Control 8*** ***Register 208 (0xD0): Port 3 Control 8*** ***Register 224 (0xE0): Port 4 Control 8*** ***Register 240 (0xF0): Port 5 Control 8***				
7 – 4	Reserved		RO	0000
3	Insert Source Port PVID for Untagged Packet Destination to Highest Egress Port Note: Enabled by the register 135 bit 2	Register 176: insert source Port 1 PVID for untagged frame at egress Port 5 Register 192: insert source Port 2 PVID for untagged frame at egress Port 5 Register 208: insert source Port 3 PVID for untagged frame at egress Port 5 Register 224: insert source Port 4 PVID for untagged frame at egress Port 5 Register 240: insert source Port 5 PVID for untagged frame at egress Port 4	R/W	0
2	Insert Source Port PVID for Untagged Packet Destination to Second Highest Egress Port Note: Enabled by the Register 135 bit 2	Register 176: insert source Port 1 PVID for untagged frame at egress pPort 4 Register 192: insert source Port 2 PVID for untagged frame at egress Port 4 Register 208: insert source Port 3 PVID for untagged frame at egress Port 4 Register 224: insert source Port 4 PVID for untagged frame at egress Port 3 Register 240: insert source Port 5 PVID for untagged frame at egress Port 3	R/W	0
1	Insert Source Port PVID for Untagged Packet Destination to Second Lowest Egress Port Note: Enabled by the Register 135 bit 2	Register 176: insert source Port 1 PVID for untagged frame at egress Port 3 Register 192: insert source Port 2 PVID for untagged frame at egress Port 3 Register 208: insert source Port 3 PVID for untagged frame at egress Port 2 Register 224: insert source Port 4 PVID for untagged frame at egress Port 2 Register 240: insert source Port 5 PVID for untagged frame at egress Port 2	R/W	0

Advanced Control Registers (Continued)

Address	Name	Description	Mode	Default
0	Insert Source Port PVID for Untagged Packet Destination to Lowest Egress Port Note: Enabled by the Register 135 bit 2	Register 176: insert source Port 1 PVID for untagged frame at egress Port 2 Register 192: insert source Port 2 PVID for untagged frame at egress Port 1 Register 208: insert source Port 3 PVID for untagged frame at egress Port 1 Register 224: insert source Port 4 PVID for untagged frame at egress Port 1 Register 240: insert source Port 5 PVID for untagged frame at egress Port 1	R/W	0
Register 177 (0xB1): Port 1 Control 9 ***Register 193 (0xC1): Port 2 Control 9*** ***Register 209 (0xD1): Port 3 Control 9*** ***Register 225 (0xE1): Port 4 Control 9*** ***Register 241 (0xF1): Port 5 Control 9***				
7 – 2	Reserved		RO	0000000
1	4 Queue Split Enable	This bit in combination with Register16/32/48/64/80 bit 0 will select the split of ½/4 queues: {Register177 bit 1, Register16 bit 0} = 11, reserved. 10, the port output queue is split into four priority queues or if map 802.1p to priority 0-3 mode. 01, the port output queue is split into two priority queues or if map 802.1p to priority 0-3 mode. 00, single output queue on the port. There is no priority differentiation even though packets are classified into high and low priority.	R/W	0
0	Enable Dropping Tag	0 = disable tag drop 1 = enable tag drop	R/W	0
Register 178 (0xB2): Port 1 Control 10 ***Register 194 (0xC2): Port 2 Control 10*** ***Register 210 (0xD2): Port 3 Control 10*** ***Register 226 (0xE2): Port 4 Control 10*** ***Register 242 (0xF2): Port 5 Control 10***				
7	Enable Port Transmit Queue 3 Ratio	0, strict priority, will transmit all the packets from this priority queue 3 before transmit lower priority queue. 1, bit [6:0] reflect the packet number allow to transmit from this priority queue 3 within a certain time.	R/W	1
6 – 0	Port Transmit Queue 3 Ratio[6:0]	Packet number for Transmit Queue 3 for highest priority packets in four queues mode.	R/W	0001000

Advanced Control Registers (Continued)

Address	Name	Description	Mode	Default
Register 179 (0xB3): Port 1 Control 11 ***Register 195 (0xC3): Port 2 Control 11*** ***Register 211 (0xD3): Port 3 Control 11*** ***Register 227 (0xE3): Port 4 Control 11*** ***Register 243 (0xF3): Port 5 Control 11***				
7	Enable Port Transmit Queue 2 Ratio	0, strict priority, will transmit all the packets from this priority queue 2 before transmit lower priority queue. 1, bit [6:0] reflect the packet number allow to transmit from this priority queue 1 within a certain time.	R/W	1
6 – 0	Port Transmit Queue 2 Ratio[6:0]	Packet number for Transmit Queue 2 for high/low priority packets in high/low priority packets in four queues mode.	R/W	0000100
Register 180 (0xB4): Port 1 Control 12 ***Register 196 (0xC4): Port 2 Control 12*** ***Register 212 (0xD4): Port 3 Control 12*** ***Register 228 (0xE4): Port 4 Control 12*** ***Register 244 (0xF4): Port 5 Control 12***				
7	Enable Port Transmit Queue 1 Rate	0, strict priority, will transmit all the packets from this priority queue 1 before transmit lower priority queue. 1, bit [6:0] reflect the packet number allow to transmit from this priority queue 1 within a certain time.	R/W	1
6 – 0	Port Transmit Queue 1 Ratio[6:0]	Packet number for Transmit Queue 1 for low/high priority packets in four queues mode and high priority packets in two queues mode.	R/W	0000010
Register 181 (0xB5): Port 1 Control 13 ***Register 197 (0xC5): Port 2 Control 13*** ***Register 213 (0xD5): Port 3 Control 13*** ***Register 229 (0xE5): Port 4 Control 13*** ***Register 245 (0xF5): Port 5 Control 13***				
7	Enable Port Transmit Queue 0 Rate	0, strict priority, will transmit all the packets from this priority queue 0 before transmit lower priority queue. 1, bit [6:0] reflect the packet number allow to transmit from this priority queue 0 within a certain time.	R/W	1
6 – 0	Port Transmit Queue 0 Ratio[6:0]	Packet number for Transmit Queue 0 for lowest priority packets in four queues mode and low priority packets in two queues mode.	R/W	0000001

Advanced Control Registers (Continued)

Address	Name	Description	Mode	Default
Register 182 (0xB6): Port 1 Rate Limit Control ***Register 198 (0xC6): Port 2 Rate Limit Control*** ***Register 214 (0xD6): Port 3 Rate Limit Control*** ***Register 230 (0xE6): Port 4 Rate Limit Control*** ***Register 246 (0xF6): Port 5 Rate Limit Control***				
7 – 5	Reserved		RO	000
4	Ingress Rate Limit Flow Control Enable	1 = Flow Control is asserted if the port's receive rate is exceeded. 0 = Flow Control is not asserted if the port's receive rate is exceeded.	R/W	0
3 – 2	Limit Mode	**Ingress Limit Mode** These bits determine what kinds of frames are limited and counted against ingress rate limiting. = 00, limit and count all frames. = 01, limit and count Broadcast, Multicast, and flooded unicast frames. = 10, limit and count Broadcast and Multicast frames only. = 11, limit and count Broadcast frames only.	R/W	00
1	Count IFG	**Count IFG bytes** = 1, each frame's minimum inter frame gap. (IFG) bytes (12 per frame) are included in Ingress and Egress rate limiting calculations. = 0, IFG bytes are not counted.	R/W	0
0	Count Pre	**Count Preamble bytes** = 1, each frame's preamble bytes (8 per frame) are included in Ingress and Egress rate limiting calculations. = 0, preamble bytes are not counted.	R/W	0
Register 183 (0xB7): Port 1 Priority 0 Ingress Limit Control 1 ***Register 199 (0xC7): Port 2 Priority 0 Ingress Limit Control 1*** ***Register 215 (0xD7): Port 3 Priority 0 Ingress Limit Control 1*** ***Register 231 (0xE7): Port 4 Priority 0 Ingress Limit Control 1*** ***Register 247 (0xF7): Port 5 Priority 0 Ingress Limit Control 1***				
7	Reserved		RO	0
6 – 0	Port-Based Priority 0 Ingress Limit	**Ingress data rate limit for priority 0 frames** Ingress traffic from this port is shaped according to the Data Rate Selected Table. See the table following the end of Egress limit control registers.	R/W	0000000

Advanced Control Registers (Continued)

Address	Name	Description	Mode	Default
Register 184 (0xB8): Port 1 Priority 1 Ingress Limit Control 2 ***Register 200 (0xC8): Port 2 Priority 1 Ingress Limit Control 2*** ***Register 216 (0xD8): Port 3 Priority 1 Ingress Limit Control 2*** ***Register 232 (0xE8): Port 4 Priority 1 Ingress Limit Control 2*** ***Register 248 (0xF8): Port 5 Priority 1 Ingress Limit Control 2***				
7	Reserved		RO	0
6 – 0	Port-Based Priority 1 Ingress Limit	**Ingress data rate limit for priority 1 frames** Ingress traffic from this port is shaped according to the Data Rate Selected Table. See the table follow the end of Egress limit control registers.	R/W	0000000
Register 185 (0xB9): Port 1 Priority 2 Ingress Limit Control 3 ***Register 201 (0xC9): Port 2 Priority 2 Ingress Limit Control 3*** ***Register 217 (0xD9): Port 3 Priority 2 Ingress Limit Control 3*** ***Register 233 (0xE9): Port 4 Priority 2 Ingress Limit Control 3*** ***Register 249 (0xF9): Port 5 Priority 2 Ingress Limit Control 3***				
7	Reserved		RO	0
6 – 0	Port-Based Priority 2 Ingress Limit	**Ingress data rate limit for priority 2 frames** Ingress traffic from this port is shaped according to the Data Rate Selected Table. See the table following the end of Egress limit control registers.	R/W	0000000
Register 186 (0xBA): Port 1 Priority 3 Ingress Limit Control 4 ***Register 202 (0xCA): Port 2 Priority 3 Ingress Limit Control 4*** ***Register 218 (0xDA): Port 3 Priority 3 Ingress Limit Control 4*** ***Register 234 (0xEA): Port 4 Priority 3 Ingress Limit Control 4*** ***Register 250 (0xFA): Port 5 Priority 3 Ingress Limit Control 4***				
7	Reserved		RO	0
6 – 0	Port-Based Priority 3 Ingress Limit	**Ingress data rate limit for priority 3 frames** Ingress traffic from this port is shaped according to the Data Rate Selected Table. See the table following the end of Egress limit control registers.	R/W	0000000
Register 187 (0xBB): Port 1 Queue 0 Egress Limit Control 1 ***Register 203 (0xCB): Port 2 Queue 0 Egress Limit Control 1*** ***Register 219 (0xDB): Port 3 Queue 0 Egress Limit Control 1*** ***Register 235 (0xEB): Port 4 Queue 0 Egress Limit Control 1*** ***Register 251 (0xFB): Port 5 Queue 0 Egress Limit Control 1***				
7	Reserved		RO	0
6 – 0	Port Queue 0 Egress Limit	**Egress data rate limit for priority 0 frames** Egress traffic from this priority queue is shaped according to the Data Rate Selected Table. See the table following the end of Egress limit control registers. In four queues mode, it is lowest priority. In two queues mode, it is low priority.	R/W	0000000

Advanced Control Registers (Continued)

Address	Name	Description	Mode	Default
Register 188 (0xBC) : Port 1 Queue 1 Egress Limit Control 2 ***Register 204 (0xCC) : Port 2 Queue 1 Egress Limit Control 2*** ***Register 220 (0xDC) : Port 3 Queue 1 Egress Limit Control 2*** ***Register 236 (0xEC) : Port 4 Queue 1 Egress Limit Control 2*** ***Register 252 (0xFC) : Port 5 Queue 1 Egress Limit Control 2***				
7	Reserved		RO	0
6 – 0	Port Queue 1 Egress Limit	**Egress data rate limit for priority 1 frames** Egress traffic from this priority queue is shaped according to the Data Rate Selected Table. See the table follow the end of Egress limit control registers. In four queues mode, it is low/high priority. In two queues mode, it is high priority.	R/W	0000000
Register 189 (0xBD): Port 1 Queue 2 Egress Limit Control 3 ***Register 205 (0xCD): Port 2 Queue 2 Egress Limit Control 3*** ***Register 221 (0xDD): Port 3 Queue 2 Egress Limit Control 3*** ***Register 237 (0xED): Port 4 Queue 2 Egress Limit Control 3*** ***Register 253 (0xFD): Port 5 Queue 2 Egress Limit Control 3***				
7	Reserved		RO	0
6 – 0	Port Queue 2 Egress Limit	**Egress data rate limit for priority 2 frames** Egress traffic from this priority queue is shaped according to the Data Rate Selected Table. See the table following the end of Egress limit control registers. In four queues mode, it is high/low priority.	R/W	0000000
Register 190 (0xBE) : Port 1 Queue 3 Egress Limit Control 4 ***Register 206 (0xCE) : Port 2 Queue 3 Egress Limit Control 4*** ***Register 222 (0xDE) : Port 3 Queue 3 Egress Limit Control 4*** ***Register 238 (0xEE): Port 4 Queue 3 Egress Limit Control 4*** ***Register 254 (0xFE): Port 5 Queue 3 Egress Limit Control 4***				
7	Reserved		RO	0
6 – 0	Port Queue 3 Egress Limit	**Egress data rate limit for priority 3 frames** Egress traffic from this priority queue is shaped according to the Data Rate Selected Table. See the table follow the end of Egress limit control registers. In four queues mode, it is highest priority.	R/W	0000000

Note:

In the port priority 0-3 ingress rate limit mode, will need to set all related ingress/egress ports to two queues or four queues mode. In the port queue 0-3 egress rate limit mode, the highest priority get exact rate limit based on the rate select table, other priorities packets rate are based upon the ratio of the Register Port Control 10/11/12/13 when use more than one egress queue per port.

Data Rate Limit Selection Limit Table

Table 14. 10/100BT Rate Selection for the Rate limit

Data Rate Limit for Ingress or Egress	**100BT** Priority/Queue 0-3 Ingress/egress limit Control Register bit [6:0] = decimal	**10BT** Priority/Queue 0-3 Ingress/egress limit Control Register bit [6:0] = decimal
	1 Mbps <= rate <= 99 Mbps rate(decimal integer 1-99)	1 Mbps <= rate <= 9 Mbps rate(decimal integer 1-9)
	0 or 100 (decimal), '0' is default value	0 or 10 (decimal), '0' is default value
Less than 1Mbps (see as below)	Decimal	
64 Kbps	7'd101	
128 Kbps	7'd102	
192 Kbps	7'd103	
256 Kbps	7'd104	
320 Kbps	7'd105	
384 Kbps	7'd106	
448 Kbps	7'd107	
512 Kbps	7'd108	
576 Kbps	7'd109	
640 Kbps	7'd110	
704 Kbps	7'd111	
768 Kbps	7'd112	
832 Kbps	7'd113	
896 Kbps	7'd114	
960 Kbps	7'd115	

Address	**Name**	**Description**	**Mode**	**Default**
Register 191(0xBF): Testing Register 1				
7 - 0	Reserved	N/A, do not change.	RO	0x80
Register 207(0xCF): Reserved Control Register				
7 - 0	Reserved	N/A, do not change.	RO	0x15
Register 223(0xDF): Testing Register 2				
7 - 0	Reserved		R/W	0x0C
Register 239(0xEF): Port 3 Copper or Fiber Control				
7	Fiber select for Port 3	0 = Port 3 is copper port (default) 1 = Port 3 is fiber port.	R/W	0
6 - 0	Reserved	N/A, Do not change.	RO	0110010
Register 255(0xFF): Testing Register 3				
7- 0	Reserved	N/A, Do not change.	RO	0x00

Static MAC Address Table

KSZ8895MQX/RQX/FQX/ML has a static and a dynamic address table. When a DA look-up is requested, both tables will be searched to make a packet forwarding decision. When an SA look-up is requested, only the dynamic table is searched for aging, migration, and learning purposes. The static DA look-up result will have precedence over the dynamic DA look-up result. If there are DA matches in both tables, the result from the static table will be used. The static table can only be accessed and controlled by an external SPI master (usually a processor). The entries in the static table will not be aged out by KSZ8895MQX/RQX/FQX/ML. An external device does all addition, modification and deletion.

Note:

Register bit assignments are different for static MAC table reads and static MAC table write, as shown in Table 15.

Table 15. Static MAC Address Table

Address	Name	Description	Mode	Default
Format of Static MAC Table for Reads (32 entries)				
63-57	FID	Filter VLAN ID, representing one of the 128 active VLANs.	RO	0000000
56	Use FID	1, use (FID+MAC) to look-up in static table. 0, use MAC only to look-up in static table.	RO	0
55	Reserved	Reserved.	RO	N/A
54	Override	1, override spanning tree “transmit enable = 0” or “receive enable = 0* setting. This bit is used for spanning tree implementation. 0, no override.	RO	0
53	Valid	1, this entry is valid, the look-up result will be used. 0, this entry is not valid.	RO	0
52-48	Forwarding Ports	The 5 bits control the forward ports, example: 00001, forward to Port 1 00010, forward to Port 2 ….. 10000, forward to Port 5 00110, forward to Port 2 and Port 3 11111, broadcasting (excluding the ingress port)	RO	00000
47-0	MAC Address (DA)	48 bit MAC address.	RO	0x0
Format of Static MAC Table for Writes (32 entries)				
62-56	FID	Filter VLAN ID, representing one of the 128 active VLANs.	W	0000000
55	Use FID	1, use (FID+MAC) to look-up in static table. 0, use MAC only to look-up in static table.	W	0
54	Override	1, override spanning tree “transmit enable = 0” or “receive enable = 0” setting. This bit is used for spanning tree implementation. 0, no override.	W	0
53	Valid	1, this entry is valid, the look-up result will be used. 0, this entry is not valid.	W	0

Table 15. Static MAC Address Table (Continued)

Address	Name	Description	Mode	Default
52-48	Forwarding Ports	The 5 bits control the forward ports, example: 00001, forward toPort 1 00010, forward to Port 2 ..... 10000, forward to Port 5 00110, forward to Port 2 and Port 3 11111, broadcasting (excluding the ingress port)	W	00000
47-0	MAC Address (DA)	48-bit MAC address.	W	0x0

Examples:

(1) Static Address Table Read (read the 2nd entry)

Write to Register 110 with 0x10 (read static table selected)

Write to Register 111 with 0x1 (trigger the read operation)

Then

Read Register 113 (63-56)

Read Register 114 (55-48)

Read Register 115 (47-40)

Read Register 116 (39-32)

Read Register 117 (31-24)

Read Register 118 (23-16)

Read Register 119 (15-8)

Read Register 120 (7-0)

(2) Static Address Table Write (write the 8th entry)

Write to Register 110 with 0x10 (read static table selected)

Write Register 113 (62-56)

Write Register 114 (55-48)

Write Register 115 (47-40)

Write Register 116 (39-32)

Write Register 117 (31-24)

Write Register 118 (23-16)

Write Register 119 (15-8)

Write Register 120 (7-0)

Write to Register 110 with 0x00 (write static table selected)

Write to Register 111 with 0x7 (trigger the write operation)

VLAN Table

The VLAN table is used for VLAN table look-up. If 802.1q VLAN mode is enabled (Register 5 bit 7 = 1), this table is used to retrieve VLAN information that is associated with the ingress packet. There are three fields for FID (filter ID), Valid, and VLAN membership in the VLAN table. The three fields must be initialized before the table is used. There is no VID field because 4096 VIDs are used as a dedicated memory address index into a 1024x52-bit memory space. Each entry has four VLANs. Each VLAN has 13 bits. Four VLANs need 52 bits. There are a total of 1024 entries to support a total of 4096 VLAN IDs by using dedicated memory address and data bits. Refer to Table 16 for details. FID has 7-bits to support 128 active VLANs.

Table 16. VLAN Table

Address	Name	Description	Mode	Initial Value suggestion
12	Valid	1, the entry is valid. 0, entry is invalid.	R/W	0
11 – 7	Membership	Specify which ports are members of the VLAN. If a DA look-up fails (no match in both static and dynamic tables), the packet associated with this VLAN will be forwarded to ports specified in this field. E.g., 11001 means port 5, port 4 and port 1.	R/W	11111
6 – 0	FID	Filter ID. KSZ8895MLU supports 128 active VLANs represented by these seven bit fields. FID is the mapped ID. If 802.1q VLAN is enabled, the look-up in MAC table will be based on FID+DA and FID+SA.	R/W	0

If 802.1q VLAN mode is enabled, KSZ8895MLU assigns a VID to every ingress packet when the packet is untagged or tagged with a null VID, the packet is assigned with the default port VID of the ingress port. If the packet is tagged with non-null VID, the VID in the tag is used. The look-up process starts from the VLAN table look-up based on VID number with its dedicated memory address and data bits. If the entry is not valid in the VLAN table, the packet is dropped and no address learning occurs. If the entry is valid, the FID is retrieved. The FID+DA and FID+SA lookups in MAC tables are performed. The FID+DA look-up determines the forwarding ports. If FID+DA fails for look-up in the MAC table, the packet is broadcast to all the members or specified members (excluding the ingress port) based on the VLAN table. If FID+SA fails, the FID+SA is learned. To communicate between different active VLANs, set the same FID; otherwise set a different FID.

The VLAN table configuration is organized as 1024 VLAN sets, each VLAN set consists of four VLAN entries, to support up to 4096 VLAN entries. Each VLAN set has 52 bits and should be read or written at the same time specified by the indirect address.

The VLAN entries in the VLAN set is mapped to indirect data registers as follow:

Entry0[12:0] maps to the VLAN set bits[12 – 0] {register119[4:0], register120[7:0]}

Entry1[12:0] maps to the VLAN set bits[25 – 13]{register117[1:0], register118[7:0], register119[7:5]}

Entry2[12:0] maps to the VLAN set bits[38 – 26]{register116[6:0], register117[7:2]}

Entry3[12:0] maps to the VLAN set bits[51 – 39]{register114[3:0], register115[7:0], register116[7]}

In order to read one VLAN entry, the VLAN set is read first and the specific VLAN entry information can be extracted. To update any VLAN entry, the VLAN set is read first then only the desired VLAN entry is updated and the whole VLAN set is written back. Due to FID in VLAN table is 7-bit, so the VLAN table supports unique 128 flow VLAN groups. Each VLAN set address is 10 bits long (Maximum is 1024) in the indirect address register 110 and 111, the bit [9 – 8] of VLAN set address is at bit [1 – 0] of register 110, and the bit [7 – 0] of VLAN set address is at bit [7-0] of register 111. Each Write and Read can access to four consecutive VLAN entries.

Examples:

(1) VLAN Table Read (read the VID=2 entry)

Write the indirect control and address registers first

Write to Register 110 (0x6E) with 0x14 (read VLAN table selected)

Write to Register 111 (0x6F) with 0x0 (trigger the read operation for VID=0, 1, 2, 3 entries)

Then read the indirect data registers bits [38-26] for VID=2 entry

Read Register 116 (0x74), (register 116 [6:0] are bits 12 – 6 of VLAN VID=2 entry)

Read Register 117 (0x75), (register 117 [7:2] are bits 5 – 0 of VLAN VID=2 entry)

(2) VLAN Table Write (write the VID=10 entry)

Read the VLAN set that contains VID=8, 9, 10, 11.

Write to Register 110 (0x6E) with 0x14 (read VLAN table selected)

Write to Register 111 (0x6F) with 0x02 (trigger the read operation and VID=8, 9, 10, 11 indirect address)

Read the VLAN set first by the indirect data registers 114, 115, 116, 117, 118, 119, 120.

Modify the indirect data registers bits [38 – 26] by the register 116 bit [6-0] and register 117 bit [7 – 2] as follows:

Write to Register 116 (0x74), (register116 [6:0] are bits 12 – 6 of VLAN VID=10 entry)

Write to Register 117 (0x75), (register117 [7:2] are bits 5 – 0 of VLAN VID=10 entry)

Then write the indirect control and address registers

Write to Register 110 (0x6E) with 0x04 (write VLAN table selected)

Write to Register 111 (0x6F) with 0x02 (trigger the write operation and VID = 8, 9, 10, 11 indirect address)

Table 17 shows the relationship of the indirect address/data registers and VLAN ID.

Table 17. VLAN ID and Indirect Registers

Indirect Address High/Low Bit[9-0] for VLAN Sets	Indirect Data Registers Bits for Each VLAN Entry	VID Numbers	VID bit[12-2] in VLAN Tag	VID bit[1-0] in VLAN Tag
0	Bits[12 – 0]	0	0	0
0	Bits[25 – 13]	1	0	1
0	Bits[38 – 26]	2	0	2
0	Bits[51 – 39]	3	0	3
1	Bits[12 – 0]	4	1	0
1	Bits[25 – 13]	5	1	1
1	Bits[38 – 26]	6	1	2
1	Bits[51 – 39]	7	1	3
2	Bits[12 – 0]	8	2	0
2	Bits[25 – 13]	9	2	1
2	Bits[38 – 26]	10	2	2
2	Bits[51 – 39]	11	2	3
1023	Bits[12 – 0]	4092	1023	0
1023	Bits[25 – 13]	4093	1023	1
1023	Bits[38 – 26]	4094	1023	2
1023	Bits[51 – 39]	4095	1023	3

Dynamic MAC Address Table

This table is read only. The contents are maintained by the KSZ8895MQX/RQX/FQX/ML only.

Table 18. Dynamic MAC Address Table

Address	Name	Description	Mode	Default
Format of Dynamic MAC Address Table (1K entries)				
71	MAC Empty	1, there is no valid entry in the table. 0, there are valid entries in the table.	RO	1
70-61	No of Valid Entries	Indicates how many valid entries in the table. 0x3ff means 1K entries 0x1 and bit 71 = 0: means 2 entries 0x0 and bit 71 = 0: means 1 entry 0x0 and bit 71 = 1: means 0 entry	RO	0
60-59	Time Stamp	2-bit counters for internal aging	RO	
58-56	Source Port	The source port where FID+MAC is learned. 000 Port 1 001 Port 2 010 Port 3 011 Port 4 100 Port 5	RO	0x0
55	Data Ready	1, The entry is not ready, retry until this bit is set to 0. 0, The entry is ready.	RO	
54-48	FID	Filter ID.	RO	0x0
47-0	MAC Address	48-bit MAC address.	RO	0x0

Examples:

(1) Dynamic MAC Address Table Read (read the 1st entry), and retrieve the MAC table size

Write to Register 110 with 0x18 (read dynamic table selected)

Write to Register 111 with 0x0 (trigger the read operation) and then

Read Register 112 (71-64)

Read Register 113 (63-56); // the above two registers show # of entries

Read Register 114 (55-48) // if bit 55 is 1, restart (reread) from this register

Read Register 115 (47-40)

Read Register 116 (39-32)

Read Register 117 (31-24)

Read Register 118 (23-16)

Read Register 119 (15-8)

Read Register 120 (7-0)

(2) Dynamic MAC Address Table Read (read the 257th entry), without retrieving # of entries information

Write to Register 110 with 0x19 (read dynamic table selected)

Write to Register 111 with 0x1 (trigger the read operation) and then

Read Register 112 (71-64)

Read Register 113 (63-56)

Read Register 114 (55-48) // if bit 55 is 1, restart (reread) from this register

Read Register 115 (47-40)

Read Register 116 (39-32)

Read Register 117 (31-24)

Read Register 118 (23-16)

Read Register 119 (15-8)

Read Register 120 (7-0)

MIB (Management Information Base) Counters

The MIB counters are provided on per port basis. These counters are read using indirect memory access as below:

For Port 1

Table 19. Port 1 MIB Counter Indirect Memory Offsets

Offset	Counter Name	Description
0x0	RxLoPriorityByte	Rx low-priority (default) octet count including bad packets.
0x1	RxHiPriorityByte	Rx hi-priority octet count including bad packets.
0x2	RxUndersizePkt	Rx undersize packets w/good CRC.
0x3	RxFragments	Rx fragment packets w/bad CRC, symbol errors or alignment errors.
0x4	RxOversize	Rx oversize packets w/good CRC (max: 1536 or 1522 bytes).
0x5	RxJabbers	Rx packets longer than 1522B w/either CRC errors, alignment errors, or symbol errors (depends on max packet size setting) or Rx packets longer than 1916B only.
0x6	RxSymbolError	Rx packets w/ invalid data symbol and legal preamble, packet size.
0x7	RxCRCerror	Rx packets within (64,1522) bytes w/an integral number of bytes and a bad CRC (upper limit depends on max packet size setting).
0x8	RxAlignmentError	Rx packets within (64,1522) bytes w/a non-integral number of bytes and a bad CRC (upper limit depends on max packet size setting).
0x9	RxControl8808Pkts	The number of MAC control frames received by a port with 88-08h in EtherType field.
0xA	RxPausePkts	The number of PAUSE frames received by a port. PAUSE frame is qualified with EtherType (88-08h), DA, control opcode (00-01), data length (64B min), and a valid CRC.
0xB	RxBroadcast	Rx good broadcast packets (not including errored broadcast packets or valid multicast packets).
0xC	RxMulticast	Rx good multicast packets (not including MAC control frames, errored multicast packets or valid broadcast packets).
0xD	RxUnicast	Rx good unicast packets.
0xE	Rx64Octets	Total Rx packets (bad packets included) that were 64 octets in length.
0xF	Rx65to127Octets	Total Rx packets (bad packets included) that are between 65 and 127 octets in length.
0x10	Rx128to255Octets	Total Rx packets (bad packets included) that are between 128 and 255 octets in length.
0x11	Rx256to511Octets	Total Rx packets (bad packets included) that are between 256 and 511 octets in length.
0x12	Rx512to1023Octets	Total Rx packets (bad packets included) that are between 512 and 1023 octets in length.
0x13	Rx1024to1522Octets	Total Rx packets (bad packets included) that are between 1024 and 1522 octets in length (upper limit depends on max packet size setting).
0x14	TxLoPriorityByte	Tx low-priority good octet count, including PAUSE packets.
0x15	TxHiPriorityByte	Tx hi-priority good octet count, including PAUSE packets.
0x16	TxLateCollision	The number of times a collision is detected later than 512 bit-times into the Tx of a packet.
0x17	TxPausePkts	The number of PAUSE frames transmitted by a port.
0x18	TxBroadcastPkts	Tx good broadcast packets (not including errored broadcast or valid multicast packets).
0x19	TxMulticastPkts	Tx good multicast packets (not including errored multicast packets or valid broadcast packets).
0x1A	TxUnicastPkts	Tx good unicast packets.
0x1B	TxDeferred	Tx packets by a port for which the 1st Tx attempt is delayed due to the busy medium.

Table 19. Port 1 MIB Counter Indirect Memory Offsets (Continued)

Offset	Counter Name	Description
0x1C	TxTotalCollision	Tx total collision, half-duplex only.
0x1D	TxExcessiveCollision	A count of frames for which Tx fails due to excessive collisions.
0x1E	TxSingleCollision	Successfully Tx frames on a port for which Tx is inhibited by exactly one collision.
0x1F	TxMultipleCollision	Successfully Tx frames on a port for which Tx is inhibited by more than one collision.

For Port 2

The base is 0x20, same offset definition (0x20-0x3f).

For Port 3

The base is 0x40, same offset definition (0x40-0x5f).

For Port 4

The base is 0x60, same offset definition (0x60-0x7f).

For Port 5

The base is 0x80, same offset definition (0x80-0x9f).

Table 20. Format of "Per Port" MIB Counter

Address	Name	Description	Mode	Default
Format of Per Port MIB Counters (16 entries)				
31	Overflow	1, Counter overflow. 0, No Counter overflow.	RO	0
30	Count Valid	1, Counter value is valid. 0, Counter value is not valid.	RO	0
29-0	Counter Values	Counter value.	RO	0

Table 21. All Port Dropped Packet MIB Counters

Offset	Counter Name	Description
0x100	Port1 Tx Drop Packets	Tx packets dropped due to lack of resources.
0x101	Port2 Tx Drop Packets	Tx packets dropped due to lack of resources.
0x102	Port3 Tx Drop Packets	Tx packets dropped due to lack of resources.
0x103	Port4 Tx Drop Packets	Tx packets dropped due to lack of resources.
0x104	Port5 Tx Drop Packets	Tx packets dropped due to lack of resources.
0x105	Port1 Rx Drop Packets	Rx packets dropped due to lack of resources.
0x106	Port2 Rx Drop Packets	Rx packets dropped due to lack of resources.
0x107	Port3 Rx Drop Packets	Rx packets dropped due to lack of resources.
0x108	Port4 Rx Drop Packets	Rx packets dropped due to lack of resources.
0x109	Port5 Rx Drop Packets	Rx packets dropped due to lack of resources.

Table 22. Format of "All Dropped Packet" MIB Counter

Address	Name	Description	Mode	Default
Format of All Port Dropped Packet MIB Counters				
30-16	Reserved	Reserved.	N/A	N/A
15-0	Counter Values	Counter value.	RO	0

Note:

All port dropped packet MIB counters do not indicate overflow or validity; therefore the application must keep track of overflow and valid conditions.

The KSZ8895MQX/RQX/FQX/ML provides a total of 34 MIB counters per port. These counters are used to monitor the port detail activity for network management and maintenance. These MIB counters are read using indirect memory access, per the following examples.

Programming Examples:

(1) MIB counter read (read port 1 Rx64Octets counter)

Write to Register 110 with 0x1c (read MIB counters selected)

Write to Register 111 with 0xe (trigger the read operation)

Then

Read Register 117 (counter value 31-24)

// If bit 31 = 1, there was a counter overflow

// If bit 30 = 0, restart (reread) from this register

Read Register 118 (counter value 23-16)

Read Register 119 (counter value 15-8)

Read Register 120 (counter value 7-0)

(2) MIB counter read (read port 2 Rx64Octets counter)

Write to Register 110 with 0x1c (read MIB counter selected)

Write to Register 111 with 0x2e (trigger the read operation)

Then

Read Register 117 (counter value 31-24)

//If bit 31 = 1, there was a counter overflow

//If bit 30 = 0, restart (reread) from this register

Read Register 118 (counter value 23-16)

Read Register 119 (counter value 15-8)

Read Register 120 (counter value 7-0)

(3) MIB counter read (read port 1 tx drop packets)

Write to Register 110 with 0x1d

Write to Register 111 with 0x00

Then

Read Register 119 (counter value 15-8)

Read Register 120 (counter value 7-0)

Note:

To read out all the counters, the best performance over the SPI bus is (160+3) × 8 × 80 = 104us, where there are 255 registers, 3 overhead, 8 clocks per access, at 12.5MHz. In the heaviest condition, the byte counter will overflow in 2 minutes. It is recommended that the software read all the counters at least every 30 seconds. The per port MIB counters are designed as “read clear.” A per port MIB counter will be cleared after it is accessed. All port dropped packet MIB counters are not cleared after they are accessed. The application needs to keep track of overflow and valid conditions on these counters.

MIIM Registers

All the registers defined in this section can be also accessed via the SPI interface. Note: different mapping mechanisms are used for MIIM and SPI. The “PHYAD” defined in IEEE is assigned as “0x1” for Port 1, “0x2” for Port 2, “0x3” for Port 3, “0x4” for Port 4, and “0x5” for Port 5. The “REGAD” supported are 0x0-0x5 (0h-5h), 0x1D (1dh) and 0x1F (1fh).

Address	Name	Description	Mode	Default
Register 0h: MII Control				
15	Soft Reset	1, PHY soft reset. 0, Normal operation.	R/W (SC)	0
14	Loop Back	1 = Perform MAC loopback, loop back path as follows: Assume the loop-back is at Port 1 MAC, Port 2 is the monitor port. Port 1 MAC Loopback (Port 1 reg. 0, bit 14 = ‘1’) Start: RXP2/RXM2 (Port 2). Can also start from port 3, 4, 5 Loopback: MAC/PHY interface of Port 1’s MAC End: TXP2/TXM2 (Port 2). Can also end at Ports 3, 4, 5 respectively Setting address ox3,4,5 reg. 0, bit 14 = ‘1’ will perform MAC loopback on Ports 3, 4, 5 respectively. 0 = Normal Operation.	R/W	0
13	Force 100	1, 100Mbps. 0, 10Mbps.	R/W	1
12	AN Enable	1, Auto-negotiation enabled. 0, Auto-negotiation disabled.	R/W	1
11	Power Down	1, Power down. 0, Normal operation.	R/W	0
10	PHY Isolate	1, Electrical PHY isolation of PHY from Tx+/Tx-. 0, Normal operation.	R/W	0
9	Restart AN	1, Restart Auto-negotiation. 0, Normal operation.	R/W	0
8	Force Full Duplex	1, Full duplex. 0, Half duplex.	R/W	0
7	Collision Test	Not supported.	RO	0
6	Reserved		RO	0
5	Hp_mdix	1 = HP Auto MDI/MDI-X mode. 0 = Micrel Auto MDI/MDI-X mode.	R/W	1
4	Force MDI	1, Force MDI. 0, Normal operation. (MDIX transmit on TXP/TXM pair)	R/W	0
3	Disable Auto MDI/MDI-X	1, Disable auto MDI/MDI-X. 0, Enable auto MDI/MDI-X.	R/W	0
2	Disable far End fault	1, Disable far end fault detection. 0, Normal operation.	R/W	0

MIIM Registers (Continued)

Address	Name	Description	Mode	Default
1	Disable Transmit	1, Disable transmit. 0, Normal operation.	R/W	0
0	Disable LED	1, Disable LED. 0, Normal operation.	R/W	0
Register 1h: MII Status				
15	T4 Capable	0, Not 100 BASET4 capable.	RO	0
14	100 Full Capable	1, 100BASE-TX full-duplex capable. 0, Not capable of 100BASE-TX full-duplex.	RO	1
13	100 Half Capable	1, 100BASE-TX half-duplex capable. 0, Not 100BASE-TX half-duplex capable.	RO	1
12	10 Full Capable	1, 10BASE-T full-duplex capable. 0, Not 10BASE-T full-duplex capable.	RO	1
11	10 Half Capable	1, 10BASE-T half-duplex capable. 0, 10BASE-T half-duplex capable.	RO	1
10-7	Reserved		RO	0
6	Preamble Suppressed	Not supported.	RO	0
5	AN Complete	1, Auto-negotiation complete. 0, Auto-negotiation not completed.	RO	0
4	far End fault	1, far end fault detected. 0, No far end fault detected.	RO	0
3	AN Capable	1, Auto-negotiation capable. 0, Not auto-negotiation capable.	RO	1
2	Link Status	1, Link is up. 0, Link is down.	RO	0
1	Jabber Test	Not supported.	RO	0
0	Extended Capable	0, Not extended register capable.	RO	0
Register 2h: PHYID HIGH				
15-0	Phyid High	High order PHYID bits.	RO	0x0022
Register 3h: PHYID LOW				
15-0	Phyid Low	Low order PHYID bits.	RO	0x1450
Register 4h: Advertisement Ability				
15	Next Page	Not supported.	RO	0
14	Reserved		RO	0
13	Remote fault	Not supported.	RO	0
12-11	Reserved		RO	0
10	Pause	1, Advertise pause ability. 0, Do not advertise pause ability.	R/W	1
9	Reserved		R/W	0

MIIM Registers (Continued)

Address	Name	Description	Mode	Default
8	Adv 100 Full	1, Advertise 100 full-duplex ability. 0, Do not advertise 100 full-duplex ability.	R/W	1
7	Adv 100 Half	1, Advertise 100 half-duplex ability. 0, Do not advertise 100 half-duplex ability.	R/W	1
6	Adv 10 Full	1, Advertise 10 full-duplex ability. 0, Do not advertise 10 full-duplex ability.	R/W	1
5	Adv 10 Half	1, Advertise 10 half-duplex ability. 0, Do not advertise 10 half-duplex ability.	R/W	1
4-0	Selector Field	802.3	RO	00001
Register 5h: Link Partner Ability				
15	Next Page	Not supported.	RO	0
14	LP ACK	Not supported.	RO	0
13	Remote fault	Not supported.	RO	0
12-11	Reserved		RO	0
10	Pause	1, link partner flow control capable. 0, link partner not flow control capable.	RO	0
9	Reserved		RO	0
8	Adv 100 Full	1, link partner 100BT full-duplex capable. 0, link partner not 100BT full-duplex capable.	RO	0
7	Adv 100 Half	1, link partner 100BT half-duplex capable. 0, link partner not 100BT half-duplex capable.	RO	0
6	Adv 10 Full	1, link partner 10BT full-duplex capable. 0, link partner not 10BT full-duplex capable.	RO	0
5	Adv 10 Half	1, link partner 10BT half-duplex capable. 0, link partner not 10BT half-duplex capable.	RO	0
4-0	Reserved		RO	00001
Register 1dh: LinkMD Control/Status				
15	Vct_enable	1 = Enable cable diagnostic. AfterVCT test has completed, this bit will be self-cleared. 0 = Indicate cable diagnostic test (if enabled) has completed and the status information is valid for read.	R/W (SC)	0
14-13	Vct_result	00 = Normal condition 01 = Open condition detected in cable 10 = Short condition detected in cable 11 = Cable diagnostic test has failed	RO	00
12	Vct 10M Short	1 = Less than 10 meter short	RO	0
11-9	Reserved		RO	0
8-0	Vct_fault_count	Distance to the fault. It's approximately 0.4m*vct_fault_count[8:0]	RO	000000000

MIIM Registers (Continued)

Address	Name	Description	Mode	Default
Register 1fh: PHY Special Control/Status				
15-11	Reserved		RO	00000
10-8	Port Operation Mode Indication	Indicate the current state of port operation mode: [000] = reserved [001] = still in auto-negotiation [010] = 10BASE-T half duplex [011] = 100BASE-TX half duplex [100] = reserved [101] = 10BASE-T full duplex [110] = 100BASE-TX full duplex [111] = PHY/MII isolate	RO	000
7-6	Reserved	N/A, don't change	RO	00
5	Polrvs	1 = Polarity is reversed 0 = Polarity is not reversed	RO	0
4	MDI-X status	1 = MDI 0 = MDI-X	RO	0
3	Force_lnk	1 = Force link pass 0 = Normal operation	R/W	0
2	Pwrsave	1 = Enable power save 0 = Disable power save	R/W	0
1	Remote Loopback	1 = Perform Remote loopback, loop back path as follows: Port 1 (PHY ID address 0x1 reg. 1f, bit 1 = '1') Start: RXP1/RXM1 (port 1) Loopback: PMD/PMA of port 1's PHY End: TXP1/TXM1 (port 1) Setting PHY ID address 0x2,3,4,5 reg. 1f, bit 1 = '1' will perform remote loopback on port 2, 3, 4, 5. 0 = Normal Operation.	R/W	0
0	Reserved		RO	0

Absolute Maximum Ratings[7]

Supply Voltage
- (V_{DDAR}, V_{DDAP}, V_{DDC}) ..... –0.5V to +2.4V
- (V_{DDAT}, V_{DDIO}) ..... –0.5V to +4.0V

Input Voltage ..... –0.5V to +4.0V
Output Voltage ..... –0.5V to +4.0V
Lead Temperature (soldering, 10s)..... 260°C
Storage Temperature (T_S)..... –55°C to +150°C
HBM ESD Rating.....5KV

Operating Ratings[8]

Supply Voltage
- (V_{DDAR}, V_{DDC}).....1.140V to 1.320V
- (V_{DDAT}) .....3.135V to 3.465V
- (V_{DDIO} @ 3.3V).....3.135V to 3.465V
- (V_{DDIO} @ 2.5V) .....2.375V to 2.625V
- (V_{DDIO} @ 1.8V) .....1.710V to 1.890V

Ambient Temperature (T_A)
- Commercial .....–0°C to +70°C
- Industrial.....–40°C to +85°C

Maximum Junction Temperature (T_J) .....125°C
128-Pin Package Thermal Resistance[9]
- PQFP Thermal Resistance (θ_{JA}) ..... 41.54°C/W
- PQFP Thermal Resistance (θ_{JC}) ..... 19.78°C/W
- LQFP Thermal Resistance (θ_{JA})..... 48.22°C/W
- LQFP Thermal Resistance (θ_{JC}) ..... 13.95°C/W

Electrical Characteristics[10,11]

V_{IN} = 1.2V/3.3V (typical); T_A = 25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
100BASE-TX Operation—All Ports 100% Utilization						
I_{DX}	100BASE-TX (Transmitter) 3.3V Analog	V_{DDAT}		86		mA
I_{Dda}	100BASE-TX 1.2V Analog	V_{DDAR}		22		mA
I_{DDc}	100BASE-TX 1.2V Digital	V_{DDC}		42		mA
I_{DDIO}	100BASE-TX (Digital IO) Standalone 5-port	V_{DDIO}		2.4		mA
I_{DDIO}	3.3V Digital IO SW5-MII MAC/PHY + P5-MII	V_{DDIO}		22/38		mA
I_{DDIO}	3.3V Digital IO SW5-RMII + P5-RMII	V_{DDIO}		39		mA
10BASE-T Operation —All Ports 100% Utilization						
I_{DX}	10BASE-T (Transmitter) 3.3V Analog	V_{DDAT}		107		mA
I_{Dda}	10BASE-T 1.2V Analog	V_{DDAR}		8.6		mA
I_{DDc}	10BASE-T 1.2V Digital	V_{DDC}		44		mA
I_{DDIO}	10BASE-TX (Digital IO) Standalone 5-port	V_{DDIO}		2.2		mA
I_{DDIO}	3.3V Digital IO SW5-MII MAC/PHY + P5-MII	V_{DDIO}		5/18		mA
I_{DDIO}	3.3V Digital IO SW5-RMII + P5-RMII	V_{DDIO}		29		mA

Notes:

7. Exceeding the absolute maximum rating may damage the device.
8. The device is not guaranteed to function outside its operating rating. Unused inputs must always be tied to an appropriate logic voltage level (ground or V_{DD}).
9. No heat spreader in package. The thermal junction to ambient (θ_{JA}) and the thermal junction to case (θ_{JC}) are under air velocity 0m/s.
10. Specification for packaged product only. There is no an additional transformer consumption due to use on chip termination technology with internal biasing for 10Bese-T and 100Base-TX.
11. Measurements were taken with operating ratings.

Electrical Characteristics[10,11] (Continued)

V_{IN} = 1.2V/3.3V (typical); T_A = 25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Auto-Negotiation Mode						
I_{DX}	10BASE-T (Transmitter) 3.3V Analog	V_{DDAT}		55		mA
I_{Dda}	10BASE-T 1.2V Analog	V_{DDAR}		22		mA
I_{EDM}	10BASE-T 1.2V Digital	V_{DDC}		46		mA
I_{DDIO}	10BASE-T (Digital IO) Standalone 5-Port	V_{DDIO}		1.5		mA
Power Management Mode (Standalone)						
I_{HPDM1}	Hardware Power-Down Mode 3.3V	V_{DDAT} + V_{DDIO}		2		mA
I_{HPDM2}	Hardware Power-Down Mode 1.2V	$V_{DDAR + VDDC}$		1		mA
I_{PSM1}	Power-Saving Mode 3.3V	V_{DDAT} + V_{DDIO}		35		mA
I_{PSM2}	Power-Saving Mode 1.2V	$V_{DDAR + VDDC}$		55		mA
I_{SPDM1}	Soft Power-Down Mode 3.3V	V_{DDAT} + V_{DDIO}		2		mA
I_{SPDM2}	Soft Power-Down Mode 1.2V	$V_{DDAR + VDDC}$		1.8		mA
I_{EDM1}	Energy-Detect Mode + PLL OFF 3.3V	V_{DDAT} + V_{DDIO}		5.5		mA
I_{EDM2}	Energy-Detect Mode + PLL OFF 1.2V	$V_{DDAR + VDDC}$		1.5		mA
CMOS Inputs						
V_{IH}	Input High Voltage (VDDIO = 3.3/2.5/1.8V)		2.0/1.8/1.3			V
V_{IL}	Input Low Voltage (VDDIO = 3.3/2.5/1.8V)				0.8/0.7/0.5	V
I_{IN}	Input Current (excluding Pull-up/Pull-down)	V_{IN} = GND ~ V_{DDIO}	–10		10	µA
CMOS Outputs						
V_{OH}	Output High Voltage (VDDIO = 3.3/2.5/1.8V)	I_{OH} = –8mA	2.4/2.0/1.5			V
V_{OL}	Output Low Voltage (VDDIO = 3.3/2.5/1.8V)	I_{OL} = 8mA			0.4/0.4/0.3	V
I_{OZ}	Output Tri-State Leakage	V_{IN} = GND ~ V_{DDIO}			10	µA
100BASE-TX/FX Transmit (measured differentially after 1:1 transformer)						
V_O	Peak Differential Output Voltage	100Ω termination on the differential output	0.95		1.05	V
V_{IMB}	Output Voltage Imbalance	100Ω termination on the differential output			2	%
t_r t_t	Rise/Fall Time		3		5	ns
	Rise/Fall Time Imbalance		0		0.5	ns
	Duty Cycle Distortion				±0.5	ns
	Overshoot				5	%
	Output Jitters	Peak-to-peak	0	0.75	1.4	ns

Electrical Characteristics[10,11] (Continued)

V_{IN} = 1.2V/3.3V (typical); T_A = 25°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
100BASE-FX Receiver						
V_{IST}	Input Signal Threshold Voltage	100Ω Impedance on RX±	400			mV
V_{FXSD}	FXSD Signal-Detect Voltage Threshold	≥1.2V: FX signal detect mode <1.2V: Non-signal detect mode		1.2		V
10BASE-T Receive						
V_{SQ}	Squelch Threshold	5MHz square wave	300	400	585	mV
10BASE-T Transmit (measured differentially after 1:1 transformer) V_{DDAT} = 3.3V						
V_P	Peak Differential Output Voltage	100Ω termination on the differential output	2.2	2.5	2.8	V
	Output Jitters	Peak-to-peak		1.4	3.5	ns
	Rise/fall Times			28	30	ns

Timing Diagrams

EEPROM Timing

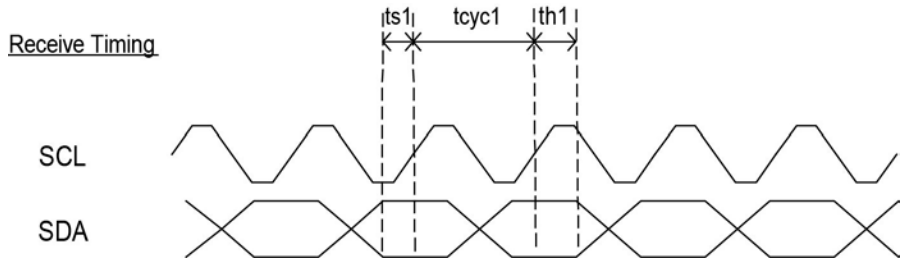


Figure 19. EEPROM Interface Input Receive Timing Diagram

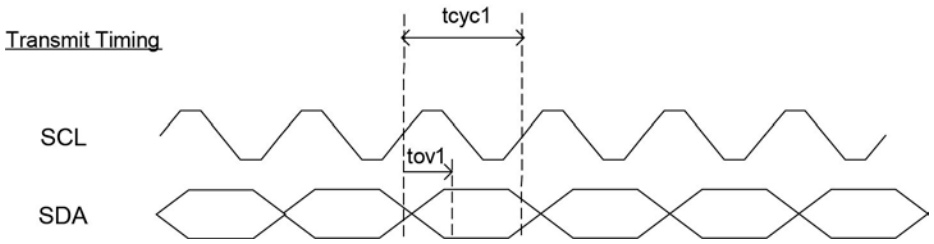


Figure 20. EEPROM Interface Output Transmit Timing Diagram

Table 23. EEPROM Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{CYC1}	Clock Cycle		16384		ns
t_{S1}	Set-Up Time	20			ns
t_{H1}	Hold Time	20			ns
t_{OV1}	Output Valid	4096	4112	4128	ns

SNI Timing

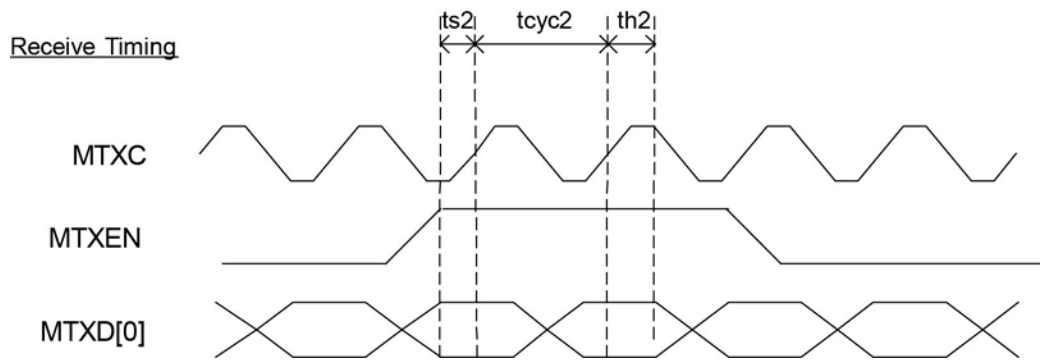


Figure 21. SNI Input Timing

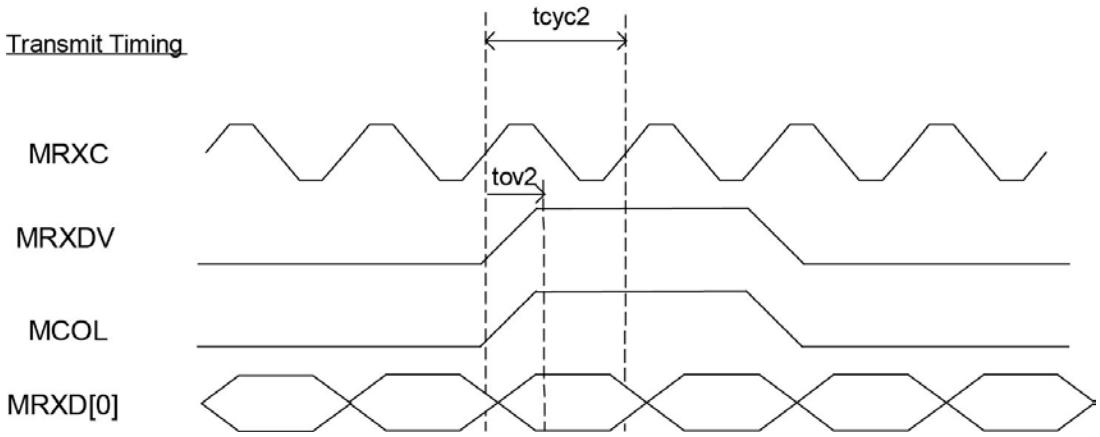


Figure 22. SNI Output Timing

Table 24. SNI Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{CYC2}	Clock Cycle		100		ns
t_{S2}	Set-Up Time	10			ns
t_{H2}	Hold Time	0			ns
t_{O2}	Output Valid	0	3	6	ns

MII Timing

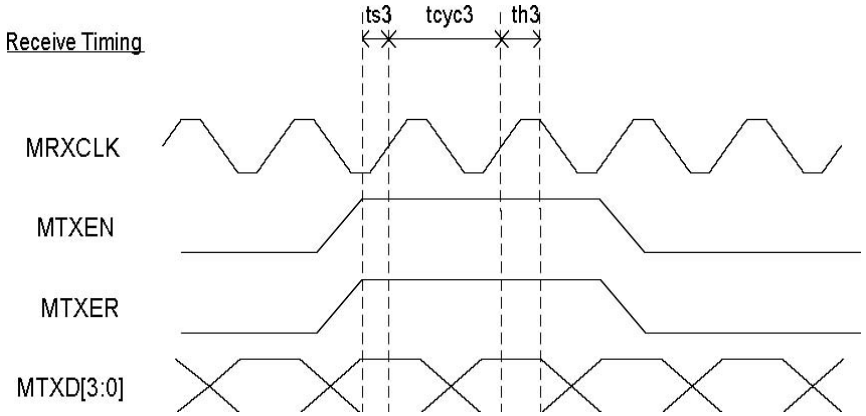


Figure 23. MAC Mode MII Timing – Data Received from MII

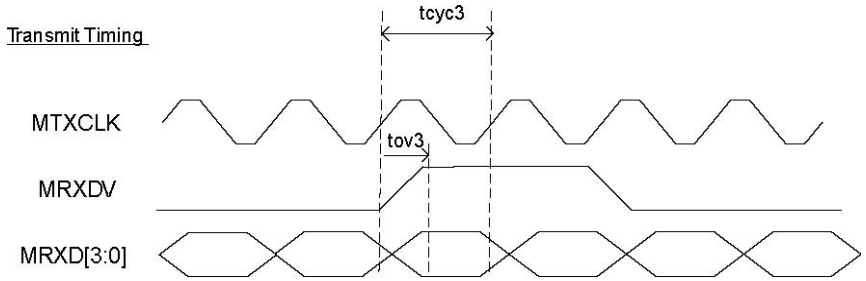


Figure 24. MAC Mode MII Timing – Data Transmitted from MII

Table 25. MAC Mode MII Timing Parameters

Symbol	Parameter	Min.	Typ.	10Base-T/100Base-TX	
				Max.	Units
t_{CYC3}	Clock Cycle		400/40		ns
t_{S3}	Set-Up Time	10			ns
t_{H3}	Hold Time	5			ns
t_{OV3}	Output Valid	3	7	25	ns

MII Timing (Continued)

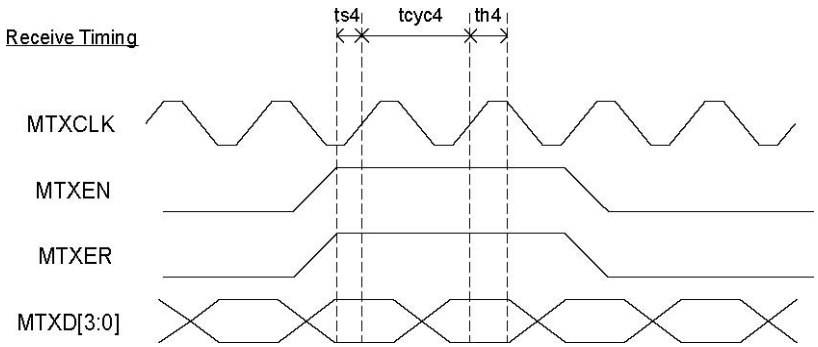


Figure 25. PHY Mode MII Timing – Data Received from MII

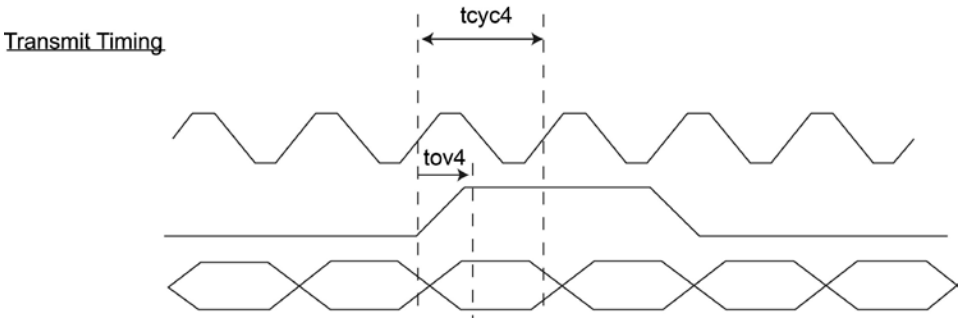


Figure 26. PHY Mode MII Timing – Data Transmitted from MII

Table 26. PHY Mode MII Timing Parameters

Symbol	Parameter	Min.	Typ.	10BaseT/100BaseT	
				Max.	Units
t_{CYC4}	Clock Cycle		400/40		ns
t_{S4}	Set-Up Time	10			ns
t_{H4}	Hold Time	0			ns
t_{OV4}	Output Valid	16	20	25	ns

RMII Timing

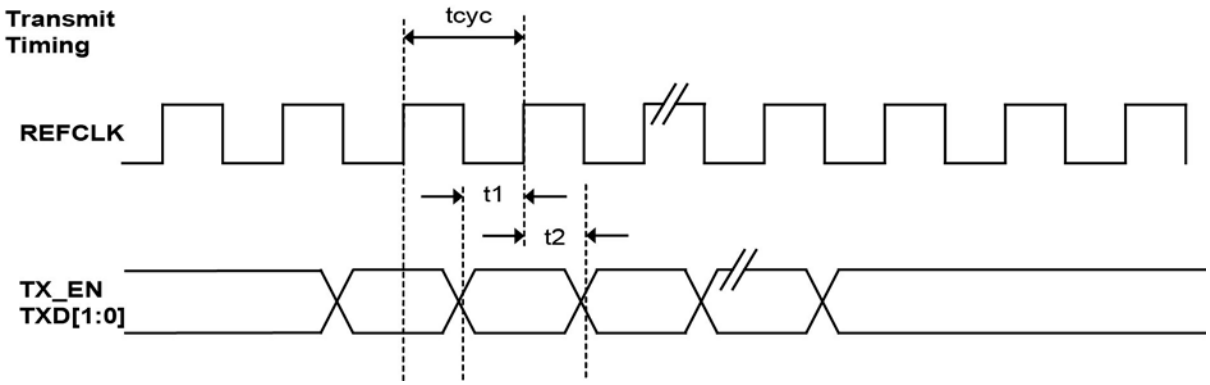


Figure 27. RMII Timing – Data Received from RMII

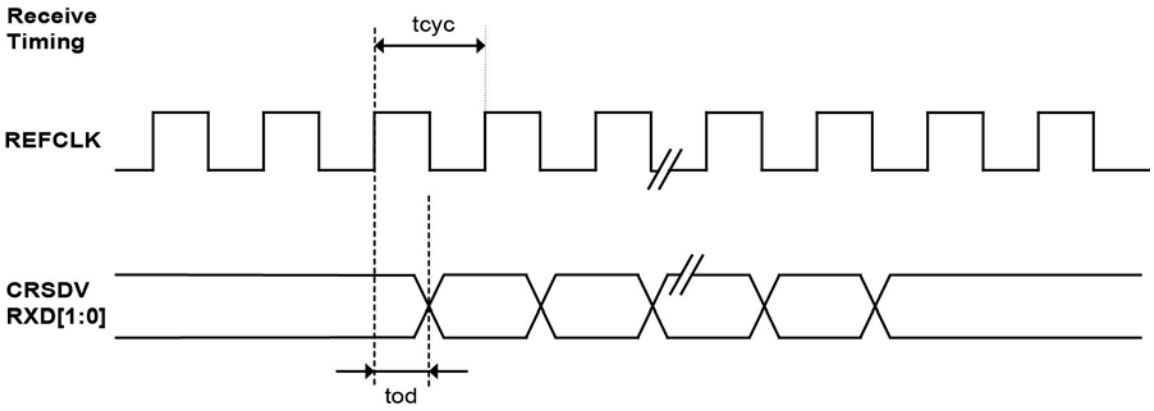


Figure 28. RMII Timing – Data Transmitted to RMII

Table 27. RMII Timing Parameters

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_{cyc}	Clock cycle		20		ns
t_1	Setup time	4			ns
t_2	Hold time	2			ns
t_{od}	Output delay	3		14	ns

SPI Timing

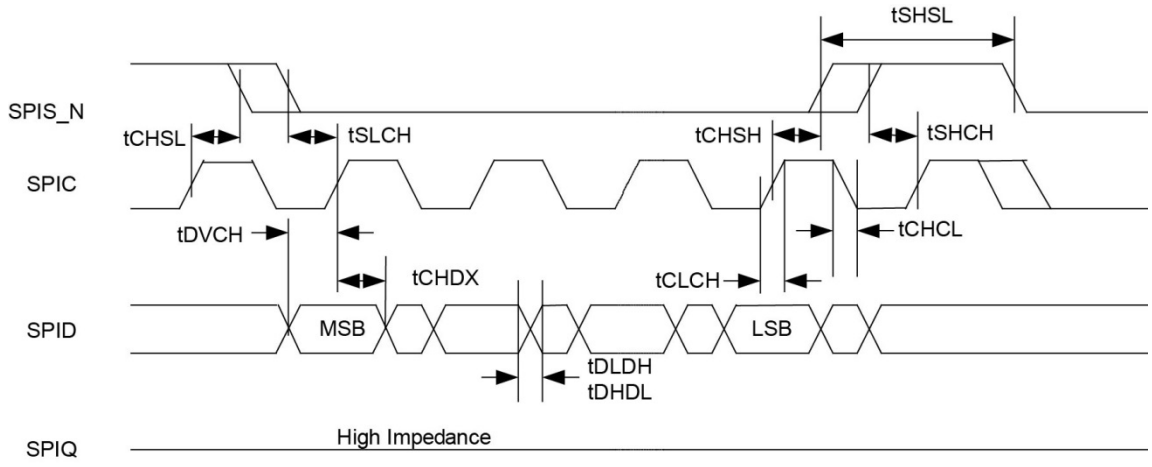


Figure 29. SPI Input Timing

Table 28. SPI Input Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units
f_C	Clock Frequency			25	MHz
t_{CHSL}	SPIS_N Inactive Hold Time	10			ns
t_{SLCH}	SPIS_N Active Set-Up Time	10			ns
t_{CHSH}	SPIS_N Active Hold Time	10			ns
t_{SHCH}	SPIS_N Inactive Set-Up Time	10			ns
t_{SHSL}	SPIS_N Deselect Time	20			ns
t_{DVCH}	Data Input Set-Up Time	5			ns
t_{CHDX}	Data Input Hold Time	5			ns
t_{CLCH}	Clock Rise Time			1	µs
t_{CHCL}	Clock fall Time			1	µs
t_{DLDH}	Data Input Rise Time			1	µs
t_{DHDL}	Data Input fall Time			1	µs

SPI Timing (Continued)

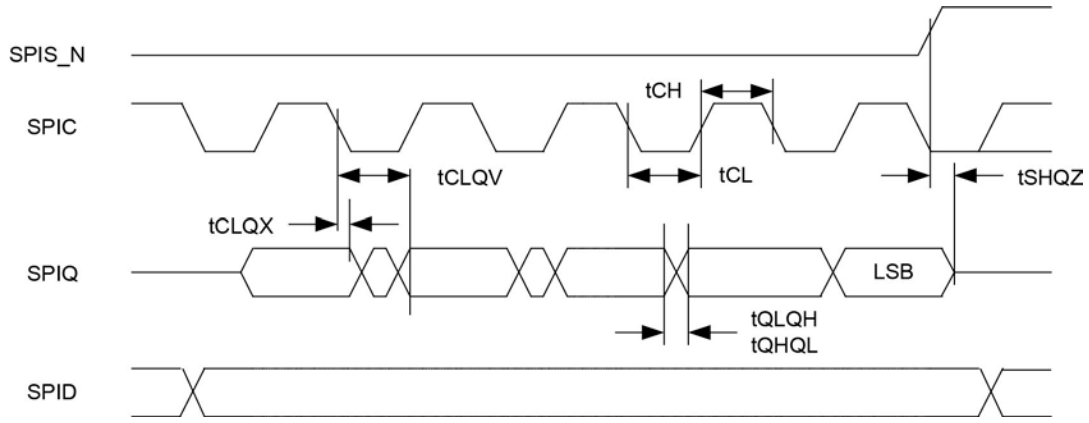


Figure 30. SPI Output Timing

Table 29. SPI Output Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units
f_C	Clock Frequency			25	MHz
t_{CLQX}	SPIQ Hold Time	0		0	ns
t_{CLQV}	Clock Low to SPIQ Valid			15	ns
t_{CH}	Clock High Time	18			ns
t_{CL}	Clock Low Time	18			ns
t_{QLQH}	SPIQ Rise Time			50	ns
t_{QHQL}	SPIQ fall Time			50	ns
t_{SHQZ}	SPIQ Disable Time			15	ns

Auto-Negotiation Timing

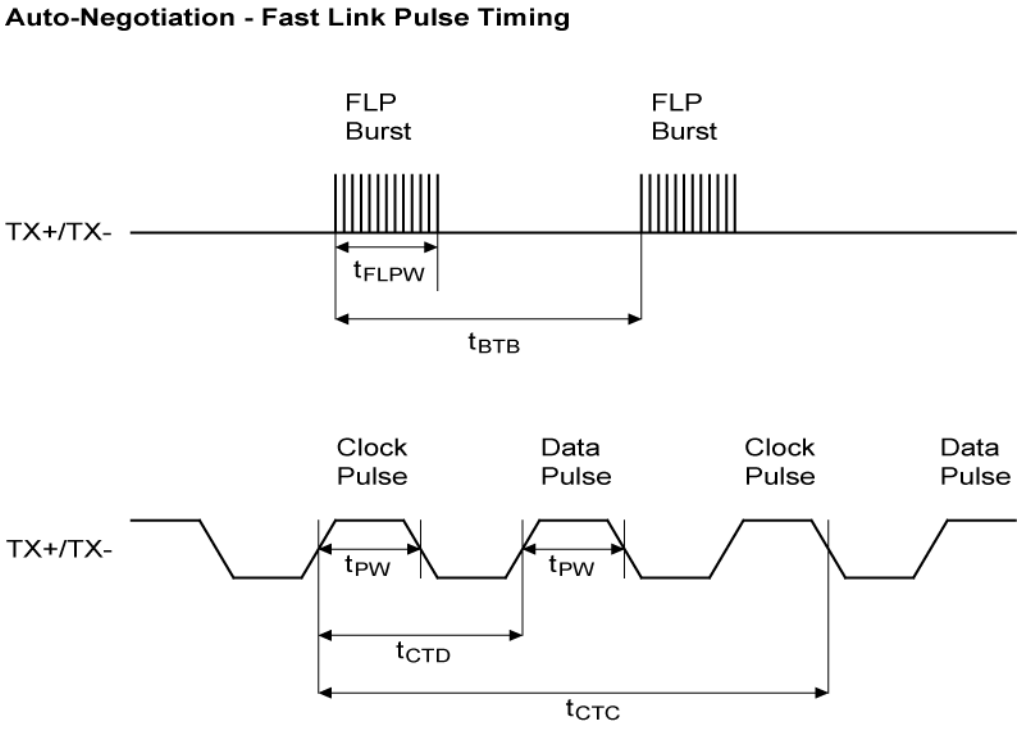


Figure 31. Auto-Negotiation Timing

Table 30. Auto-Negotiation Timing Parameters

Symbols	Parameters	Min.	Typ.	Max.	Units
t_{BTB}	FLP burst to FLP burst	8	16	24	ms
t_{FLPW}	FLP burst width		2		ms
t_{PW}	Clock/Data pulse width		100		ns
t_{CTD}	Clock pulse to Data pulse	55.5	64	69.5	µs
t_{CTC}	Clock pulse to Clock pulse	111	128	139	µs
	Number of Clock/Data pulse per burst	17		33	

MDC/MDIO Timing

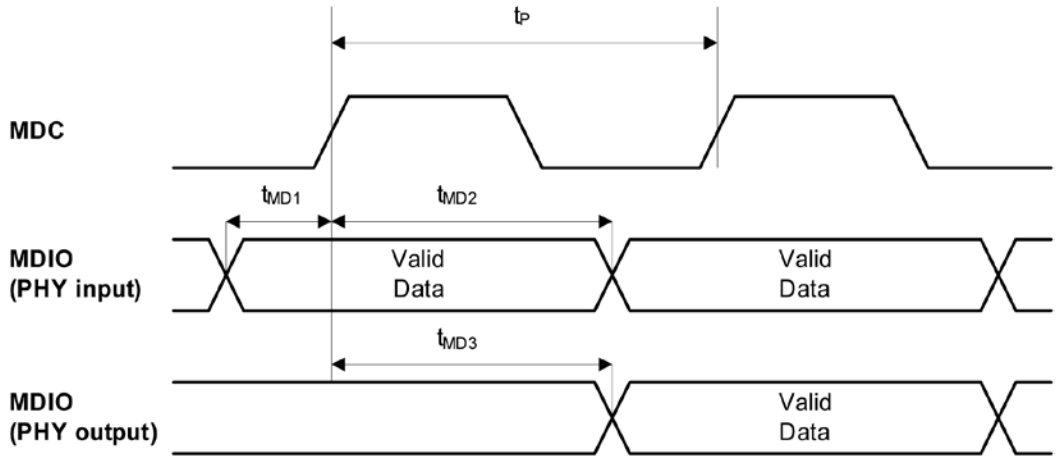


Figure 32. MDC/MDIO Timing

Table 31. MDC/MDIO Typical Timing Parameters

Timing Parameter	Description	Min.	Typ.	Max.	Unit
t_P	MDC period		400		ns
t_{1MD1}	MDIO (PHY input) setup to rising edge of MDC	10			ns
t_{MD2}	MDIO (PHY input) hold from rising edge of MDC	4			ns
t_{MD3}	MDIO (PHY output) delay from rising edge of MDC		222		ns

Reset Timing

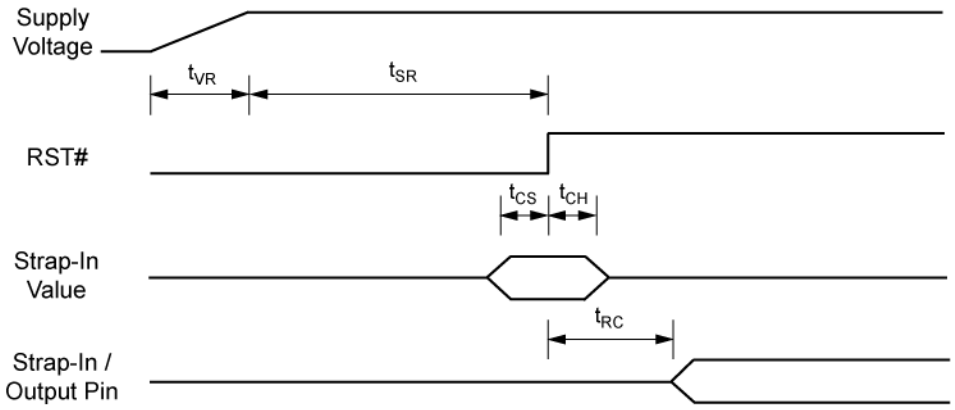


Figure 33. Reset Timing

Table 32. Reset Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{SR}	Stable Supply Voltages to Reset High	10			ms
t_{CS}	Configuration Set-Up Time	50			ns
t_{CH}	Configuration Hold Time	50			ns
t_{RC}	Reset to Strap-In Pin Output	50			ns
tvr	3.3V rise time	100			us

Reset Circuit Diagram

Micrel recommends the following discrete reset circuit as shown in Figure 34 for the power-up reset circuit.

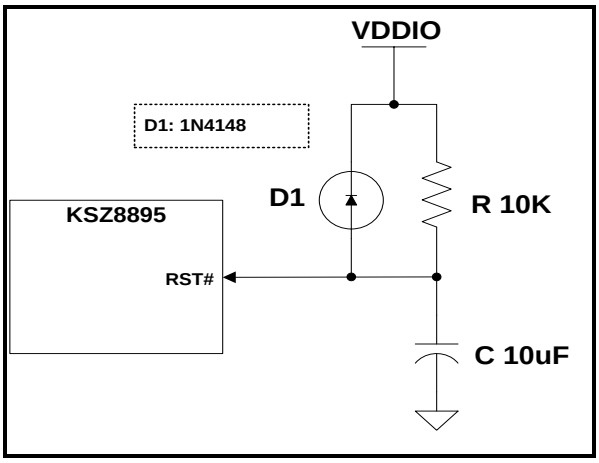


Figure 34. Recommended Reset Circuit

Figure 35 shows a reset circuit recommended for applications where reset is driven by another device (for example, the CPU or an FPGA). The reset out RST_OUT_n from CPU/FPGA provides the warm reset after power up reset. D2 is required if using different VDDIO voltage between switch and CPU/FPGA. Diode D2 should be selected to provide maximum 0.3V VF (Forward Voltage), for example, VISHAY BAT54, MSS1P2L. Alternatively, a level shifter device can also be used. D2 is not required if switch and CPU/FPGA use same VDDIO voltage.

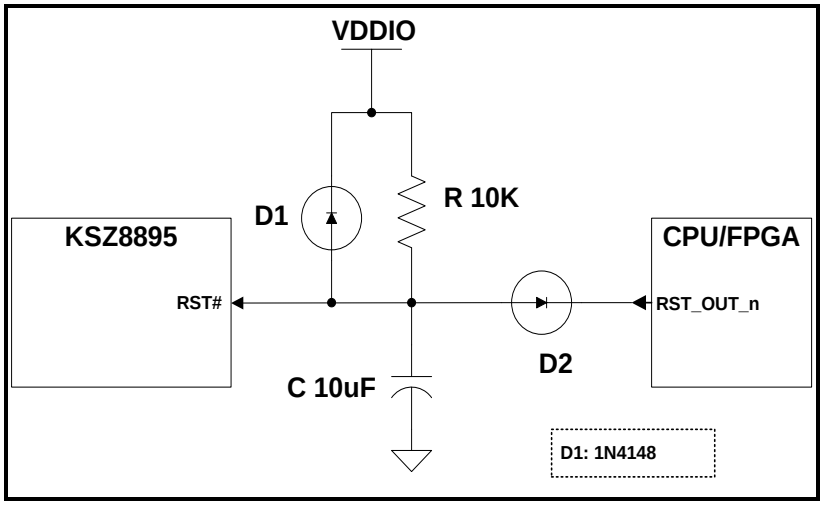


Figure 35. Recommended Circuit for Interfacing with CPU/FPGA Reset

Selection of Isolation Transformer[12]

One simple 1:1 isolation transformer is needed at the line interface. An isolation transformer with integrated common-mode choke is recommended for exceeding FCC requirements at line side. Request to separate the center taps of RX/TX at chip side. Table 33 gives recommended transformer characteristics.

Table 33. Transformer Selection Criteria

Characteristics Name	Value	Test Condition
Turns Ratio	1 CT : 1 CT	
Open-Circuit Inductance (minimum)	350µH	100mV, 100kHz, 8mA
Insertion Loss (maximum)	1.1dB	0.1MHz to 100MHz
HIPOT (minimum)	1500Vrms	

Note:

12. The IEEE 802.3u standard for 100BASE-TX assumes a transformer loss of 0.5dB. For the transmit line transformer, insertion loss of up to 1.3dB can be compensated by increasing the line drive current by means of reducing the ISET resistor value.

The following transformer vendors provide compatible magnetic parts for Micrel's device:

Table 34. Qualified Magnetic Vendors

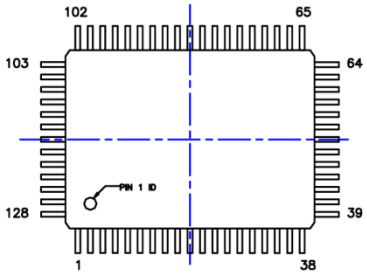
Vendors and Parts		Auto MDIX	Number of Ports	Vendors and Parts		Auto MDIX	Number of Ports
Pulse	H1664NL	Yes	4	Pulse	H1102	Yes	1
Pulse	H1164NL	Yes	4	Bel Fuse	S558-5999-U7	Yes	1
TDK	TLA-6T718A	Yes	1	YCL	PT163020	Yes	1
LanKom	LF-H41S	Yes	1	Transpower	HB726	Yes	1
Datatronic	NT79075	Yes	1	Delta	LF8505	Yes	1

Selection of Reference Crystal

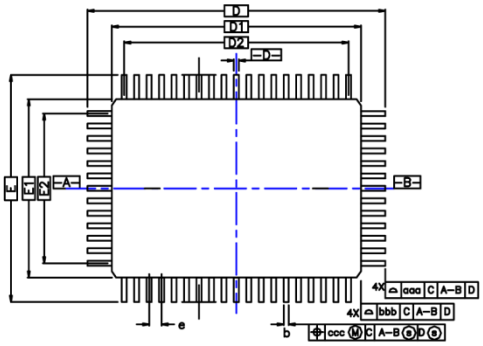
Table 35. Typical Reference Crystal Characteristics

Chacteristics	Value	Units
Frequency	25.00000	MHz
Frequency tolerance (maximum)	≤ ±50	ppm
Load capacitance (maximum)	27	pF
Series resistance (ESR)	40	Ω

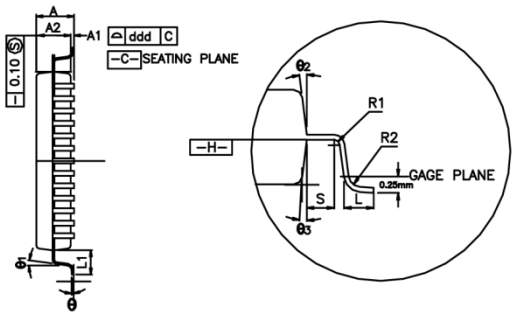
Package Information and Recommended Land Pattern[13]



TOP VIEW
Note 1,2,3



BOTTOM VIEW
Note 1,2,3



SIDE VIEW
Note 1,2,3

DETAILED VIEW

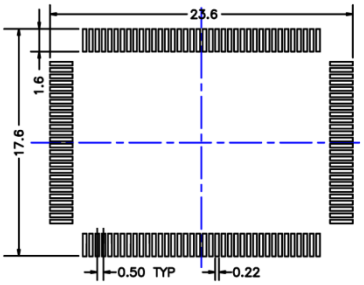
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E1	14.00 BASIC			0.551 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
θ2 , θ3	15° REF			15° REF		

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—
b	0.170	0.200	0.270	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC		
D2	18.50			0.728		
E2	12.50			0.492		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

COTROL DIMENSIONS ARE IN MILLIMETERS.

NOTES :

1. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-
2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
3. THE DIAGRAMS DO NOT REPRESNET THE ACTUAL PIN COUNT.
4. ALL UNITS IN mm. TOLERANCE +/− 0.05 IF NOT NOTED.



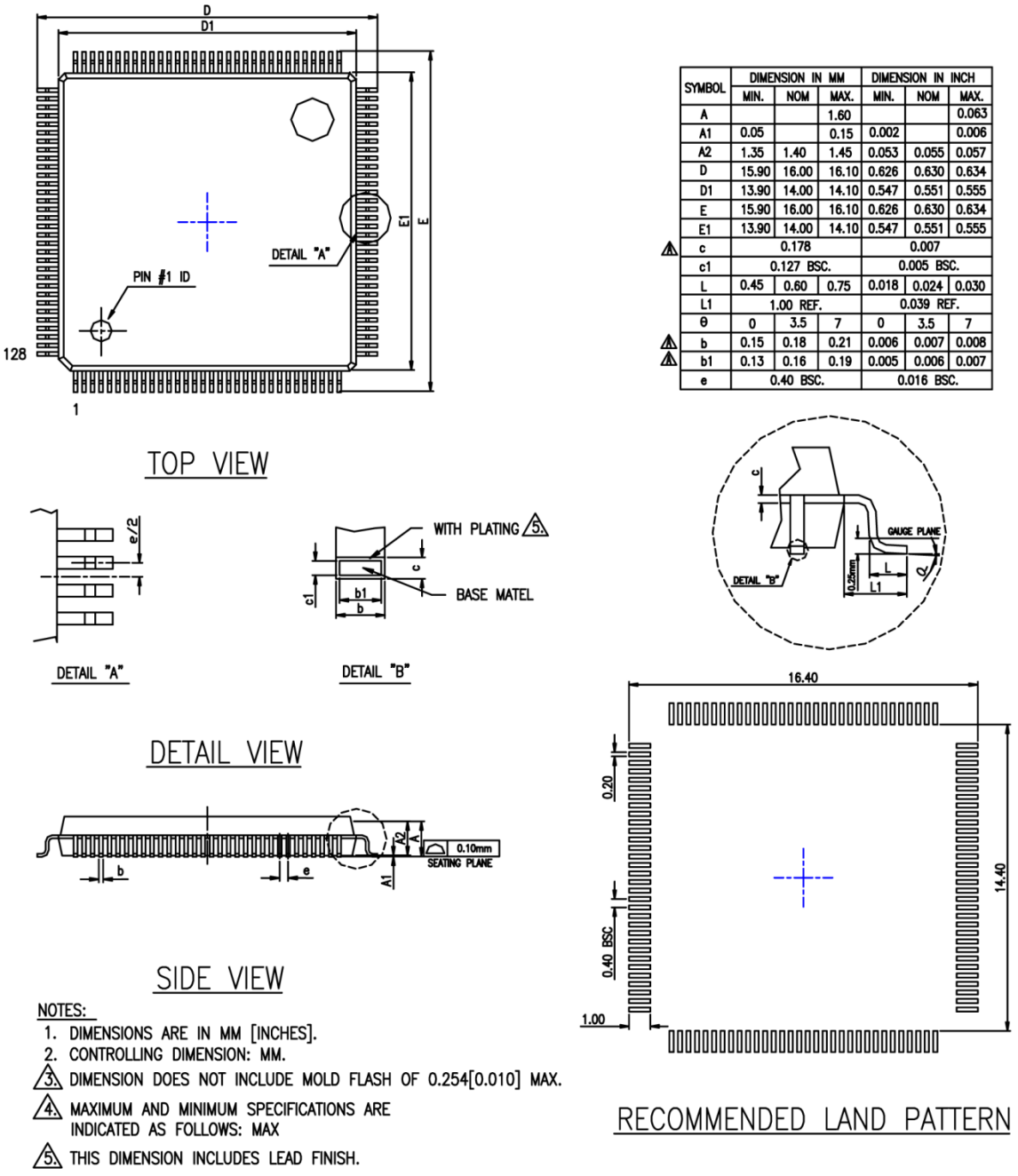
RECOMMENDED LAND PATTERN
Note 4

128-Pin PQFP (MM)

Note:

13. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

Package Information and Recommended Land Pattern[13] (Continued)



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	15.90	16.00	16.10	0.626	0.630	0.634
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.90	16.00	16.10	0.626	0.630	0.634
E1	13.90	14.00	14.10	0.547	0.551	0.555
c	0.178			0.007		
c1	0.127 BSC.			0.005 BSC.		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
b	0.15	0.18	0.21	0.006	0.007	0.008
b1	0.13	0.16	0.19	0.005	0.006	0.007
e	0.40 BSC.			0.016 BSC.		

NOTES:
1. DIMENSIONS ARE IN MM [INCHES].
2. CONTROLLING DIMENSION: MM.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OF 0.254[0.010] MAX.
4. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX
5. THIS DIMENSION INCLUDES LEAD FINISH.

128-Pin LQFP (MM)

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