UCC5642
LVD-ONLY SCSI TERMINATOR WITH REGULATOR AND SPI-3 DELAY

SLUS477 – FEBRUARY 2000 – REVISED DECEMBER 2000

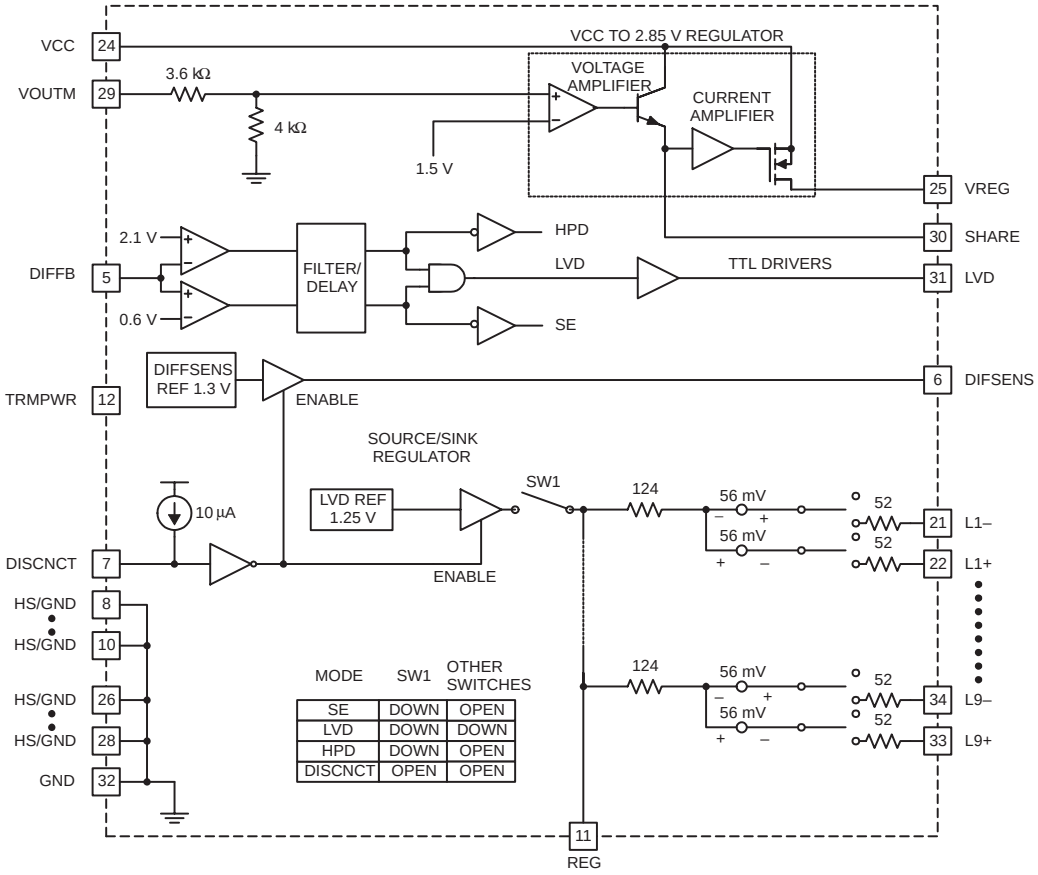
- **LVD-Only Active Termination**
- **2.7-V to 5.25-V Operation**
- **Differential Failsafe Bias**
- **Integrated SPI-3 Mode Change/Filter Delay**
- **Thermal Packaging for Low Junction Temperature and Better MTBF**
- **2.85-V Regulator With Load Share**
- **Meets Ultra2 (SPI-2 LVD), Ultra3/Ultra160 (SPI-3) and Ultra320 (SPI-4) Standards**

description

The UCC5642 is an LVD-only small computer system interface (SCSI) terminator that integrates the mode change delay function required by the SPI-3 specification. The device senses what types of SCSI drivers are present on the bus via the voltage on the DIFFSENS SCSI control line. Single-ended (SE) and high-voltage differential (HVD) (EIA485) SCSI drivers are not supported. If the chip detects the presence of an SE or HVD SCSI driver, it disconnects itself by switching all terminating resistors off the bus and enters a high-impedance state. The terminator can also be commanded to disconnect the terminating resistors with the DISCNCT input. Impedance is trimmed for accuracy and maximum effectiveness. Bus lines are biased to a failsafe state to ensure signal integrity. A 2.85-V, 300-mA sourcing regulator on chip can share with two other UCC5642 devices in a parallel configuration for a 900 mA total.

The UCC5642 is offered in a 36-pin QSOP (MWP) package for a temperature range of 0°C to 70°C.

block diagram



UDG-00158

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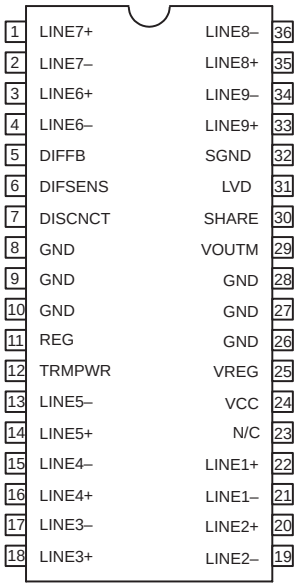
package information

MWP PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_J	PACKAGED DEVICES
	QSOP (MWP)
0°C to 70°C	UCC5642MWP

† Available tape and reeled. Add R suffix to device type to order quantities of 1000 devices per reel.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

TRMPWR voltage . . . . . 6 V
Signal line voltage . . . . . 0 V to 5 V
Storage temperature, T_{stg} . . . . . –65°C to 150°C
Junction temperature, T_J . . . . . –55°C to 150°C
Lead temperature (soldering, 10 sec.) . . . . . 300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the *Interface Products Data Book (TI Literature Number SLUD002)* for thermal limitations and considerations of packages.

recommended operating conditions

TRMPWR voltage . . . . . 2.7 V to 5.25 V

electrical characteristics, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 2.7 V to 5.25 V, VCC = 4.75 V to 5.25 V,(unless otherwise stated)

TRMPWR supply current section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRMPWR supply current	LVD SCSI mode		25	40	mA
	DISCNCT mode		0.5	1	mA
V_{CC} supply current			5	10	mA

regulator section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1.25 V regulator output voltage	$0.5 \le V_{CM} \le 2$, See Note 1	1.15	1.25	1.35	V
1.25 V regulator source current	V_{REG} = 0 V		–100	–80	mA
1.25 V regulator sink current	V_{REG} = 3.0 V	80	100		mA
2.85 V regulator output voltage		2.79	2.85	2.91	V
2.85 V regulator source current		–800	–600	–400	mA
2.85 V regulator sink current		3	5	8	mA
Share output gain		4.8	6.2	7.2	V/A
Share input gain		0.130	0.160	0.192	A/V
V_{OUTM} input resistance		4	7.6	12	kΩ

diff sense driver (DIFFSENS) section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1.3 V DIFFSENS output voltage	$0.5\ mA \le I_{DIFFSENS} \le 50\ \mu A$	1.2	1.3	1.4	V
1.3 V DIFFSENS source current	$V_{DIFFSENS}$ = 0 V	–15		–5	mA
1.3 V DIFFSENS sink current	$V_{DIFFSENS}$ = 2.75 V	50		200	µA

differential termination section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Differential impedance		100	105	110	Ω
Common mode impedance	L+ and L– shorted together, See Note 2	110	140	165	Ω
Differential bias voltage		100		125	mV
Common mode bias	L+ and L– shorted together	1.15	1.25	1.35	V

NOTES: 1. VCM is applied to all L+ and L– lines simultaneously.

2. $Z_{CM} = \dfrac{(2.0\ V - 0.5\ V)}{I\left[I_{VCM(max)} - I_{VCM(min)}\right]}$ @ $V_{CM(max)}$ = 2.0, $V_{CM(min)}$ = 0.5 V.

3. Ensured by design. Not production tested.

electrical characteristics, these specifications apply for $T_A = T_J = 0°C$ to 70°C, TRMPWR = 2.7 V to 5.25 V, VCC = 4.75 V to 5.25 V, (unless otherwise stated)

disconnected termination section (applies to each line pair, 1–9, in DISCNCT, SE or HVD mode)

Output leakage			400	nA
Output capacitance	Single ended measurement to ground, See Note 3		3	pF

disconnect (DISCNCT) and diff buffer (DIFFB) input section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DISCNCT threshold		0.8		2.0	V
DISCNCT input current		–30	–10		µA
DIFFB SE to LVD SCSI threshold		0.5		0.7	V
DIFFB LVD SCSI to HPD threshold		1.9		2.4	V
DIFFB input current		–1		1	µA

low voltage differential (LVD) status bit section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{SOURCE}	V_{LOAD} = 2.4 V		–6	–4	mA
I_{SINK}	V_{LOAD} = 0.4 V	2	5		mA

time delay/filter section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Mode change delay	A new mode change can start any time after a previous mode change has been detected.	100	190	300	ms

thermal shutdown section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Thermal shutdown threshold	For increasing temperature, See Note 3	140	155	170	°C
Thermal shutdown hysteresis			10		°C

NOTES: 1. VCM is applied to all L+ and L– lines simultaneously.

2. $Z_{CM} = \dfrac{(2.0\ V - 0.5\ V)}{I_{\left[I_{VCM(max)} - I_{VCM(min)}\right]}}$ @ $V_{CM(max)}$ = 2.0, $V_{CM(min)}$ = 0.5 V.

3. Ensured by design. Not production tested.

pin descriptions

DIFFB: Input pin for the comparators that select SE, LVD or HIPD modes of operation. This pin should be decoupled with a 0.1-μF capacitor to ground and then coupled to the DIFSENS pin through a 20-kΩ resistor.

DIFSENS: SCSI bus DIFFSENS line driver.

DISCNCT: Input pin used to shut down the terminator if the terminator is not connected at the end of the bus. Connect this pin to ground to activate the terminator or open to disable the terminator.

HS/GND: Heat sink ground pins. Connected to large ground area PC board traces to increase the power dissipation capability.

GND: Power supply return.

L1– thru L9–: Line termination pins. Negative lines in differential pair. In HIPD and SE mode, these lines are high impedance.

L1+ thru L9+: Line termination pins. Positive lines in differential pair. In HIPD and SE mode, these lines are high impedance.

REG: Regulator bypass pin, must be connected to a 4.7-μF capacitor to ground and a high frequency, low ESR 0.01-μF capacitor to ground.

SHARE: Load share pin for the 2.85-V regulator. Connect to the SHARE pins of the other devices in a parallel configuration.

TRMPWR: 2.7-V to 5.25-V power input pin. Bypass near the terminators with a 4.7-μF capacitor and a high frequency, low ESR 0.01-μF capacitor to ground.

VCC: 4.75-V to 5.25-V power-input pin. Connect to a 4.7-μF capacitor and a low ESR 0.01-μF capacitor to ground.

VOUTM: V_{REG} voltage feedback input pin for the 2.85-V regulator.

VREG: 2.85-V regulator output pin, must be connected to a 10-μF low ESR capacitor.

APPLICATION INFORMATION

All SCSI buses require a termination network at each end to function properly. Specific termination requirements differ, depending on which types of SCSI driver devices are present on the bus. The UCC5642 is a low-voltage differential (LVD) only device. It senses which types of drivers are present on the bus. If it detects the presence of a single-ended (SE) or high-voltage differential (HVD) driver, the UCC5642 will place itself in a high-impedance input state, effectively disconnecting the chip from the bus.

The UCC5642 senses what kinds of drivers are present on the bus by the voltage on SCSI bus control line DIFFSENS, which is monitored by the DIFFB input pin. The DIFSENS output pin on the UCC5642 attempts to drive a DIFFSENS control line to 1.3 V. If only LVD devices are present, the DIFFSENS line will be successfully driven to that voltage. If HVD drivers are present, they will pull the DIFFSENS line high. If any single-ended drivers are present, they pull the DIFSENS line to ground (even if HVD drivers are also present on the bus). If the voltage on the DIFFB is below 0.5 V or above 2.4 V, the UCC5642 enters the high-impedance SE/HVD state. If it is between 0.7 V and 1.9 V, the UCC5642 enters the LVD mode. These thresholds accommodate differences in ground potential that can occur between the ends of long bus lines.

APPLICATION INFORMATION

Three UCC5642 ICs are required at each end of the SCSI bus to terminate 27 lines (18 data, 9 control). Every UCC5642 contains a DIFSENS driver, but only one should be used to drive the line at each end. The DIFSENS pin on the other devices should be left unconnected.

On power up (the voltage on the TRMPWR pin rising above 2.7 V), the UCC5642 assumes the SE/HVD mode. If the voltage on the DIFFB input indicates LVD mode, the chip waits 100 ms to 300 ms before changing the mode of the bus. If the voltage at the DIFFB input later crosses one of the thresholds, the UCC5642 again waits 100 ms to 300 ms before changing the mode of the bus. The magnitude of the delay is the same when changing in or out of either bus mode. A new mode change can start anytime after a previous mode change has been detected.

The DIFFB inputs on all three chips at each end of the bus should be connected together. Properly filtered, noise on DIFFB will not cause a false mode change. There should be a shared 50-Hz noise filter implemented on DIFFB at each end of the bus as close as possible to the DIFFB pins. This is implemented with a 20-kΩ resistor between the DIFFB and DIFSENS pins, and a 0.1-μF capacitor from DIFFB to ground. See the *Typical Application diagram* at the end of this data sheet.

The 5-V to 2.85-V regulator in the UCC5642 can run as a stand-alone regulator by connecting the output (VREG) to the voltage-feedback input (VOUTM). Also connect to VREG a low ESR 10-μF capacitor. The other side of the low ESR capacitor is connected to GND. When the load sinks current from VREG the voltage will start to drop, this drop will be detected by the feedback at VOUTM, and more current will be driven by VREG. Because the feedback loop has a slight delay the 10-μF low ESR capacitor is very important to supply current for fast transient and to stabilize the loop. In this configuration VREG can supply about 300-mA.

To supply more current, all three VREG output can be connected together. To keep one regulator from supplying all the current the SHARE pins need to be connected together. Because this is an unusual feature a short description follows.

In the stand alone configuration, the SHARE pin voltage is proprotional to the output current. By design, the SHARE pin drive is a strong pullup and a weak pulldown. When the share pin is pulled up from outside the UCC5642 the current out of VREG is proportional to the voltage on the SHARE pin.

In the parallel configuration, the VREG pins are connected together to provided the load current. The SHARE pins are connected together so the regulators will share the load current. When the load is appllied, one regulator will start to supply more current than the other two and will drive the common SHARE connection higher. This higher voltage on the common SHARE connection will cause each of the other two regulators to supply the same current, thus sharing the load current. In this configuration one regulator sets the voltage and supplies one-third of the load current. Each of the other regulators supply an additional one-third of the current.

Because the 10 μF stabilizes the voltage feedback loop, there must be one 10-μF low ESR capacitor near each V_{REG} output for each UCC5642. If better transient response is required there can be as much as 100 μF for each UCC5642.

APPLICATION INFORMATION

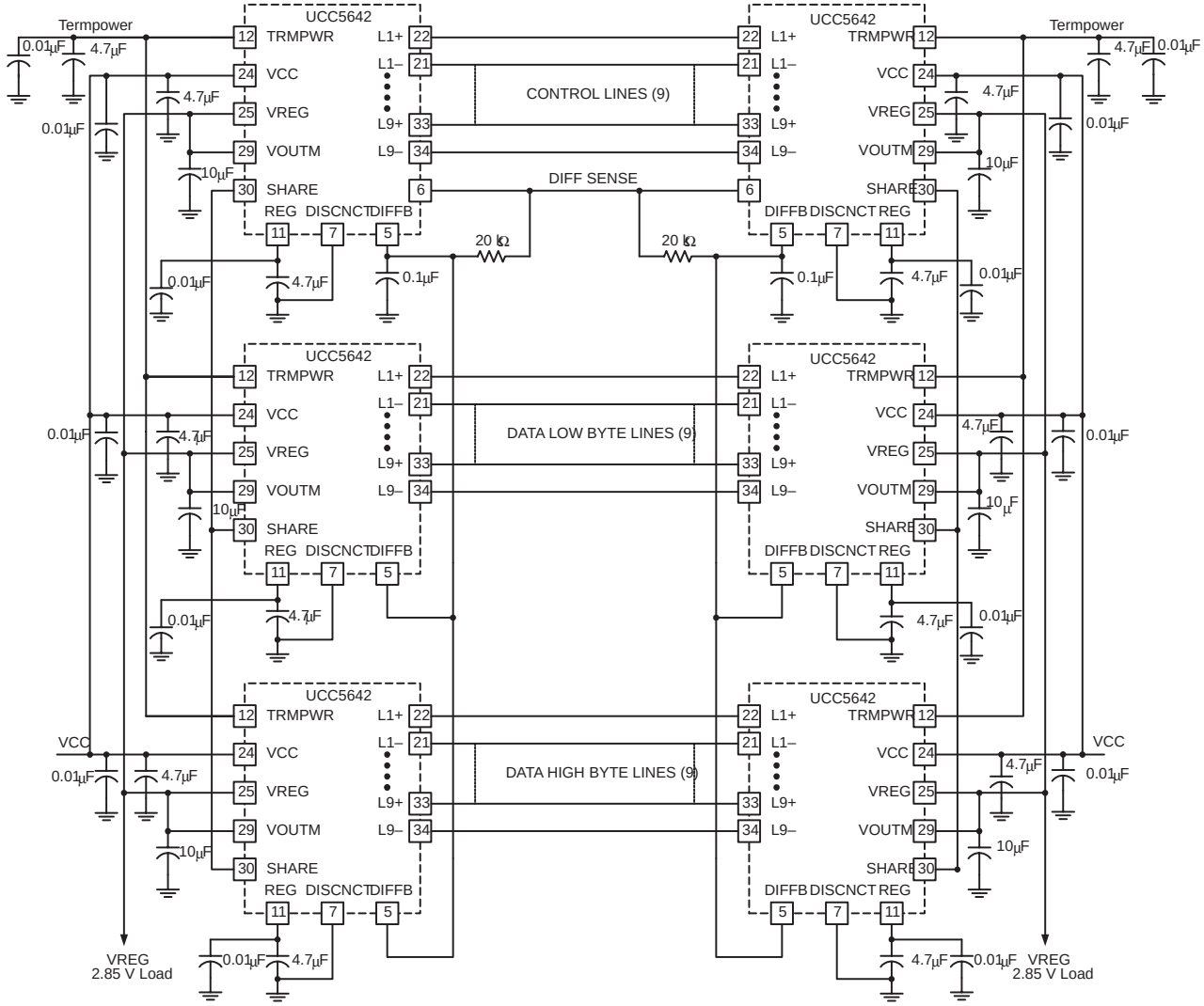


Figure 1. Application Diagram

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC5642MWP	ACTIVE	SSOP	DCE	36	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC5642MWPG4	ACTIVE	SSOP	DCE	36	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC5642MWPTR	ACTIVE	SSOP	DCE	36	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC5642MWPTRG4	ACTIVE	SSOP	DCE	36	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

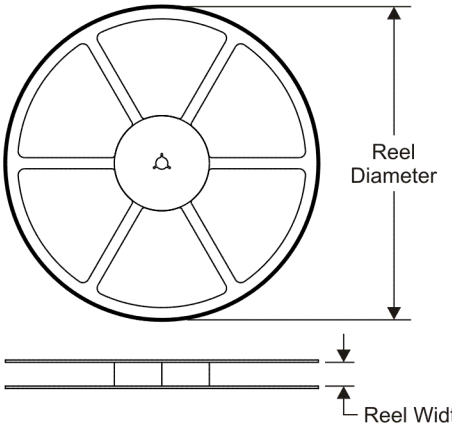
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

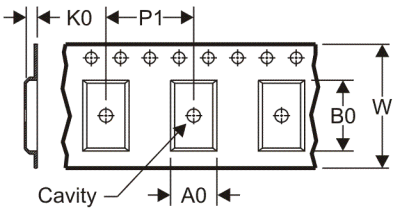
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

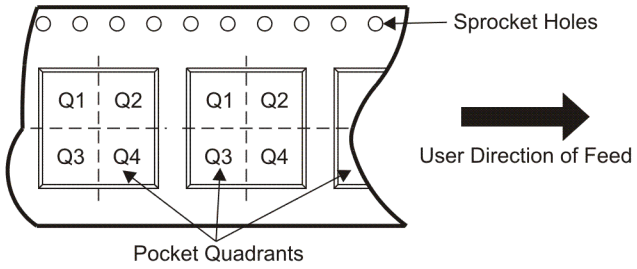


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

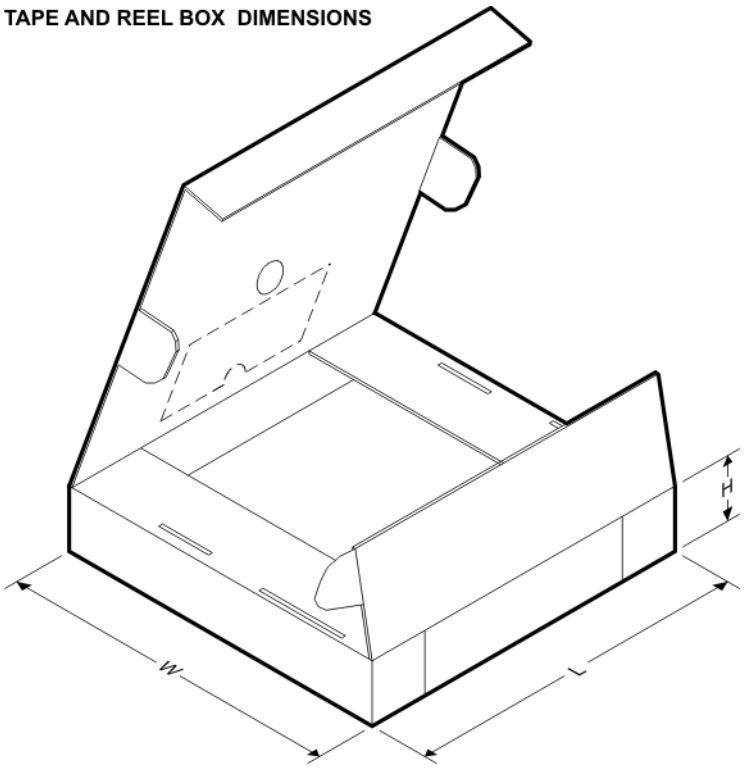
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC5642MWPTR	SSOP	DCE	36	1000	330.0	24.4	10.85	15.8	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



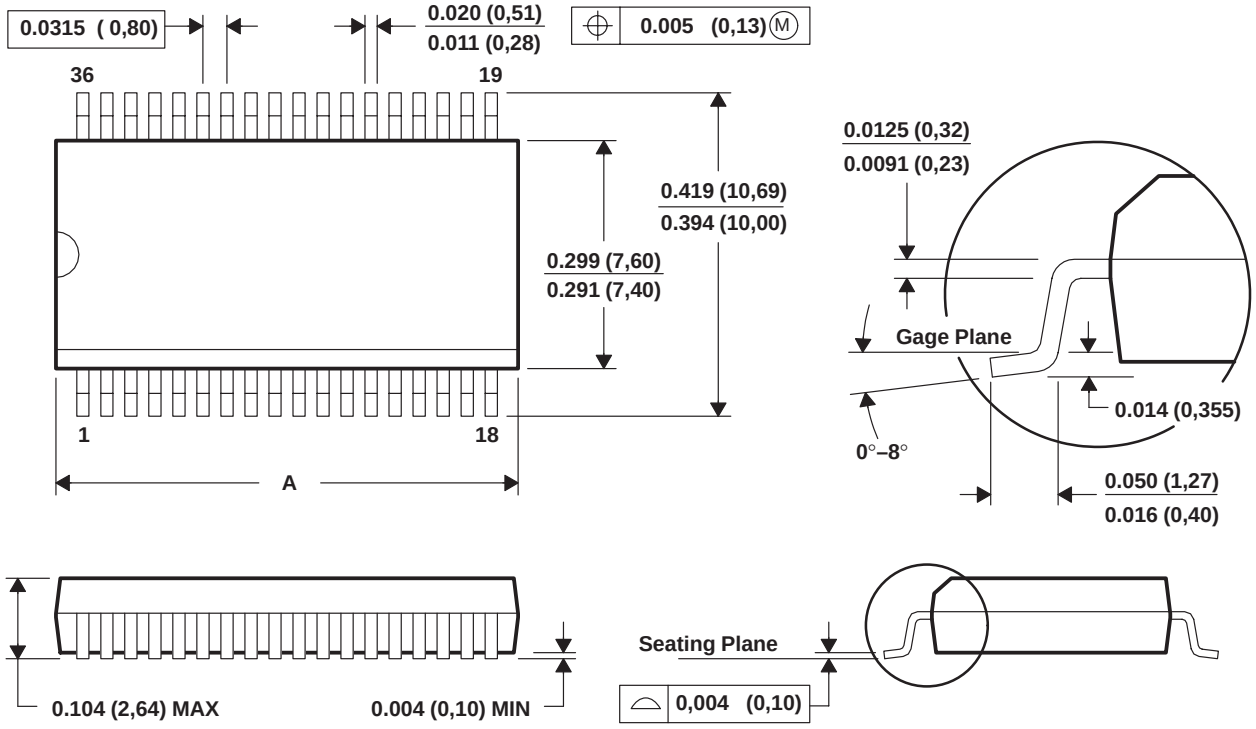
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC5642MWPTR	SSOP	DCE	36	1000	346.0	346.0	41.0

DCE (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

36 PINS SHOWN



DIM \ PINS **	36	44
A MAX	0.613 (15,57)	0.713 (18,11)
A MIN	0.598 (15,20)	0.697 (17,70)

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265