# IEEE 1394-1995 High-Speed Serial-Bus Link-Layer Controller

## FEATURES

- **Link Core**
  - **Supports Provision of IEEE 1394-1995 (1394) Standard for High-Performance Serial Bus**
  - **Transmits and Receives Correctly Formatted 1394 Packets**
  - **Supports Asynchronous and Isochronous Data Transfers**
  - **Performs Function of 1394 Cycle Master**
  - **Generates and Checks 32-Bit CRC**
  - **Detects Lost Cycle-Start Messages**
  - **Contains Asynchronous, Isochronous, and General-Receive FIFOs Totaling 2K Bytes**
- **Physical-Link Interface**
  - **Compatible With Texas Instruments Physical Layer Devices (PHYs)**
  - **Supports Transfer Speeds of 100, 200, and 400 Mbits/s**
  - **Timing Compliant with IEEE 1394a–2000**
- **Host Bus Interface**
  - **Provides Chip Control With Directly Addressable Registers**
  - **Is Interrupt Driven to Minimize Host Polling**
  - **Has a Generic 32-Bit Host Bus Interface**
- **General**
  - **Operates From a 3.3-V Power Supply While Maintaining 5-V Tolerant Inputs**
  - **Manufactured With Low-Power CMOS Technology**
  - **100-Pin PZT Package for 0°C to 70°C and -40°C to 85°C (I Temperature) Operation**

## DESCRIPTION

The TSB12LV01B is an IEEE 1394-1995 standard (from now on referred to only as 1394) high-speed serial-bus link-layer controller that allows for easy integration into an I/O subsystem. The TSB12LV01B provides a high-performance IEEE 1394-1995 interface with the capability of transferring data between the 32-bit host bus, the 1394 PHY-link interface, and external devices connected to the local bus interface. The 1394 PHY-link interface provides the connection to the 1394 physical (PHY) layer device and is supported by the link-layer controller (LLC). The LLC provides the control for transmitting and receiving 1394 packet data between the FIFO and PHY-link interface at rates of 100 Mbits/s, 200 Mbits/s, and 400 Mbits/s. The TSB12LV01B transmits and receives correctly-formatted 1394 packets and generates and inspects the 32-bit cyclic redundancy check (CRC). The TSB12LV01B is capable of being cycle master and supports reception of isochronous data on two channels. TSB12LV01B has a generic 32-bit host bus interface, which will connect to most 32-bit hosts. The LLC also provides the capability to receive status from the physical layer device and to access the physical layer control and status registers by the application software. An internal 2K-byte memory is provided that can be configured as multiple variable-size FIFOs and eliminates the need for external FIFOs. Separate FIFOs can be user configured to support general 1394 receive, asynchronous transmit, and isochronous transmit transfer operations. These functions are accomplished by appropriately sizing the general receive FIFO (GRF), asynchronous transmit FIFO (ATF), and isochronous transmit FIFO (ITF).

The TSB12LV01B is a revision of the TSB12LV01A, with feature enhancements and corrections. It is pin for pin compatible with the TSB12LV01A with the restrictions noted below. It is also software compatible with the extensions noted below.

All errata items to the TSB12LV01A have been fixed, and the following feature enhancements have been made:

- Two new internal registers have been added at CFR address 40h and 44h. The *Host Bus Control Register* at 40h and the *Mux Control Register* @44h .
- Three programmable general-purpose output pins have been added.
- Several pin changes have been made. Refer to *TSB12LV01A to TSB12LV01B Transition Document,* TI literature number SLLA081 dated May 2000.

However, there are three restrictions that were not present in the TSB12LV01A device:

- The TSB12LV01B may only operate with a 50 MHz host-interface clock (BCLK) if the duty cycle is less than 5% away from the 50-50 point, (i.e., the duty cycle must be within 45-55% inclusive). A 40-60% duty cycle clock is acceptable for host clock frequencies at or below 47 MHz.
- The TSB12LV01B does not have bus holder cells on the PHY-link interface.
- As a result of removing the bus holder cells, the $\overline{\text{ISO}}$ pin (pin 69) was replaced with a Vcc pin on the TSB12LV01B.

This document is not intended to serve as a tutorial on 1394; users are referred to the IEEE 1394-1995 serial bus standard for detailed information regarding the 1394 high-speed serial bus.

**NOTE:**

This product is for high-volume applications only. For a complete datasheet or more information contact support@ti.com.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TSB12LV01BPZT | ACTIVE | TQFP | PZT | 100 | 90 | RoHS & Green | NIPDAU | Level-4-260C-72 HR | 0 to 70 | TSB12LV01B F711934 | Samples |
| TSB12LV01BPZTG4 | ACTIVE | TQFP | PZT | 100 | 90 | RoHS & Green | NIPDAU | Level-4-260C-72 HR | 0 to 70 | TSB12LV01B F711934 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

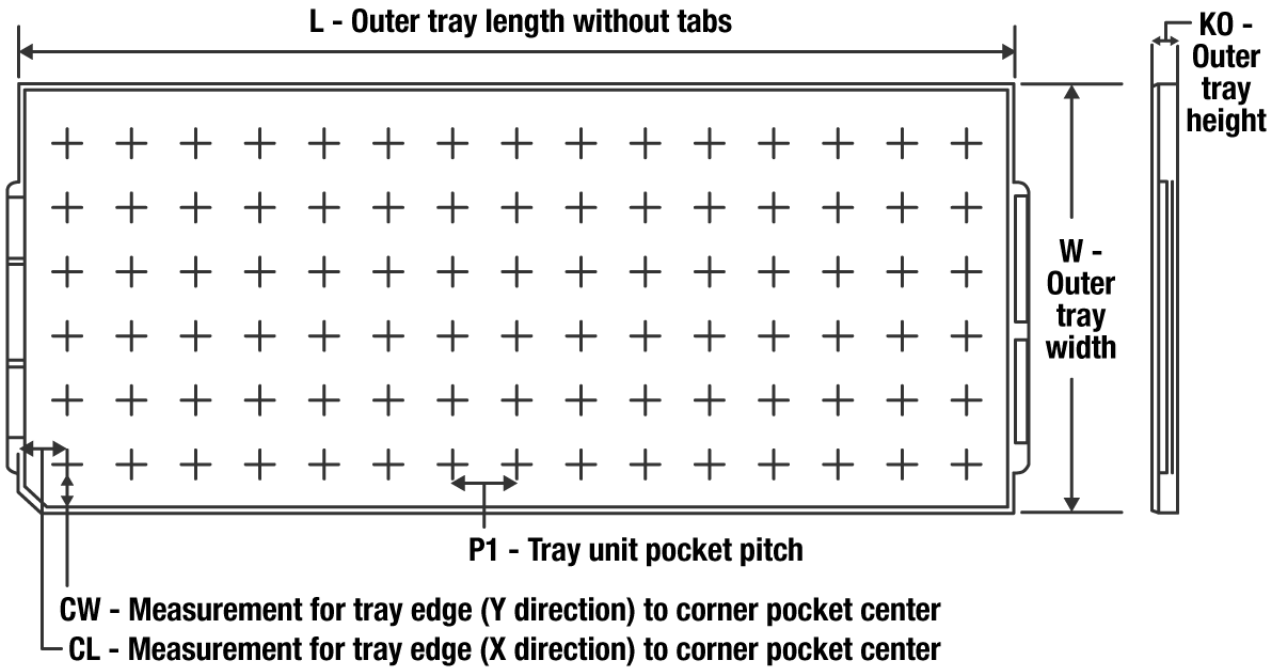
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TRAY




Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TSB12LV01BPZT | PZT | TQFP | 100 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 15.4 | 20.3 | 21 |
| TSB12LV01BPZTG4 | PZT | TQFP | 100 | 90 | 6 X 15 | 150 | 315 | 135.9 | 7620 | 15.4 | 20.3 | 21 |

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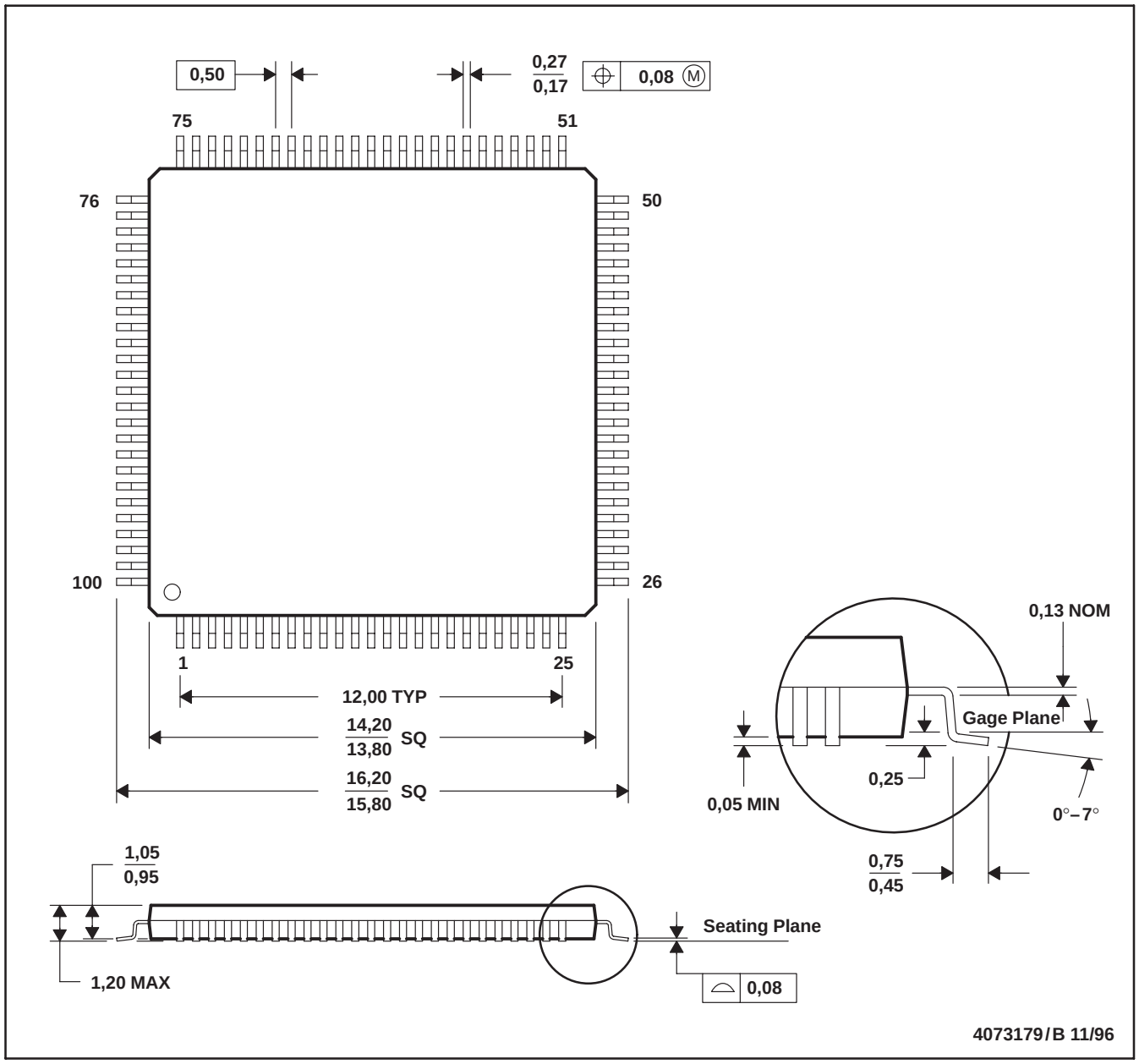
**PZT (S-PQFP-G100)** **PLASTIC QUAD FLATPACK**




NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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