

TLV3501A-Q1 4.5-ns Rail-to-Rail, High-Speed Comparator in Microsize Packages

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
 - Device Temperature Grade 1: -40°C to $+125^{\circ}\text{C}$ Ambient Operating Temperature Range
 - Device HBM Classification Level 2
 - Device CDM Classification Level C4B
- High Speed: 4.5 ns
- Rail-To-Rail I/O
- Supply Voltage: 2.7 V to 5.5 V
- Push-Pull CMOS Output Stage
- Shutdown
- Micro Package: SOT23-6
- Low Supply Current: 3.2 mA
- Z-Suffix Offers Improved Delamination

2 Applications

- HEV/EV and Powertrain Applications
- DC-DC Converter
- Inverter
- Fuel Sensing
- Hybrid Power Control Unit
- Automatic Test Equipment
- Threshold Detector
- Zero-Crossing Detector
- Window Comparator

3 Description

The TLV3501A-Q1 push-pull output comparator features a fast 4.5-ns propagation delay and operation from 2.7 V to 5.5 V. The input voltage supports a common-mode range that goes beyond the rails which makes the device an ideal choice for low-voltage applications. The rail-to-rail output directly drives either CMOS or TTL logic. The fast delay and wide common-mode range also makes TLV3501A-Q1 device ideal for EMI reduction through frequency dithering by lowering the EMI peaks. These parameters allow the device to be ideal for both DC-DC converter and inverter applications in HEV/EV and powertrain.

The SOT23-6 microsize package provides options for portable and space-restricted applications. The Z-suffix offers reduced delamination compared to the standard device.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV3501A-Q1	SOT-23 (6)	2.90 mm x 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Propagation Delay vs Overdrive Voltage

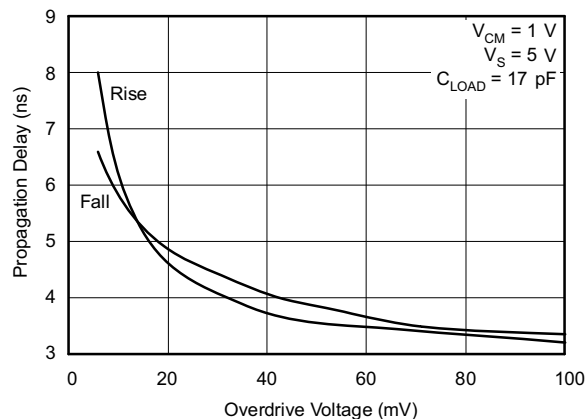


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4 Revision History

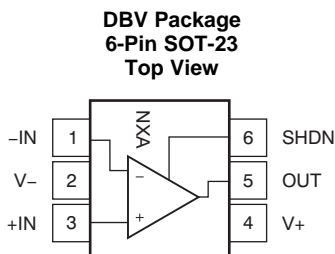
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2010) to Revision B	Page
• Added z-suffix for improved delamination	1
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Deleted the <i>Ordering Information</i> table	3
Changes from Original (September, 2010) to Revision A	Page
• Added new feature bullet regarding automotive application qualification.....	1

5 Related Products

PART NUMBER	FEATURES
TLV3701-Q1 TLV3702-Q1	Automotive Nanopower, 560-nA I_{CC} , push-pull comparators
TLC3702-Q1 TLC3704-Q1	Automotive micropower, 100- μ W, LinCMOS™ voltage, push-pull comparators
TLV3012-Q1	Automotive nanopower, 1.8-V, SOT23 push-pull comparator with voltage reference
TLC393-Q1	Automotive dual-micropower LinCMOS voltage comparator

6 Pin Configuration and Functions



Pin 1 is determined by orienting the package marking as indicated on the diagram.

Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	-IN	I	Inverting input
2	V-	I	Negative (lowest) power supply
3	+IN	I	Noninverting input
4	V+	I	Positive (highest) power supply
5	OUT	O	Output
6	SHDN	—	Shutdown (the device is idle when this pin is not in use)

(1) I = input, O = output

7 Specifications

7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage		5.5	V
Signal input terminal voltage ⁽²⁾	(V-) - 0.3	(V+) + 0.3	V
Signal input terminal current ⁽²⁾		10	mA
Output short-circuit current ⁽³⁾		74	mA
Thermal impedance, junction to free air		200	°C/W
Operating temperature	-40	125	°C
Junction temperature		150	°C
Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3 V beyond the supply rails should be current limited to 10 mA or less.
- (3) Short circuit to ground, one comparator per package.

7.2 ESD Ratings

		VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	
		Charged-device model (CDM), per AEC Q100-011	All pins	±500
			Corner pins (1, 3, 4, and 6)	±750

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V _S Supply voltage	2.2	2.7	5.5	V
V _{IL} Low-level input voltage, SHDN (comparator is enabled) ⁽¹⁾			(V+) - 1.7	V
V _{IH} High-level input voltage, SHDN (comparator is disabled) ⁽¹⁾	(V+) - 0.9			V
T _A Operating temperature	-40		125	°C

- (1) When the SHDN pin is within 0.9 V of the most positive supply, the part is disabled. When it is more than 1.7 V below the most positive supply, the part is enabled.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TLV3501A-Q1	UNIT
		DBV (SOT-23)	
		6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	192.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	134.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	37.1	°C/W
ψ _{JT}	Junction-to-top characterization parameter	28.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	36.7	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	—	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

$T_A = 25^\circ\text{C}$ and $V_S = 2.7\text{ V}$ to 5.5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage ⁽¹⁾	$V_{CM} = 0\text{ V}$, $I_O = 0\text{ mA}$		±1	±6.5	mV
dV_{OS}/dT	Input offset voltage ⁽¹⁾ vs temperature	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$		±5		μV/°C
PSRR	Input offset voltage ⁽¹⁾ vs power supply			100	400	μV/V
	Input hysteresis			6		mV
INPUT BIAS CURRENT						
I_B	Input bias current ⁽²⁾	$V_{CM} = V_{CC} / 2$, $\Delta V_{IN} = \pm 5.5\text{ V}$		±2	±10	pA
I_{OS}	Input offset current ⁽²⁾⁽³⁾	$V_{CM} = V_{CC} / 2$, $\Delta V_{IN} = \pm 5.5\text{ V}$		±2	±10	pA
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range		(V-) – 0.2 V		(V+) + 0.2 V	V
CMRR	Common-mode rejection	$V_{CM} = -0.2\text{ V}$ to $(V+) + 0.2\text{ V}$		57	70	dB
				55		dB
INPUT IMPEDANCE						
	Common-mode			$10^{13} \parallel 2$		Ω pF
	Differential			$10^{13} \parallel 4$		Ω pF
OUTPUT						
V_{OH} , V_{OL}	Voltage output swing from rail	$I_{OUT} = \pm 1\text{ mA}$		30	50	mV
SHUTDOWN						
t_{OFF}	Shutdown turnoff time			30		ns
t_{ON}	Shutdown turnon time			100		ns
V_H	SHDN high threshold	Comparator is enabled ⁽⁴⁾			(V+) – 1.7	V
V_L	SHDN low threshold	Comparator is disabled ⁽⁴⁾	(V+) – 0.9			V
	Input bias current of the SHDN pin			2		pA
I_{QSD}	Quiescent current in shutdown			2		μA
POWER SUPPLY						
V_S	Specified voltage		2.7		5.5	V
	Operating voltage range			2.2 to 5.5		V
I_Q	Quiescent current	$V_S = 5\text{ V}$, $V_O = \text{High}$		3.2	5	mA
TEMPERATURE RANGE						
	Specified temperature		–40		125	°C
	Operating temperature		–40		125	°C
	Storage temperature		–65		150	°C
$R_{\theta JA}$	Thermal resistance, SOT23-6 package			200		°C/W

(1) V_{OS} is defined as the average of the positive and the negative switching thresholds.

(2) Not production tested.

(3) The difference between I_{B+} and I_{B-} .

(4) When the shutdown pin is within 0.9 V of the most positive supply, the part is disabled. When it is more than 1.7 V below the most positive supply, the part is enabled.

7.6 Switching Characteristics

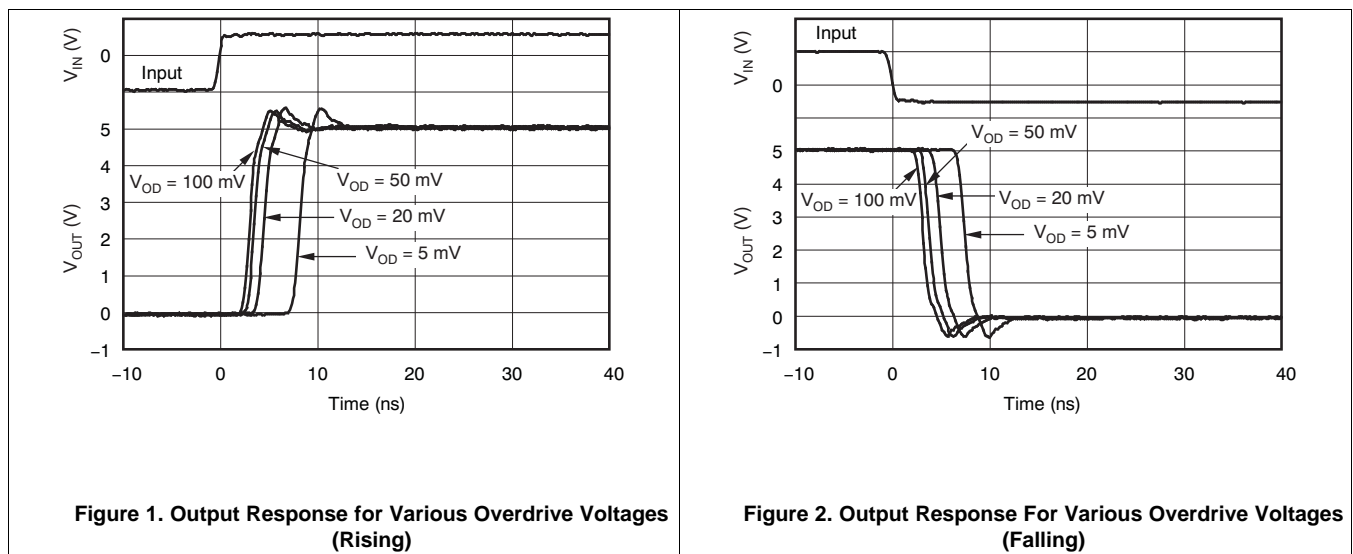
$T_A = 25^\circ\text{C}$ and $V_S = 2.7\text{ V}$ to 5.5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
T_{pd}	Propagation delay time ⁽¹⁾⁽²⁾	$\Delta V_{IN} = 100\text{ mV}$, Overdrive = 20 mV	$T_A = 25^\circ\text{C}$	4.5	6.4	ns	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			7	ns
		$\Delta V_{IN} = 100\text{ mV}$, Overdrive = 5 mV	$T_A = 25^\circ\text{C}$	7.5	10	ns	
			$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			12	ns
$\Delta t_{(SKEW)}$	Propagation delay skew ⁽³⁾	$\Delta V_{IN} = 100\text{ mV}$, Overdrive = 20 mV			0.5		ns
f_{MAX}	Maximum toggle frequency	Overdrive = 50 mV, $V_S = 5\text{ V}$			80		MHz
t_R	Rise time ⁽⁴⁾				1.5		ns
t_F	Fall time ⁽⁴⁾				1.5		ns

- (1) Not production tested.
- (2) Propagation delay cannot be accurately measured with low overdrive on automatic test equipment. This parameter is ensured by characterization at 100-mV overdrive.
- (3) The difference between the propagation delay going high and the propagation delay going low.
- (4) Measured between 10% of V_S and 90% of V_S .

7.7 Typical Characteristics

At $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, and input overdrive = 100 mV (unless otherwise noted).



Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, and input overdrive = 100 mV (unless otherwise noted).

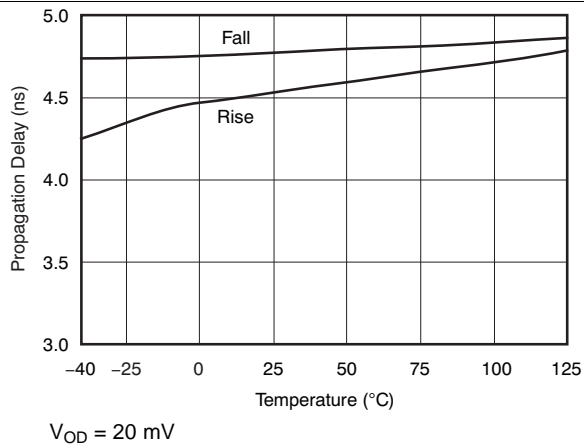


Figure 3. Propagation Delay vs Temperature

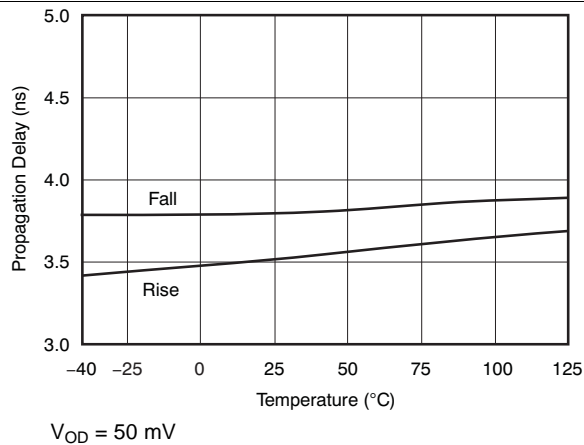


Figure 4. Propagation Delay vs Temperature

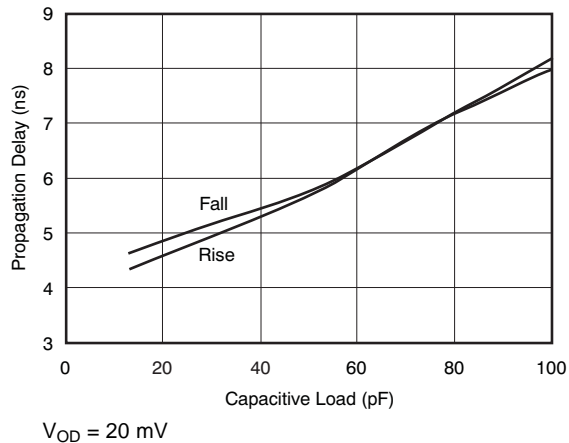


Figure 5. Propagation Delay vs Capacitive Load

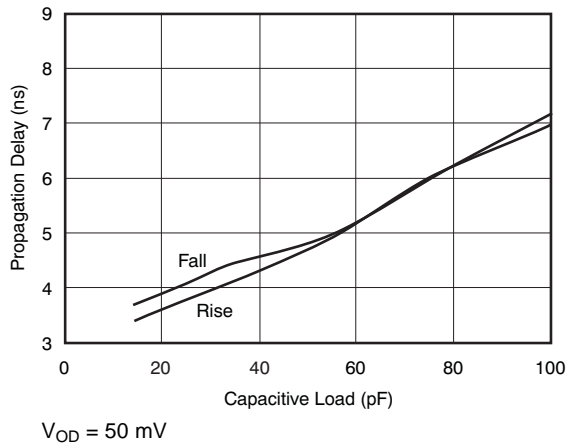


Figure 6. Propagation Delay vs Capacitive Load

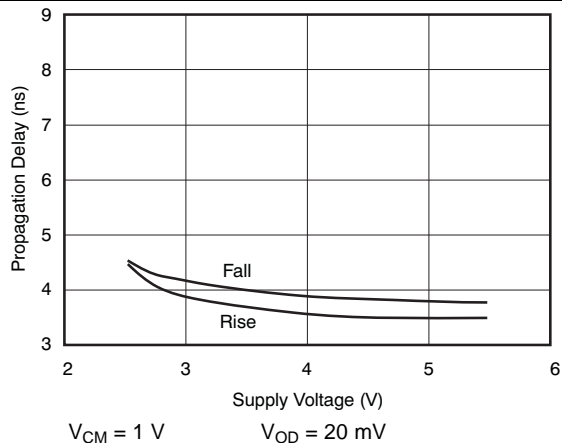


Figure 7. Propagation Delay vs Supply Voltage

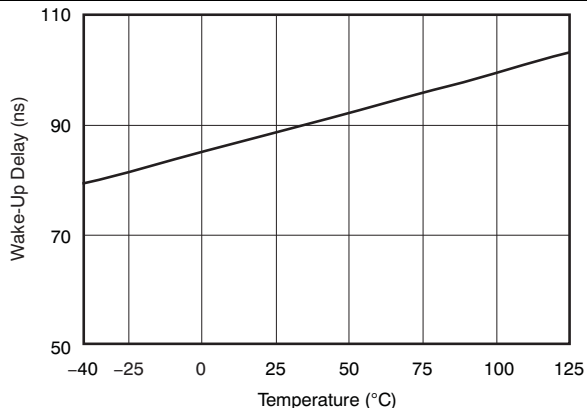
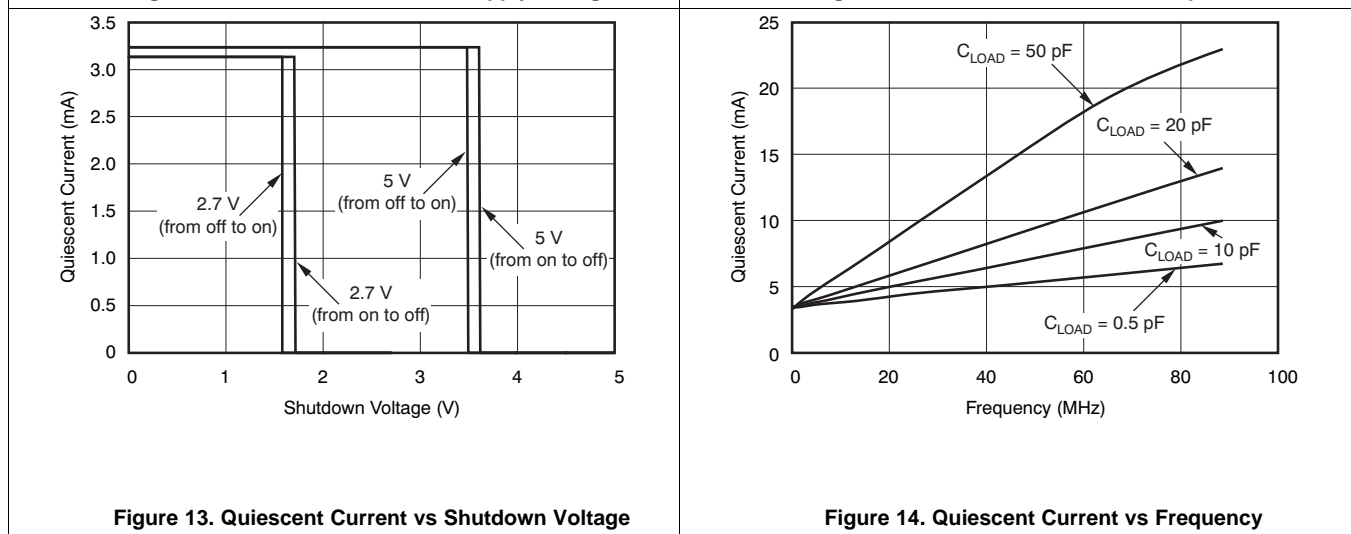
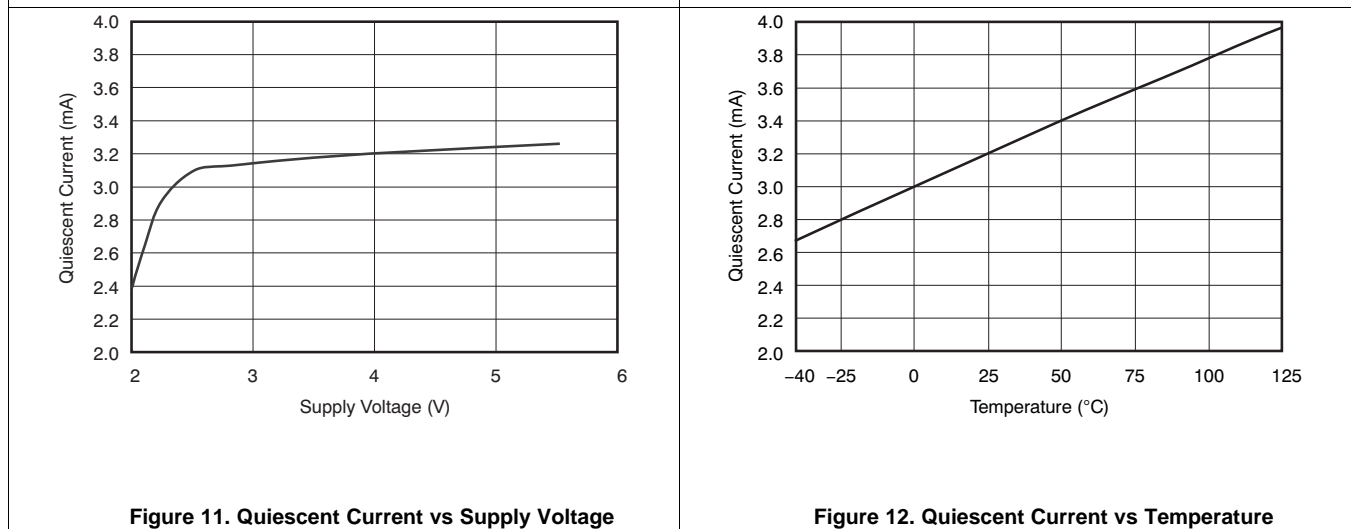
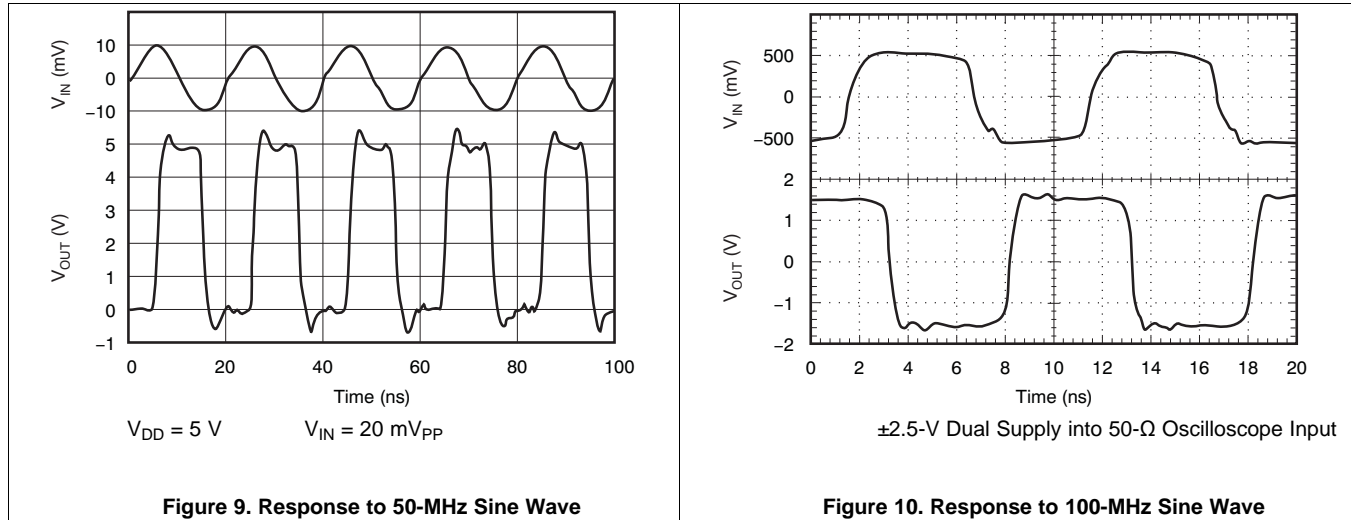


Figure 8. Wake-Up Delay vs Temperature

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, and input overdrive = 100 mV (unless otherwise noted).

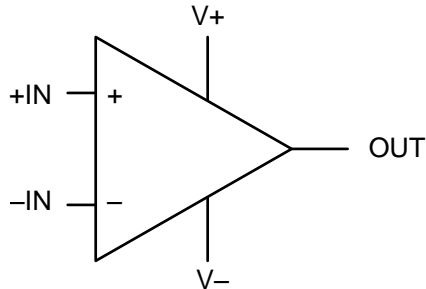


8 Detailed Description

8.1 Overview

The TLV3501A-Q1 device features high-speed response and includes 6 mV of internal hysteresis for improved noise immunity with an input common-mode range that extends 0.2 V beyond the power-supply rails.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The TLV3501A-Q1 comparators are specified for use on a single supply from 2.7 V to 5.5 V (or a dual supply from ± 1.35 V to ± 2.75 V) over a temperature range of -40°C to $+125^{\circ}\text{C}$. The device continues to function below this range, but performance is not specified.

8.3.2 Input Overvoltage Protection

The device inputs are protected by electrostatic discharge (ESD) diodes that conduct if the input voltages exceed the power supplies by more than approximately 300 mV. Momentary voltages greater than 300 mV beyond the power supply can be tolerated if the input current is limited to 10 mA. This limiting is easily accomplished with a small input resistor in series with the comparator, as shown in [Figure 15](#).

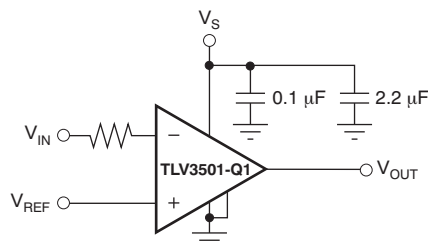


Figure 15. Input Current Protection for Voltages Exceeding the Supply Voltage

8.4 Device Functional Modes

8.4.1 Shutdown

A shutdown pin (SHDN) allows the device to go idle when the SHDN pin is not in use. When the SHDN pin is high, the device draws about 2 μA and the output goes to high impedance. When the shutdown pin is low, the TLV3501A-Q1 device is active. When the TLV3501A-Q1 shutdown feature is not used, connect the shutdown pin to the most negative supply, as shown in [Figure 16](#). Exiting shutdown mode takes about 100 ns.

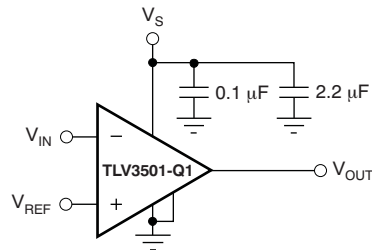


Figure 16. Basic Connections for the TLV3501A-Q1

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Adding External Hysteresis

The TLV3501A-Q1 device has a robust performance when used with a good layout. However, the comparator inputs have little noise immunity within the range of specified offset voltage (± 5 mV). For slow moving or noisy input signals, the comparator output can cause an undesirable switch state as input signals move through the switching threshold. In such applications, the 6 mV of internal hysteresis of the TLV3501A-Q1 device might not be sufficient. In cases where greater noise immunity is desired, external hysteresis can be added by connecting a small amount of feedback to the positive. [Figure 17](#) shows a typical topology used to introduce 25 mV of additional hysteresis, for a total of 31-mV hysteresis when operating from a single 5-V supply. Use [Equation 1](#) to calculate the approximate total hysteresis.

$$V_{\text{HYST}} = \frac{(V_{+}) \times R_1}{R_1 + R_2} + 6 \text{ mV} \quad (1)$$

The total hysteresis, V_{HYST} , sets the value of the transition voltage required to switch the comparator output by enlarging the threshold region, thereby reducing sensitivity to noise.

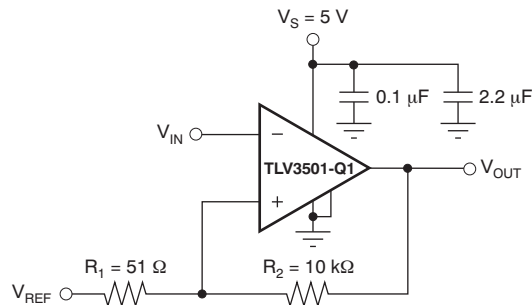


Figure 17. Adding Hysteresis to the TLV3501A-Q1

9.2 Typical Application

9.2.1 Relaxation Oscillator

The TLV3501A-Q1 device can easily be configured as a simple and inexpensive relaxation oscillator. In [Figure 18](#), the R_2 network sets the trip threshold at 1/3 and 2/3 of the supply. Because this circuit is a high-speed circuit, the resistor values are rather low to minimize the effect of parasitic capacitance. The positive input alternates between 1/3 of V_{+} and 2/3 of V_{+} depending on whether the output is low or high. The time to charge (or discharge) is $0.69 \times R_1 C$. Therefore, the period is $1.38 \times R_1 C$. For 62 pF and 1 kΩ as shown in [Figure 18](#), the output is calculated to be 10.9 MHz. An implementation of this circuit oscillated at 9.6 MHz. Parasitic capacitance and component tolerances explain the difference between theory and actual performance.

Typical Application (continued)

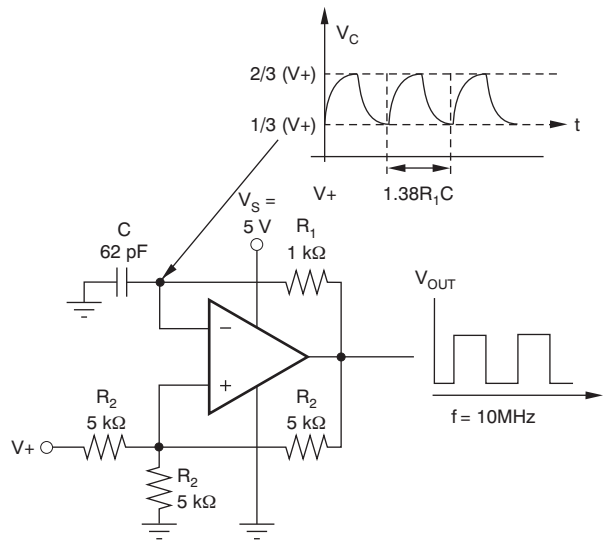


Figure 18. Relaxation Oscillator

9.2.1.1 Design Requirements

For hysteresis of 1/3 of V+ and threshold levels between 1/3 of V+ and 2/3 of V+, the resistors connected to comparator positive input should be equal in value. The resistor value should be kept low enough so it does not create additional time constant because of the input capacitor and board parasitic capacitor. The value of the charging resistor, R₁, should be relatively low for high frequency switching without drawing high current and effecting the output high and low level. The value of the charging capacitor should be high enough to avoid errors cause by parasitic capacitance.

9.2.1.2 Detailed Design Procedure

For the positive input, +IN = 1/3 V_{OUT} + 1/3 V+ = 1/3 V+ if V_{OUT} is low and assuming V_{OL} is very close to GND. Or, +IN = 1/3 V_{OUT} + 1/3 V+ = 1/3 V+ = 2/3 V+ if V_{OUT} is high and assuming V_{OH} is very close to V+.

For the negative input, the capacitor charges to 2/3 V+ and discharges to 1/3 V+ exponentially at the same rate with a time constant of R₁C.

9.2.1.3 Application Curve

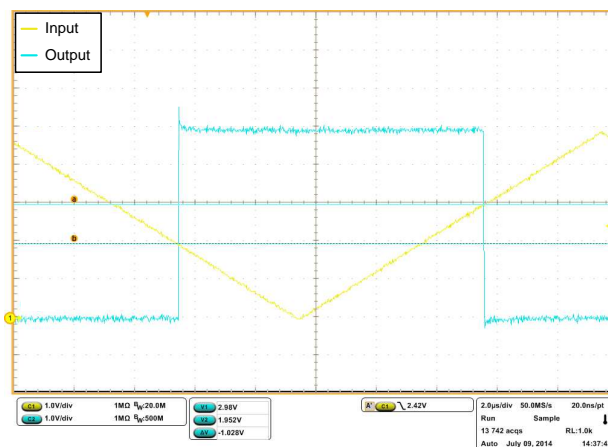


Figure 19. TLV3501A-Q1 Device With Upper and Lower Threshold With 1-V Hysteresis

Typical Application (continued)

9.2.2 High-Speed Window Comparator

A window comparator circuit is used to determine when a signal is between two voltages. The TLV3501A-Q1 device can readily be used to create a high-speed window comparator. The V_{HI} value is the upper voltage threshold, and the V_{LO} value is the lower voltage threshold. When V_{IN} is between these two thresholds, the output in Figure 20 is high. Figure 21 shows a simple means of obtaining an active low output. Note that the reference levels are connected differently between Figure 20 and Figure 21. The operating voltage range of either circuit is 2.7 V to 5.5 V.

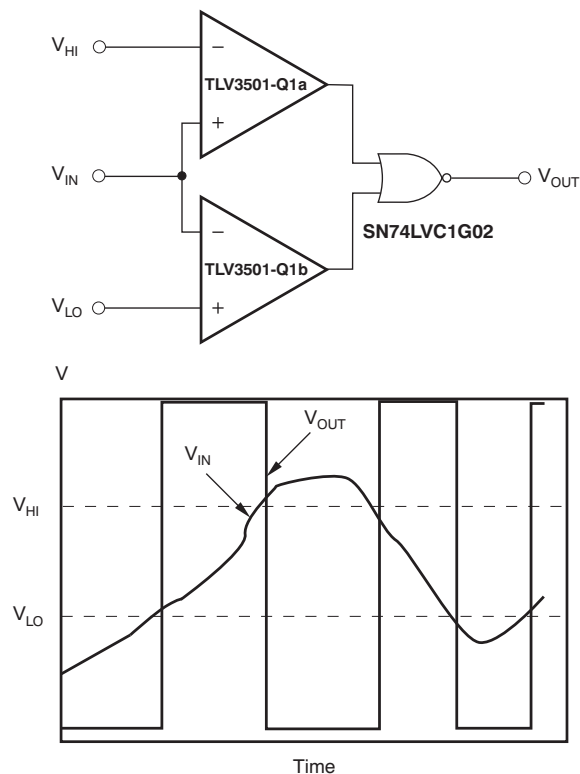


Figure 20. Window Comparator: Active High

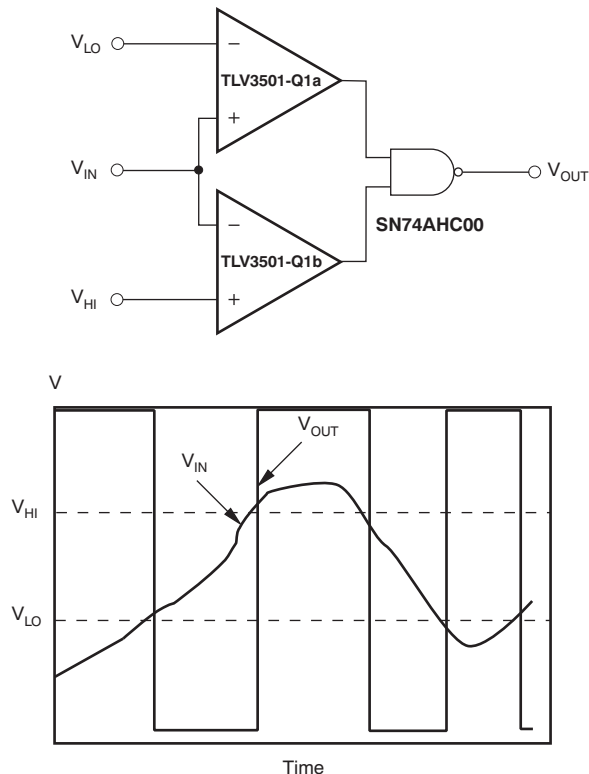


Figure 21. Window Comparator: Active Low

10 Power Supply Recommendations

The TLV3501A-Q1 comparator is specified for use on a single supply from 2.7 V to 5.5 V (or a dual supply from ± 1.35 V to ± 2.75 V) over a temperature range of -40°C to $+125^{\circ}\text{C}$. The device continues to function below this range, but performance is not specified.

Place bypass capacitors close to the power supply pins to reduce noise coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout Guidelines](#) section.

11 Layout

11.1 Layout Guidelines

For any high-speed comparator or amplifier, proper design and printed circuit board (PCB) layout are necessary for optimal performance. Excess stray capacitance on the active input, or improper grounding, can limit the maximum performance of high-speed circuitry.

Layout Guidelines (continued)

Minimizing resistance from the signal source to the comparator input is necessary to minimize the propagation delay of the complete circuit. The source resistance along with input and stray capacitance creates an RC filter that delays voltage transitions at the input, and reduces the amplitude of high-frequency signals. The input capacitance of the TLV3501A-Q1 along with stray capacitance from an input pin to ground results in several picofarads of capacitance.

The location and type of capacitors used for power-supply bypassing are critical to high-speed comparators. The suggested 2.2- μF tantalum capacitor does not need to be as close to the device as the 0.1- μF capacitor, and can be shared with other devices. The 2.2- μF capacitor buffers the power-supply line against ripple, and the 0.1- μF capacitor provides a charge for the comparator during high-frequency switching.

In a high-speed circuit, fast rising and falling switching transients create voltage differences across lines that would be at the same potential at DC. To reduce this effect, a ground plane is often used to reduce difference in voltage potential within the circuit board. A ground plane has the advantage of minimizing the effect of stray capacitances on the circuit board by providing a more desirable path for the current to flow. With a signal trace over a ground plane, at high-frequency the return current (in the ground plane) tends to flow directly under the signal trace. Breaks in the ground plane (as simple as through-hole leads and vias) increase the inductance of the plane, making it less effective at higher frequencies. Breaks in the ground plane for necessary vias should be spaced randomly.

Figure 22 shows a schematic of this circuit.

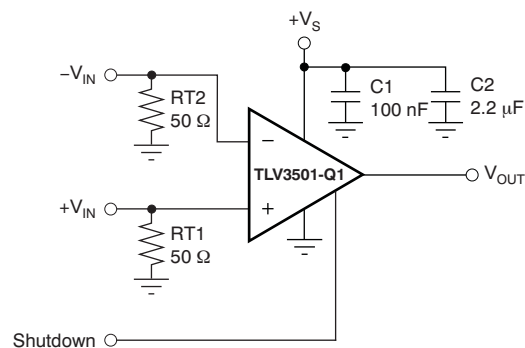


Figure 22. Schematic for Figure 23

Figure 23 shows an evaluation layout for the TLV3501A-Q1 SOT23-6 package which is shown with SMA connectors bringing signals on and off the board. The RT1 and RT2 resistors are termination resistors for $+V_{IN}$ and $-V_{IN}$, respectively. The C1 and C2 capacitors are power-supply bypass capacitors. Place the 0.1- μF capacitor closest to the comparator. The ground plane is not shown, but the pads connected the resistors and capacitors are shown.

11.2 Layout Example

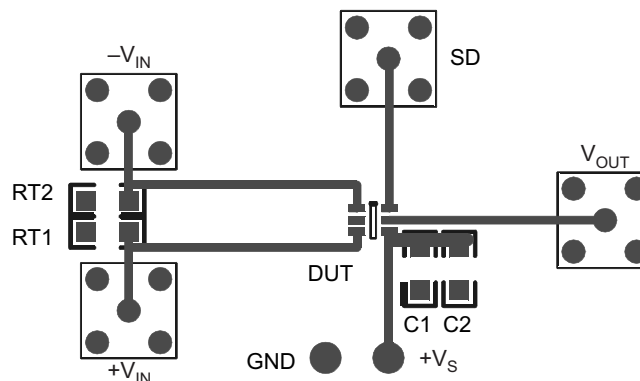


Figure 23. TLV3501A-Q1 (SOT23) Sample Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- TLV370x-Q1 *Family of Nanopower Push-Pull Output Comparators*, [SGLS154](#)
- TLC3702-Q1 *Dual Micropower LinCMOS™ Voltage Comparators*, [SGLS156](#)
- TLC3704-Q1 *Quad Micropower LinCMOS™ Voltage Comparators*, [SGLS191](#)
- TLV301x-Q1 *Nanopower 1.8-V Comparator With Voltage Reference*, [SBOS551](#)
- TLC393-Q1 *Dual Micropower LinCMOS™ Voltage Comparator*, [SGLS198](#)

12.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

LinCMOS, E2E are trademarks of Texas Instruments.
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12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV3501AQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	VCBQ	Samples
TLV3501AZQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	11Q2	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV3501AQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TLV3501AZQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV3501AQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0
TLV3501AZQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0

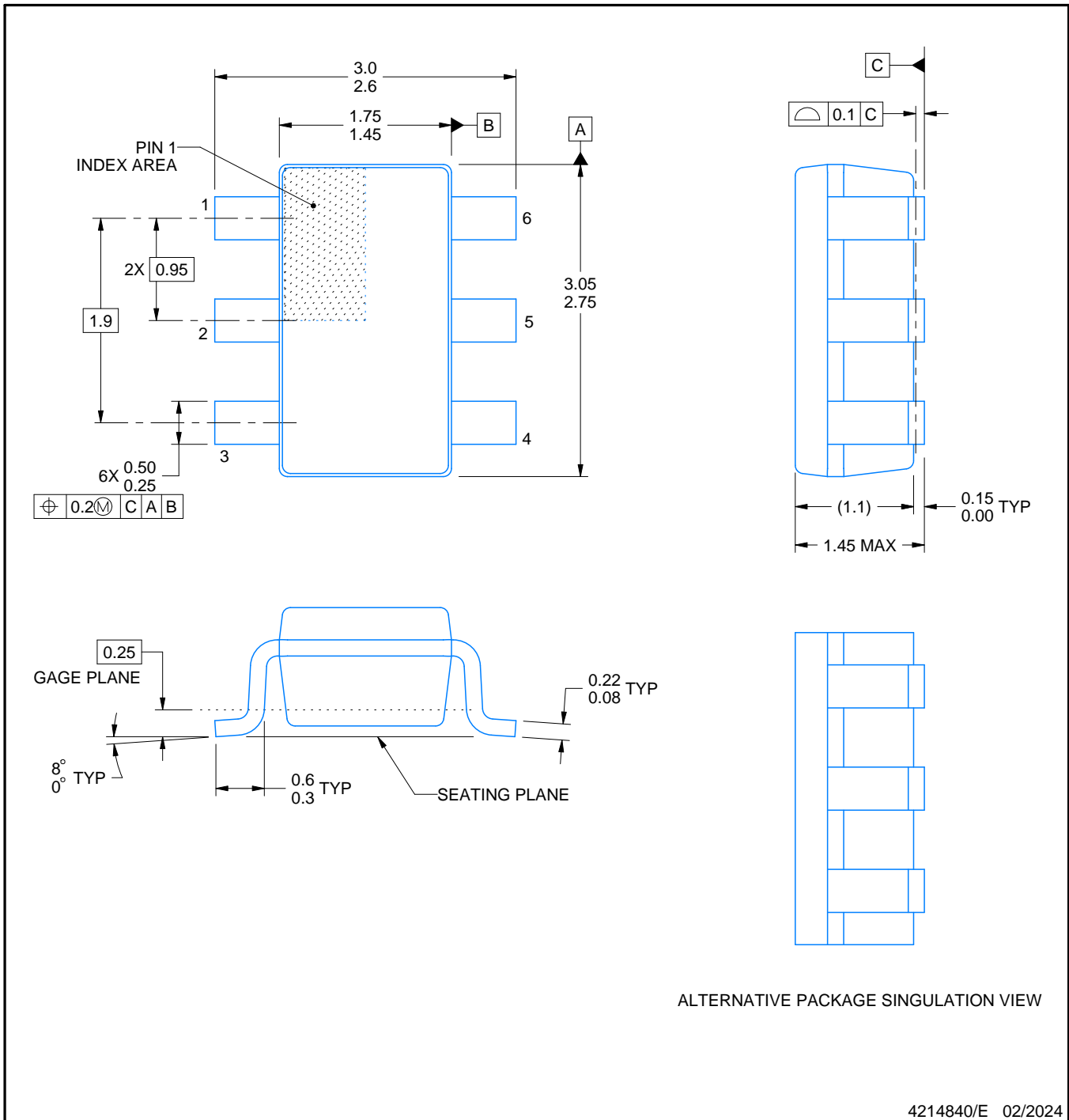


DBV0006A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/E 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

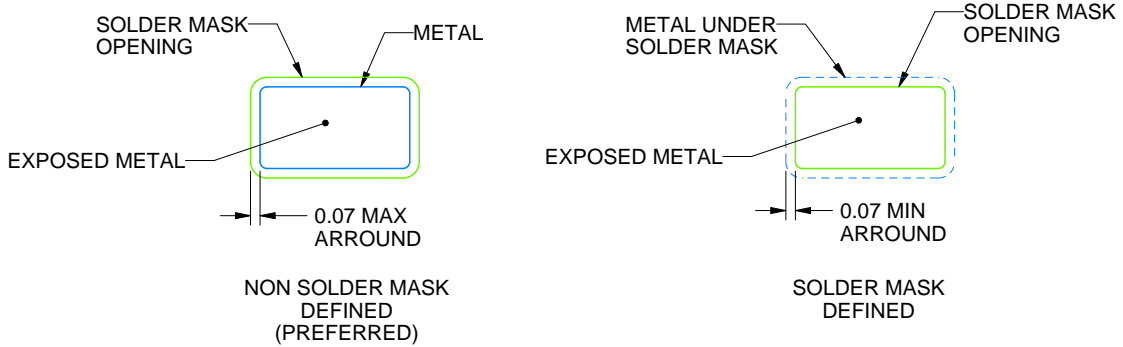
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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